ENGINEERING DATA

ALLISON EGC-101 and RELATED CIRCUITS

The EGC-101 is a current ratioing device which is intended as a control element in Voltage/Current controlled devices requiring extremely low distortion and noise, together with very wide control range, bandwidth, and slew rate.

These applications include voltage controlled amplifiers, filters, current sources, and other applications.

The EGC-101 design allows the control of bipolar signals, on a "Class A" basis, thereby eliminating crossover region anomalies, modulation noise or gain dependent distortion components, as associated with previous VCA's using "Class AB" techniques.

An equivalent electrical circuit of the Patented EGC-101 cell is shown in Figure 2, while mechanical data is provided in Figure 1.

BASIC DEPLOYMENT AS A VCA

Figure 3 illustrates the basic circuit for implementing a "Class A" VCA, utilizing the EGC-101.

Biasing: Resistors RB 1 and RB 4 serve to bias the EGC-101 cell to a current level appropriate for "Class A" operation. The optimum range of EGC-101 bias will generally fall in the range of from .5ma to 2ma. In calculating the bias through the EGC cell, the shunt path through RB 2 and RB 3 must be considered. (The values shown for RB 2 and RB 3 are typically optimum for most deployments.)

A four diode drop voltage (2.4v) will exist across EGC-101 pins 1 and 9 during normal operation. Thus, the shunt current through RB 2 and RB 3 may be calculated by $I = \frac{E}{R} = \frac{2.4v}{RB2\&RB3} = \frac{2.4v}{2,300 \text{ ohms}} = 1.043ma$, for the values shown.

The value of resistors RB 1 and RB 4 may be calculated, for a desired EGC bias level, by the following formula: $RB\ 1 + RB\ 2 = \frac{(+v)-(-v)-(2.4v)}{I_{EGC\ Bias}+I_{RB\ 1/RB\ 2}}$

Example: Assume a desired EGC bias of 1ma, using a ±15v supplies and RB 2+RB 3= 2,300 ohms.

$RB\ 1+RB\ 4 = \frac{(+15v)-(-15v)-(2.4v)}{1ma + 1.043ma} = \frac{27.6v}{2.043ma} = 1,3509 \text{ ohms}$,

or RB 1=RB 4=6.75K

EFFECT OF BIAS CHOICE:

In general, increasing the EGC bias will result in lowering the noise levels, raising the device slew/bandwidth parameters, and making distortion trimming more critical. Very high bias currents also place more stringent requirements on the impedances at the control ports. Little is to be gained in noise performance by bias currents beyond 2ma.

Conversely, decreasing the bias currents will relax the trimming and control port impedance requirements, while having only a small effect on noise and bandwidth performance.

When operated with .5ma bias, the slew/bandwidth parameters are well beyond those of commercially available op-amps, noise levels are within 4 to 5 dB of those achievable @ 2ma, and in most cases, distortion trimming will be unnecessary.

The optimum circuit for the very highest performance will normally be realized at around 1ma bias. In such a circuit, both SMPTE IMD and THD, may reliably be trimmed to under .01% at the gain and signal level extremes, and around .001% at nominal signal levels. Noise performance will be typically within 1 to 2 dB of that achievable at higher currents.(See Noise Performance)

AUDIO INPUT AND OUTPUT CURRENTS

As would be expected in a "Class A" circuit, the peak audio current must be limited to the bias current range to avoid clipping.

The structure of the EGC VCA circuit causes the bias current, as well as signal current, to be ratioed between the input and output ports, as directed by the control ports. This is an ideal situation, in that the circuit may handle a larger input signal swing when attenuating, than while giving gain. (When gain is indicated, one is concerned with output clipping rather than input overload, and vice versa.)

The mechanics of the situation are such that the combined input and output currents may equal twice the bias current, without clipping. As an example, if we assume a bias of 1ma, and a current gain of unity, the input current may be as high as 1ma peak, and will result in 1ma of output current. Now, if we assume 12 dB of current attenuation in the EGC cell, the output signal current will become 1/4 of the input signal current. Since we are allowed a total of 2ma combined input and output current, the input may now reach 1.6ma, producing .4ma of output current. This satisfies both the 12 dB attenuation criteria, as well as, the combined 2ma signal criteria. Note, then, that the input overload point has risen 4 dB, relative to the same parameter at unity gain.

TYPICAL CIRCUIT APPLICATION

Let us assume an EGC VCA is to be structured, using ±15 volt supplies, and that unity voltage gain is to be realized at zero

control volts. Assume, from previous chapters, a bias level of 1ma.(RB 1=RB 4= 6.8K)

Since most op-amps clip at around 2.4volts below the power supply rails, R in and R out should be calculated so that a 1ma peak signal current coincides with a peak voltage level of 15v-2.4v(±12.6v), or +21.2 dBv, using Ohm's Law, $R=\frac{E}{I}=\frac{12.6v}{1ma}=12.6K.$ Thus, a 12.6v input will produce 1ma input current. At unity current gain, the 1ma output current will produce an output voltage of 12.6v.

A circuit configured in this manner(and powered by ±15v), then will clip at +21.2 dBv input @ unity gain, +25.2 dBv @ 12 dB attenuation, +27.2 dBv at high attenuation, and +21.2 dBv output (limited by output op-amp), when operated at gain.

DEPARTURES FROM UNITY NOMINAL VOLTAGE GAIN

Not all VCA circuits will be structured for unity voltage gain at unity current gain (the current ratio realized at zero control volts).

Good engineering practice will generally dictate that, for optimum dynamic range, the EGC current to voltage conversion capabilities be utilized to their fullest potential in equalizing the input and output voltage clipping points to correspond to the maximum anticipated input signal and desired maximum output level.

Assume, for instance, the applied input originates from a low level stage which has a nominal signal level of -20 dBv and a maximum signal excursion of 0 dBv. Further assume an output interface to a high level output buss with a nominal signal level of +4 dBv and a +24 dBv clip point. For this example, assume a bias level of 1ma.

For optimum dynamic range, the input resistor should be selected such that the maximum 0 dBv anticipated level produces 1ma of input signal current, using the formula, $R=\frac{E}{I}=\frac{1.096v\ peak}{1ma}$, or R in= 1.1K.

The output resistor should be calculated to produce a +24 dBv level, at a signal current of 1ma. $R=\frac{E}{I}=\frac{17.4v\ peak}{1ma}=17.4K.$ Note, that in this application, the output op-amp must be capable of handling a 17.4v peak signal swing and thus, must be powered by at least ±20 volts.

In looking at the circuit at zero control volts, we find the 24 dB difference in R in and R out values will cause a nominal 24 dB voltage gain (@ zero control volts), with VCA clipping points equalized to the external clip points. It should be noted that this voltage gain is taken in the input amplifier, rather than in the VCA currents. Thus, the noise levels produced still relate to operation at unity EGC current gain. (See Noise Graphs)

As for powering the VCA input op-amp, any convenient bipolar voltage may be used, as the input stage is not restricted by input voltage swings, but rather, by input current swings. The user must, however, be careful to equate the value of the bias resistors RB 1 and RB 4 to the supply voltage of the input op-amp, using RB 1 + RB 4= $\frac{(+v)-(-v)-(2.4v)}{I_{EGC\ Bias}+I_{RB\ 2/RB\ 3}}$.

COUPLING THE VCA OUTPUT TO LOW LEVEL STAGES

In some applications, it might be desirable to couple the VCA output to a low level input stage. An example of this structure might be found in configuring a physical VCA replacement for a conventional potentiometric gain control. In such applications, the original equipment will generally be found to have a boost amplifier following the gain control, typically of from 10 dB to 30 dB gain. At first glance, it would appear logical to simply structure the VCA to operate only in the attenuation quandrant, as did the original gain control.

This approach, while simple to implement, compromises the available noise and maximum attenuation parameters, due to the post gain of the boost amplifier.

Again, the best possible performance may be obtained by the expedient of matching the VCA output clipping point to the input clipping point of the following stage, in this case with a suitable resistive pad on the VCA output.

Example:

A professional audio console, powered by ±15 volts is rated to accept a maximum input level of +24 dBv, which is applied through a 10K resistive fader to a fader boost amplifier having a 20 dB gain, and a nominal 0 dBv output. Thus, 20 dB net circuit gain is available by operating the fader full open. The maximum level which may be applied to the boost amplifier without clipping its +21.2 dBv output is +1.2 dBv, due to the 20 dB gain.

In structuring the VCA replacement, with an assumed bias of 1ma, one should first calculate the input resistor to correspond with the desired +24 dBv clip point. $R=\frac{E}{I}=\frac{17.4v\ peak}{1ma}=17.4K$, R in.

Next, the VCA output resistor should be calculated so that at unity current gain, the output current clip point coincides with the +21.2 dBv voltage capability of the VCA output op-amp. $R=\frac{E}{I}=\frac{12.6v\ peak}{1ma}=12.6K$, R out. Finally, a resistive output pad should be calculated so that the +21.2 dBv VCA clip point is reduced to match the +1.2 dBv clip point at the input of the boost amp, thereby attenuating noise as well as signal.
(+21.2 - +1.2= 20 dB pad)

In looking at the total circuit gain characteristics, it will be seen that, at zero control volts, a +24 dBv input will produce 1ma of EGC signal current, producing a +21.2 dBv VCA output voltage, +1.2 dBv pad output voltage, and a +21.2 dBv boost amp output. All clipping points have been equalized, and the nominal net voltage gain is -3.8 dB. Note that the zero control volt gain closely corresponds with a typical fader placement, when a nominal +4 dBv input signal is applied and a 0 dBv output is desired.

The net circuit gain may now be altered, by applying VCA control voltages, to in excess of 100 dB attenuation to 40 dB net gain.(In the original potentiometer version, the probable gain range was from 70 dB attenuation(-90 dB fader shutoff, +20 dB boost gain) to 20 dB gain.)

Also note that the same performance could have been implemented by removing the original boost amplifier and VCA pad, and directly utilizing the VCA output. Although this would have been preferable, from a minimum circuit complexity standpoint, it might be impractical in a retrofit situation, for mechanical reasons.

CONTROL PORTS

The control ports of the EGC-101 cell should be terminated to ground with resistors RC 1 and RC 2, as shown in Figure 3. The value of these resistors should be as low as practical, typically under 100 ohms, in order to maintain minimum device distortion. (See Distortion Considerations)

The control ports should be configured as two cross coupled pairs, as indicated in Figure 3. When so configured, the application of a D.C. control voltage at pins 7 and 16 will result in a 1 dB EGC current gain per +6mv control, or 1 dB EGC current attenuation per -6mv control, with unity current gain at Ec=0vdc. Conversely, the application of control voltages to pins 3 and 12 will result in 1 dB EGC current gain per -6mv control, or 1 dB current attentuation per +6mv control. In the case of differentially applied control voltages, the EGC current ratio will be governed by the logical differential total of the two control ports.

Example: With +6mv applied to pins 7 and 16, and -6mv applied to pins 3 and 12, device current gain will be +2 dB.

In theory, the EGC current ratio will follow an exact log or "dB/volt" relationship over around a 360 dB range (-180 dB to +180 dB).

In a practical circuit, the useable gain range will be reduced to the range of -100 to -125 dB attenuation to +40 to +70 dB gain, due to the stray capacities and ground loops at the attenuation end, and the input amplifier's gain X bandwidth and bias current parameters at the gain end.

The stated 6mv/dB scale factor, as in all non-temperature compensated devices performing a "dB/volt" relationship, is stat-

ed at room temperature (25°C), and is affected by +.3% per degree C temperature dependence.

Example: At 35°C temperature, the scale factor will increase by 3%, to 6.18mv/dB.

In practice, this scale factor deviation is normally ignored for two reasons:

1. Well engineered circuits will place the nominal operating gain point in coincidence with the 0 control volt point, thereby eliminating any temperature induced gain dependence at the normal operating point.

2. In most audio applications, the gain range where absolute gain accuracy is required is between 30 dB attenuation and 30 dB gain. At the extremes of these limits, a maximum error of under 1 dB will exist, with a ±20°F deviation from the normal operating temperature, and all VCA's in a system will track this error. The error will diminish to zero as the gain is brought to the normalized zero control volt point.

For applications requiring temperature independence in the scale factor, a thermistor specially designed to compensate for this .3%/°C error is available from TEL Labs, Inc., Dept. EM, 154 Harvey Rd., Londonderry, NH 03053, Tel: 603-625-8994, under the designation, "Q 81", which may easily be incorporated in the control scaling circuitry.

CONTROL SCALING:

In most VCA applications, a series resistor will be inserted between the control voltage source and the EGC control port(s), thus forming a resistive "L pad" with terminating resistor RC 1 or RC 2. The purpose of this network is to "scale" the control voltage to some convenient value such as 20dB/volt (50mv/dB), or 10dB/volt (100mv/dB). Simple mathematics are involved in calculating the resistor value.

Example: Assume RC 1 is 100 ohms, and a +10dB/volt scaling is desired (100mv/dB). In order to reduce the 100mv/dB applied control voltage to the 6mv/dB required at RC 1, a loss of 16.67 to 1 is required in the L pad. This may be accomplished by the inclusion of a 1,567 ohm series resistor.

OBTAINING MAXIMUM PERFORMANCE

The circuit of Figure 4 (The Allison EGC-205M) incorporates additional circuitry which may be beneficial to obtaining the very highest level of precision from the EGC-101 cell, in VCA usage.

CONTROL SIGNAL REJECTION:

As gain changes are directed, via the application of control voltages, the signal and bias currents are ratioed between the

input and output ports. In order to facilitate gain changes without serious D.C. level shifts appearing at the output, the currents through the EGC elements must be equalized such that the net bias current at the output is maintained at zero (through cancellation within the EGC cell). This principle is inherent in all VCA designs utilizing bipolar transistors, and becomes somewhat more critical in a "Class A" design, due to higher bias currents.

The accepted method of specifying control rejection is to state the magnitude of D.C. voltage change at the output (with no applied input signal) vs. the amount of gain change directed at the control port(s).

In Figure 4, the network of R 11 through R 16 is employed to facilitate the adjustment of R 16 for maximum control rejection. With the values shown, the circuit may be adjusted to yield no more than 10mv D.C. level change (typically 3 to 5mv), at the output, over the gain range of -100 dB to +30 dB. For applications requiring more critical performance, the value of R 15 may be adjusted to make up for manufacturing differences from one EGC-101 cell to another.

In order to maintain the excellent control rejection characteristics of the EGC-101, attention must be paid to the thermal environment in which it operates. While the absolute operating temperature is not critical, thermal gradients, or temperature differences across the EGC-101 cell can cause deterioration of the control rejection parameters. To this end, the EGC cell should not be mounted in close proximity to heat producing elements, particularly when these elements are mounted on the same P.C. board, where thermal gradients may develop across the board itself and be transmitted through the EGC leads. For extremely critical applications, a thermally insulative "cocoon" (such as styrofoam) might be considered around the gain cell.

It is interesting to note that, in most "Class AB" VCA's, the same thermal conditions exist, but manifest themselves upon the distortion parameters rather than on the control rejection. In the EGC, the distortion parameters are exceedingly low, and are relatively immune to temperature effects.

Another point regarding control rejection...any variable gain device will produce output level shifts, during gain changes, if any D.C. component appears at its input. Accordingly, an input blocking capacitor should always be employed, as shown in Figure 3. If the device must specifically operate to D.C., the input must be carefully offset to zero.

BUFFERING AND TRIMMING THE CONTROL PORTS:

As a requisite to obtaining the extremely low distortion capability of the EGC-101, the termination resistors RC 1 and RC 2 in Figure 3, or R 8, R 9, and R 10 in Figure 4, must be kept at as low an impedance as practical, particularly when the device is operated at high bias currents. A good rule of thumb is to keep these resistors below about 1% of the value of the biasing resistors. (RB1 & RB4)

Additionally, for minimum distortion, it is desirable to be able to adjust the ratio of the two control port impedances to compensate for minor manufacturing inbalances in each EGC-101 cell. This is performed, in Figure 4, by adjusting R 10. Note that this trim point is made on the control port which is not being fed control voltages, as adjustments of R 8 would alter the scale factor.

Many VCA applications benefit from the ability to sum control voltages from a number of controlling sources, so that the VCA gain is a function of the algebraic combination of several control inputs. (i.e. channel fader, group fader, master fader, etc.)

The purpose of OA 3 then is to:

1. Provide a virtual ground summing input for such purposes.
2. Present a higher impedance to the control voltage sources than that provided at the control ports themselves.
3. Buffer the impedance at the EGC control ports from changes incurred by different values of scaling resistors, etc.

In analyzing Figure 4, it can be seen that resistors R 7 and R 8 form a "L pad", which causes a +10 dB/volt scaling at the output of OA 3 to be attenuated to the required +166.7 dB/volt (6mv/dB) scaling required at pins 7 and 16 of the EGC-101 cell.

Feedback resistor R 6 establishes the magnitude of control current which must be applied at OA 3 pin 2, to achieve a given control voltage at the output of OA 3. For the value shown for R 6, a -1ma must be applied to OA 3 pin 2, to achieve a +10v output. Thus, OA 3 pin 2 becomes a current summing point which produces -100 dB VCA gain per applied positive ma., and is designated a "-100 dB/ma", or "-10ua/dB" control current input.

All that is necessary in order to produce any number of voltage control inputs is the connection of appropriate value resistors to OA 3 pin 2.

Example: A 10K resistor produces a -10 dB/v input, 5K= -20 dB/volt, etc. To assure an accurate scale factor and good tracking between VCA's in a system, resistors R 6, R 7, and R 8, and the voltage to current converting input resistors should be precision 1% units.

If the inverse control polarity is desired (i.e. +20 dB/volt), OA 3's output should be coupled to pin 3 of the EGC-101, and R 8 should be crossed with R 9 and R 10.

DISTORTION CONSIDERATIONS

In any VCA, it is of paramount importance to insure that no audio signal is allowed to leak into the control ports, as self

modulation will result in the production of distortion. This is particularly true at the higher frequencies where the probability of coupling through stray capacities is increased.

In Figure 4, control integrating capacitor C 3 serves to reduce the control port frequency response to 1 kHz (1msec time constant) in order to gain freedom from self modulation effects, as well as for R.F. and general noise suppression at the control port.

In applications requiring faster VCA gain control response, the integration time may be decreased and, if necessary, the 741 op-amp may be replaced with a faster slewing device such as a TL 071, or 741s. In such applications, however, extreme care must be excercised in the board layout and control port wiring, in order to prevent signal or noise leakage into the control circuit.

TRIMMING THE BIAS NETWORK

In referring to Figure 3, the ratio of RB 2 to RB 3 will have some effect on the VCA distortion parameters. Owing to slight differences in the EGC-101 cell geometry, the optimum ratio will generally indicate that RB 3 be about 10% lower in value than RB 2. As stated earlier, the RB 2/RB 3 ratio, as well as the RC 1/RC 2 ratio becomes more critical as the bias current is increased.

In structuring for the lowest possible distortion, the circuit of Figure 4 is recommended.

ADJUSTMENT PROCEDURE - CIRCUIT OF FIGURE 4

1. Connect a 13K resistor in series with a 10 mfd. capacitor to "I in" terminal, thus forming an AC coupled Signal Voltage Input.
2. Connect a 4.99K resistor to the "I control" terminal, thus forming a -20 dB/volt control voltage input.
3. Power the circuit with a ±15 volt supply.
4. Ground the Signal Voltage Input, apply a low frequency (i.e. 100 kHz) sine wave of 2v peak to peak amplitude to -20 dB/volt control input. This will cause gain modulation over the range of -20 dB to +20 dB.
5. Adjust R 16 for minimum signal (control feedthrough) at audio output. NOTE: If trimming for critical control rejection, also test and connect the optimum value for R 15 for minimum output.
6. Connect a voltage source, variable from -1 volt to +1 volt, to the control voltage input, in place of the audio oscillator. Connect the output of a SMPTE IM analyzer to the Signal Voltage Input.
7. Adjust the output of the IM analyzer for a +20 dBv equivalent sine wave level (1.095 volts peak). Set the control voltage for 0 volts (unity gain).
8. Adjust R 10 for minimum I.M.D. at the audio output (should be less than .01%).
9. Adjust the control voltage for +1.00vdc (-20 dB gain).

10. Adjust R 3 for minimum I.M.D. (should be less than .01%).
11. Reduce the I.M.D. analyzer output to 0 dBv sine wave equivalent (1.095v peak). Adjust the control voltage for -1.00v (+20 dB gain).
12. Re-adjust R 3 if necessary to achieve best compromise distortion between tests #10 and #12 (attenuation and gain). You should be able to maintain under .01% I.M.D. at both points.

STABILITY CONSIDERATIONS

In referring to Figure 3, CC 1, CC 2, RB 2, and RB 3 are stabilizing elements, required to compensate for the distributed capacitance of the EGC-101 cell.

At the input circuit, the values shown for CC 1, RB 2, and RB 3 should prove optimum for most circuits operating in the bias range of .5ma to 2ma, using any of the following op-amps for OA 2: T L 070 series, LF 353 series, NE 5532, etc. Such configurations will result in an effective VCA Gain X Bandwidth product of between 5 and 6 mHz, with excellent square wave response and stability.

The output op-amp must be stabilized with CC 2, whose value will set the maximum frequency response of the VCA. A minimum suggested value for CC 2 is 10 pfd.

Gain/Bandwidth contours for a typical audio VCA deployment are shown in Figure 7.

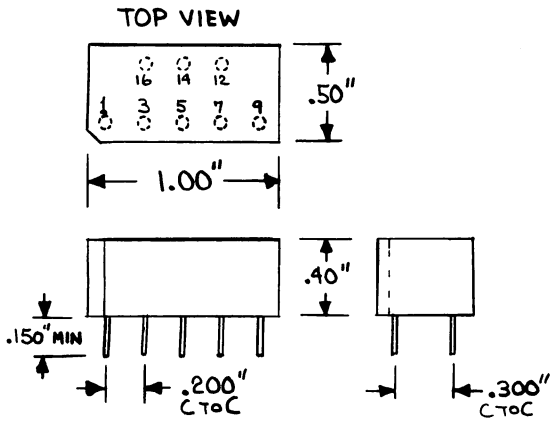
PATENT NOTICE

The circuitry of the Allison EGC-101, as well as the external circuitry portrayed herein, is protected by one or more of the following U.S. Patents: 3,237,028, 3,293,450, 3,714,462.

Unauthorized use is prohibited by law.

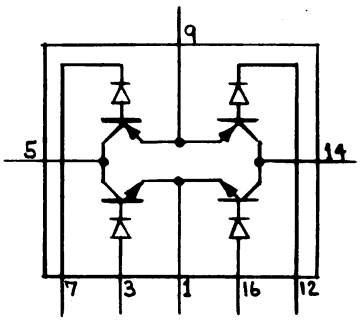
Additional patents are pending.

allison research, inc.
2817 ERICA PLACE (P.O. BOX 40288), NASHVILLE, TENNESSEE 37204
(615) 385-1760 or (615) "ALLISON"



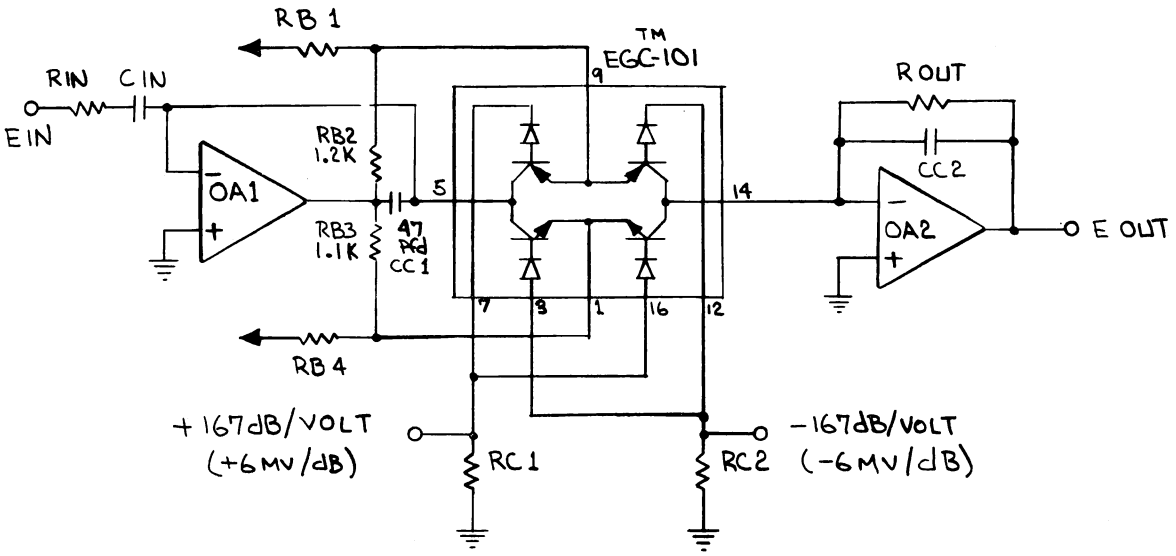
.025" DIA LEADS 8 PLACES
TIN ON COPPER ON STEEL

FIGURE 1



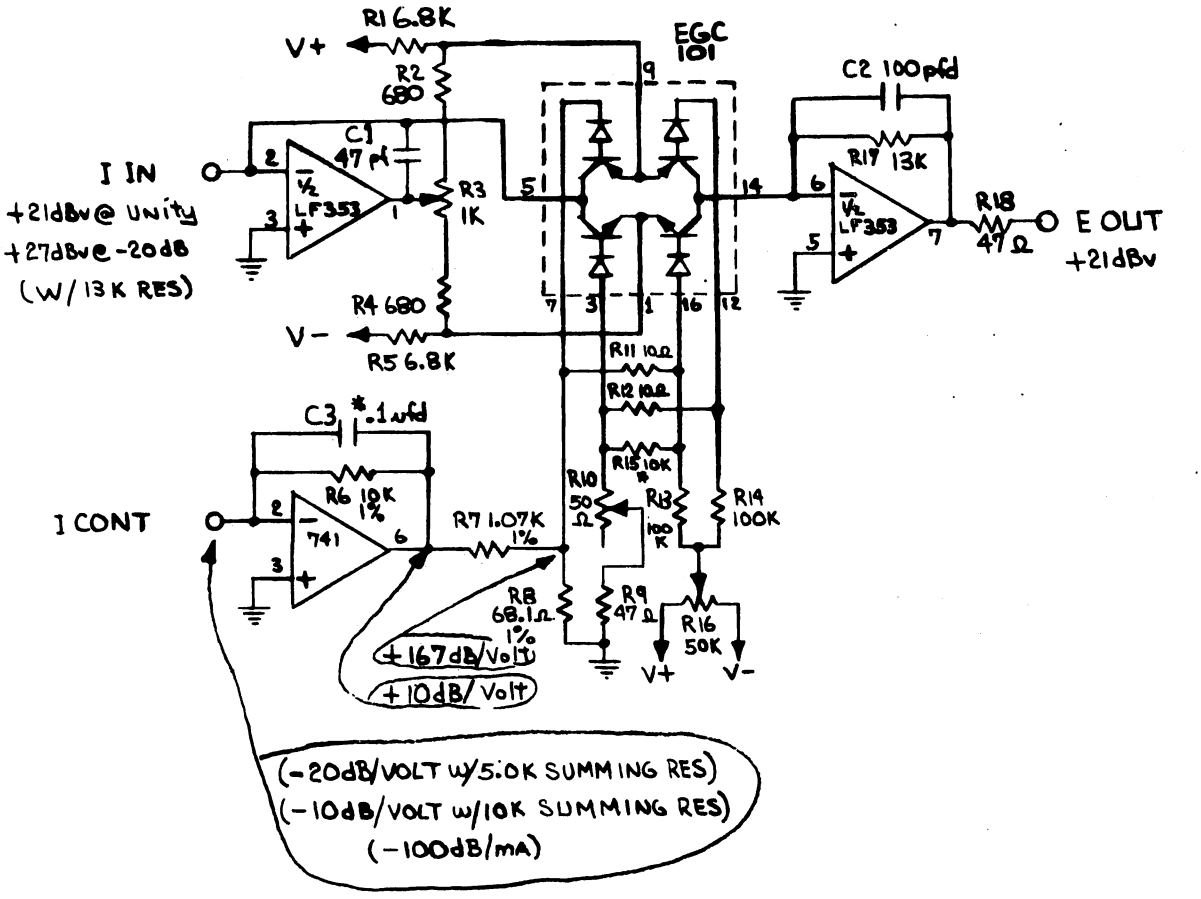
EGC-101™ EQUIVALENT CIRCUIT
U.S. PATENT #3,714,462
OTHER PATENTS PENDING

FIGURE 2

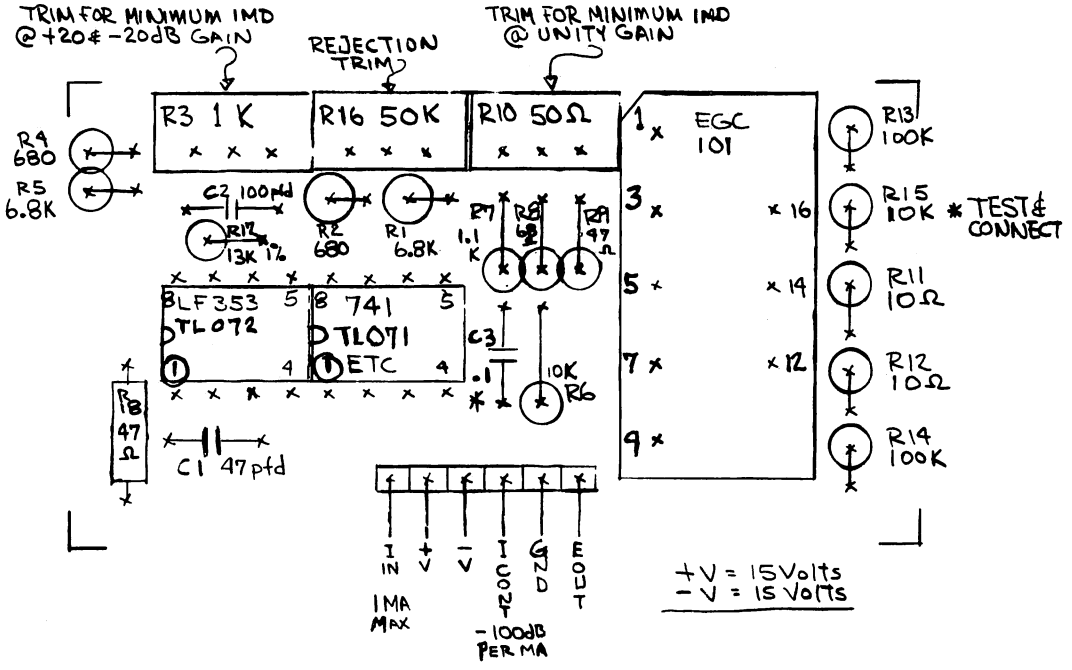


BASIC VCA UTILIZING EGC-101™
US PATENT #3,714,462
OTHER PATENTS PENDING

FIGURE 3



EGC-205M (FULLY TRIMMED VCA CKT WITH CURRENT INPUTS & VOLTAGE OUTPUT
US PATENT # 3,714,462 AND OTHER PATENTS PENDING
FIGURE 4



EGC-205 PARTS PLACEMENT (PARTS SIDE)
FIGURE 5

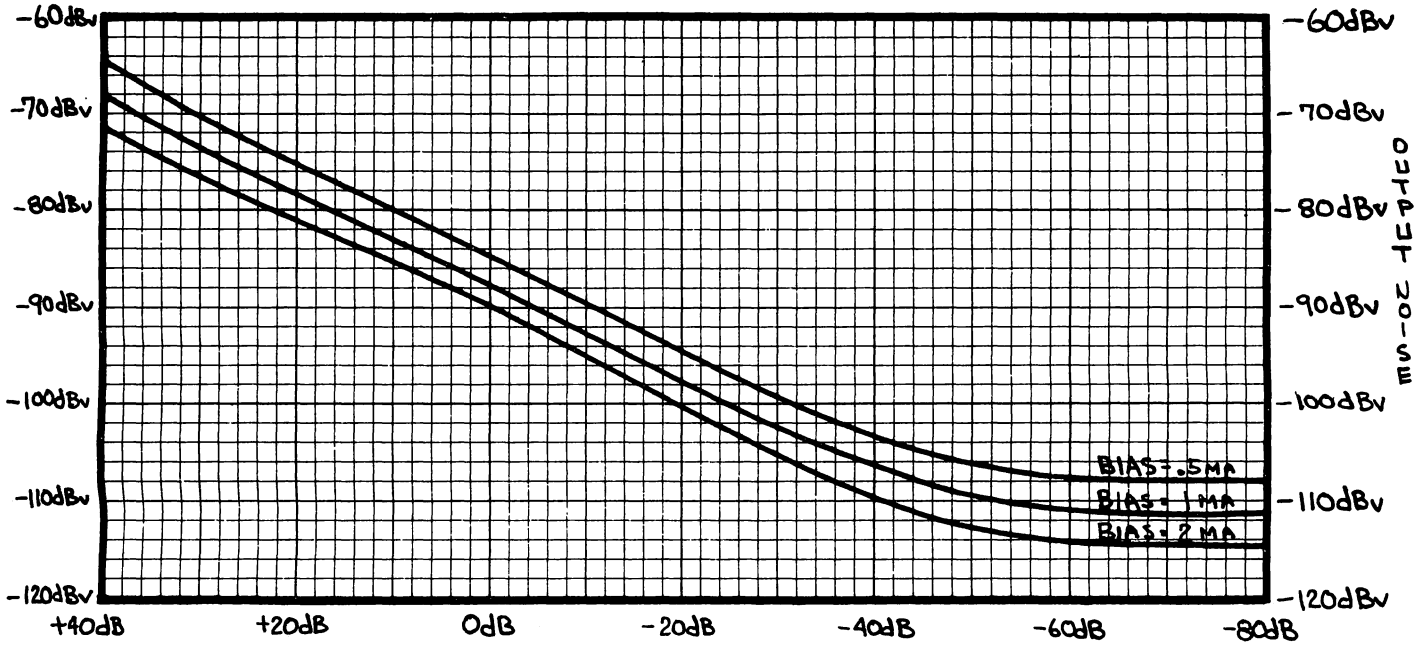


FIGURE 6

NOISE CONTOURS FOR AN EGC VCA AT .5MA, 1MA & 2MA BIAS
NOISE BANDWIDTH = 20Hz to 20KHz, AVERAGE RESPONDING METER, REF .775V$_{rms}$
DEVICE POWERING = ±15V, CONFIGURED FOR UNITY GAIN @ ZERO CONTROL VOLTS

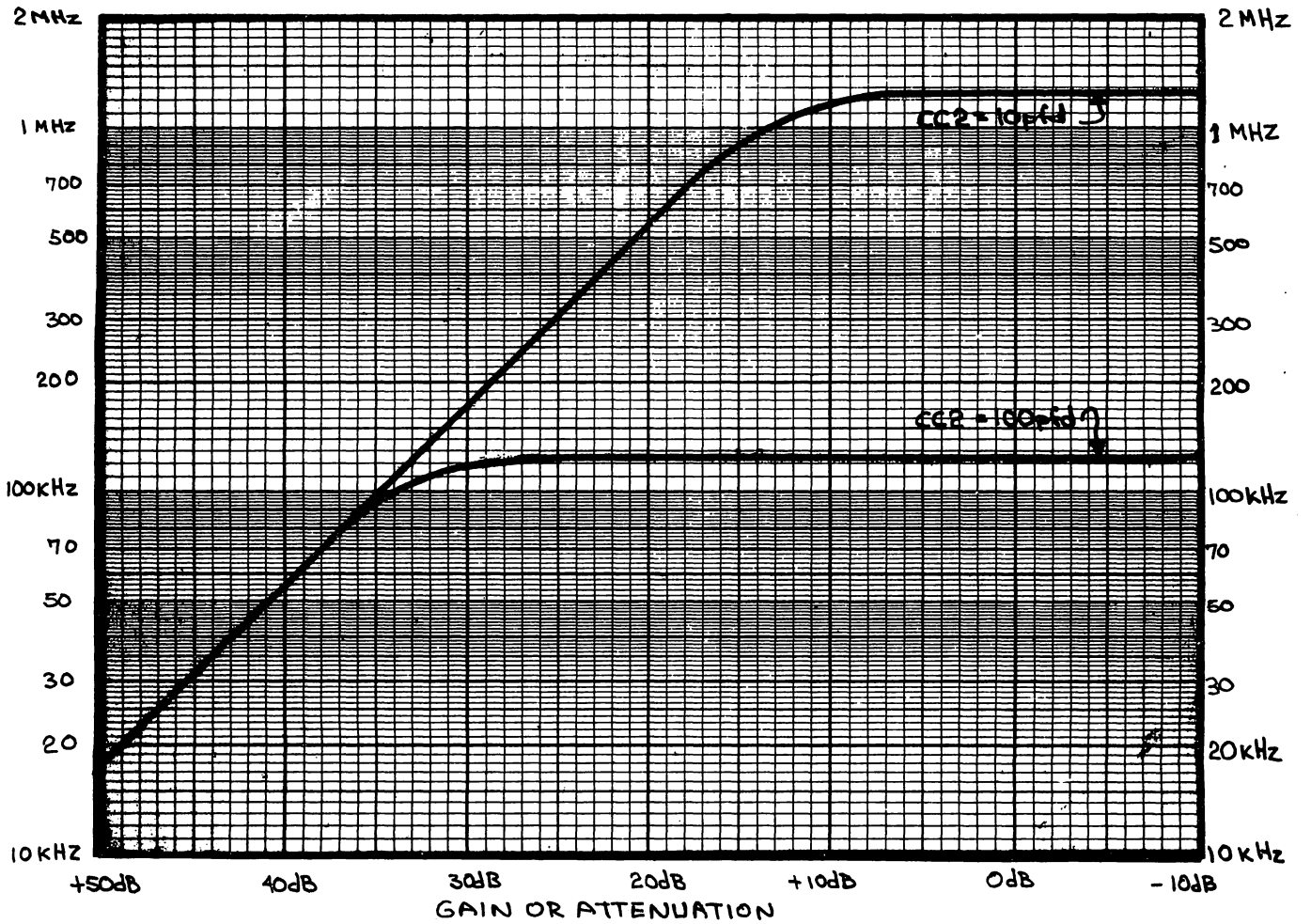


FIGURE 7

UPPER 3dB FREQUENCY VS. GAIN FOR AN EGC VCA @ 1MA BIAS (CC1=47pfd, RB2=1200Ω, RB3=1100Ω)