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Digital-Centric RF CMOS Technologies

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SUMMARY Analog-centric RFCMOS technology has played an important role in motivating the change of technology from conventional discrete device technology or bipolar IC technology to CMOS technology. However it introduces many problems such as poor performance, susceptibility to PVT fluctuation, and cost increase with technology scaling. The most important advantage of CMOS technology compared with legacy RF technology is that CMOS can use more high performance digital circuits for very low cost. In fact, analog-centric RF-CMOS technology has failed the FM/AM tuner business and the digital-centric CMOS technology is becoming attractive for many users. It has many advantages; such as high performance, no external calibration points, high yield, and low cost. From the above facts, digital-centric CMOS technology which utilizes the advantages of digital technology must be the right path for future RF technology. Further investment in this technology is necessary for the advancement of RF technology.

key words: *CMOS, RF, analog, digital, tuner, PLL, sampling, mixer, wireless*

1. Introduction

RF CMOS technology is based on an idea of integrating all needed components, circuits, and functions for realizing wireless systems to increase the performance and to decrease power consumption and cost [1]. It is however not easy to integrate analog and RF circuits in highly-scaled CMOS technology [2].

This paper reviews the current status of FM/AM tuner ICs in which CMOS technology has not been used sufficiently and will reveal the advantage of the digital-centric RF CMOS technology compared to conventional analog centric technology. Furthermore digital RF technology which can use digital technology in RF circuits is reviewed to point out the features and issues on this technology.

2. Analog-Centric RF CMOS Technology

An application of CMOS technology to FM/AM tuners sounds easy compared to wireless network systems and cellular phone systems, however this is the toughest area in realty. Low frequency requires large inductors and capacitors such that integration on a chip is not reasonable and results in many external components still being required. AM signal suffers from 1/f noise directly; furthermore higher sensitivity and durability against the unwanted signals are required compared to the wireless network systems and the cellular phone systems.

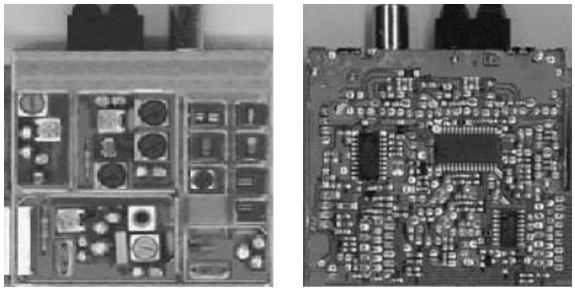

Fig. 1 Current FM/AM tuner board.

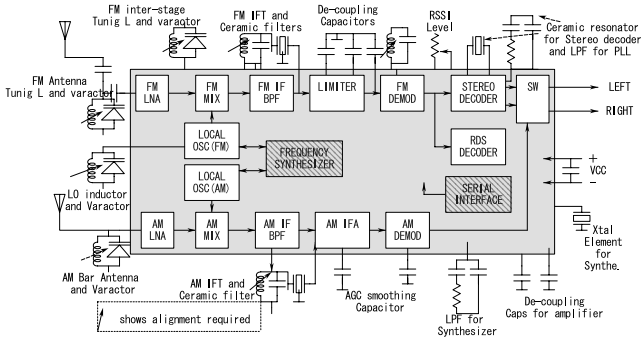

Fig. 2 Block diagram of current FM/AM tuner.

Figure 1 and Fig. 2 show current FM/AM tuner board and block diagram, respectively. Many external components and many adjustment points are needed, for example; in this case three ICs, 187 external components, and 12 adjustment points are needed. Important external components are LC tanks and ceramic filters.

The first trial to apply CMOS technology to this FM/AM tuner started by integrating the functions of these external components on a chip by using analog-centric technology.

Table 1 shows the circuit technologies used and the problems caused by each technique. Low IF architecture has been chosen to address 1/f noise and the DC offset issues when direct conversion architecture is applied. Active filters; such as gm-C filter and switched capacitor filter were used for channel select filters and the poly-phase filter was used to reject the image signal. Pulse count method and a multi-vibrator circuit were used for FM demodulation and reconstruction of stereo sound, respectively.

Figure 3 shows FM/AM tuner board using analog-

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Table 1 Analog-centric technology and issues.

Parts	Methods for on-chip	Problems
AM/FM IF BPF	1. Low IF(a few hundred KHz) 2.Gm-C BPF with auto alignment, SCF	1.poor selectivity(-45dB), 2. SCF Switch noise 3. Center frequency shift by DC offset 4. Poor image rejection ratio (25 to 35dB)
FM Demodulator	Pulse count FM detector	Poor THD (0.5%)
Stereo Decoder	Multi-vibrator VCO, SCF filter	Large variation of free-run frequency Still need external LPF for PLL
RSSI Level adj.	Signal detector with DC compensation	Can't cover all process corner
Varactor	MOS varactor	Too much sharp C-V curve, distorted signal
AGC smoother	Time division charge and discharge	Needs large capacitor for low audio frequency
Capacitors	Stages Direct connection, use small value coupling capacitor	High impedance required, Difficult for low frequency

Fig. 3 FM/AM tuner board using analog-centric CMOS IC.

centric CMOS IC. The performance was not attractive. The selectivity and image rejection ratio were only −45 dB and 30 dB, respectively. Furthermore performance was seriously affected by PVT fluctuations and the yield was not sufficient. The number of external components and adjustment points were 69 and 11, respectively. Thus both performance and cost are not attractive to users in spite of use of advanced CMOS technology.

3. Digital-Centric RF CMOS Technology

This failure of IC development promoted the change of the technology from analog-centric IC technology to digital-centric IC technology.

The basic concept of the digital-centric IC technology is that analog technology should be minimized and digital technology should be used as much as possible.

Figure 4 shows a block diagram of digital-centric RF CMOS IC for FM/AM tuner.

Low IF architecture was used for FM signal. A digital filter was used for the channel select filter and attained high selectivity of 65 dB. AM modulated signal is directly converted to digital signal without a conventional mixer and demodulated by multiplication by a negative career frequency as shown in (1) in digital domain.

$$[1 + S(t)] \exp(j\omega t) \times \exp(-j\omega t) = [1 + S(t)] \tag{1}$$

FM signal can be demodulated by time derivation of phase component as shown in (2), (3).

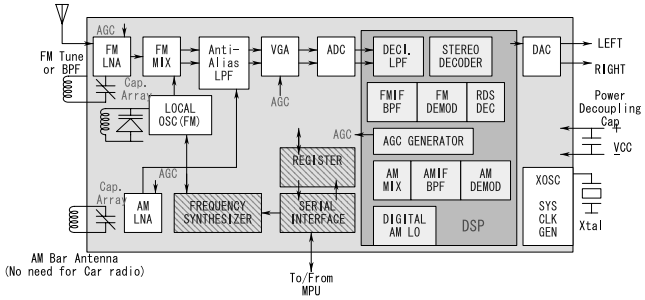

Fig. 4 Block diagram of digital-centric CMOS LSI.

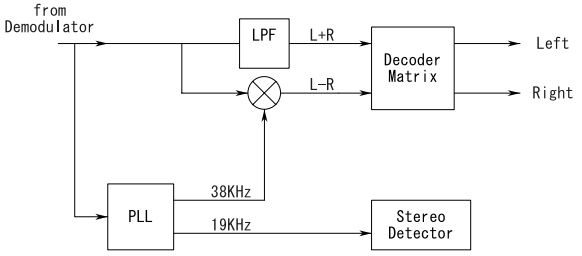

Fig. 5 Demodulation system for stereo signal.

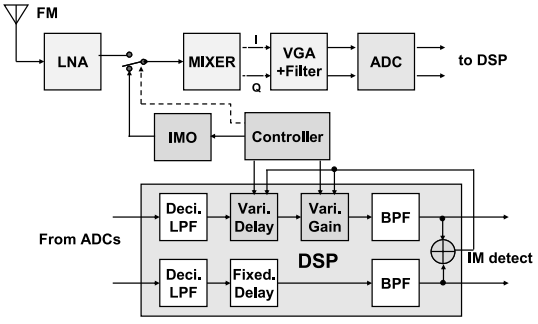

Fig. 6 Image rejection system.

$$R(t) \exp\left(j\left(\Delta\omega t + K_d \int m(\tau)\, d\tau\right)\right) \tag{2}$$

$$\frac{d\theta}{dt} = \Delta\omega + K_d m(t) \tag{3}$$

Where $R(t)$ is amplitude variation, $\Delta\omega$ is frequency offset, and $m(\tau)$ is the baseband signal to be recovered.

The stereo signal has the following structure.

$$S(t) = (L + R) + (L - R)\cos\omega_s t + K\cos\omega_p t \tag{4}$$

Thus the stereo sound can be reconstructed in digital domain using the block diagram shown in Fig. 5.

PLL, mixer, and filter are formed in digital domain. A good stereo separation of 55 dB has been attained.

Image rejection is a serious issue in low IF systems.

A conventional image reject ratio attained by using the analog method is about 40 dB at most. Thus the digital image rejection method shown in Fig. 6 was applied.

Image signal oscillator generates the image signal and the controller controls signal delay and gain in one path of I/Q signal to minimize the image signal in digital domain.

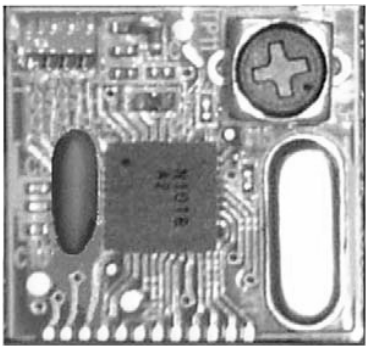

Fig. 7 FM/AM tuner board using digital-centric CMOS LSI.

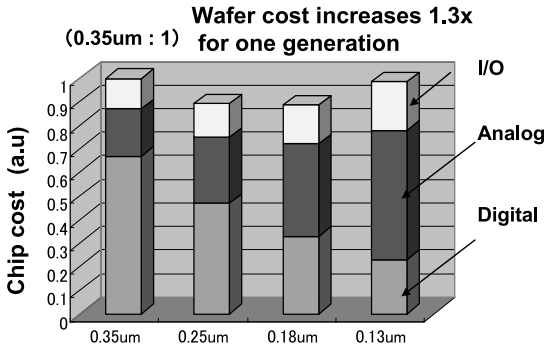

Fig. 8 Estimated cost of mixed signal LSI.

Sufficiently high image rejection of 60 dB has been attained.

Figure 7 shows the tuner board on which the digital-centric RF CMOS IC is mounted. There are only 11 external components and no adjustment point is required. This IC can realize stable reception by controlling the gain of each stage and various parameters by monitoring unwanted signals as well as wanted signal to attain a high quality of the received signal.

4. Digital-RF Technology

The global trend of RF CMOS technology is to use digital technology as much as possible and to use analog technology for only the essential parts [3]. The biggest reason of this trend is that analog circuits are so seriously affected by device mismatches, PVT fluctuations, and the change of environment that the performance and production yield are unstable. The other reason is the cost increase by technology scaling.

Figure 8 shows the cost estimation of mixed signal LSI for each technology generation normalized by 0.35 μm CMOS under the assumption that the areas of the original LSI are 70% for digital circuits and 30% for analog and I/O circuits and the area for digital circuit will be reduced along with technology scaling and the area for analog and I/O circuits are kept constant. The cost for analog will increase even if area is kept constant, because wafer cost increases about 30% for one technology generation advancement. Thus it is important to shrink analog circuits along with technology scaling [3].

Furthermore, more flexible and reconfigurable wireless systems are demanded to realize multi-standard and multi-mode wireless systems and technology called "digital RF technology" has emerged [4]. I will review important technologies that form "digital RF technology."

4.1 ALL Digital PLL

PLL is a very important building block for wireless systems. Accurate and pure signal generation is always required. Phase frequency detector, charge pump, loop filter, voltage controlled oscillator, and frequency divider are needed to form the PLL system. Analog circuit technology

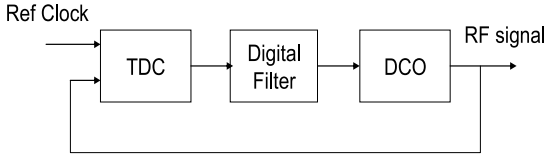

Fig. 9 All digital PLL.

is still used and becomes tough to design in recent scaled CMOS technology.

Conventional loop filter requires large silicon area to form a long time constant and suffers leakage problem that becomes serious due to the increase of gate leakage current caused by the reduction of gate oxide thickness. Circuit design of charge pump becomes tough due to operation voltage lowering. Furthermore varactor in VCO increases phase noise when the control voltage contains noise.

The idea of all digital PLL is to use digital circuits as much as possible to form PLL instead of conventional analog circuits to address these issues.

Figure 9 shows system configuration of full digital PLL [5], [6]. Time to Digital Converter (TDC), digital filter, and Digital controlled Oscillator (DCO) are used instead of conventional Phase Frequency Detector (PFD), analog filter, and Voltage Controlled Oscillator (VCO), respectively.

The conventional TDC uses inverter delay circuit and latches and realizes several 10 ps resolution, as shown in Fig. 10.

However shorter time resolution is required to realize lower phase noise. The resolution of current TDC is determined by the signal propagation delay of inverters. Furthermore latches and inverters have uncertainty in timing; therefore time resolution may not be improved by technology scaling. Further investigation on TDC is required.

Figure 11 shows one attempt to compensate the delay mismatches [7].

First each time delay element is selected to replace the inverter that constructs the ring oscillator and the oscillating frequency is measured. Second the delay time of the delay element is adjusted so as to reduce the delay mismatch.

The delay mismatch is suppressed from 40 fs to 18 fs and time resolution of 0.88 ps has been realized.

DCO uses an array of varactors. A conventional VCO

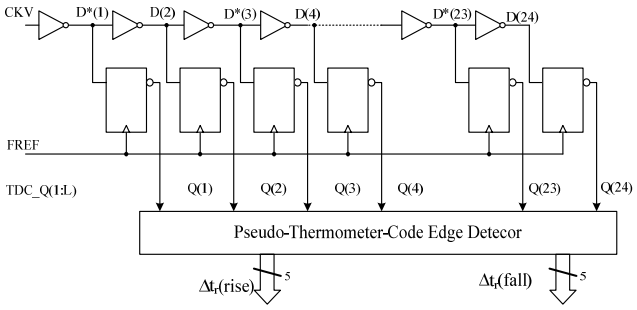

Fig. 10 Time to digital converter.

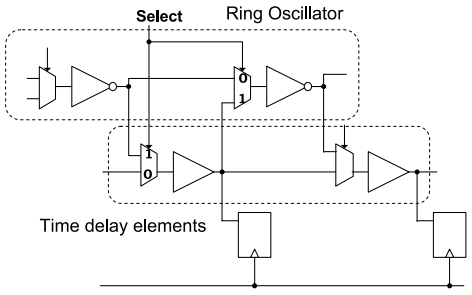

Fig. 11 TDC with delay compensation.

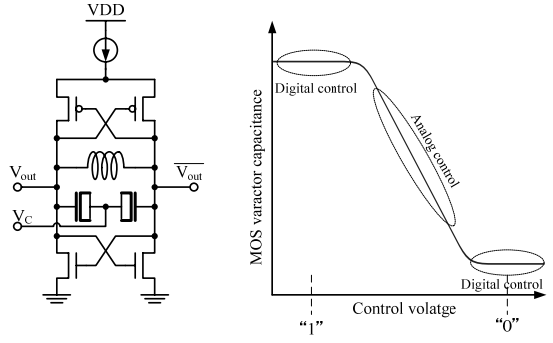

Fig. 12 Digitally controlled oscillator (DCO).

also uses varactors, however the DCO uses varactors in a different operation mode as shown in Fig. 12.

DCO uses two low sensitivity regions and changes the number of states by digital words in contrast to the sensitive region that is used in a conventional VCO. One serious issue of VCO is the increase of phase noise caused by modulation of varactor voltage in the high sensitivity operating region. Digital control in low sensitivity region is an effective solution. However one issue of this DCO is that it requires very small capacitance to realize high control resolution of oscillating frequency. A very small capacitance of less than 1 fF is required and it is not easy to realize such extremely small capacitance. The delta sigma method can relax this issue however some noise will be generated and will increase

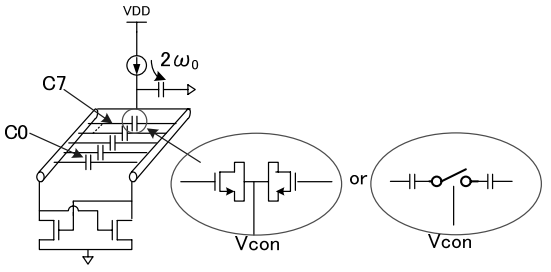

Fig. 13 DCO using distributed capacitor array along with transmission line.

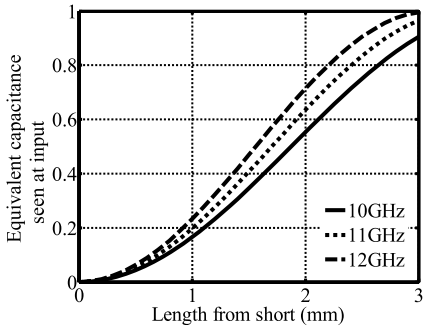

Fig. 14 Equivalent normalized reflected capacitance example, total length 3 mm.

phase noise.

To address this issue, we proposed a distributed capacitor array along with transmission line, shown in Fig. 13 [8]. The voltage of the oscillating wave has a distribution along with position. The voltage at the open end is the largest and at the short end it is smallest, thus the sensitivity of capacitor to oscillating frequency depends on the position, as shown in Fig. 14. Large sensitivity difference of more than 100 times has been measured and this effect will relax the capacitor array issue. Using this technique we will realize more fine resolution DCO with reasonable capacitance.

4.2 Sampling Mixer

A sampling mixer is an interesting idea to process the RF signal [4]. The signal processing method for RF signal is conventionally the continuous time method, however recent technology scaling enables the application of discrete time signal processing to RF signal. Figure 15 shows the sampling mixer circuit. RF signal is sampled and an array of passive switching capacitor circuits realizes the filter function without any active circuit such as operational amplifiers.

The transfer function of this circuit is;

$$|H(f)| = (1-a)\left|\frac{\sin\left(MN\pi\frac{f}{f_s}\right)}{\sin\left(\pi\frac{f}{f_s}\right)}\right| \cdot \frac{1}{\sqrt{1+a^2-2a\cos\left(N2\pi\frac{f}{f_s}\right)}}$$

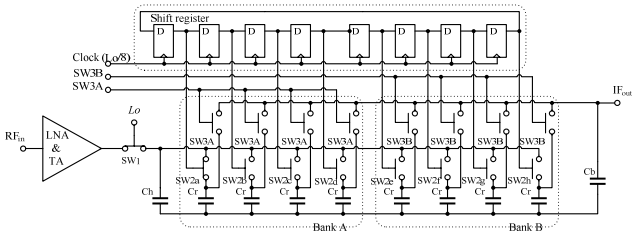

Fig. 15 Sampling mixer.

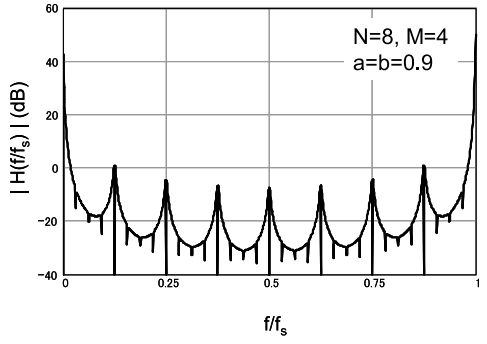

Fig. 16 Frequency characteristics of the sampling mixer.

$$\cdot \frac{1}{\sqrt{1 + b^2 - 2b\cos\left(MN2\pi\frac{f}{f_s}\right)}} \tag{5}$$

where,

$$a = \frac{C_h}{C_h + C_r} \quad b = \frac{C_b}{4C_r + C_b}$$

Figure 16 shows frequency characteristics. Relatively sharp filter characteristics as RF filter and second order filter function as a base band filter can be obtained. Also mixing function can be realized through sampling process.

This circuit technology looks interesting for future multi-band and multi-mode wireless systems; this is because the filter characteristics can be changed easily by changing the number of taps, capacitor ratios, and clock frequency. However in reality, the filter performance is not sufficient for many applications and wide change of clock frequency is not easy. Furthermore no remarkable advantage compared to conventional mixer and continuous time base-band filter has been demonstrated. This technology also needs further investigation.

Recently one interesting technique has been proposed for reconfigurable base-band filter in SDR [9]. Figure 17 shows a variable transconductance circuit.

The duty of the pulse of the switches controls an effective transconductance as shown in Eq. (6).

$$G_{m\_eff} = \frac{i_{out}}{v_{in}} = \left(\frac{T_{on}}{T_{CLK}}\right) G_{m0} \tag{6}$$

Therefore filter characteristics can be controlled by controlling clock duty ratio or transcondactance G_{m0} or

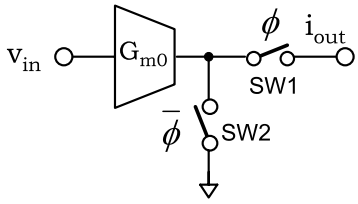

Fig. 17 Variable transconductance circuit.

both. Furthermore this control can be done by software. A wide tuning range of cutoff frequency from 400 kHz to 30 MHz has been demonstrated.

5. Conclusion

Analog-centric RFCMOS technology has played an important role to motivate the change of technology from conventional discrete device technology or bipolar IC technology to CMOS technology. However it has many issues such as poor performance, susceptibility to PVT fluctuations, and cost increase with technology scaling. The most important advantage of CMOS technology to legacy RF technology is the feature that CMOS can use more high performance digital circuits at a cheap cost. In fact, analog-centric RF-CMOS technology has failed to succeed in the FM/AM tuner business and the digital-centric CMOS technology is becoming attractive for many users. It has many advantages; such as high performance, no adjustment points, high yield, and low cost.

Therefore digital-centric RF CMOS technology, which can apply digital technology to RF circuits, must be the right way forward in integration of RF to CMOS technology. Further investing on this technology must be expected.

Acknowledgement

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