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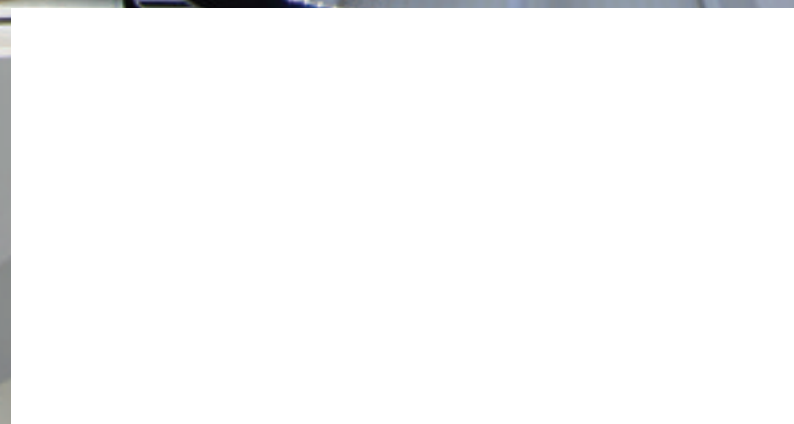
Insights for Electronics Manufacturing

450mm Gas  
Flows P.17

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## Verifying Incident Implant Angles P.12



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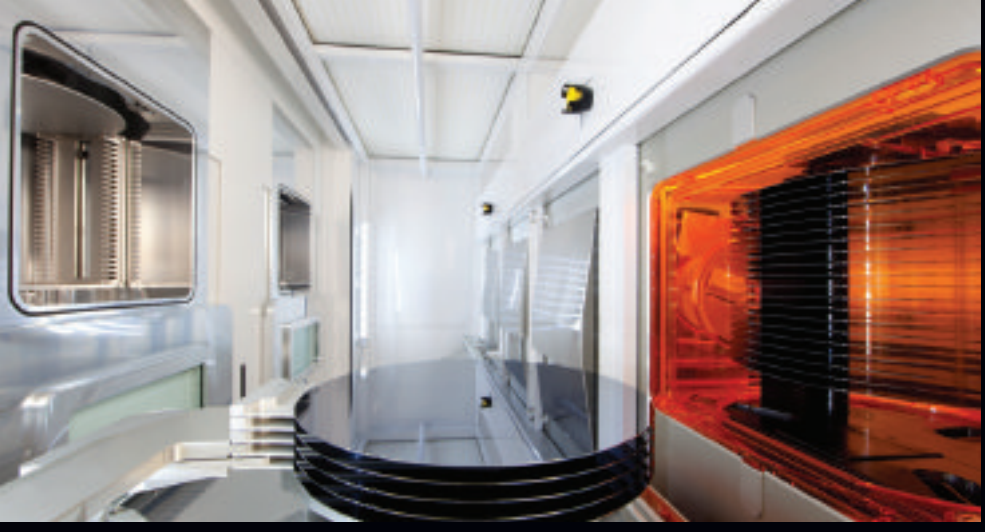
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Inside the Applied Materials VIISta Trident system, single-wafer high-current ion implantation system.

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Results can depend on the properties of the wafers used, the conditions of the implant, the conditions of the anneal process, and even the measurement technique. *Bobby Isaacs and Anya Cornell, Texas Instruments, Dallas, Tex.*

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3D atomic force microscopes can measure critical dimensions, line edge roughness and sidewall roughness in a way that is highly accurate, non-destructive and cost-effective. *Keibock Lee, Park Systems, Santa Clara, CA.*

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The choice between buying new systems from OEMs or fully capable refurbished gear from qualified used equipment vendors is examined. *Julian Gates and Tim Johnson, AG Semiconductor Services; and Darrell McDaniel, NSTAR Global Services, M+W Group*

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## Web Exclusives

### Moore's Law dead by 2022: Crying wolf?

Zvi Or-Bach, President & CEO of MonolithIC 3D Inc. blogs about recent predictions regarding the demise of continued scaling.

<http://bit.ly/1a6scct>

### The advantages of a hybrid test solution

Scan testing is the standard practice for test of integrated circuits. The vast majority of IC production test is based on automatic test pattern generation (ATPG) using the scan logic. However, some devices must be tested when there is little or no tester interface available.

<http://bit.ly/14PrSXM>

### Insights from the Leading Edge reviews the SUSTechnology workshop at SEMI-CON WEST 2013

Dr. Phil Garrou discusses the talking points from the SUSTechnology workshop.

<http://bit.ly/196IKKX>

### Next level of MEMS industry development to be examined at SEMICON Europa

Driven by value-creating applications in mobile phones, automotive, displays and other systems, the global MEMS industry has grown to over \$11 billion in 2012, a 10 percent compound annual average growth rate since 2008. The next stage of MEMS industry development is forecast to grow even faster, but industry drivers will diversify to include new technologies, new business models and new manufacturing strategies.

<http://bit.ly/17bNAID>



### Apple A7 uses Samsung's 28nm process

There has been much speculation that Apple would be moving their processor chips over to TSMC, but I think that we can now decisively say that this has not occurred – they have migrated to 28nm, but still at Samsung.

<http://bit.ly/18Pause>

### Tune in to the Solid StateWatch

Get up-to-date quickly with our weekly wrap-up newscasts, hosted by Web Editor Shannon Davis.

<http://bcove.me/e4jbu8yr>

### New kind of ultraviolet LED could lead to more portable, low-cost devices

Commercial uses for ultraviolet light are growing, and now a new kind of LED under development at The Ohio State University could lead to more portable and low-cost uses of the technology.

<http://bit.ly/1d2zrjp>

### Pitching for IC packages

Itty bitty computers, smart phones, ipods, and more – these “must have” small electronic devices that Apple Computer and other companies have popularized, are forcing the hand of IC package designers to shrink the package to fit within these little hand-held gadgets.

<http://bit.ly/18iFMI1>





# Europe's 10/100/20 program

Despite some economic woes in recent years, Europe remains dedicated to building a strong electronics industry. This was brought home to me recently when, in advance of Semicon Europa (October 7-10 in Dresden), I had a chance to talk with Heinz Kundert, president of SEMI Europe. "There are several initiatives like the KET (key enabling technology) initiative that are working on the same goals to increase the competitiveness but also to get more manufacturing back to Europe," he said. One of these is the Horizon 2020 effort, the EU's new program

The 10/200/20 program has a goal of €10 billion in R&D funding, €100 billion for manufacturing, and 20% marketshare by 2020.

for research and innovation is part of the drive to create new growth and jobs in Europe, which will run from 2014 to 2020 with a budget of just over €70 billion (some announcement during Europa is planned). France also announced Nano 2017 and plans to invest approximately €3.5 billion in France up to 2017 in nanoelectronics.

Another interesting project, specifically aimed at boosting semiconductor manufacturing in Europe is

the 10/200/20 program, which has a goal of generating €10 billion in public/private funding for R&D, €100 billion euros investment for manufacturing, and 20% share of global chip production market by 2020. Neelie Kroes, European Commission Vice-President, commented in May of this year: "I want to double our chip production to around 20% of global production. It's a realistic goal if we channel our investments properly. A rapid and strong coordination of public investment at EU, Member State and regional level is needed to ensure that transformation."

Five new pilot lines were launched in May 2013 under the ENIAC Joint Undertaking (EU public-private funding program), worth over €700 million and bringing together over 120 partners. These pilot lines allow research centers and companies to cooperate across borders to test and perfect new technologies and tools, such as: technologies and equipment for GaN-based substrates; 450mm equipment and materials; 300 mm power semiconductors; new MEMS materials and packaging; 28/20nm FD SOI.

In the past, Europe was home to around 17% of global semiconductor manufacturing, but that has declined to around 6-7% today. Turning that around to reach 20% in the next seven years will be a challenge, but where there's a will there's a way.

—Pete Singer, Editor-in-Chief

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# news

## worldnews

**WORLD | Mentor Graphics** completed enhancements to its digital tool set for **TSMC's** 16nm FinFET manufacturing processes.

**USA | RFMD** introduced the world's first 6-inch GaN-on-SiC wafers for manufacturing RF power transistors.

**EUROPE | KULeuven, imec and AIST** developed a solid phase epitaxy process to integrate GermaniumTin (GeSn) metal-oxide semiconductor field-effect transistor (MOSFET) devices on silicon.

**USA | The eBeam Initiative** released a survey that predicts that multibeam technology would be in use for advanced photomask production by 2016.

**WORLD | STMicroelectronics and X2 Biosystems** celebrate shipment of 5,000th concussion sensor system.

**WORLD | imec and Veeco** are collaborating on a project aimed at lowering the cost of producing gallium nitride on silicon (GaN-on-Si)-based power devices and LEDs.

**WORLD | Entegris and imec** announced they are collaborating to advance the development and broaden the adoption of 3D integrated circuits.

**USA | SunEdison** said it would spin off its semiconductor business in an initial public offering and use the proceeds to build solar farms.

**USA | Graphene Frontiers** was awarded a grant from the National Science Foundation to develop roll-to-roll production of graphene.

**INDIA |** India's government gave an initial approval for plans to set up two semiconductor-manufacturing facilities, but said it would seek proposals from more chipmakers before making a final decision.

## SUNY CNSE to develop center for 450mm computer chip manufacturing

The SUNY College of Nanoscale Science and Engineering and Mohawk Valley EDGE announced an expanded partnership through which CNSE will lead development of the Marcy Nanocenter site by serving as the site end user.

The EDGE-SUNY CNSE partnership is designed to accelerate the attraction of next-generation 450mm computer chip manufacturing to the Mohawk Valley. With this announcement, CNSE is broadening its partnership with Mohawk Valley EDGE and SUNYIT to further the historic agreement announced in 2011 by Governor Cuomo to establish the G450C at CNSE. Spearheaded by CNSE, the \$4.8 billion G450C has brought together five leading global high-tech companies – Intel, IBM, GLOBALFOUNDRIES, TSMC, and Samsung – at CNSE as part of a first-of-its-kind wafer and equipment development environment that will enable a transition from the current 300mm wafer technology to the new 450mm technology.

CNSE Senior Vice President and CEO Alain Kaloyeros said, "The NanoCollege's role in leading development of the Marcy Nanocenter site builds upon Governor Cuomo's visionary leadership and strategic investments in leveraging assets that not only remain under public ownership, but also attract substantially greater private industry investment. We look forward to working closely with Mohawk Valley EDGE and SUNYIT to ensure expansion of the nanotechnology research, development, commercialization and manufacturing ecosystem in the Mohawk Valley, which is further strengthening New York's innovation-enabled economy."

"The Mohawk Valley Regional Economic Development Council has made the development of the Marcy Nanocenter site and the investments in the Quad C at SUNYIT regional priorities that can have a catalytic economic impact on the Mohawk Valley region and build a technology corridor that extends across I-90," said Larry Gilroy, Co-Chair for the Mohawk Valley Regional Economic Development Council.

CNSE has already built the NanoFab Xtension (NFX) to provide state-of-the-art cleanroom facilities, tools, and infrastructure to support the research, development and pilot prototyping for 450mm wafer technology. Similarly, with the Marcy Nanocenter site, CNSE will lead development of a full-scale manufacturing facility designed to serve the world's leading high-tech companies.

A new Wetlands Permit application will be filed with the Buffalo District of the US Army Corps of Engineers that names CNSE as the end user to develop the site for semiconductor manufacturing, satisfying one of the requirements under Section 404 of the Clean Water Act. Concurrently, an application for Preliminary Development Plan approval is being filed with the Town of Marcy. Securing these local and federal approvals will enable site development and infrastructure improvements that are required before CNSE can undertake plans for initial phases of development.

CNSE and EDGE expect that a new Wetlands Permit will be issued within the next few months so that work can commence on development of the site and support critical time-to-market requirements.



As part of the CNSE development plan, the potential full build-out of the Marcy site would include: Up to 8.25 million square feet of facilities, with up to three 450mm computer chip fabs, each with a cleanroom of approximately 450,000 square feet; total public and private investment of \$10 Billion to \$15 Billion for each phase of development; and creation of approximately 5,000 direct jobs and approximately 15,000 indirect jobs. A rendering of the Marcy site of the future is shown in the accompanying figure. ◀

## Entegris to partner with SEMATECH on surface conditioning and wafer cleaning technology

Entegris, Inc. and SEMATECH announced they have partnered to move forward the development of advanced nanoscale particle removal processes and cleaning technologies for next-generation wafers and devices.

This collaboration will address some of the profound changes taking place in the semiconductor industry that are impacting fundamental aspects of process and equipment design—such as integration of new materials and process technology for sub-20nm node manufacturing, next-generation lithography requirements and the progression to 450mm wafers. One key issue relates to the preparation of critical surfaces through the entire semiconductor manufacturing process. Entegris will work with experts from SEMATECH's Nanodefekt Center to develop new

technologies and solutions to reduce nano-scale particle contamination during wafer processing.

"We are pleased to partner with SEMATECH to provide early solutions for wafer surface cleaning," said Bertrand Loy, president and CEO of Entegris. "Our goal is to leverage our contamination control expertise to develop filtration and particle detection methods for the most advanced cleaning processes."

"SEMATECH's Nanodefekt Center aims to build industry participation in detecting, modeling, characterizing, and providing solutions for defect issues as geometries shrink below the 10nm node," said Michael Lercel, senior director of Nanodefektivity and Metrology. "Our partnership with Entegris brings additional expertise to SEMATECH, and in turn will raise the level of our research efforts and further strengthen SEMATECH's commitment in identifying the challenges of future technology nodes." ◀

## New magnetic semiconductor material holds promise for 'spintronics'

Researchers at North Carolina State University have created a new compound that can be integrated into silicon chips and is a dilute magnetic semiconductor – meaning that it could be used to make "spintronic" devices, which rely on magnetic force to operate, rather than electrical currents.

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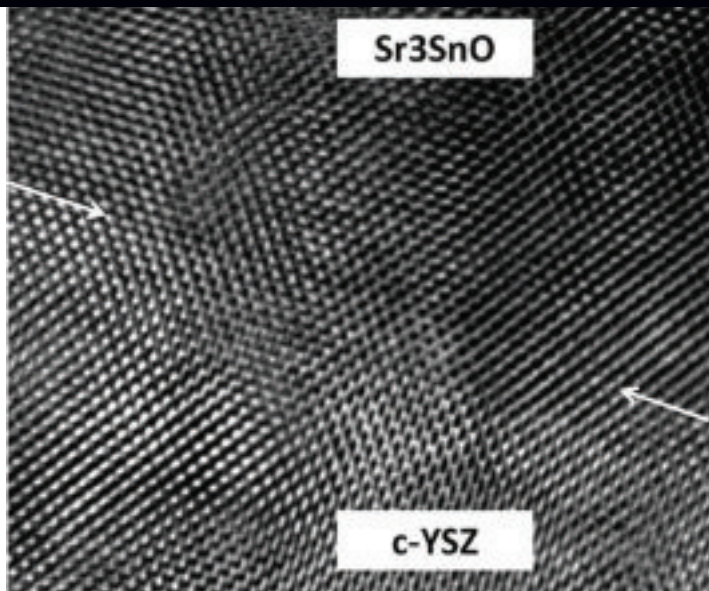
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The researchers synthesized the new compound, strontium tin oxide ( $\text{Sr}_3\text{SnO}$ ), as an epitaxial thin film on a silicon chip. Epitaxial means the material is a single crystal. Because  $\text{Sr}_3\text{SnO}$  is a dilute magnetic semiconductor, it could be used to create transistors that operate at room temperature based on magnetic fields, rather than electrical current.

“We’re talking about cool transistors for use in spintronics,” says Dr. Jay Narayan, John C. Fan Distinguished Professor of Materials Science and Engineering at NC State and senior author of a paper describing the work. “Spintronics” refers to technologies used in solid-state devices that take advantage of the inherent “spin” in electrons and their related magnetic momentum.

“There are other materials that are dilute magnetic semiconductors, but researchers have struggled to integrate those materials on a silicon substrate, which is essential for their use in multifunctional, smart devices,” Narayan says. “We were able to synthesize this material as a single crystal on a silicon chip.”

“This moves us closer to developing spin-based devices, or spintronics,” says Dr. Justin Schwartz, co-author of the paper, Kobe Steel Distinguished Professor and Department Head of the Materials Science and Engineering Department at NC State. “And learning that this material has magnetic semiconductor properties was a happy surprise.”

The researchers had set out to create a material that would be a topological insulator. In topological insulators, the bulk of the material serves as an electrical insulator, but the surface can act as a highly conductive material – and these properties are not easily affected or destroyed by defects in the material. In effect, that means that a topological insulator material can be a conductor and its own insulator at the same time.

Two materials are known to be topological insulators – bismuth telluride and bismuth selenide. But theorists predicted that other materials may also have topological insulator properties.  $\text{Sr}_3\text{SnO}$  is one of those theoretical materials, which is why the researchers synthesized it. However, while early tests are promising, the researchers are still testing the  $\text{Sr}_3\text{SnO}$  to confirm whether it has all the characteristics of a topological insulator. ◀

## Chip carrier packaging grows on widespread adoption of QFN package

Advanced packaging of semiconductor chips has emerged as a key enabler in many of today’s electronic system products. Put another way, package selection is increasingly important to the success of the end product. While much attention with regard to IC packaging is on 3D stacking and integration technologies, there is another area of packaging that has quietly been flourishing during the past decade-and-a-half.

Introduced in 1998, the quad flat no-lead (QFN) package design (including the related dual-sided DFN) has enjoyed phenomenal growth from the very beginning. With its low cost, small size, and excellent thermal and electrical performance characteristics, the QFN quickly became the mainstream package of choice for many low-to-medium I/O count ICs. In the past decade, new dual-row and even triple-row technologies have enabled QFNs to support many more I/Os and, thus, enter a wider range of IC product segments. Today, the QFN is one of, if not the, most widely used IC package types.

IC Insights forecasts that the continuous high growth in demand for QFN-type packages will help push the flatpack/chip carrier (FP/CC) category of packages past the “old” small outline (SO) group of packages for the first time ever in 2013. The QFN is a type of chip carrier. The SO packages emerged in the early 1980s and then grew to become the industry’s most widely used package type by 1995. The FP/CC packages emerged around the same time and they offered higher I/O capabilities than the SO packages because they had leads on all four sides. The QFN package category in the JEDEC standards includes a variety of manufacturer-specific designs such as the MicroLeadFrame (MLF) package from Amkor, Fujitsu’s Bumped Chip Carrier (BCC) and small outline no-lead (SON) packages, Carsem’s Micro Leadframe Package (MLP), and ASE’s microchip carrier (MCC). There



are similar JEDEC standards for DFN packages that have external bond pads or "lands" on two sides instead of four like the QFN. Besides being categorized in the FP/CC group of packages, QFNs and DFNs are also considered part of a larger group of packages called leadframe CSPs, or chip-scale packages.

QFN and DFN packages are inexpensive to manufacture—they typically don't have solder balls, are targeted at low-I/O applications (typically <85), and make use of pre-plated leadframes. Either wirebonds or flip-chip bumps are used to attach the IC to the leadframe. Versions like the MLF and BCC have an exposed die-attach paddle on the bottom of the package, which serves as an excellent thermal path away from the chip as well as a good ground-plane if the pad

is grounded on the circuit board. That, in conjunction with the high electrical performance offered by short I/O connections, has made these leadframe CSPs attractive for use in packaging RF circuits for cellphones and other wireless and portable product applications.

Many companies have migrated from SO-type packages to QFNs and DFNs and their popularity continues to spread as new advancements make QFNs/DFNs capable of handling a greater amount of circuitry and functionality. The QFNs with dual rows of lands can support as many as 180 I/Os. There are also a growing variety of QFNs/DFNs such as versions with multiple chips stacked inside, or types that have an air-cavity designed into the package for high-frequency microwave applications.◀

## Gartner predicts 14% growth in 2014 equipment spending

Gartner predicts that 2014 semiconductor capital spending will increase 14.1 percent, followed by 13.8 percent growth in 2015. The next cyclical decline will be a mild drop of 2.8 percent in 2016, followed by a return to growth in 2017.

That rosy prediction is a huge improvement over the numbers from 2013. Worldwide semiconductor manufacturing equipment spending is projected to total \$34.6 billion in 2013, an 8.5 percent decline from 2012 spending of \$37.8 billion, according to Gartner. The firm said that capital spending will decrease 6.8 percent in 2013, due to diminishing 28nm investment from a softening in the mobile phone market.

"Weak semiconductor market conditions that continued into the first quarter of 2013 generated downward pressure on new equipment purchases," said Dean Freeman, research vice president at Gartner. "However, semiconductor equipment quarterly revenue is beginning to improve, and positive movement in the book-to-bill ratio indicated that spending for equipment will pick up in the remainder of 2013. Looking beyond 2013, we expect that the current economic malaise will have worked its way through the industry, and spending will follow a generally increasing pattern in all sectors throughout the rest of the forecast period."

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Logic spending has been the key driver of capital spending in 2013; however, a softening in the mobile phone markets has dampened investment in 28nm during the third quarter, and this is projected to continue into the fourth quarter of 2013. Memory spending has picked up some of the slack and the total spending in the second half of 2013 should outpace the first half of the year.

Gartner said that capital spending is highly concentrated among a handful of companies. The top three companies (Intel, TSMC and Samsung) account for more than half of 2013 spending. Spending by the top five semiconductor manufacturers exceeds 65 percent of total 2013 spending, with the top 10 accounting for 76 percent of the total. 2013 spending will be back-half-loaded, with capacity increases occurring as memory market conditions improve, and Intel prepares for initial 14nm production late in the year.

"In 2013, the wafer fab equipment (WFE) picture is one of continuous quarter-over-quarter growth as major manufacturers come out of a period of high inventories and a generally weak semiconductor market," said Mr. Freeman. "Early in the year, the book-to-bill ratio passed 1-to-1 for the first time in months, signaling that the need for new equipment is strengthening because demand for leading-edge devices is improving."

Gartner predicts that wafer fab manufacturing capacity utilization will hover in the high-70 percent to low-80 percent range during the first half of 2013 and building to the mid-80 percent range at the beginning of 2014. Leading-edge utilization will move into the low-90 percent range by the end of 2013, providing for a positive capital investment environment.

The capital spending forecast estimates total capital spending from all forms of semiconductor manufacturers, including foundries and back-end assembly and test services companies. This is based on the industry's requirements for new and upgraded facilities to meet the forecast demand for semiconductor production. Capital spending represents the total amount spent by the industry for equipment and new facilities.

The WFE forecast estimates market revenue based on future global sales of the equipment needed to produce the wafers on which semiconductor devices are fabricated. WFE demand is a function of the number of fabs in operation, capacity utilization, their size and their technology profile. ◀

## Applied Materials and TEL to merge

Applied Materials, Inc. and Tokyo Electron Limited (TEL) announced a definitive agreement to create a global innovator in semiconductor and display manufacturing technology via an all-stock combination which values the new combined company at approximately \$29 billion (¥2.8 trillion). This combination, which has been unanimously approved by the Boards of Directors of both companies, brings together complementary leading technologies and products to create an expanded set of capabilities in precision materials engineering and patterning that are strategically important for customers. The closing of the transaction is subject to customary conditions, including approval by Applied Materials' and Tokyo Electron's shareholders and review by regulators. The companies expect the transaction to close in mid to second half of 2014.

Tetsuro Higashi, Chairman, President and CEO of Tokyo Electron, said, "Today, we are launching a new company and taking a bold step forward for our industry. Built on a foundation of people, technology and commitment, we are creating a truly global company that we believe will expand the value we deliver to our customers and be able to achieve new levels of financial performance."

Gary Dickerson, President and CEO of Applied Materials, said, "We are creating a global innovator in precision materials engineering and patterning that provides our new company with significant opportunities to solve our customers' high-value problems better, faster and at lower cost. We believe the combination will accelerate our momentum for profitable growth, increase the value we deliver to shareholders and create great opportunities for our employees."

The combined organization is intended to accelerate the existing strategic visions of Applied Materials and Tokyo Electron and increase the new company's opportunity to enable major, future technology inflections and advance customers' roadmaps in both semiconductor and display. Extraordinary advances in semiconductor and display technology have made it possible to mass produce affordable personal electronics, putting PCs, smartphones, tablets and other amazing devices in the hands of consumers around the world.



Today, the mobility trend is driving a new phase of industry growth and introducing dramatic and fundamental technology changes in the way devices are made. Materials innovation is the most significant lever for customers to drive cost-effective performance gains in mobile chips and displays. With the best and broadest capability in materials engineering, Applied Materials and Tokyo Electron believe this new company will be well-positioned to provide valuable, differentiated device performance and yield solutions that enable the new device architectures and cost-effective scaling that customers need to win.

Said Higashi and Dickerson jointly, "We are building this new company in the spirit of a merger of equals. For five decades, we have each made significant contributions to the semiconductor industry and we have deep respect for the capabilities that the other brings to this combination. Both companies have a strong heritage of customer service and an enduring commitment to push the boundaries of technology and engineering. We share many common values and are confident we will execute together to achieve our strategic and financial goals."

As a clear signal of the commitment to create a new global enterprise, the company will have a new name, dual headquarters in Tokyo and Santa Clara, a dual listing on the Tokyo Stock Exchange and the NASDAQ, and will be incorporated in The Netherlands.

The new company will have a shared leadership team. Tetsuro Higashi will serve as Chairman, and Gary Dickerson will serve as Chief Executive Officer. The board will be made up of eleven directors with five directors appointed by each company and one additional director to be mutually agreed upon. Seven of the eleven directors will be independent. Bob Halliday of Applied Materials will serve as Chief Financial Officer.

Under the terms of the agreement, Tokyo Electron shareholders will receive 3.25 shares of the new company for every Tokyo Electron share held. Applied Materials shareholders will receive 1 share of the new company for every Applied Materials share held. After the close, Applied Materials shareholders will own approximately 68% of the new company and Tokyo Electron shareholders approximately 32%.

The companies expect to achieve \$250 million in annualized run-rate operating synergies by the end of the first full fiscal year and \$500 million in run-rate operating synergies



realized in the third full fiscal year. In addition, the new company expects to realize meaningful savings as a result of the new corporate structure. The new company intends to commence a \$3.0 billion stock repurchase program targeted to be executed within 12 months following the close of the transaction. On a non-GAAP basis, taking into account the buyback, the transaction is expected to be EPS accretive at the end of the first full fiscal year after transaction close. ◀

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# Silicon interposers, CoWoS and microbumps

At the recent ECTC conference, various presentations addressed silicon interposers for 2.5D (Shinko), CoWoS reliability (TSMC) and microbumping (imec).

Shinko and CEA Leti detailed their presentation entitled “Warpage Control of Silicon Interposer for 2.5D Package Applications.”

Large silicon-interposers when attached to an organic substrate can cause significant warpage problems. Shinko/Leti examined several warpage control techniques including:

- Using a “chip first process” where chips are mounted on the interposer first vs “chip last process” where the silicon-interposer is mounted on the organic substrate first and chips are mounted onto the interposer last.
- Using various underfill resins.
- Using Sn-57Bi solder and thus lowering peak temperature 45-90 degree C. This reduced warpage after reflow to 75% of that using SAC305.

Warpage of silicon-interposer using three types of underfills for 0 level assembly (micro bumps) were investigated. Maximum warpage using U.F. A1, A2 and A3 were 108, 123 and 132mm, respectively. The lowest warpage was obtained at using U.F. A1. With U.F.A3, solder bump open failures were observed. The authors conclude that “using underfill material with low Tg and high storage modulus for 0 level leads to high reliability.”

TSMC and customer Xilinx presented “Reliability Evaluation of a CoWoS-enabled 3D IC Package” which used FEA to study the thermo-mechanical response of the interposer-based package during thermal cycle reliability stressing. Focus was especially on the fatigue failures of the C4 and BGA joints. Experimental data collected on CoWoS test vehicles

were used to validate the FEM models. Parametric study of key package material and geometric parameters was performed to analyze their

effects on C4 bump thermal cycle reliability. Package materials of interest include UF (underfill), lid and substrate, and the geometric parameters include lid thickness and C4 bump scheme.

Results showed that the CoWoS package using AlSiC lid has better C4 bump life than the CoWoS package using Cu lid. While a thicker lid has the higher stiffness and better co-planarity, the higher constraint from the thicker lid induces higher stress inside the package which negatively impacts C4 bump fatigue and the micro-bump Ti/Al delamination.

C4 bump layer underfill with Tg of 70°C or 120°C, were studied. The underfill with lower Tg has higher driving force to C4 bump fatigue. When temperature is above Tg, the underfill has much lower Young’s Modulus which has much lower capability to protect C4 bump; and therefore the underfill with lower Tg has higher driving force to C4 bump fatigue. On the contrary, the underfill with lower Tg has lower driving force to Ti/Al delamination in the micro-bump structure. The C4 underfill with lower stiffness can play as a buffer layer and results in lower driving force to Ti/Al delamination in microbump.

imec reported on “Key Elements for Sub-50µm Pitch Micro Bump Processes.” Scaling the microbump pitch from hundreds to a few tens of microns is not straightforward. Several process parameters need to be taken into account to allow a reliable Cu(Ni)Sn ubumping process. One of the challenges for fine pitch Cu(Ni)Sn stacking is to obtain a high bump uniformity. The non-uniformity prevents Cu and Sn from having good contact and subsequent intermetallic formation and increases the risk of underfill entrapment.

A bump scheme that offers better margin for alignment error is better based on a scheme where the size of top die bumps is smaller than the size of the bottom pads. For example it is better to achieve 20µm pitch with 7.5µm bump on 12.5µm pad than with 10µm bump and pad because equal bump and pad diameter can tolerate only 2µm misalignment whereas the 7.5µm/12.5µm bump/pad can tolerate 5µm. This is a significant difference when working close to the stacking tool’s limit of alignment accuracy.

Details on the plasma treatments necessary when attempting to plate into these fine featured plating resists are also discussed ◀▶



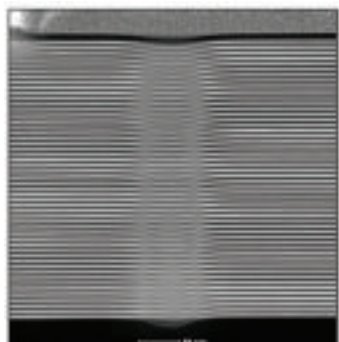
**Dr. Phil Garrou,**  
Contributing Editor

## Packaging





# Defect-free mask blanks next EUV challenge



**FIGURE 1.** A small pit on the substrate surfaces gets magnified through the multilayer stack.

*The next major roadblock to progress in the ongoing push to develop EUV lithography for volume production is the availability of defect-free mask blanks.*

According to Veeco's Tim Pratt, Senior Director, Marketing, the tools in place today are not capable of producing mask blanks with the kind of yield necessary to

support a ramp in EUV. "Based on the yield today, the mask blank manufacturing capacity can't produce enough mask blanks to support the ASML scanners that they're planning to ship," Pratt said.

The requirement for 2015 is to have zero blank defects larger than 62nm. SEMATECH in 2012 reported work showing eight defects larger than 50nm. "A lot of progress being made but the elusive zero defects has not yet been hit," Pratt said. Veeco, which is the sole supplier of EUV multilayer deposition tools, has plans to upgrade the existing Odyssey tool and launch a new platform in the 2017/2018 timeframe.

An EUV mask is considerably more complicated than conventional photomasks. The EUV mask begins with a substrate. On the back of the substrate you have some material that's used for chucking (an electrostatic chuck is used to hold the mask to a stage in the ASML tool and in the Veeco ion beam deposition tool). On top of the substrate is a multilayer sandwich made

up of 40-50 moly silicon pairs that creates a mirror.

A ruthenium capping layer helps protect the mask. The top layer is an absorber, and that's what gets patterned.

**FIGURE 1** shows a small pit on the substrate. "As the multilayer gets deposited on top of it, you take what in the beginning might have been a small pit and at the top it becomes 1.5X or so larger," Pratt said.

Where is EUV today? Billions have already been invested to build the EUV infrastructure with particular emphasis on the light source. Chipmakers have invested in ASML, and ASML acquired light-source provider Cymer. There has also been a very large Industry investment in Zeiss to build the AIMS tool, which is a defect detection and repair system at EUV wavelengths.

In July, ASML said NXE:3300 scanner imaging and overlay performance reached levels where they are engaging with customers on a strategy for the 10nm logic node insertion (23nm half pitch). Good imaging performance was shown down to 13nm half pitch, and overlay between the NXE:3300 and NXT systems, had been demonstrated at less than 3.5nm. Good performance, stability and reliability of the pre-pulse source concept was demonstrated with a rate of around 40 wafers per hour, and ASML expressed confidence in reaching the goal of 70 wafers per hour productivity in 2014.

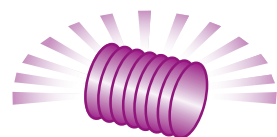
What could derail the EUV ramp, according to Pratt, is a supply of defect-free mask blanks. "EUV is, despite many years and many dollars of investment, not yet in production. The two main gaps are the EUV light sources and the defects on the mask. As they start to make progress, people start to look more seriously at the list of things to worry about for EUV going to production. Number one on that list is the mask defects," Pratt said. "The most dangerous (un-repairable) defects come from the ML (multilayer) coating process during mask blank manufacturing. You can't clean them and you can't repair them and if you have more than some very small amount, there's really nothing you can do about it. You just have to throw that mask blank away and try again," Pratt said.

Veeco is addressing the defect challenge in two ways. The short-term solution is an Odyssey upgrade. The long-term solution is a new platform. "The Odyssey upgrade improves the yield of the tool. But then longer term we think the next gen is needed, especially as you get out to years 4 and 5 where high volume manufacturing starts to occur," Pratt said. ♦



**Pete Singer,**  
Editor-in-Chief

## Semiconductors



# How to verify incident implant angles on medium current implants

**BOBBY ISAACS** and **ANYA CORNELL**, Texas Instruments, Dallas, Tex.

*Results can depend on the properties of the wafers used, the conditions of the implant, the conditions of the anneal process, and even the measurement technique.*

Semiconductor chip geometries continue to shrink, causing once unimportant parameters in the manufacturing process to become more critical. With the shrinkage in transistor size and requirements for improved precision in devices, ion implantation has become an increasingly more delicate and accurate operation. Implantation angle has become extremely important as transistors have decreased in size and voltage specifications. Adjustment and pocket implants, channeling implants, and high accuracy sidewall and HALO implants have become requirements for high performance, with little to no tolerance for incorrect implantation placement.

Older generations of ion implanters have been designed with only cursory regard to the extreme precision now required for implant placement. Because of this, semiconductor manufacturers must regularly monitor the implantation angle of these tools as part of normal production operations. In this monitoring, multiple potential issues exist that could cause a misinterpretation of the proper implantation angle, resulting in faulty tool calibration or production of out of tolerance product. This article will describe several variables to be considered when defining the angle of implant for a tool, and offer recommended conditions to achieve reliable and repeatable performance on two older implant tool sets.

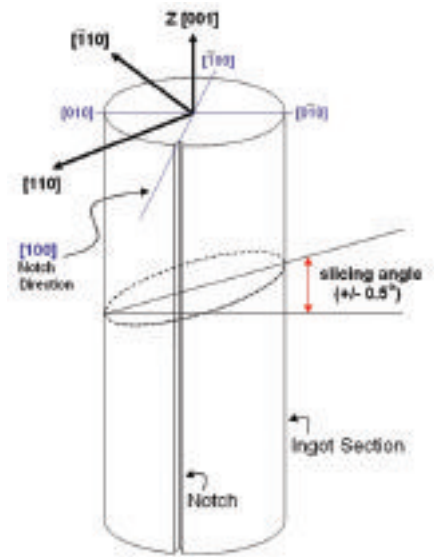
The standard production test to determine if the

angle of implant is accurate involves implanting 5 to 7 wafers tilted around a theoretical channeling angle, annealing the wafers to activate the implant, and charting the sheet resistance vs. implanted angle to find the channel.

This procedure is commonly called a V-curve test. The as-measured channeling angle (found by identifying the minimum sheet resistance of the charted curve for the wafers, or the bottom of the “V”) should be equal to the theoretical channeling angle if the tool set-up is accurate. Unfortunately, the number of steps required by this procedure introduces errors that could lead to a false result. The properties of the wafers used, the conditions of the implant, the conditions of the anneal process, and even the measurement technique can all significantly affect the outcome.

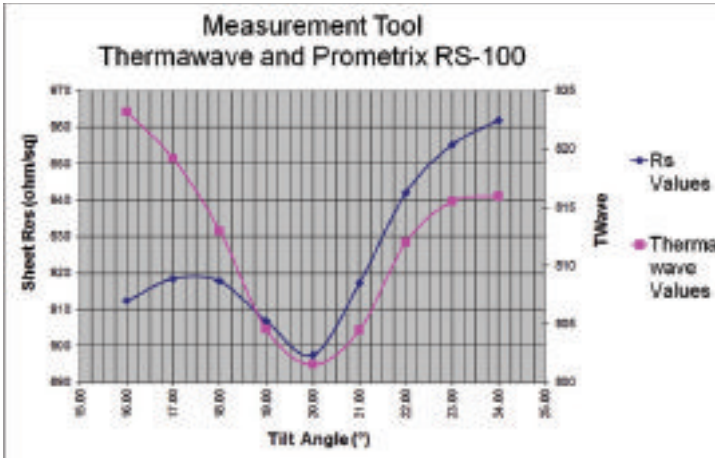
## Experimental

One of the most commonly overlooked variables that can introduce significant error into measurement of the angle

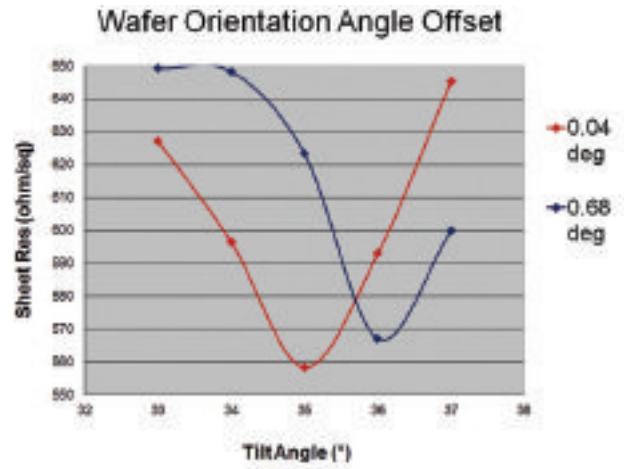


**FIGURE 1.** Illustration of wafer slicing angle and associated offset.

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**FIGURE 2.** Comparison of Varian E500 V-curves generated using Thermawave vs TRS-100.



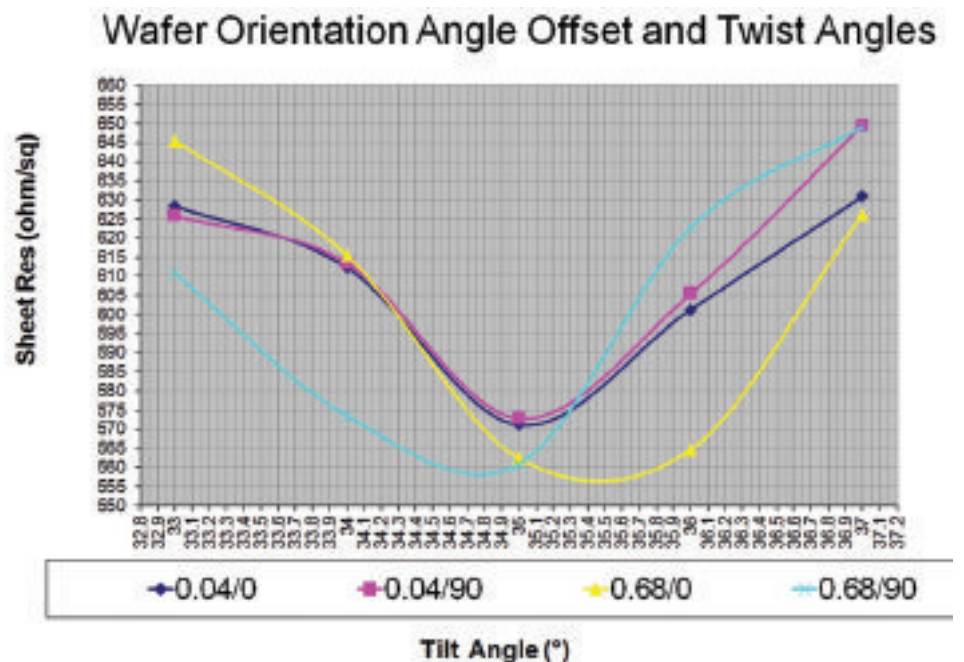
**FIGURE 3.** Effect of wafer orientation angle offset on V-curve of Axcelis Optima MD.

of implant is the wafer which is used for the testing. One relevant silicon property of the wafers, the surface orientation angle offset (angle tolerance of the on-axis cut), has a significant effect. All wafers have a base surface orientation angle offset, as required by the process of slicing the wafers from the ingot (**FIGURE 1**).

This offset can directly translate into an offset in the V-curve measurement, depending on the angular rotation of the slice. It has been shown in previous work[3] that channeling is minimized at implant angles higher than 0.5°. In this work, the effect of the orientation angle offset on channeling was similarly studied. Implants were performed with 200mm, <100>, N-type (phosphorus-doped) CZ wafers of resistivity 3-5 Ω-cm, surface orientation angle of 0.0+/-1°(on-axis <100>), Oi spec of <=32 ppm (ASTM-79), and LLS of <20 @0.20µm. The wafer type was chosen for use with Boron implant (P-type dopant) and the <100> orientation was picked for its good channeling properties. Using the above specification, wafers were chosen at various extremes of the angle window (close to 0° and close to 1°) in order to characterize the effect of wafer angle variation. Other silicon properties shown in the spec above, such as surface defects, oxygen concentration, and

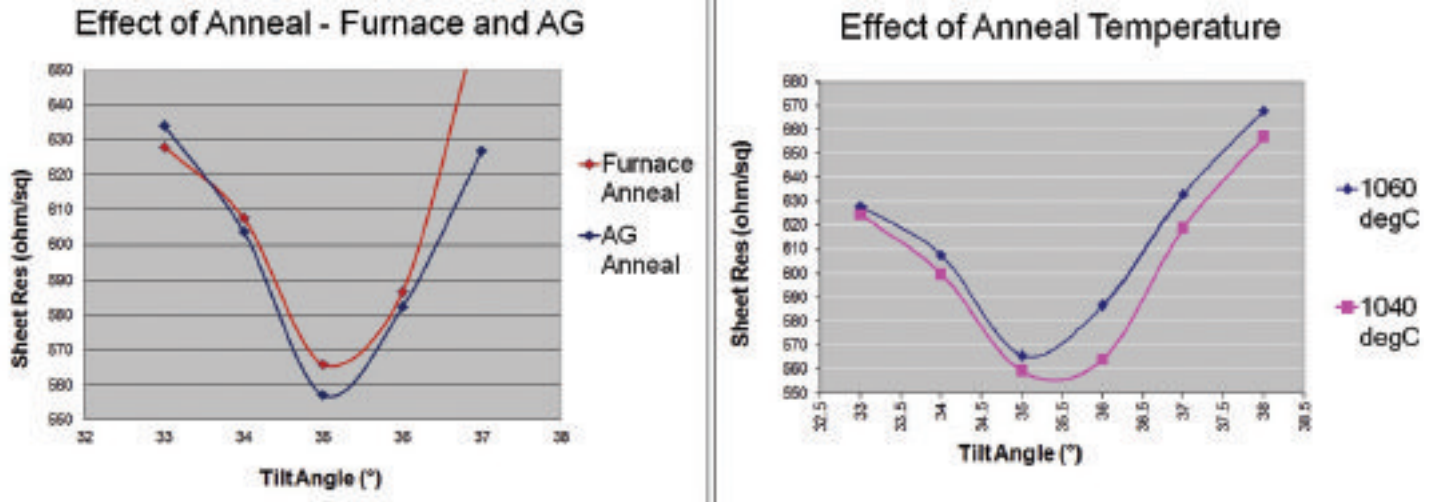
resistivity are in the standard range for a typical test wafer. These parameters have a lesser effect on the implant angle measurement and were not explored in this study.

The two implant tool types used were an Axcelis Optima MD implanter and a Varian E500 implanter. Implant conditions were chosen as follows based on experimentation and comparison of common processes among multiple manufacturing facilities utilizing several tool types: Boron11 at 100 keV energy, 1.0e14 ion/sq dose, 35° tilt, and 0° twist. Boron11 was chosen as the dopant for its small mass and channeling properties, as discussed in Downey, et.al.[2] Energy of 100 keV is high enough to



**FIGURE 4.** Effect of wafer orientation angle offset and wafer rotation on V-curve of Varian E500.





**FIGURE 5.** Effect of anneal tool and temperature on V-Curve of Varian E500.

prevent outgassing of the dopant during the anneal process, and  $1.0 \times 10^{14}$  ion/sq dose was chosen to place the resultant resistance as measured on a standard Tencor RS-100 into a stable range for the measurement equipment.[1] For all tests, the ion beam was optimally tuned to minimize beam instability or non-linearity. The potential process variables influencing beam steering on the tool were not explored during this experimentation, but it should be commented that an improperly tuned ion beam will also significantly affect the result. A tilt angle of  $35^\circ$  was chosen as the optimal channeling condition. Although multiple potential channeling angles exist for [100] N-type silicon wafers, the angle of  $35.26^\circ$  has shown the most sensitive, clear channel for implant angle testing[1], and it is also recommended by Varian Semiconductor[4]. A twist angle of  $0^\circ$  was applied for best resolution of the channel in all but one of the tests, which utilized a rotation angle of  $90^\circ$  to characterize the effect of the wafer substrate angle offset.

The anneal process needed to be selected in such a way as to eliminate any variation or sensitivity due to temperature of anneal, anneal time, or even annealer tool type. An anneal temperature of  $1060^\circ\text{C}$  for 30 seconds was selected from earlier work[1] as the condition at which small temperature variations can be tolerated. Two types of annealer tools were used – an Axcelis Summit furnace annealer, and an AG Associates 8800 lamp annealer – to determine if the V-curve could be shifted through anneal by varying the tool type.

Measurement of sheet resistance is well documented for ion implant processing. For this experimentation, Thermawave and Tencor RS-100 measurement tools were researched to identify possible areas of concern in

the measurement of V-curve wafers. The advantage to Thermawave processing is the elimination of the need for anneal after implant, removing this source of potential variation. Also, a previous experiment with a different implant has shown that the Tencor RS-100 produces a sharper V-curve than the Thermawave (see sample V-curve in **FIGURE 2**). Therefore, the Tencor RS-100 tool was chosen for the present work. Testing on the Tencor RS-100 was performed using both 9-point and 49-point radial measurement patterns.

### Results and discussion

By far the strongest effect was observed from the silicon wafer orientation angle offset. In particular, at angles above  $0.5^\circ$ , the effect was so pronounced that it shifted the V-curve. See below graph of two sets of wafers processed with identical implant and anneal conditions. The only difference was the orientation angle offset ( $0.04^\circ$  vs  $0.68^\circ$ ), as shown in **FIGURE 3**.

In an effort to further characterize the effect of a larger orientation angle offset of the wafers, testing was performed by rotating the wafers  $90^\circ$  during the implant to measure the change in the resultant V-curve. Using wafers with very small surface orientation offset angles ( $0.04^\circ$ ), the change in the measured V-curve could not be easily seen. However, using wafers with a surface orientation offset angle above  $0.5^\circ$  ( $0.68^\circ$ ), the change in the measured rotated V-curve became much more visible (**FIGURE 4**). Repeatability of the tests using high surface orientation angles was also noted to be inconsistent, with significant variance in results from test to test.

Based on the results presented above, it is our recommendation that high-angle offset wafers (above  $0.5^\circ$ ) should not be used for implant angle qualifications. It is also recommended that the surface orientation angle of the test wafers be scrutinized if the V-curve produced shows abnormal variance from the expected outcome. To reduce variability from other wafer parameters, we also recommend a tight resistivity specification (ex: 3-5 ohm-cm) for the silicon ingot, and advocate the use of wafers not only from the same ingot, but from the same area of the ingot, to ensure similar properties.

Minor effects were observed from other variables studied. An experiment comparing two anneal temperatures confirmed earlier findings<sup>1</sup> of 1060C being the optimal temperature to produce a sharper V-curve (**FIGURE 5**). The type of anneal tool was also a factor. Although the process was matched as closely as possible through matching of the thermal budget, a difference could be seen between the annealer types (Fig. 5, left). Based on the clarity of the V-curve inflection on the lamp annealer, this tool was used as the benchmark for anneals during other experiments.

As for the Sheet Resistance measurement, very little to no effect was observed from varying the measurement pattern and number of measured points.

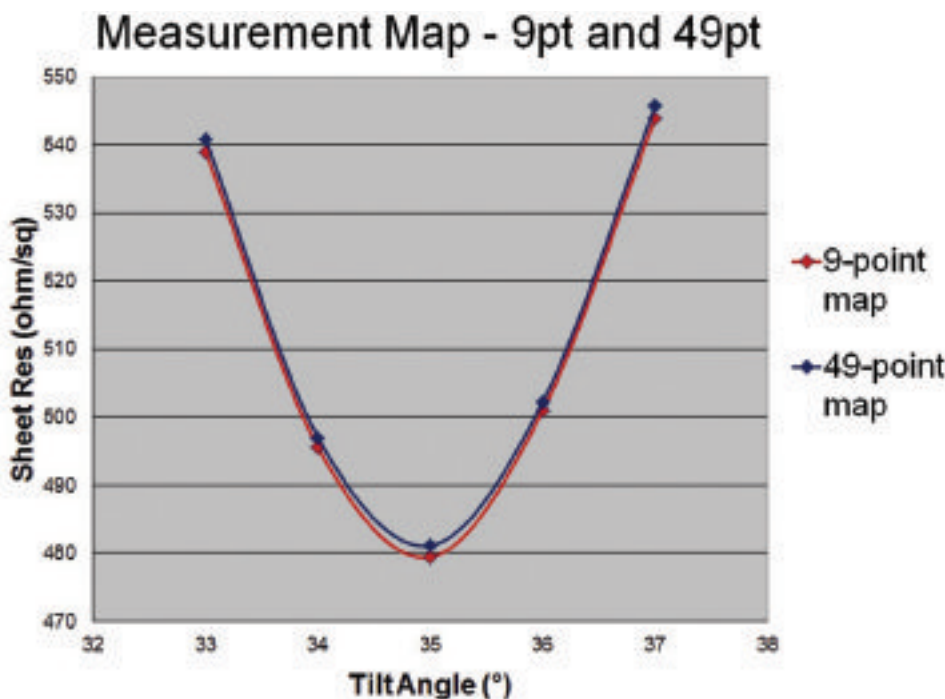
A 9-point measurement showed the same accuracy as a 49-point measurement, making the additional points unnecessary (**FIGURE 6**).

### Conclusion

As a result of this testing, multiple recommendations can be made to ensure accurate and repeatable measurement of the implant angle of a tool. These areas can result in significant variation of results if not accounted for during testing. The silicon quality of the wafers is one of the most overlooked variables in performance of implant angle measurement. The surface orientation angle offset can significantly change the measured implant angle, especially in ranges above  $0.5^\circ$  (from on-axis  $\langle 100 \rangle$  cut). Wafers with angle cut tolerance greater than  $0.5^\circ$  produce inconsistent results, severe enough to shift the sheet resistance values or even the entire V-curve, and are therefore not recommended for implant angle testing.

The parameters used in implantation also contribute significantly to the resolution and accuracy of a V-curve test. Although multiple potential channeling angles exist for [100] N-type silicon wafers, a  $35^\circ$  angle is recommended as the most sensitive, clear channel for implant angle testing.[1,4] The implanted species, energy, and dose all contribute to the stability and repeatability of the measurements. Once implanted, the anneal of the wafer must be tuned to a temperature and thermal budget that minimizes variation, as this will also cause slight changes in results. Finally, measurement techniques can change the outcome of a V-curve test through differences in the measurement tool used.

Once the angle of implant of a given tool is characterized, regular verification (qualification) is highly recommended, especially for events which involve components handling wafer orientation. To save on wafer cost, a test may be performed using 1 or 3 wafers once the baseline sheet resistance of the channeling angle



**FIGURE 6.** Effect of measurement map resolution on V-Curve of Axcelis Optima MD.

is obtained, and charted through standard SPC techniques. If a failure is observed, escalation of the testing can then include a full 5 or 7 wafer V-curve test to determine if the angle of implant has shifted. Standard troubleshooting for common sheet resistance failure events should be included in disposition of a failure, since hardware issues in the form of leaks, contamination and other failure modes can influence the sheet resistance measurement obtained during angle testing.

### Acknowledgments

The authors would like to thank TI silicon material technologist Thomas McKenna for valuable insight into starting material properties, as well as Jeff Bell of SUMCO-USA for providing substrate orientation angle data. ◀▶

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# 450mm higher gas flows pose opportunities

**DR. MIKE CZERNIAK, ANDREW CHAMBERS** and **ADRIENNE PIERCE**, Edwards, Clevedon, UK.

*The move to 450mm wafers will likely result in gas flow increased on process vacuum and abatement equipment.*

**T**he semiconductor industry is gearing-up for a transition in silicon wafer diameter from 300mm to 450mm, driven by the requirement to reduce device manufacturing costs. This transition is the latest in a series of wafer size increases, as illustrated in **FIGURE 1**. The transition to 450mm wafer high volume manufacturing is currently predicted to occur sometime beyond 2020.

With each new generation, the corresponding process gas flows have increased in order to maintain throughput for the larger wafers and the larger process chambers they required. A similar increase in process gas flow rates is anticipated for the 300mm to 450mm transition, but with industry demands to reduce overall utility consumption while simultaneously increasing productivity, there is pressure to reduce the gas flow scaling factor relative to the 2.25 times geometrical scaling factor of the larger wafer surface area. Nevertheless, a significant increase in gas flows is still anticipated.

## Impact of increased gas flows

When process gases or by-products are corrosive, flammable, condensable, or contain significant quantities of solid material, nitrogen is often added into the pump mechanism itself and/or into the downstream exhaust pipe. So, higher process gas flows will drive a proportional increase in nitrogen purges added to the exhaust, which in turn, will augment the vacuum and abatement capacity required by 450mm processes. This nitrogen serves a number of important purposes:

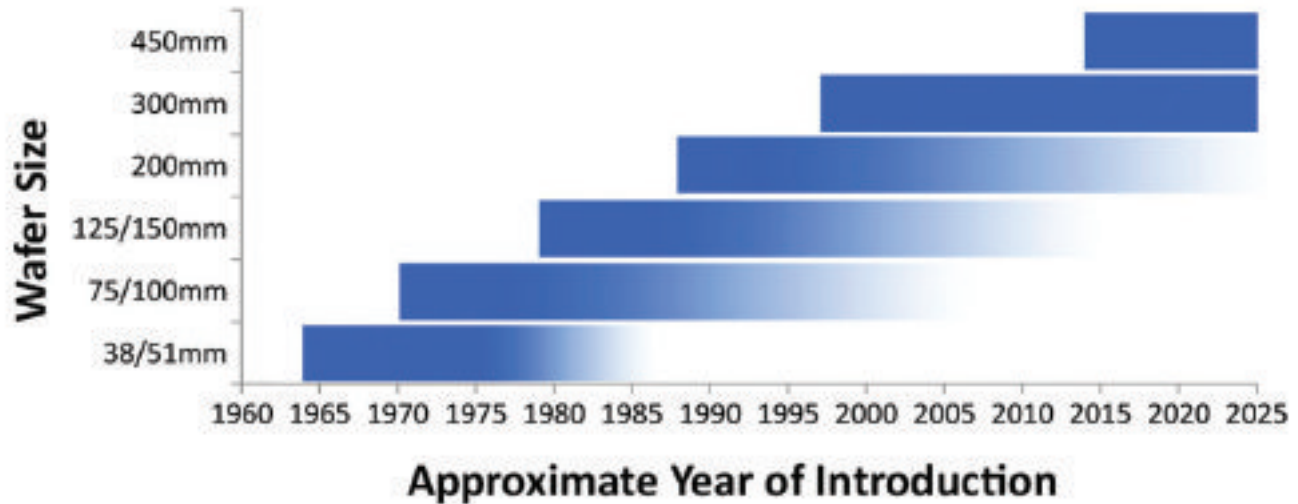
- 1) diluting corrosive gases to reduce damage to pump components,
- 2) diluting flammable gases to avoid flammable mixtures when either an oxidant is also present or in the event of an air leak into the system,
- 3) diluting condensable gases to avoid condensation of damaging materials onto equipment surfaces,
- 4) assisting the pumping of light gases, and
- 5) increasing the gas velocity to ensure that entrained particulate matter keeps moving through the pump mechanism and exhaust pipe.

In practice, the total nitrogen purge and dilution flow rate is scaled with the process gas flow to maintain overall system reliability or to meet a specific operational requirement, for example, dilution of a flammable gas to avoid a potential flammable mixture.

For vacuum pumps, higher process gas flows require the deployment of larger capacity pumps, increasing not only the capital cost and but also the total operating cost due to higher nitrogen and pump power consumption. Furthermore, the increased flow rates also affect the capacity requirements of point-of-use (PoU) gas abatement systems. The impact of the increased gas flow on the abatement system is similar to that on the vacuum pumps, namely, higher capital cost for greater capacity, potentially physically larger systems, higher operating costs for more fuel or electricity to heat the gas to a sufficient reaction temperature for destruction, and more water to cool the system and scrub reaction by-products from the exhaust stream.

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**DR. MIKE CZERNIAK**, is a product marketing manager, **ANDREW CHAMBERS**, is technical manager and **ADRIENNE PIERCE** is business development manager with Edwards, Clevedon, UK.



**FIGURE 1.** Historical evolution of Si wafer diameter in the semiconductor industry.

### Integrated vacuum and abatement

The most obvious scenario for the 450mm transition would simply scale the capital and operating requirements of vacuum and abatement systems to match the increased gas flows. While this approach would still capture the economic efficiencies accruing from a gas flow scaling factor that is lower than the wafer surface area scaling factor, it misses other significant opportunities to enhance overall efficiency and realize even larger reductions in cost per unit area - the intended goal of the 450mm transition.

Since 450mm wafer processes are still under development, the gas flows that will ultimately be deployed are unknown at this time. However, it is possible to investigate methods to reduce nitrogen dilution or purge flow rates now, based on 300mm processes and 450mm projections. With clear process specification, the optimal pump design can be selected, and the requirement for purging of the pump mechanism itself can be reduced. For instance, the use of chemically-resistant seals would allow exposure to higher concentrations of corrosive gases. Similarly, running the pump at higher operating temperatures could allow the passage of higher concentrations of condensable gases without the build-up of solids. Examples include  $\text{NH}_4\text{Cl}$  from low pressure CVD (LPCVD) nitride deposition processes and  $\text{AlCl}_3$  from metal etch processes.

The practical limitation to reducing nitrogen purge flows is often the pipeline that connects the pump exhaust to the PoU gas abatement system, which can be

very long. Because the gas in this pipe is at approximately atmospheric pressure, the risk of corrosion is greater than at the reduced pressure found in the vacuum foreline and the gas is often diluted to avoid damage to the equipment. Likewise, condensable gases are most prone to condense into solids and block the pipe when the pressure is higher, and the typical response to this problem is to increase the nitrogen purge flow rate. A flammable gas may be diluted to prevent fire or explosion if the gas leaks into the fab environment.

A viable solution is to make the pump exhaust pipe very short, which minimizes the volume of enclosed gas and reduces the cooling that occurs over extended pipe runs, as illustrated in **FIGURE 2**. While it is common practice to actively heat long pump exhaust runs, the power used for heating can exceed the power consumed by the pump itself. In addition, bends, valves and joints all need to be properly heated and insulated otherwise they act as sites for solids accumulation and blockages. To minimize the risk of flammable, toxic or hazardous gas escaping into the fab environment, the vacuum pumps and gas abatement can be housed in a common extracted enclosure held at lower pressure than the fab, ensuring that any leaking gas does not escape into the fab. By monitoring the cabinet extraction, the presence of a gas leak can be detected and suitable alarms raised for remedial action, while the leaking gas remains confined within the equipment enclosure and factory personnel are protected from exposure.

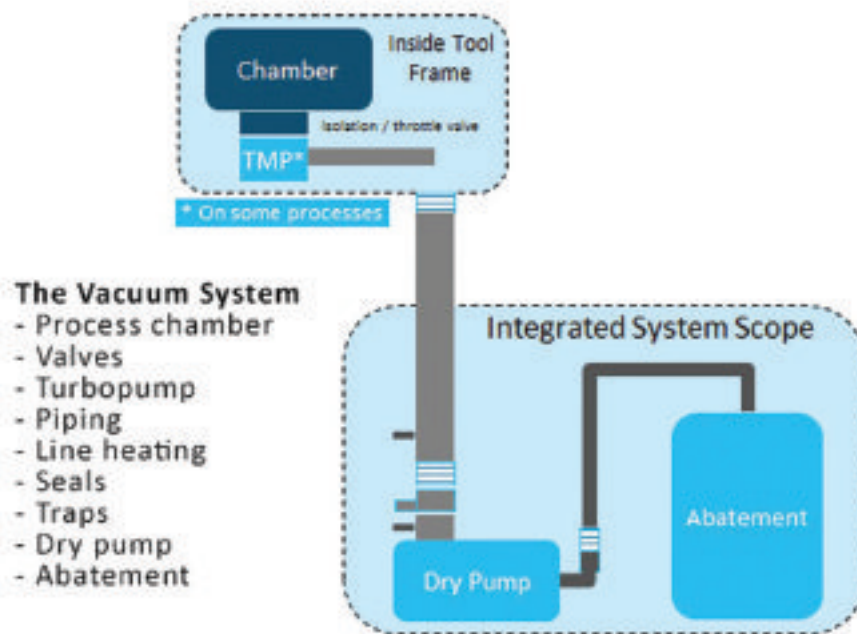
The opportunity to optimize exhaust pipe config-

uration and system operation while minimizing nitrogen purging equipment size and utility costs constitutes a major benefit for adopting an “integrated system” approach to vacuum and abatement. An expertly integrated design can resolve potential conflicts between reducing utility costs and ensuring operational safety in the presence of flammable or reactive gases. New approaches to safe equipment operation can be better implemented and more readily accepted, in the context of an integrated system in which the various elements are designed to be complementary and mutually supportive. The integrated supervisory monitoring and control system can be designed to ensure safe operation, monitor leak integrity, detect equipment malfunction, and shut-off process gas if a critical situation arises. The integrated system also offers better alignment with sub-system performance requirements under specific process conditions driving optimized BKMs (Best Known Methods). For example, during a deposition versus a clean process, and a purge only mode can be added when appropriate.

Additional benefits of sub-fab equipment integration include:

- Reduced overall equipment footprint compared to traditional “stand-alone” configurations.
- Reduced utilities hook-up requirements, since facilities connections can be shared between vacuum and abatement systems, reducing hook-up cost and installation time.
- Easier implementation of “Green Mode” utility-saving strategies - the process tool only needs to send one set of signals to the integrated system controller to trigger low power or idle mode operation.
- Overall system ownership and the reduction of unintended consequences.

Integrated vacuum and abatement systems, such as the one shown in figure 3, are installed and operating at more than fifteen 300mm fabs across



**FIGURE 2.** Integrated vacuum and abatement.

the full spectrum of process applications. The higher overall costs and productivity requirements for 450mm processing make the arguments for adopting integrated systems even more compelling. The industry has a unique opportunity to incorporate and enhance these cost-saving system considerations in the 450mm fab. Collaborative 450mm initiatives are at the forefront of “changing the game” to reduce the higher overall costs while improving the value of wafer throughput and reducing the manufacturing cost by area of device produced.

### Summary

The transition from 300mm to 450mm is underway and it is likely to be accompanied by significant increases in not only process gas flows, but also the consequential nitrogen purges used in process vacuum pumps and downstream exhaust systems. Simply increasing pump and abatement capacity will result in increased capital and operating costs proportional to the increased flow. An alternative strategy is to integrate the vacuum pumps and gas abatement into a combined system with optimized exhaust pipe configuration, process exhaust temperature control, a common extracted housing, single utilities connection points and a single supervisory control system. These integrated systems with better tool communications interfaces have the potential to increase the value of the 450mm transition by further reducing operating costs. ◀



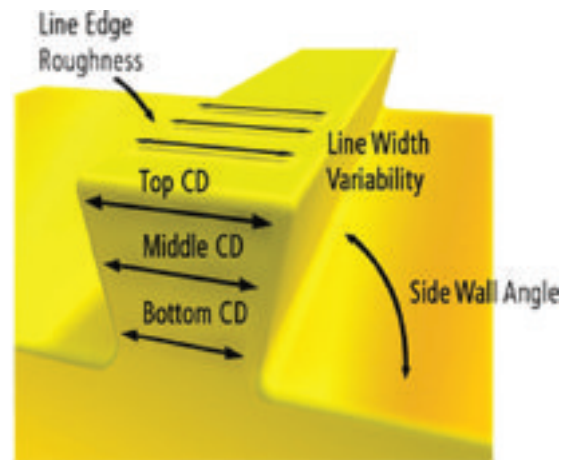
# Three-dimensional atomic force microscopy

**KEIBOCK LEE**, Park Systems, Santa Clara, CA.

*3D atomic force microscopes can measure critical dimensions, line edge roughness and sidewall roughness in a way that is highly accurate, non-destructive and cost-effective.*

One of the most challenging features in the semiconductor industry is the continuous research and the subsequent fabrication of integrated circuits with enduringly smaller critical dimensions (CDs). As shown in **FIGURE 1**, CDs must be measured at the top, middle and bottom of features, as well as various parameters such as line edge roughness (LER), the line width roughness (LWR) and the sidewall roughness (SWR).

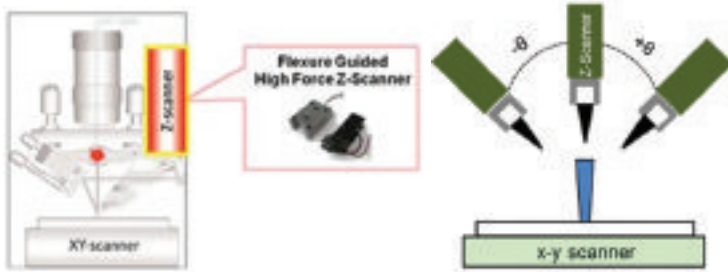
The characterization of such factors that determine the shape and the roughness of the device patterns for device manufacturers is of utmost importance due to the fact that they directly affect the device performance. Optical measurement techniques, which are limited in terms of resolution. Therefore, the existing prevalent method for measuring these factors prior was primarily the scanning electron microscopy (SEM) with its image analysis software. Despite the fact that this technique offers substantial advantages such as automation and compatibility with standard critical dimension SEM tools, it cannot provide the user with high resolution LER data due to the fact that SEM resolution is reaching its limits, therefore 3D AFM offers a highly desirable solution. Leading manufacturers have implemented AFM that can measure resist profile, LER and SWR in a way that is highly accurate, non-destructive and cost-effective. The precise and full characterization of such features is extremely essential during the pattern transfer process as it offers the possibility of imaging all surfaces of the pattern.



**FIGURE 1.** LER, LWR and SWR are the limiting factors of resolution in optical lithography.

## What is non-contact 3D AFM?

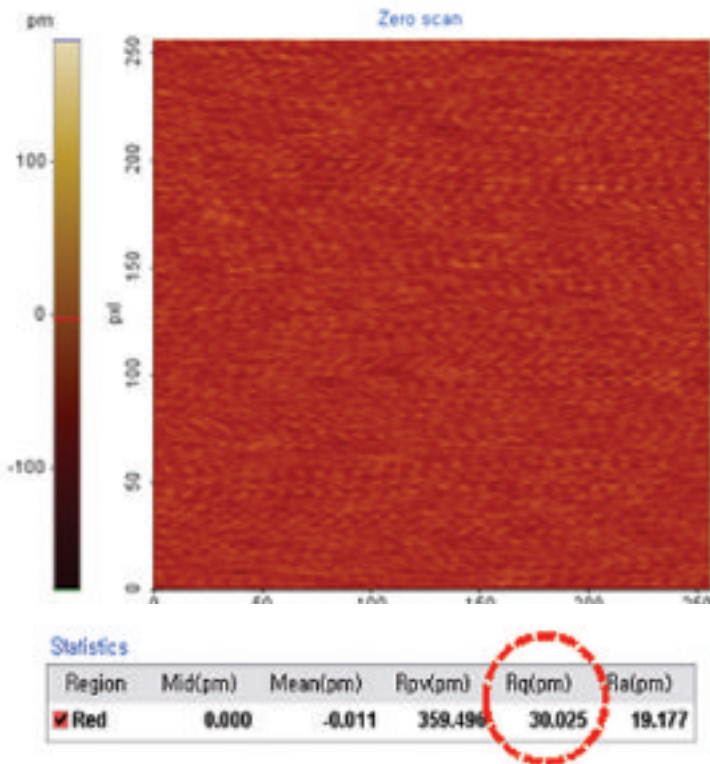
The basic principle of non-contact 3D-AFM is that a cantilevered beam rapidly oscillates just above the surface of the imaging sample. This offers several advantages, as compared to the traditional contact and intermittent modes. One of the advantages is that there is no physical contact between the tip and the surface of the sample. Moreover, as depicted in **FIGURE 2**, the Z-scanner, which moves the tip, is decoupled from the XY scanner, which solely moves the sample, thus, offering flat scanning and an additional benefit of improved Z-scan bandwidth. Furthermore, by tilting the Z-scanner, the sidewall of the nanostructures can be accessed and roughness measurements performed along the sidewall of photoresist lines. At the same time,



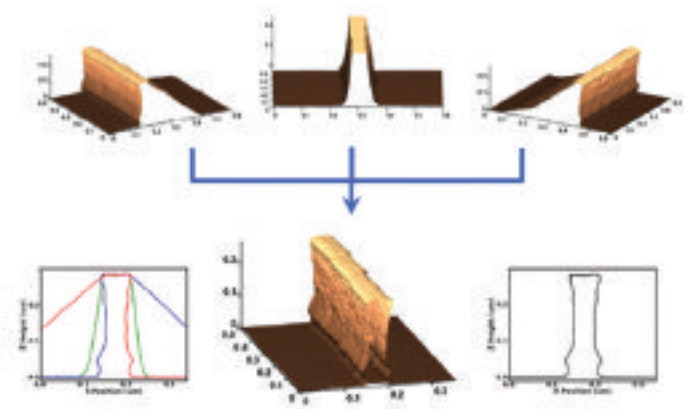
**FIGURE 2.** The independent tilted Z-scanner enables measurements of the sidewalls of features.

measurements of the critical dimensions of top, middle, and bottom lines can be made.

Data acquisition is performed by a conical tip in predefined tilted angles, typically  $0^\circ$ ,  $a$ , and  $-a^\circ$ . Consequently, and by combining these three scans (a method called image stitching), the 3D pattern can be constructed, as shown in **FIGURE 3**. This provides an excellent and extremely accurate method that takes advantage of the interference pattern of the standing waves in order to measure features such as the total height, the top, middle, and bottom width. 3D AFM is capable of advanced three-dimensional imaging of both isolated, and dense line profiles. It is less costly than the alternative techniques (CD-SEM and focused ion beam (FIB)) for imaging and measuring



**FIGURE 4.** 3D AFM noise levels on a 300 mm wafer. The system noise level is less than 0.05 nm at every position and typically 0.02~0.03 nm RMS.



**FIGURE 3.** Combination of the three acquired images for 3D AFM pattern reconstruction.

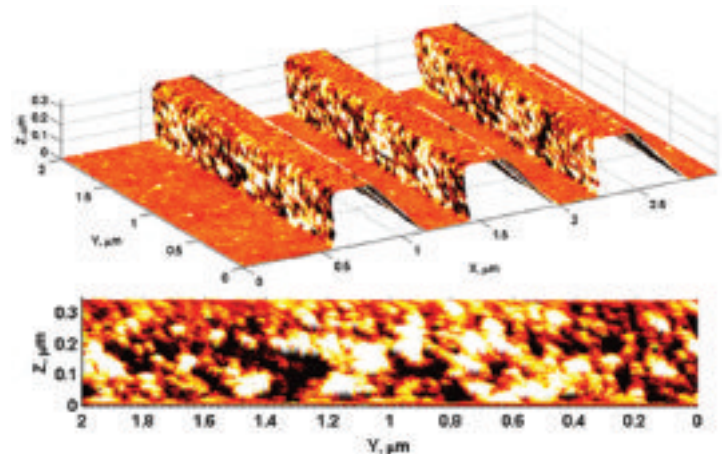
parameters of line profiles since the preparation of the sample is by far simpler.

### Noise levels in 3D-AFM

A critical requirement when dealing with metrology tools is associated with constraining the level of noise in the manufacturing environment. A study of noise levels on a 300 mm wafer (**FIGURE 4**) shows the overall 3D AFM system noise at levels are lower than 0.05 nm (0.5 angstrom).

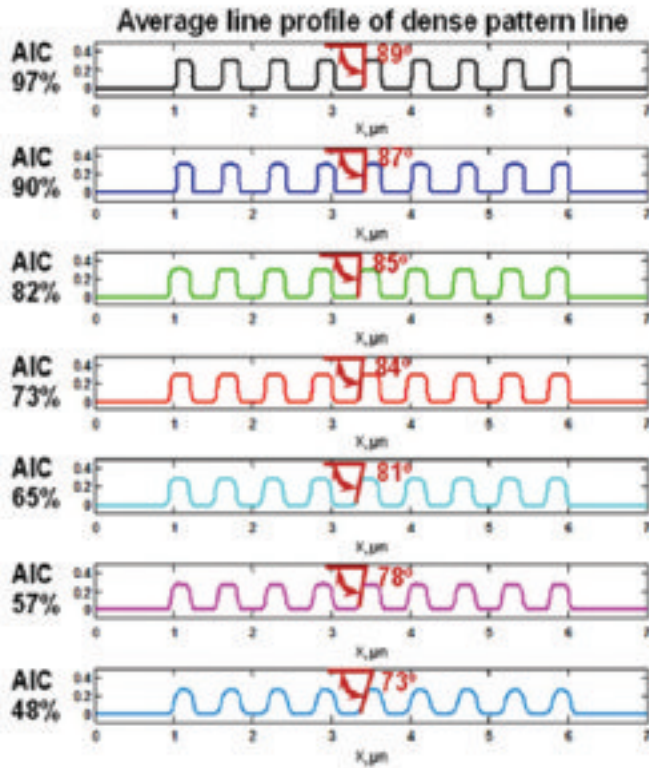
### Roughness measurements

Roughness can be transferred into the final etched profile, thus, roughness measurements can describe and determine the quality of the patterns. The tilted Z scanner in combination with the low noise levels that are prevalent during the AFM process can provide accurate results in terms of sidewall roughness measurements. **FIGURE 5** depicts the 3D AFM imaging of a photo-



**FIGURE 5.** 3D AFM image of a photoresist semi-dense line pattern imaged with Z-scanner tilt. The bottom figure clearly depicts the grainy structure of the sidewall.





**FIGURE 6.** Park 3D AFM line profiles at different AIC levels reveal the proportionate relationship between SWA and AIC.

resist semi-dense line pattern and the respective grainy structure of its sidewall. The precision with which the SWR was measured is validated by the high repeatability (0.08nm 1 sigma for 5 sites wafer mean) for the sidewall roughness of about 6.0 nm.

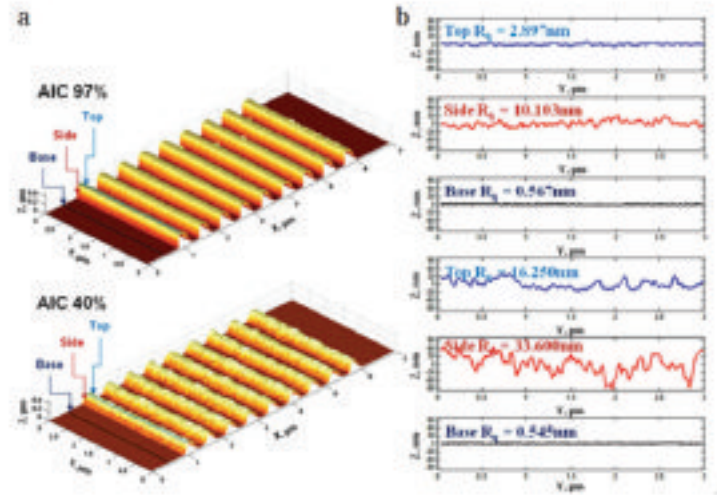
It needs to be noted that roughness depends, amongst others, on the aerial image contrast (AIC) or in other words the physics of exposure. AIC is determined as the quotient between the subtraction and

$$AIC = \frac{I_{max} - I_{min}}{I_{max} + I_{min}}$$

the addition of the maximum and minimum image intensities.

Several consequent series of images with variable exposure reveal that LER significantly increases when the AIC is decreased, a fact that underlines that AIC is a controlling factor for LER. Moreover, and as depicted in **FIGURE 6**, reduced levels of AIC produced line profile images of the resist that were more blunted, and also smaller sidewall angles (SWA).

**FIGURE 7** illustrates the capability of Park 3D AFM to image all surfaces of the pattern, in contrast to the conventional AFM or the SEM, which cannot fully characterize the surface data, and obtain information such as base, top and both sidewall roughness from



**FIGURE 7.** A 3D AFM image of a 300 nm photoresist line pattern yields full information regarding the morphology of the sidewall (top) Side-wall Roughness is different at different AIC levels, a fact that indicates the connection between LER and SWR (bottom).

sidewall characterization. A 300 nm photoresist line pattern was imaged and the respective line profiles were obtained that clearly showed a substantial difference in terms of SWR between 97% and 40% AIC. More specifically, the lower the value of AIC, the more increased was the measured roughness. This intense decrease of roughness is underlying the fact that LER and the measured sidewall roughness are clearly correlated.

Finally, it needs to be emphasized the role of non-contact 3D AFM in terms of preserving the tip sharpness of the cantilever. In an independent study, researchers performed 150 consecutive measurements using the same tip and the tip wearing proved to be minimal. This is a prominent feature of AFM that prevents the continuous costly replacement of the tip but also ensures that the sample will be viable and not damaged by the AFM cantilever. The preservation of the tip sharpness allows for continual measurements of high resolution roughness data.

### Conclusions

The potentialities of the innovative, non-destructive imaging technique of 3D AFM has several advantages compared to conventional SEM systems. An independent and tilted Z-scanner overcomes the disadvantages of alternative metrology tools and measure parameters such as detailed sidewall morphology and roughness, and sidewall angle characterization that render the optimization and evaluation process easier and far more detailed. ◀



# Managing legacy fabs and the role of secondary equipment

**JULIAN GATES** and **TIM JOHNSON**, AG Semiconductor Services; and **DARRELL MCDANIEL**, NSTAR Global Services, M+W Group.

*The choice between buying new systems from OEMs or fully capable refurbished gear from qualified used equipment vendors is examined.*

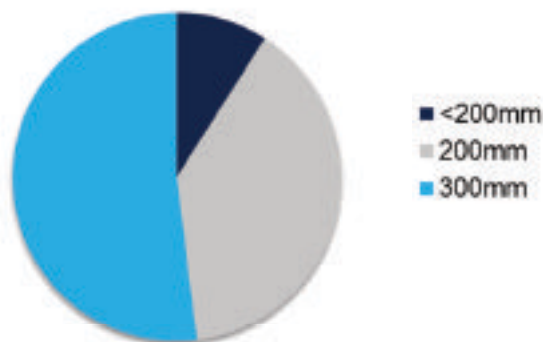
A significant portion of semiconductor production continues to take place in facilities equipped with 200mm or smaller equipment, which run processes for analog, mixed-signal, power ICs, and other mature device types. Recent data from Semico shown in **FIGURES 1** and **2** reveal that 39% of the silicon consumed is devoted to 200mm, with another 9% going for wafers of <200mm, while technology nodes of 130nm and above account for approximately 50% of the silicon used.

Managers of these legacy fabs must balance tight process and time-to-market requirements with limited capital and operational budgets to stay competitive with

low-cost producers. As the major original equipment manufacturers devote more of their budgets to 300mm tooling (or even 450mm) and invest less into their 200mm efforts, older semiconductor factories need high-quality sources of used systems and components as well as the tribal process knowledge that goes with them. The emergence and growth of the market for refurbished 300mm production tools has added even more complexity and challenges.

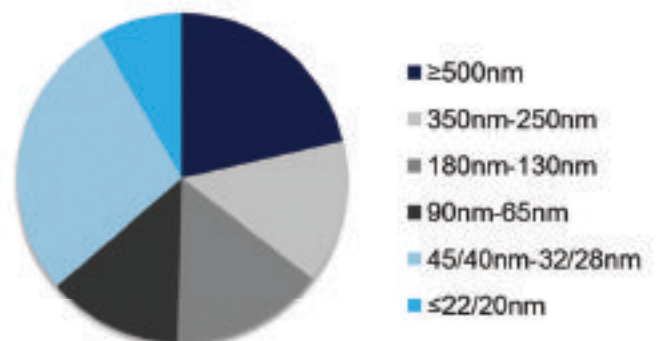
After growth fueled by thousands of tools coming on the secondary market in the mid- to late 2000s followed by an extended recession-fueled downturn, the secondary equipment market is seeing increased

**Figure 1: Silicon Demand by Wafer Size**



**FIGURE 1.** 39% of the silicon consumed is devoted to 200mm, with another 9% going for wafers of <200mm.

**Figure 2: 2013 Wafer Demand by Technology Node**



**FIGURE 2.** Technology nodes of 130nm and above account for approximately 50% of the silicon used.

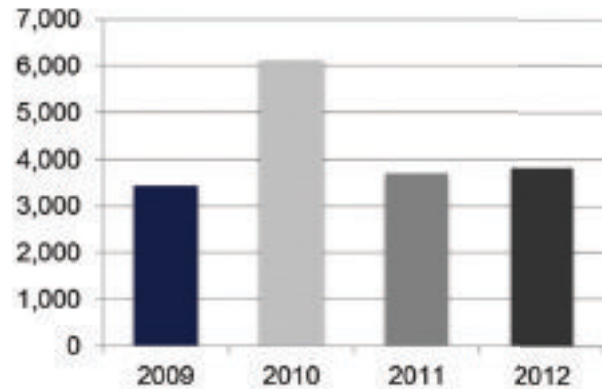
**JULIAN GATES** is a managing partner at AG Semiconductor Solutions, **TIM JOHNSON** is senior director at AG Semiconductor Solutions and **DARRELL MCDANIEL** is president at NSTAR Global Services, a Company of the M+W Group.

order activity and is expected to grow into a \$3 billion-plus sector this year (see **FIGURE 3**). During this cycle, the companies specializing in procuring, modifying, reconfiguring, refurbishing, installing, qualifying and offering ongoing warranty and service support for those thousands of pieces of process equipment have become key partners with the likes of Texas Instruments, GLOBALFOUNDRIES, ON Semiconductor, STMicroelectronics, Fairchild, Maxim, Tower, and other IDM, foundry and OEM firms.

### High quality, low cost

One key question facing legacy fab operators is how to upgrade their processes and factories or expand their capacity in a timely and cost-effective manner. When there is a choice between buying new systems from OEMs or fully capable refurbished gear from qualified used equipment vendors, whether the mission is to convert from a 150mm to a 200mm line or push to a more advanced technology node, the difference in price can range from hundreds of thousands of dollars to a few million dollars per tool for big-ticket systems such as lithography steppers and scanners. The price tag for secondary equipment ranges from as little as 20-30% of what a new tool would cost, depending on the age, condition, availability, and provenance of the system, to a tighter 70-80% of the new-tool price. In some cases, fab management may have to choose between different pieces of used gear, as the OEM either does not manufacture those particular 200mm systems or is no longer in business.

Considering the risk-averse personalities of most fab engineers, they need to be assured that any tool, new or used, that they bring onto their factory floor will produce the level of product needed, at profitably high yields and a compelling cost of ownership and productivity metrics. They also want to see lead times for equipment delivery, installation and qualification narrowed as much as possible. This means secondary equipment providers must now offer a detailed and exhaustive evaluation of any tool that comes into inventory, working up a detailed configuration, baseline and dataset for prospective buyers. To meet demand, suppliers often maintain large inventories in cleanroom-equipped warehouses located in strategic global locations that can provide and qualify fully process capable equipment in a matter of weeks



**FIGURE 3.** The secondary equipment market is expected to grow into a \$3 billion-plus sector this year.

not months (**FIGURE 4**). The old model of aggressively brokered, “what you see is what you get” used equipment of unknown condition sitting in unopened containers has been replaced by a value-added, collaborative approach that brings new tool-like quality and reliability to the secondary space as well as a dedicated support team of experts with deep knowledge about older equipment and processes.

### Exceeding specifications

Despite the increased quality of secondary equipment and related services, there are still instances when process engineers might be taken out of their comfort zone and must be convinced that the used solution will meet or exceed requirements. A recent example involved the acquisition of surplus toolsets from a leading-edge IC manufacturer by a secondary equipment company,



**FIGURE 4.** Used semiconductor equipment in AG Semiconductor Services' Nijmegen, The Netherlands refurbishing facility.

	IDM/ Foundry	OEM	Used Equipment Vendor
Cannot get replacement parts	•	•	
Cannot get replacement parts in a timely manner	•	•	•
Cannot get replacement parts at a reasonable price	•	•	•
Cannot get parts because suppliers of components and board manufacturers are discontinuing parts		•	
Current suppliers cannot afford to maintain parts and services for all technologies. Older parts are dropped more frequently	•	•	
Cannot get equipment documentation which includes part specifications and equipment schematics	•	•	•
Cannot notify customers when a part is being discontinued because there are too many parts to keep track of		•	•
The industry continues to move quickly to new technologies. Parts are becoming obsolete faster.	•	•	
Some parts that were also used in other industries, such as aerospace and other industrial, are also moving on to new technologies.		•	•
Government regulations have changed, restricting the use of certain materials, making it impossible to manufacture exact replacement parts.		•	•
Cannot get software support	•		•
Cannot find skilled labor to provide technical services	•		•
License fees to operate equipment are too expensive	•		•
Equipment vendors can no longer support the tool maintenance, yet will not release licensing rights or tool schematics for others to utilize.	•		•

**TABLE 1:** Legacy fab equipment issues (Source: Semico Research, 200mm Equipment Obsolescence Study).

which then sold the systems to a 200mm foundry operation seeking to expand its capacity. The original specifications of the tools indicated that they would be functional up to the 180nm process node, but the previous owners of the equipment had successfully extended the equipment capability down to at least the 130nm node. After their initial reticence, the foundry engineers were convinced of the refurbished tools' enhanced capability through a combination of compelling performance data such as etch and via depth results as well as domain expertise and consultation provided by the secondary equipment provider. The resulting upgrade saved the customer millions of dollars in avoided new capital equipment expenditures.

### Spare parts conundrum

A study on 200mm equipment obsolescence conducted by Semico for ISMI focused on issues surrounding legacy fabs' tool issues. As **TABLE 1** shows, chief concerns of the chipmakers, OEMs, and secondary tool companies include the inability to find replacement parts at

a reasonable price, the struggle to get equipment documentation that includes part specifications and equipment schematics, and the difficulty in notifying customers when a part is being discontinued because of the large number of parts to keep track of. In addition to the general issue of parts obsolescence, other underlying causes can be tracked back to the OEMs use of subcontractors and subsequent loss of control over their spares inventory, as well as the general trend of consolidation among the process equipment manufacturer ranks and premature exit from active 200mm development and production. One industry group, the Fab Owners Association, has come up with a method to alleviate spare parts shortages, by maintaining a network of fab managers who share parts when they can with other members of the group who can't wait for new parts to be produced and delivered.

The used semiconductor equipment sector has evolved significantly in recent years. Texas Instruments' purchase of Qimonda's 300mm fab equipment for dimes on the dollar in 2009 and subsequent



conversion and qualification of tools originally designed for memory chip production for use on its own analog RFAB lines forced competitors and others in the industry to look more seriously at making the 200- to 300mm wafer-size transition in their own operations. Duke characterized the 200mm secondary market as “the new 150mm,” as fewer new systems are made, and engineering and sourcing efforts become more difficult to keep legacy parts available.

### Mix and match, ‘more than Moore’ and more

Despite the challenges of equipment and parts availability and obsolescence, some industry experts are bullish on the potential for using refurbished equipment at more demanding technology nodes, seeing used tools as capable of playing a key role in converting a 130nm LSI line into one that processes 60nm and even 45nm devices. Kato provided a step-by-step explanation of his “mix-and-match” philosophy, where he stated that 180 used tools, or 67% of a total toolset, could be deployed to produce 60nm requiring 29 masks. A dozen tools would require remanufacturing upgrades and 82 tools (30%) would need the latest technology only available on new tools. He noted that certain metal layers and N- and P-well implantation could be done with used tools, while other layers requiring fine patterns would need new equipment, and several steps could be carried out with a blend of new, used, and remanufactured tools. Many of the processing steps in his 60nm example can be accomplished with readily available secondary CMP, CVD, etch, and wet processing systems. 3-D interconnect and packaging lines also provide a market for repurposed wafer-processing gear.

Bignell discussed how STMicro has evolved and repurposed older fabs for “more than Moore” chip designs using “derivative technology.” In cases where process steps were similar, an existing toolset could be deployed, modified or upgraded, such as the example of converting an older wet bench to a new process chemical mix. Equipment from other sites has been transferred to the repurposed fabs, such as the case where a decommissioned front-side PVD system was used for backside metallization. In addition to adapting and optimizing fab layouts and facilities, the purchase of 200- and 300mm second-hand tools whenever possible as well as the acquisition of new equipment featuring new capabilities continue to be central tenets

of the manufacturer’s life-cycle extension strategy.

An area of future growth in the secondary equipment market will come from customers, many in regions of the world with little or no domestic semiconductor manufacturing base, that want to establish at least an R&D, pilot, or other start-up facility and may seek a complete fab. An integrated “super turnkey,” soup-to-nuts solution for this kind of project features an experienced secondary equipment company that can leverage a large 200mm tool inventory, an engineering, procurement, and construction partner that that can design and build a new facility or retrofit an existing one, and highly trained equipment and process engineering teams that provide infrastructure and other support functions.

### Conclusion

As more of the secondary equipment market segues from 200mm to 300mm demand and applications, the lessons learned over the past few years will help ease the transition, lowering engineers’ anxiety levels and providing a cost-effective, process-centric strategy for extending fab and product lifetimes.

### Acknowledgment

The authors would like to thank Joanne Itow of Semico Research for her valuable insights to this article. ◀

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# Will 2014 be the Next Golden Year?

**CHRISTIAN GREGOR DIESELDORFF**, SEMI Industry Research & Statistics Group, San Jose, CA.

*Some unexpected underdogs spur spending spree*

**N**ext year could be a golden year for the industry. While GDP in 2013 is generally about the same as in 2012, it is expected to rise in 2014, to 3.8 percent from 3.1 percent. Semiconductor revenue has improved in 2013 compared to 2012 and early forecasts for 2014 project revenue growth averaging about 8 percent. Semiconductor companies have adjusted their capital expenditure accordingly, and the SEMI World Fab Forecast data now indicates fab equipment spending for 2014 will reach historic highs.

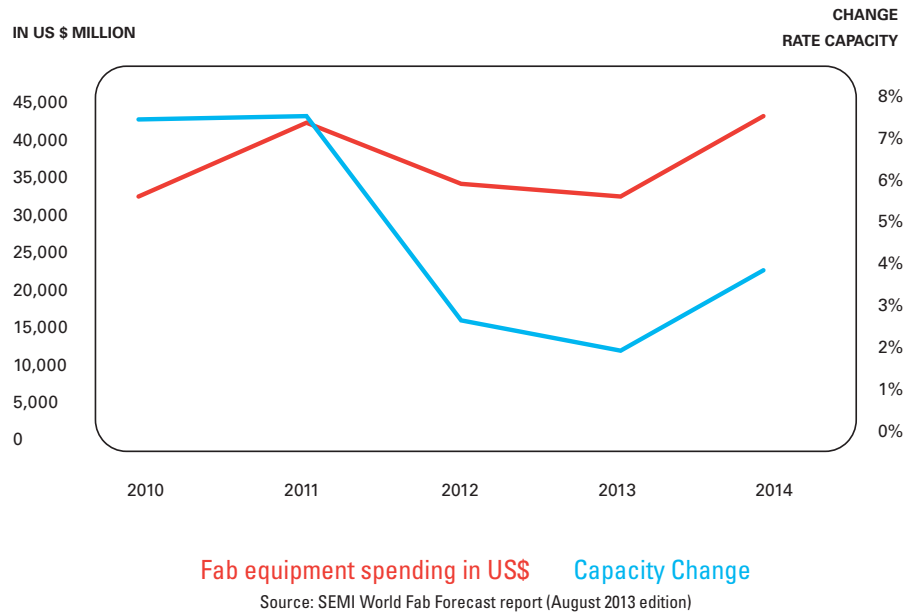
The SEMI World Fab Forecast report tracks over 200 projects, with details revealing that fab equipment spending declines by 1 percent in 2013, but will increase 25 percent in 2014, including new, used and in-house equipment.

Overall fab spending in the first half of 2013 was slower, especially for fab equipment spending. Excluding a large purchase by GLOBALFOUNDRIES for used 300mm equipment from Promos (NT\$20 to NT\$30 billion) the decline in 2013 would have been -3.4 percent instead of -1 percent. Fab equipment spending is expected to be stronger in the second half of 2013, with a 30 to 40 percent increase over the first half, though the year will end with an overall equipment spending decrease of -1 percent.

SEMI's data show a different outlook for fab construction projects, forecasting a 25 percent increase in 2013 and then a drop of 16 percent in 2014. Fabs being built this year will begin

## Fab equipment vs change of installed capacity

(not including Discretes & LEDs)



**FIGURE 1.** More capacity will be added in the 2nd half of 2013 and even more in 2014.

equipping next year which affects fab equipment spending.

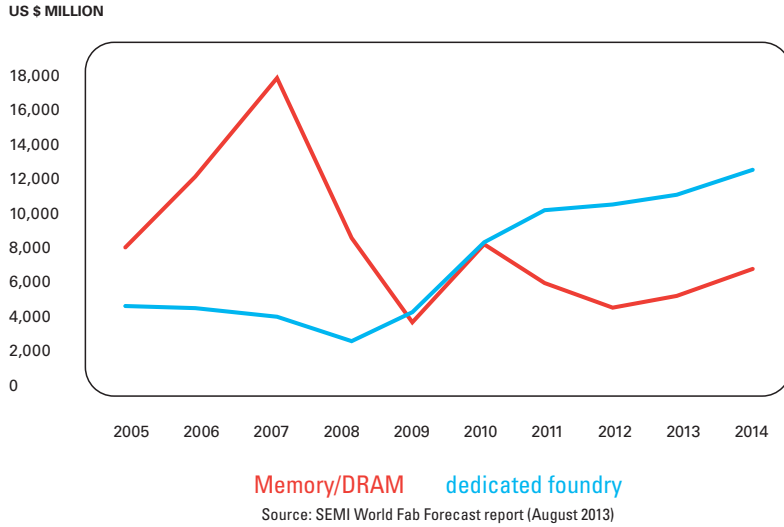
Semiconductor device revenues did not grow in 2012 (dropped by about 2.7 percent), thus many companies slowed down capacity additions last year. With some improvement in the market, the SEMI data indicate that more capacity will be added in the 2nd half of 2013 and even more in 2014, for overall capacity growth of about 4 percent (**FIGURE 1**).

### Underdog DRAM surges to the front of the pack

Fab equipment spending for dedicated foundries remains strong in 2013 (\$12B) and in 2014 (\$13B) — a growth rate of 5 percent in 2014. Foundry equipment spending growth rates have been more controlled and not changing

**CHRISTIAN GREGOR DIESELDORFF** is the Senior Analyst, Director, Industry Research & Analysis Industry Research and Statistics Department at SEMI, San Jose, CA.

### FAB Equipment Spending DRAM vs Dedicated Foundry



**FIGURE 2.** Since 2011, however, the dedicated foundry sector replaced DRAM as the leading industry sector.

as dramatically as in other industry segments. In the years prior to the economic downturn, fab equipment spending for DRAM was the highest spending industry segment. Since 2011, however, the dedicated foundry sector replaced DRAM as the leading industry sector (**FIGURE 2**).

Fab equipment spending growth for DRAM turned negative in 2011 and 2012, as companies consolidated or diverted memory capacity into other products such as System LSI. DRAM equipment spending dropped by double digits in 2011 and 2012 (-35 percent and -25 percent respectively). SEMI's data show that this will change dramatically, with DRAM fab equipment spending surging by 17 percent in 2013 and at least 30 percent in 2014. Driven by increased average selling prices (ASPs), up by about 40 percent in 2013, companies will begin to see profit on DRAM and slowly invest in new capacity (**FIGURE 3**).

An increase of about 2 to 3 percent for installed capacity for DRAM in 2014 is small but remarkable, given that the industry has not added any new DRAM capacity for years and actually decreased capacity between 2011 and 2013.

The sector with largest growth rate for fab equipment spending in 2014 is expected to be Flash with 40 percent to 45 percent (YoY). Over the last few years, with fears of oversupply and price collapse, capacity additions for the Flash

sector also stagnated. Some companies even stopped or reduced adding new capacity (for example, Sandisk in 2012 and in 2013), leading to a tight supply, but a rebound in capacity is expected in the 2nd half of 2013 and through 2014. SEMI's reports show detailed predictions for robust spending in DRAM and Flash by several large companies.

For example, Micron, which officially acquired Elpida and Rexchip in July 2013, will dedicate almost half of its total 2014 capital expenditure to DRAM. After converting several fabs from memory to System LSI, rival Samsung is also expected to change tactics, spending less on System LSI and more on Memory in 2013 and 2014. Samsung's Flash

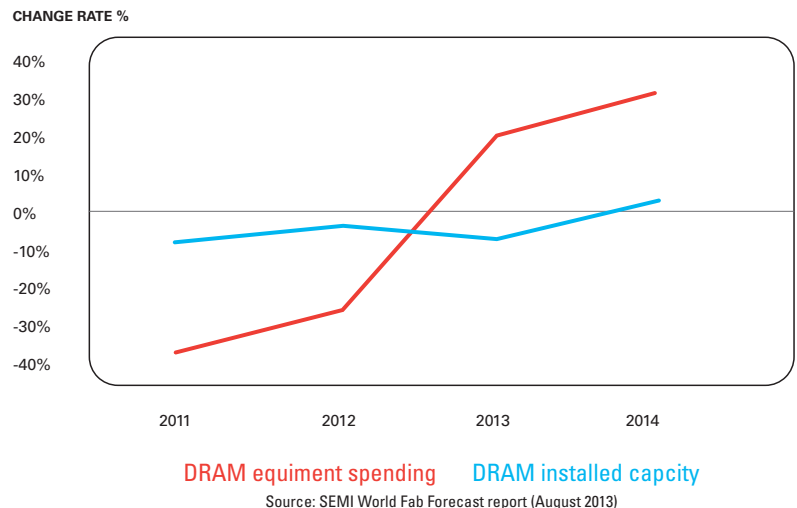
facility in China is expected to ramp to phase 1 by end of 2014. (The World Fab Forecast report reveals more detail on this and other surprising changes for S1 facilities and Line 16.) Overall fab equipment spending for Flash alone is expected to hit a record of almost \$8B in 2014. The largest contributors are the Samsung fab in China and Line 16, Hynix M12 and M11, Flash Alliance fabs and Micron fabs.

### MPU Joins DRAM as the next underdog

After Flash and DRAM, MPU is expected to show the next largest growth in 2014, with fab equipment spending growing by over 40 percent (YoY). While MPU languished

### DRAM

Fab equipment spending vs installed capacity



**FIGURE 3.** Companies will begin to see profit on DRAM and slowly invest in new capacity.



in 2011 and 2012, and even dipped into negative growth in 2013, with low utilization in some fabs, Intel is now preparing for 14nm, kicking off an MPU surge for 2014. The World Fab Forecast report gives insight into Intel's preparations for 14nm.

Semiconductor companies appear to have mastered the art of fast adaptation to chip prices and business developments. With improving prices for DRAM, similar changes steer various sectors of the industry into unprecedented growth. With GDP predictions around 3 to 4 percent, revenue expectations in upper single digits, and historic numbers for equipment spending, next year could be a golden year for many semiconductor companies and equipment manufacturers.

### SEMI World Fab Forecast report

Since the last fab database publication at the end May 2013 SEMI's worldwide dedicated analysis team has made 242 updates to 205 facilities (including Opto/LED fabs) in the database. The latest edition of the World Fab Forecast lists 1,147 facilities (including 247 Opto/LED facilities), with 66 facilities with various probabilities starting production this year and in the near future. We added 14 new facilities and closed 8 facilities.

The SEMI Worldwide Semiconductor Equipment Market Subscription (WWSEMS) data tracks only new equipment for fabs and test and assembly and packaging houses. The SEMI World Fab Forecast and its related Fab Database reports track any equipment needed to ramp fabs, upgrade technology nodes, and expand or change wafer size, including new equipment, used equipment, or in-house equipment. ◀

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# New Products

### Sigma PVD for 300mm power devices

SPTS Technologies launched a Sigma fxP physical vapor deposition (PVD) system for 300mm power device manufacturing. Available system options include modules for frontside thick aluminum processing and backside metal deposition on ultra-thin wafers. The new system is designed to address the technical challenges customers face as they scale power PVD processes up to 300mm wafer size. Due to the high currents involved, thick aluminum alloy layers are deposited on the frontside of the wafer (typically  $> 4 \mu\text{m}$  rather than  $< 1 \mu\text{m}$  for mainstream silicon interconnects). However, depositing thick films puts unusually large heat loads on process chamber hardware, potentially resulting in film contamination from outgassing chamber furniture. This contamination can lead to the formation of aluminum whiskers/extrusions in the growing film that can ultimately result in device killer defects. In traditional front end fab deposition equipment, a common technique to mitigate this issue is to reduce film deposition rates with a corresponding reduction on system productivity. However, the Sigma fxP design overcomes that challenge without compromising

throughput. Sigma fxP users routinely deposit thick Al layers at rates  $> 1.4 \mu\text{m}/\text{min}$  without any yield destroying whiskers or extrusions. With frontside processing complete, wafers are thinned down to  $50 \mu\text{m}$  or less to reduce 'on-state' resistance and solder metal layers are deposited on the backside. No supporting carrier substrates are used and the ultra-thin, large area wafer will deform under the influence of uncontrolled film stresses, with miss-handling a potential consequence. The Sigma fxP carries thin wafer handling hardware and uses film deposition stress control techniques to deliver high throughput processes with low wafer bow.

**SPTS Technologies**, Newport, U.K., [www.spts.com](http://www.spts.com)

### CNTs for NRAM

Brewer Science announced that the next generation of carbon nanotube materials, the CNTRENE 1020 material series, is officially qualified for NRAM nanotube random access memory device manufacturing by Nantero Inc. NRAM memory is a high-density, non-volatile memory technology invented by Nantero to

serve as a universal memory device, which can replace flash, DRAM, and others in embedded and stand-alone memory applications. Brewer Science is a licensed supplier of CMOS-grade carbon nanotube solutions utilizing processes developed by Nantero for use in the manufacture of NRAM devices. The next generation of CNTRENE materials manufactured by Brewer Science provides an increased concentration of CNTs in solution, with lower ion content (<10 ppb) and extended stability for use in standard coater track systems. This new generation of Brewer Science CNT materials allows for reduced process costs and improved on-wafer coating performance, consistent with the company's focus on integrated solutions.

**Brewer Science**, Rolla, MO, [www.brewerscience.com](http://www.brewerscience.com).

**Compact linear piezo nanopositioning stage**

PI (Physik Instrumente) L.P., a manufacturer of nanopositioning equipment, introduced the LPS-45 series of piezo positioning stages manufactured by PI subsidiary PI miCos. This low profile linear translation stage is driven by a PIshift inertia-type piezo motor. The closed-loop stage is equipped with a high precision optical linear encoder providing for nanometer-level repeatability. An open-loop version and vacuum compatible and non-magnetic versions are also offered. The PIshift piezo inertia drive is very quiet, due to its high operating frequency of 20 kHz. It provides high holding forces of 10 N. The drive principle works similar to the classic tablecloth trick, a cyclical alternation of static and sliding friction between a moving runner and the drive element. When at rest, the maximum clamping force is available, with no holding current and consequently no heat generation. Despite the very low profile of only 0.8" (20 mm) and compact dimensions, the stage offers a standard travel range of 30 mm (1.2") and can be scaled up for longer travels, if needed.

**Physik Instrumente**, Auburn, MA, [www.physikinstrumente.com](http://www.physikinstrumente.com)

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Over the last two years, the industry has launched nearly a dozen consortium-like entities in 450mm and related areas of development. Joining Belgium's imec, Germany's Fraunhofer Institute, Taiwan's ITRI, and France's CEA-Leti—to name a few—are a number of new consortia established to collaborate on joint R&D for 450mm wafers and other next-generation semiconductor challenges. GLOBALFOUNDRIES, Intel, IBM, Samsung and TSMC formed the Global 450 Consortium (G450C) to manage 450mm wafer processing requirements. Recently, G450C set up a separate fab facility consortium. Europe has launched five separate 450mm projects or consortiums, with two others on the drawing board. Israel has established 450mm consortium on metrology and Japan has collaborative arrangement on 450mm with Toshiba.

With uncertainties on 450mm wafer processing, EUV lithography, and the continued transition to new transistor architectures, many experts are questioning the continuation of Moore's Law. It's been reported that cost targets at 28nm were not reached, 20nm may be delayed and also come in at a high price. Consequently, the industry has been excited about More-Than-Moore applications, especially 3D stacked ICs that promise to improve bandwidth, reduce footprint, decrease power consumption, and lower cost.

We have seen the proliferation of stacked die with wire bond or flip chip, stacked packages, package-on-package, and chip-on-chip packages. But today, the most anticipated innovation is 2.5 and 3D stacked ICs using TSVs to achieve both the power and bandwidth benefits associated with a radical new interconnect solution.

Like 450mm wafer processing, critical standards foundation work for the adoption 3D-IC is well underway. At SEMI, Standards task forces have been established in thin wafer handling, inspection and metrology, and wafer bonding. But like 450mm wafer processing, enabling the 3D-IC revolution will require more than industry standards activities.

While a promising technology, technical challenges remain with 3D stacked ICs. Many companies have a silicon interposer or 2.5D solution on their packaging roadmaps where a logic device is mounted next to a stack of memory and the TSVs are in the substrate. However, while Samsung and others have made

announcements, affordable stacked memory is not yet available. In addition, many companies are also looking at alternatives to silicon interposers, such as glass interposers, to bring the price down. So, even 2.5D has been delayed and questions remain about its configuration at high volume. For heterogeneous integration of memory and logic, the industry still needs design tools, thermal solutions, continued work on wafer bonding and de-bonding, and accepted test methodologies, to name a few requirements.

Gartner estimates that TSV adoption for memory will be pushed out to 2014 or 2015, with non-memory applications delayed to 2016-17 if that. They currently forecast that TSV devices will account for less five percent of the units in the total wafer-level packaging market by 2017.

For 3D-IC to be widely adopted, meaningful collaboration throughout the value chain still needs to occur. At this time in the market, all the important players in the ecosystem have a different perspective. All the players have a business model that must be defended or exploited based on what technical discoveries occur and what customers eventually want. TSMC sees an integrated approach that threatens the traditional Fabless/Foundry/OSAT model. Obviously leading OSATs prefer this vision as it provides an opportunity to expand their business. But OSATs themselves are looking at ways to differentiate. IDMs like Intel probably see the fabless model coming full circle with 3D IC. Fabless companies believe that 3D must emerge in ways that continue their own—and their customer's—familiar multiple-sourcing considerations.

We'll continue to see discoveries, inventions and new products in 3D-IC and progress will continue. Hundreds of patents in the area have already been issued. We're seeing innovation and invention in wafer bonding, via manufacturing, and other areas. Standards work at JEDEC and SEMI will also contribute to the market's development, both to enable processes and cost-reduce manufacturing, but without the emergence of a new, robust collaboration model that can deliver meaningful agreements between key constituencies, the promise of 3D innovation will remain distant and illusive. ◀

## Collaboration needed on 3D-IC

The history of semiconductors has been a history of collaboration. For decades, the great leaps forward in semiconductor cost reductions and performance improvements have been achieved through widespread industry collaboration efforts in technology roadmaps, manufacturing standards, wafer size transitions, collaborative R&D consortia, international trade agreements, and other areas. Today, a similar industry-wide collaborative approach to 3D stacked ICs is needed to reach widespread 3D-IC adoption and continue the amazing progress our industry has historically achieved.

In the past, when the industry was small, semiconductor progress as defined by Moore's Law occurred nearly simultaneously in different companies. Progress was achieved through science and technology innovation occurring through independent R&D labs and spread through academia and commercial competition. Later, as the scale, scope and complexity of semiconductor manufacturing expanded exponentially—with much of the R&D distributed throughout the supply chain involving hundreds of equipment and materials suppliers each specializing on their unique role in the fabrication process—industry roadmaps were required to keep

everyone on pace. No single firm could master all the elements of innovation required for Moore Law improvements. For several years it was an American effort, but in 1998 the roadmap became an international process, today's International Technology Roadmap for Semiconductors (ITRS). Today, the ITRS has expanded to address not only critical requirements to sustain Moore's Law, but also the key development milestones necessary in the More-Than-Moore—in areas like advanced packaging and MEMS.

R&D costs have also expanded to meet the targets dictated by Moore's Law. In the early days, only the largest R&D lab in the world, Bell Labs, could manage the multi-disciplinary requirements for semiconductor chip development. Eventually, collaborative research consortia emerged that allowed industry players to pool resources in a pre-competitive environment to develop the science and technology needed for the next generation chip.

While a promising technology, technical challenges remain with 3D stacked ICs.

In addition to collaborative roadmaps and R&D, the semiconductor industry also agreed upon collective industry standards that reduced cost and spur innovation. These standards involve such areas as wafer size and dimensions, software and hardware interfaces, materials characterization and test methods, and hundreds of other areas. Today, there are nearly 4,000 volunteers from every major company working together on SEMI industry standards. They have produced hundreds of widely-accepted standards that have reduced costs and allowed companies to compete on innovation. In addition to SEMI Standards, other standards bodies have emerged such as IEEE and JEDEC to address semiconductor standards needs in electrical, signaling, form factor, packaging and other areas.

With roadmaps, standards and consortia in place, the semiconductor industry targeted what was considered by some an "easy" wafer transition to 300mm silicon. It was anything but easy. As many of you know, the transition went poorly. The industry couldn't agree when to introduce 300mm production and stop advanced development at 200mm, and they couldn't afford to do both. There were several false starts and hundreds of millions of dollars were lost.

Today, the industry is planning a 450mm wafer transition while at the same time trying to manage the increasingly complex R&D challenges of new materials development, new transistor architectures, and new packaging paradigms. The cost of advanced semiconductor development has skyrocketed. The industry has responded by dramatically expanding the Consortia model for collaborative R&D.

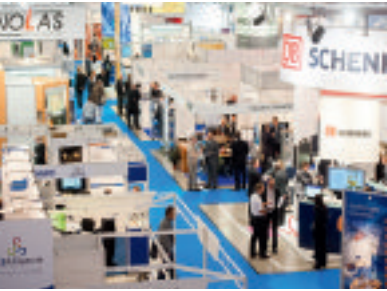


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