UM11732

I^{2}S bus specification

Rev. 3.0 — 17 February 2022   **User manual**

Revision history

Rev	Date	Description
v.3	20220217	• This document has been reconstructed from the I^{2}S bus specification, February 1986, revised June 5, 1996 by Philips Semiconductors. The format has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Updated terms "Master" and "Slave" to "Controller" and "Target" to support coherent inclusive language use in conjunction with the I^{2}S bus which is in broad use in the electronics community.
v.2	19960605	Second version
v.1	19860201	Initial version

UM11732

User manual

All information provided in this document is subject to legal disclaimers.

Rev. 3.0 — 17 February 2022

© NXP B.V. 2022. All rights reserved.

2 / 14

1 Introduction

Many digital audio systems are being introduced into the consumer audio market, including compact disc, digital audio tape, digital sound processors, and digital TV-sound. The digital audio signals in these systems are being processed by a number of (V)LSI ICs, such as:
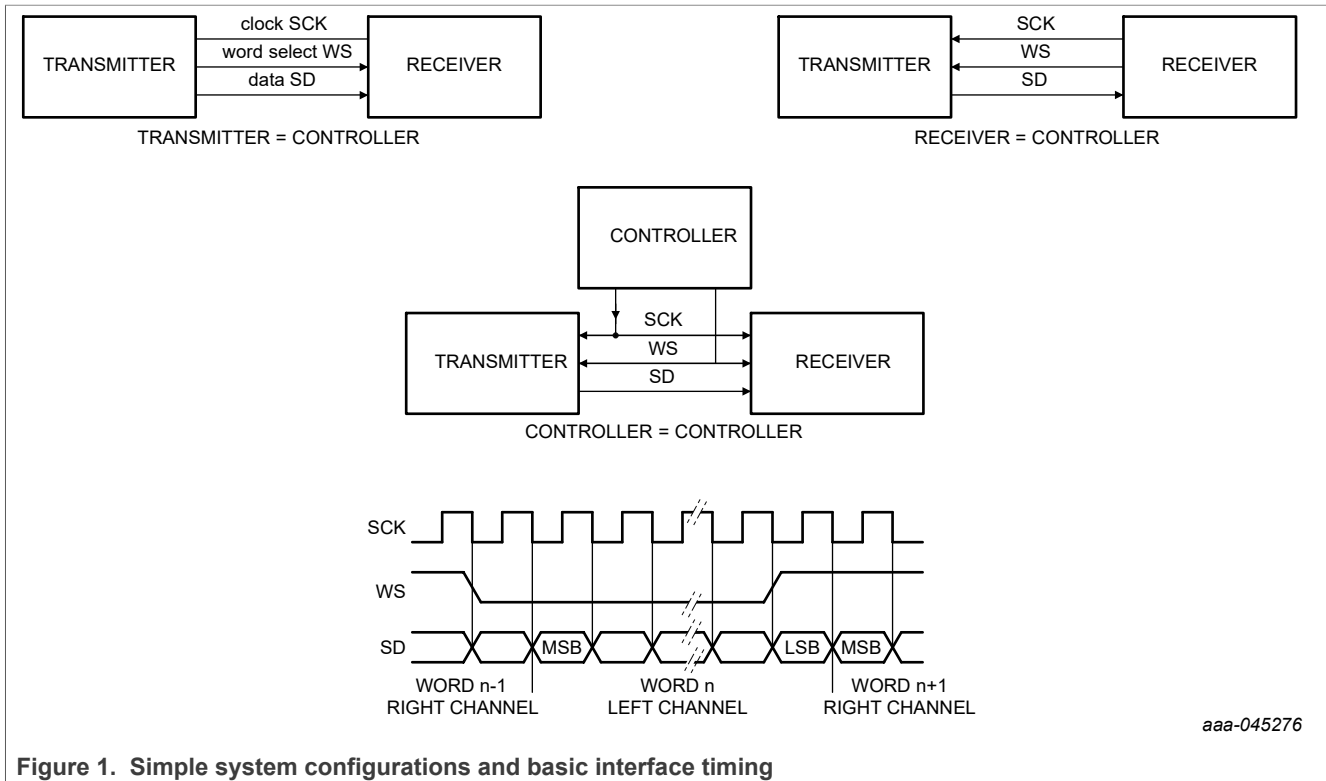
- A/D and D/A converters;
- digital signal processors;
- error correction for compact disc and digital recording;
- digital filters;
- digital input/output interfaces.

Standardized communication structures are vital for both the equipment and the IC manufacturer, because they increase system flexibility. To this end, we have developed the inter-IC sound (I^{2}S) bus – a serial link especially for digital audio.

2 Basic serial bus requirements

The bus has only to handle audio data, while the other signals, such as sub-coding and control, are transferred separately. To minimize the number of pins required and to keep wiring simple, a 3-line serial bus is used consisting of a line for two time-multiplexed data channels, a word select line and a clock line.

Since the transmitter and receiver have the same clock signal for data transmission, the transmitter as the controller, has to generate the bit clock, word-select signal and data. In complex systems however, there may be several transmitters and receivers, which makes it difficult to define the controller. In such systems, there is usually a system controller controlling digital audio data-flow between the various ICs. Transmitters then, have to generate data under the control of an external clock, and so act as a target. Figure 1 illustrates some simple system configurations and the basic interface timing. Note that the system controller can be combined with a transmitter or receiver, and it may be enabled or disabled under software control or by pin programming.

UM11732

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2022. All rights reserved.

User manual

Rev. 3.0 — 17 February 2022

3 / 14

Figure 1. Simple system configurations and basic interface timing

3 The I²S bus

As shown in [Figure 1](#), the bus has three lines:

- Continuous Serial Clock (SCK);
- Word Select (WS);
- Serial Data (SD);

and the device generating SCK and WS is the controller.

3.1 Serial data

Serial data is transmitted in two's complement with the MSB first. The MSB is transmitted first because the transmitter and receiver may have different word lengths. It isn't necessary for the transmitter to know how many bits the receiver can handle, nor does the receiver need to know how many bits are being transmitted.

When the system word length is greater than the transmitter word length, the word is truncated (least significant data bits are set to '0') for data transmission. If the receiver is sent more bits than its word length, the bits after the LSB are ignored. On the other hand, if the receiver is sent fewer bits than its word length, the missing bits are set to zero internally. And so, the MSB has a fixed position, whereas the position of the LSB depends on the word length. The transmitter always sends the MSB of the next word one clock period after the WS changes.

Serial data sent by the transmitter may be synchronized with either the trailing (HIGH-to-LOW) or the leading (LOW-to-HIGH) edge of the clock signal. However, the serial data must be latched into the receiver on the leading edge of the serial clock signal, and so

there are some restrictions when transmitting data that is synchronized with the leading edge (see Figure 2 and Table 1).

3.2 Word select

The word select line indicates the channel being transmitted:

- WS = 0; channel 1 (left);
- WS = 1; channel 2 (right).

WS may change either on a trailing or leading edge of the serial clock, but it doesn't need to be symmetrical. In the target, this signal is latched on the leading edge of the clock signal. The WS line changes one clock period before the MSB is transmitted. This allows the target transmitter to derive synchronous timing of the serial data that will be set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next word (see Figure 1).
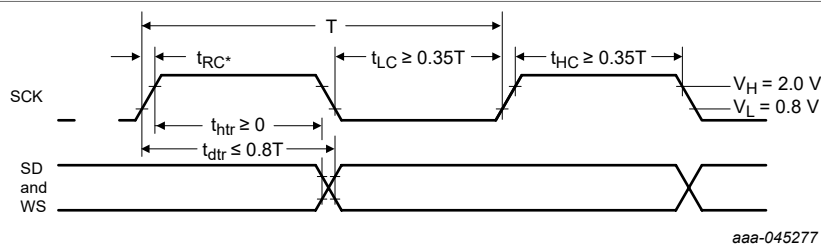
4 Timing

In the I^{2}S format, any device can act as the system controller by providing the necessary clock signals. A target will usually derive its internal clock signal from an external clock input. This means, taking into account the propagation delays between controller clock and the data and/or word-select signals, that the total delay is simply the sum of:

- the delay between the external (controller) clock and the target's internal clock; and

- the delay between the internal clock and the data and/or word-select signals.

For data and word-select inputs, the external to internal clock delay is of no consequence because it only lengthens the effective set-up time (see Figure 2). The major part of the time margin is to accommodate the difference between the propagation delay of the transmitter, and the time required to set up the receiver.

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device. This means that higher data rates can be used in the future.

T = clock period

T$_{tr}$ = minimum allowed clock period for transmitter

T > T$_{tr}$

* t$_{RC}$ is only relevant for transmitters in target mode.

Figure 2. Timing for I^{2}S transmitter

T = clock period

T_r = minimum allowed clock period for transmitter

$T > T_r$

Figure 3. Timing for I^2S receiver
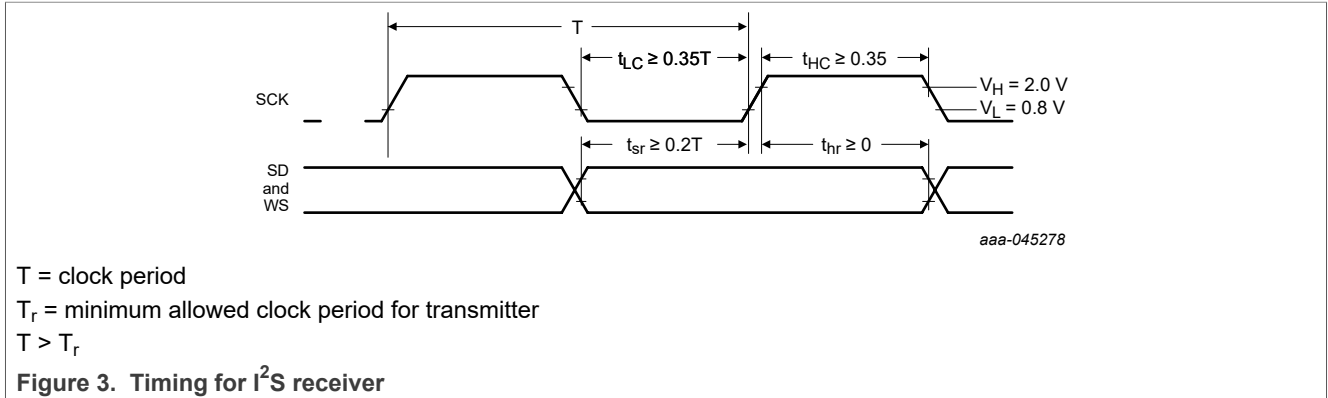
Note that the times given in both Figure 2 and Figure 3 are defined by the transmitter speed. The specification of the receiver has to be able to match the performance of the transmitter

Table 1. Controller transmitter with data rate of 2.5 MHz (±10 %) (all values in ns)

	MIN	TYP	MAX	CONDITION
clock period T	360	400	440	T_{tr} = 360
clock HIGH t_{HC}	160			min > 0.35T = 140 (at typical data rate)
clock LOW t_{LC}	160			min > 0.35T = 140 (at typical data rate)
delay t_{dtr}			300	max < 0.80T = 320 (at typical data rate)
hold time t_{htr}	100			min > 0
clock rise-time t_{RC}			60	max > $0.15T_{tr}$ = 54 (only relevant in target mode)

Table 2. Target receiver with data rate of 2.5 MHz (±10 %) (all values in ns)

	MIN	TYP	MAX	CONDITION
clock period T	360	400	440	T_{tr} = 360
clock HIGH t_{HC}	110			min < 0.35T = 126
clock LOW t_{LC}	110			min < 0.35T = 126
set-up time t_{sr}	60			min < 0.20T = 72
hold time t_{htr}	0			min < 0

Table 3. Timing for I^{2}S transmitters and receivers

All timing values are specified with respect to high and low threshold levels.

		TRANSMITTER				RECEIVER				NOTES
		LOWER LIMIT		UPPER LIMIT		LOWER LIMIT		UPPER LIMIT		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Clock period	T	T_{tr}				T_r				[1]
Controller mode: clock generated by transmitter or receiver	HIGH t_{HC}	$0.35T_{tr}$				$0.35T_{tr}$				[2]
	LOW t_{LC}	$0.35T_{tr}$				$0.35T_{tr}$				[2]
Target mode: clock accepted by transmitter or receiver	HIGH t_{HC}		$0.35T_{tr}$				$0.35T_{tr}$			[3]
	LOW t_{LC}		$0.35T_{tr}$				$0.35T_{tr}$			[3]
	rise-time t_{RC}			$0.15T_{tr}$						[4]
Transmitter	delay t_{dtr}				$0.8T$					[5]
	hold time t_{htr}	0								[4]
Receiver	set-up time t_{sr}						0.2_{Tr}			[6]
	hold time t_{hr}						0			[6]

[1] The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.

[2] At all data rates in the controller mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason t_{HC} and t_{LC} are specified with respect to T.

[3] In the target mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used (see Figure 3

[4] Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.

[5] To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient set-up time.

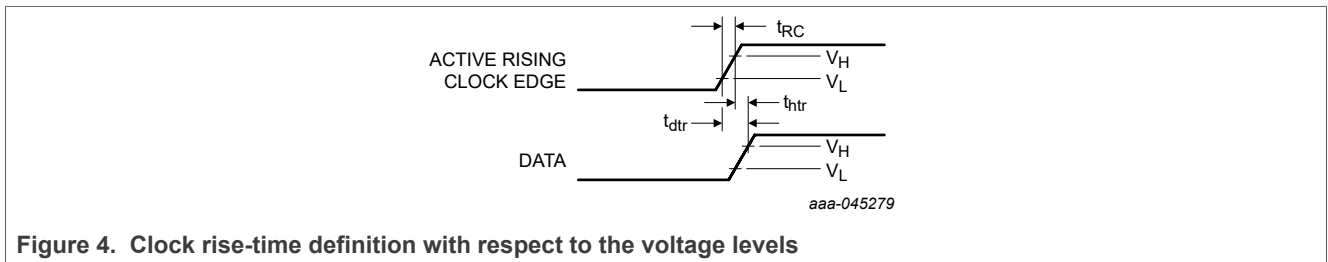[6] The data set-up and hold time must not be less than the specified receiver set-up and hold time.

Figure 4. Clock rise-time definition with respect to the voltage levels

5 Voltage level specification

5.1 Output levels

V_L < 0.4 V

V_H > 2.4 V both levels able to drive one standard TTL input (I_{IL} = −1.6 mA and I_{IH} = 0.04 mA).

5.2 Input levels

V_{IL} = 0.8 V

V_{IH} = 2.0 V

Note: *At present, TTL is considered a standard for logic levels. As other IC (LSI) technologies become popular, other levels will also be supported.*

6 Possible hardware configurations

6.1 Transmitter

At each WS-level change, a pulse WSP is derived for synchronously parallel-loading the shift register. The output of one of the data latches is then enabled depending on the WS signal. Since the serial data input is zero, all the bits after the LSB will also be zero (see Figure 5).

UM11732
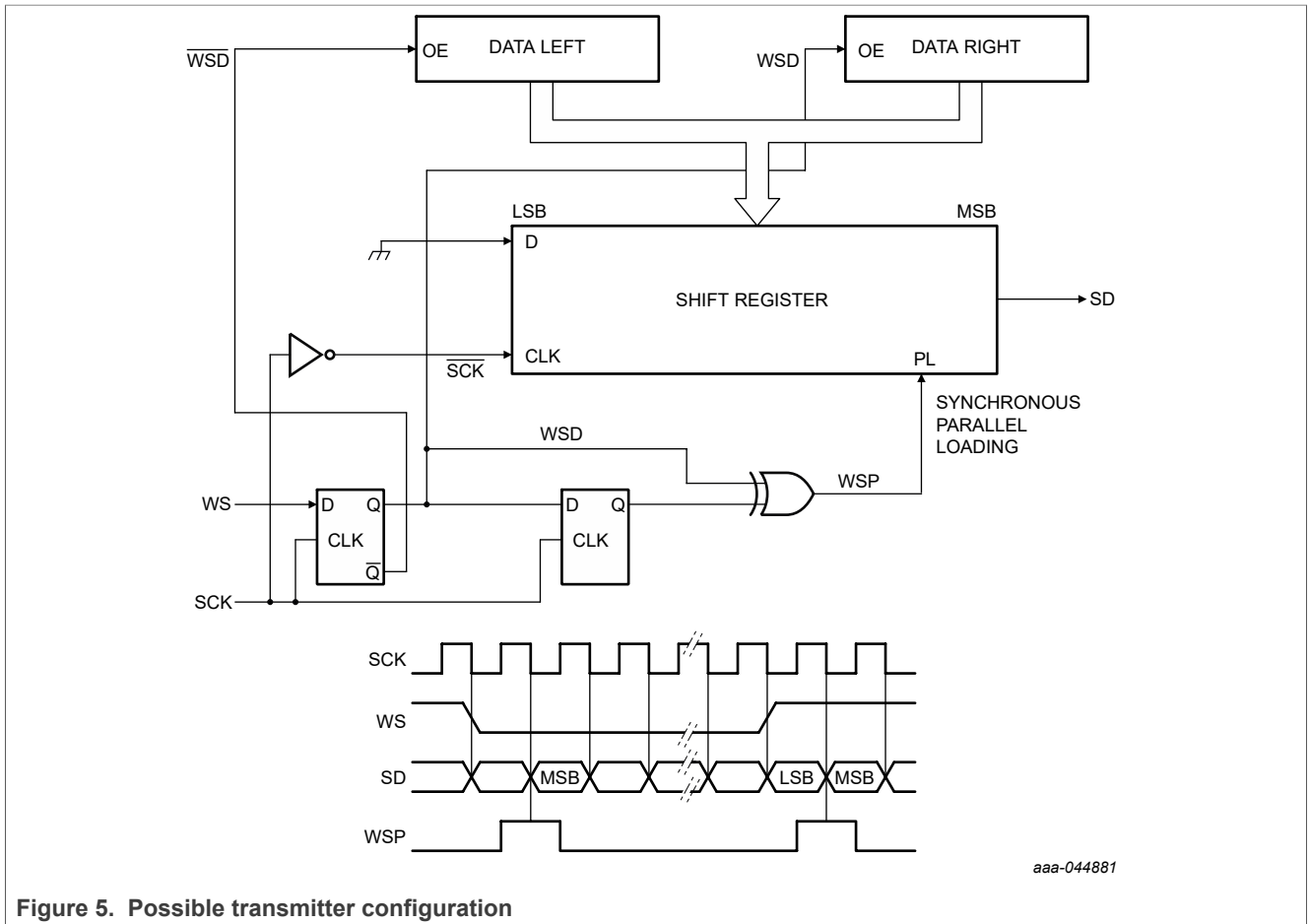
User manual

All information provided in this document is subject to legal disclaimers.

Rev. 3.0 — 17 February 2022

© NXP B.V. 2022. All rights reserved.

8 / 14

Figure 5. Possible transmitter configuration

6.2 Receiver

Following the first WS-level change, WSP will reset the counter on the falling edge of SCK. After decoding the counter value in a "1 out of n" decoder, the MSB latch (B1) is enabled (EN1 = 1), and the first serial data bit (the MSB) is latched into B1 on the rising edge of SCK. As the counter increases by one every clock pulse, subsequent data bits are latched into B2 to Bn.

On the next WS-level change, the contents of the n latches are written in parallel, depending on WSD, into either the left or the right data-word latch. After this, latches B2 to Bn are cleared and the counter reset. If there are more than n serial data bits to be latched, the counter is inhibited after Bn (the receiver's LSB) is filled and subsequent bits are ignored (see Figure 6).

***Note:** The counter and decoder can be replaced by an n-bit shift-register (see Figure 7) in which a single '1' is loaded into the MSB position when WSP occurs. On every subsequent clock pulse, this '1' shifts one place, enabling the N latches. This configuration may prove useful if the layout has to be taken into account.*
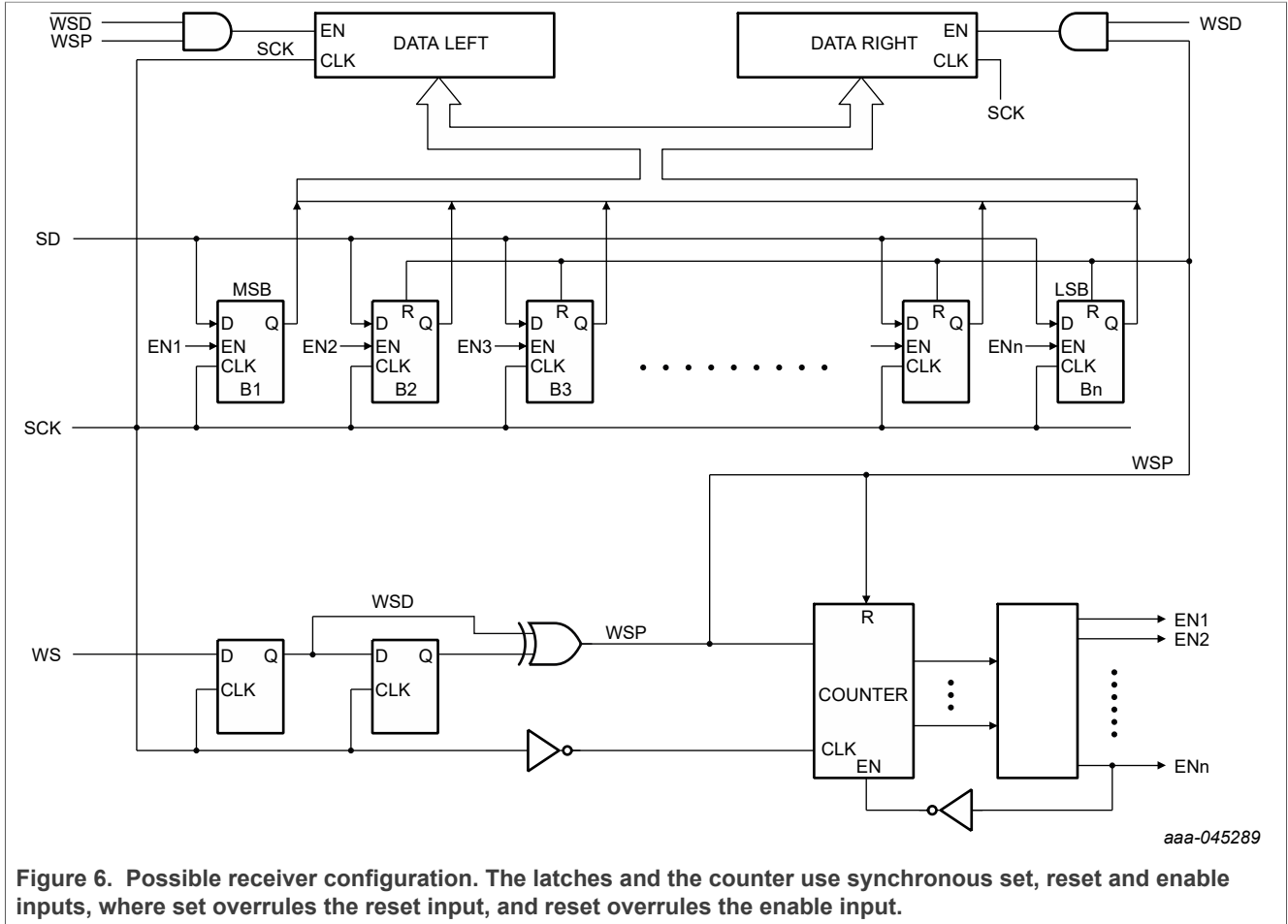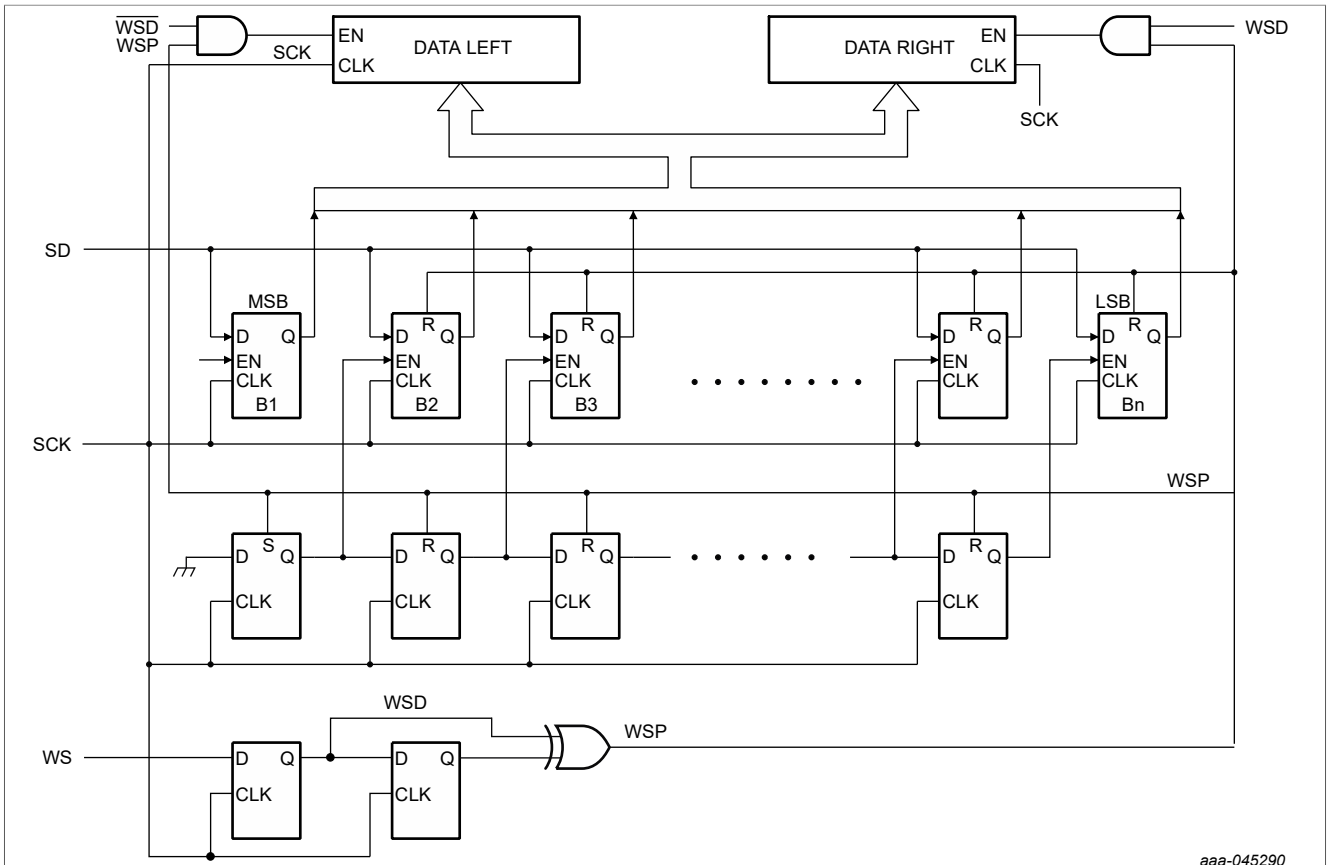
Figure 6. Possible receiver configuration. The latches and the counter use synchronous set, reset and enable inputs, where set overrules the reset input, and reset overrules the enable input.

aaa-045290

Figure 7. Possible receiver configuration, using an n-bit shift-register to enable control of data input register.

UM11732

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2022. All rights reserved.

User manual

Rev. 3.0 — 17 February 2022

11 / 14

7 Legal information

7.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

7.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

7.3 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

UM11732

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2022. All rights reserved.

User manual

Rev. 3.0 — 17 February 2022

12 / 14

Tables

Figures

UM11732

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2022. All rights reserved.

User manual

Rev. 3.0 — 17 February 2022

13 / 14

Contents