RSFQ Asynchronous Switch Matrix

Alex Kirichenko, Deepnarayan Gupta, and Saad Sarwana

***Abstract*—A switch matrix operating with multi-rate digital data streams has been developed and demonstrated. The circuit is to serve as a commutating switch in a multi-band multi-channel receiver. The switch works in space-division mode commutating single-bit multi-rate data streams. A 2 × 2 version of the switch matrix was designed, fabricated at HYPRES 1-kA/cm^2, and tested at data rates in excess of 20 GHz. The design and test results will be presented. The final version of the device will be a 3 × 8 switch matrix operating at 40 Gbit/s data rate.**

***Index Terms*—DSP, network switch, RSFQ.**

I. Introduction

A MULTI-BAND RF communication system consists of an antenna subsystem to capture electromagnetic energy in different RF bands and a transceiver subsystem to transmit and receive information from each RF band through a variety of signal processing steps (e.g., up/down-conversion, filtering, modulation, demodulation, coding, decoding). The antenna and transceiver subsystems interact through an RF distribution unit, which for all current systems resides in the analog domain. The goal for truly flexible operations is to dynamically distribute the available signal processing resources among the input bands to fulfill changing communication needs. This requires programmable RF distribution and routing.

Analog RF switching systems, even those employing digital control, have severe deficiencies in terms of losses, isolation, crosstalk, and the ability to multicast. They also suffer from lack of scalability and re-configurability. We are developing a new *digital-RF* communication architecture that solves this problem by moving the boundary between analog and digital domains directly behind the antenna subsystem, and allowing the RF distribution to be implemented in the digital domain.

Digital-RF refers to direct conversion of RF signals to digital, followed by all subsequent processing in the digital domain. Here, we take advantage of the core strengths of superconductor integrated circuit technology: high-linearity data converters, on-chip integration of mixed signal electronics, and ultrafast initial digital processing, starting at GHz digital-RF domain and extending down to the digital-IF domain, where the state-of-the-art semiconductor processors can take over. This approach is well matched to the current level of maturity of superconductor electronics, featuring very fast (up to 40 GHz) digital circuits of modest complexity (10–20,000 Josephson junctions per chip). The receive side of a multi-band, multi-channel digital-RF communication system is depicted in Fig. 1.

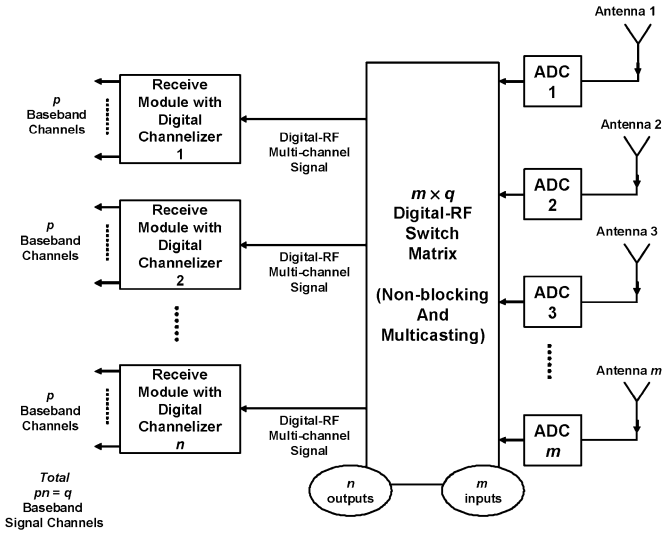

Fig. 1. The receive side of the RF communication system shows the placement of the switch matrix. Each antenna is banded together with an ADC at the input side of the switch matrix. The switch routes one or more of m digitized antenna outputs to each output port that is connected to a multi-channel receive module.

II. Switch Design

Let us consider a multi-band communication system that has a fixed number (n) of transceiver units and a fixed number (m) of antennas. The requirements of a switch matrix for digital-RF distribution are as follows.

1) The switch should route each of the m input streams to one or more output terminals. More generally, multiple input terminals can be connected to one output, if data collision conditions are observed.
2) The switch should be able to operate with multi-bit input data streams at a rate up to 40 GHz.
3) One special requirement for the switch is its ability to support multiple input data rates, since the ADCs may not share the same clock frequency.
4) The routing table of the switch does not have to be changed very often. So, the switch can be reprogrammed serially and at low speed.

Based on these requirements, a simple cross-point switch architecture was chosen (Fig. 2). It comprises an $m \times n$ matrix of the switching nodes, connecting m inputs to n outputs. Each node in the matrix row is directly connected to the corresponding output terminal. Here, each input propagates horizontally through a set of switch nodes. If a switch node is turned on, a copy of the input data stream is routed down by merging to the

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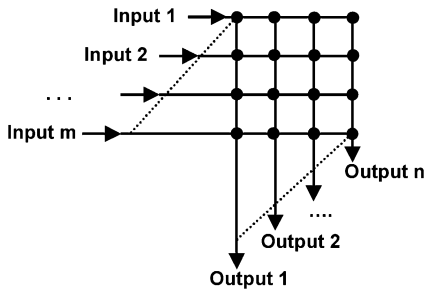

Fig. 2. General architecture of the switch matrix.

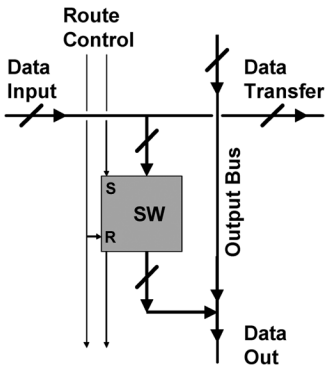

Fig. 3. Block diagram of a single node of the switch matrix, comprising a switch cell (SW) and associated routing and control.

corresponding column towards an output port. Any number of switches may be turned on in each row.

There is a potential problem in this structure, since the signal propagation paths from an input port to different output ports is different. For most communications applications, such small differences in propagation delays do not matter. However, delay compensation networks can be added for applications sensitive to delay mismatches.

The block-diagram of a switch matrix node is shown in Fig. 3. The routed data bus comprises a clock line and N data lines (one for each bit). Only the clock line is routed through a Non-Destructive Read-Out element (NDRO) [1], which stores the control information. All data lines go through the set of latches (RS flip-flops) [1] driven by the clock. Thus, if a clock signal did not pass through the NDRO, the latches block data propagation (Fig. 4). Besides the obvious advantage in hardware saving, this simple approach allows to keep data in sync, thus increasing coherent throughput. The minor drawback of this approach is the necessity to clear the contents of RS flip-flops after each rewriting of the routing table. It can be achieved by sending a single clock pulse through all inputs, and discarding the produced data output. For most DSP applications this is not relevant.

We have designed a single-bit switch matrix node for the 1.0 $\mathrm{kA/cm^2}$ and 4.5 $\mathrm{kA/cm^2}$ standard HYPRES fabrication process [2]. The switch was constructed from basic library cells and did not require extensive simulations. The size of a single switch node is $470\ \mu\mathrm{m} \times 540\ \mu\mathrm{m}$, mostly occupied by the relatively complex data bus wiring. We plan to reduce it further in the next design iterations.

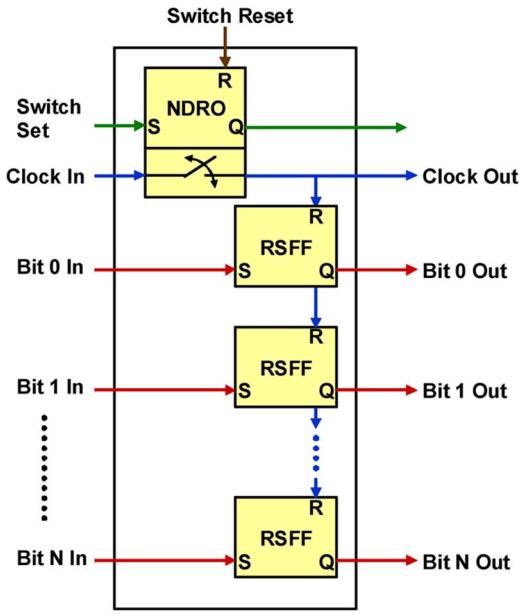

Fig. 4. Switch circuit for N-bit data stream.

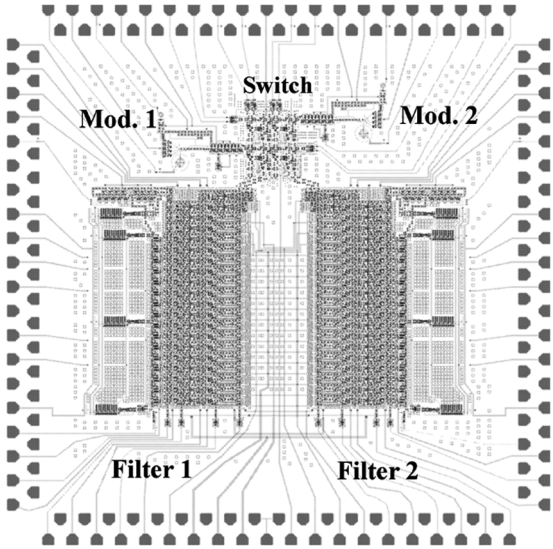

Fig. 5. Layout of 1 cm × 1 cm ADC comprising two modulators connected to two digital filters through the 2 × 2 switch matrix.

As a high-speed digital-RF test bed for the switch we have designed a chip comprising two low-pass ADC [4] modulators connected to two low-pass digital filters through a 2 × 2 switch matrix (Fig. 5). This chip is intended to prove the operation of the switch matrix as a digital-RF signal distributor. It will also allow us to compare the behavior of two ADCs and two digital filters. We also designed a stand-alone 2 × 2 switch matrix test chip.

III. Experiment

Using a low-speed automated test setup Octopux [3], we have performed an extensive functionality test on a single switch matrix node (Fig. 6). The experimentally observed dc current bias margins for the switch are $+/-27\%$.

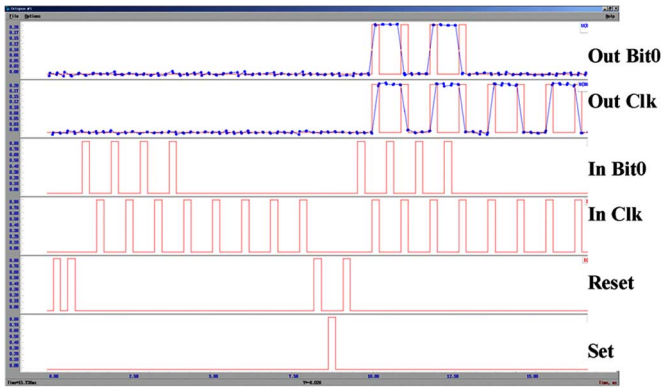

Fig. 6. Functionality test for single node of the switch matrix. Traces from top to bottom are: Output Bit0, Output Clock, Input Bit0, Input Clock, Node Reset, Node Set.

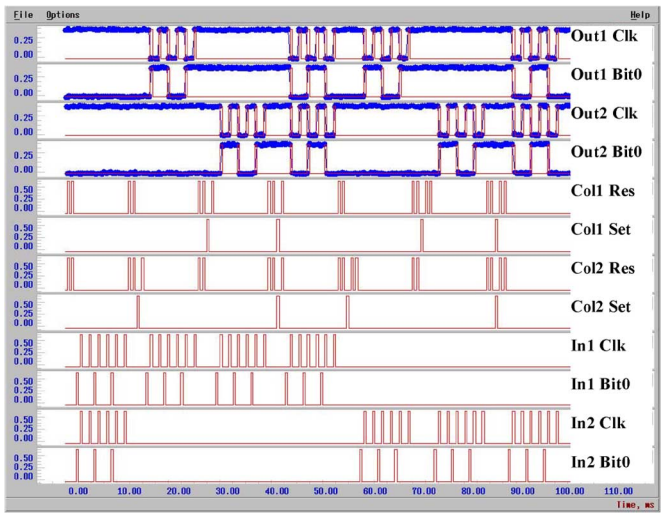

Fig. 7. Functionality test for 2 × 2 switch matrix. Traces from top to bottom are: Output1 Clock, Output1 Bit0, Output2 Clock, Output2 Bit0, Column1 Reset, Column1 Set, Column2 Reset, Column2 Set, Input1 Clock, Input1 Bit0, Input2 Clock, Input2 Bit0.

The 2 × 2 switch matrix functionality test has shown +/−20% dc current bias operating margins. Fig. 7 shows the correct routing of one of the two inputs to both outputs. It takes two Node Reset signals to write down a two-bit routing sequence into a switch column.

The same 2 × 2 switch chip was tested at high speed (Fig. 8). In this test, a 20-GHz clock and 400-kHz data signals were applied to the second input of the switch matrix (second row). The routing sequence was chosen to test all possible output combinations and was in sync with the data signal. A single line on the clock output indicates presence of high-speed signal, while a double line indicates the absence of it. The comparably low-frequency data output (Bit0) exhibits a stable pattern, showing no noticeable bit error rate. That indicates absence of collision on the RS flip-flops between high-speed clock pulses and data bit stream.

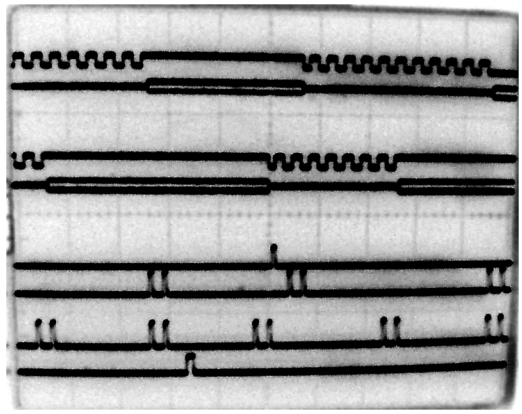

Fig. 8. High-speed test for 2 × 2 switch matrix. Traces from top to bottom are: Output1 Bit0, Output1 Clock, Output2 Bit0, Output2 Clock, Column1 Set, Column1 Reset, Column2 Set, Column2 Reset.

Preliminary testing of the chip shown in Fig. 5 has confirmed programmable distribution of high-speed data and clock signals from an ADC to either decimation filter.

IV. Conclusion

We have designed an asynchronous RSFQ switch matrix. The 2 × 2 version of the switch was fabricated with the standard HYPRES fabrication process and successfully tested. The switch was designed as a part of a universal multi-band band-pass ADC.

Acknowledgment

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References

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