Silicon Image

Digital Visual Interface

&

TMDS Extensions

WHITE PAPER

October 2004

CONTENTS

INTRODUCTION

The PC monitor landscape has changed dramatically in recent years, with the venerable yet bulky CRT rapidly being replaced by the sleek LCD monitor. LCD monitors now exceed CRT monitors in units shipped, and according to IDC are projected to dominate the market with approximately 80 percent share by 2007. Unlike their CRT brethren, LCD monitors are inherently digital devices. As such, having an LCD monitor convert digital signals to analog and back again to digital, as is done with CRTs, is entirely unnecessary and can negatively impact image quality.

Enter the Digital Visual Interface (DVI). DVI is the accepted standard for transferring serially uncompressed digital data at high speeds between a PC host and a digital display, such as an LCD monitor. DVI enables a video signal to be transferred from a PC source to a digital display in its native digital form, simplifying the way PCs communicate with displays and improving display image quality.

LCD monitors are increasingly sporting a DVI connector. In a recent LCD monitor roundup by CNET (LCDs With Looks That Kill), all five of the LCD monitors profiled featured a DVI connector. DVI adoption in PC hosts, including motherboards and add-in-boards (AIBs), is also growing, driven largely by pull-through demand from LCD monitor users. DVI is featured on 79 percent of all AIBs available for sale, and according to market research firm DisplaySearch's Q1 2004 Display Electronics Report, host-side DVI adoption has reached 37 percent.

WHY DVI?

The CRT display is an analog device that is driven by analog technology (VGA). With the growing popularity of digital displays such as LCD monitors, a new digital interface was required. In the late 1990s, several different digital standards began to emerge. In 1998, the Digital Display Working Group (DDWG) was formed to address the limitations of these proposed digital solutions and to develop a universal digital interface standard between a host and a display to facilitate the transition from analog to digital devices. The group's initial members included Fujitsu, Compaq, HP, IBM, Intel, NEC and Silicon Image.

In April 1999, the DDWG released the Digital Visual Interface (DVI) 1.0 specification. Silicon Image contributed its Transition Minimized Differential Signaling (TMDS®) technology to serve as the underlying protocol for DVI. TMDS is the key to cost-effectively transferring digital data at high speeds in a single-link configuration, while also offering a means of doubling the bandwidth with the use of a second, or dual, link. TMDS is proven in Silicon Image's PanelLink™-branded DVI

solutions, which have been shipping since 1997. More than 40 million PanelLink DVI ICs have been shipped to date, more than from any other supplier.

Other Digital Interfaces

Plug & Display and Digital Flat Panel

Before DVI was accepted as the digital interface standard of choice, two other standards were introduced, but neither gained any real market acceptance. These two short-lived standards were Plug & Display (P&D) and Digital Flat Panel (DFP).

Developed by VESA, the P&D standard used Silicon Image's PanelLink TMDS interface protocol and provided optional support for USB, IEEE 1394 and analog. It featured an expensive connector and provided no dual-link option. Due to the expense of the connector and the lack of interest in supporting USB and IEEE 1394, P&D was a short-lived standard.

In response, the DFP standard was developed to provide a less-complex, more cost-effective solution. Adopted by VESA as a standard, DFP introduced a smaller, more cost-effective connector. Like P&D, it was also based on Silicon Image's PanelLink TMDS protocol. However, P&D offered no analog support and no dual-link option or upgrade path for faster speeds.

Addressing the limitations of P&D and DFP, DVI became the standard of choice by offering the best features, less complexity and an upgrade path for faster speeds, all while balancing overall cost. Like the earlier digital interface alternatives, DVI is based on Silicon Image's PanelLink TMDS technology. DVI offers analog support through pins on the host side connector, which eliminates the need for a redundant VGA analog connection. DVI is available in a dual-link option, providing an upgrade path for even higher-level resolutions. DVI is cross compatible with P&D and DFP via a mechanical dongle connector.

Low Voltage Differential Signaling

Within a notebook, Low Voltage Differential Signaling (LVDS) is currently the most common interface between the display controller and the LCD panel. There are two primary reasons why LVDS was never considered as the external interface between a graphics board and a display. First, LVDS's speed (supported resolutions) is limited by cable length, whereas DVI can support cables up to 15 meters, depending on the robustness of the DVI transmitter and receiver. Second,

various video modes would require cabling and connectors with more or less signals (or pins), resulting in no universal connection solution.

In addition, LVDS can only support resolutions up to QXGA (2048 x 1536), while DVI can support QXGA and greater resolutions with a dual-link configuration.

Probably the most confusing and complicated aspect of implementing LVDS in a PC is the use of multiple channels for different resolutions and color depths. While TMDS uses only four channels (Red, Green, Blue and Clock) to support up to QXGA (2048 x 1536), LVDS needs 20 channels. It should be noted that the DVI standard supports speeds up to 165 MHz, while TMDS can support speeds up to 225 MHz **[Figure 1]**.

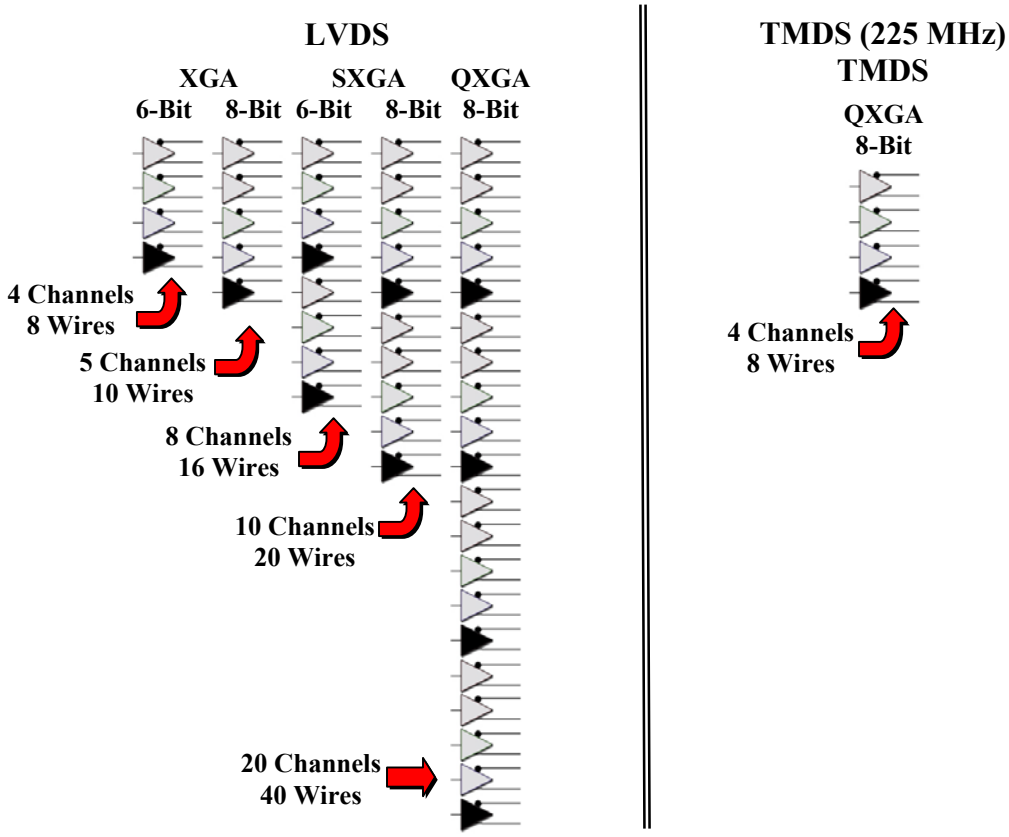


Figure 1: LVDS vs. TMDS

Digital vs. Analog

The advantages of digital (DVI) vs. analog (VGA) are numerous. However, the key difference is that all PC hosts and LCD monitors are innately digital. Because CRTs have analog inputs, a PC must take an additional step and convert the digital data, essentially a string of digital ones and

zeros, into analog voltages before it can be transmitted to a CRT monitor. This is done through the addition of a digital to analog converter (DAC) in the PC. Because LCD monitors are innately digital devices, LCD monitors with analog inputs require two such conversions. First, the PC must convert the data to analog format, as is the case with a CRT monitor. Then, the analog LCD monitor must have an analog to digital converter (ADC) and associated logic to convert the signal back to digital ones and zeros before it can be shown on the display **[Figure 2]**. The biggest drawback of this approach is that the quality of the image is degraded with each of these conversions. For instance, static content, such as text, can appear to move, or "jitter." In addition, analog interface technology is prone to errors and noise, requiring users to make frequent image adjustments to correct fuzziness and color variations. Finally, the need for this analog to digital conversion on the display side of the link adds unnecessary costs to the monitor.

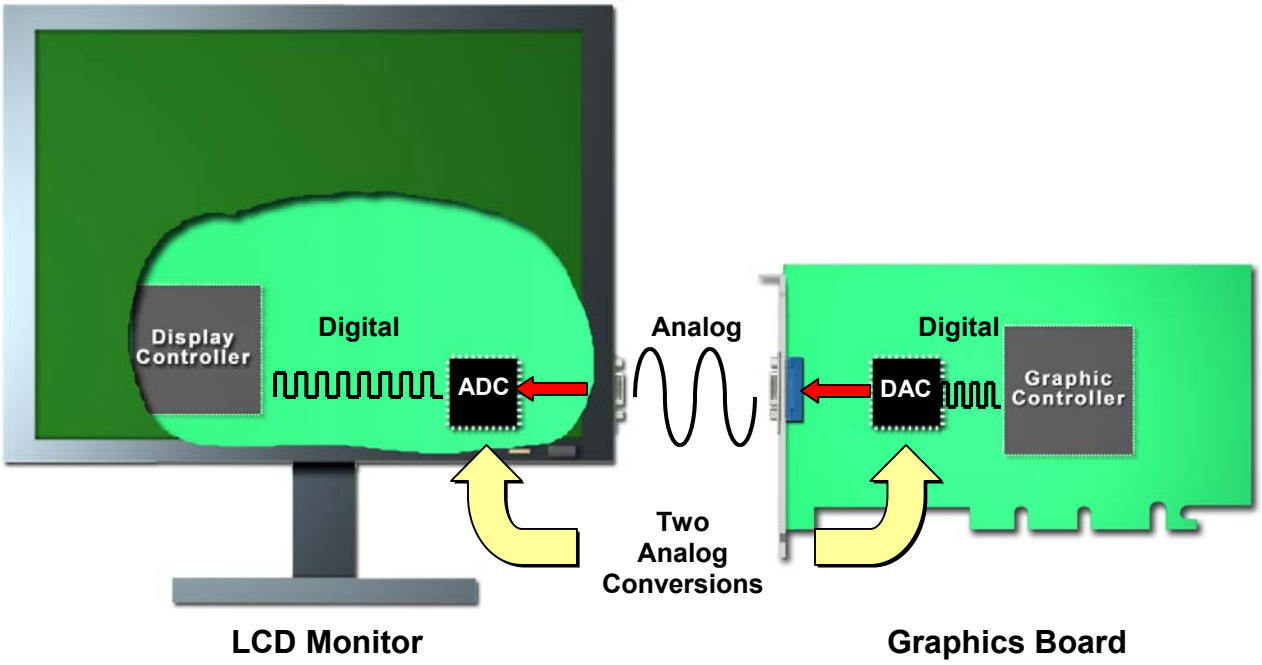


Figure 2: Analog Conversions

Figure 3 below represents a pure-digital signal from a graphics controller directly to an LCD monitor using a TMDS transmitter and receiver from Silicon Image with no data conversions. This method ensures no errors are introduced by converting data back and forth.

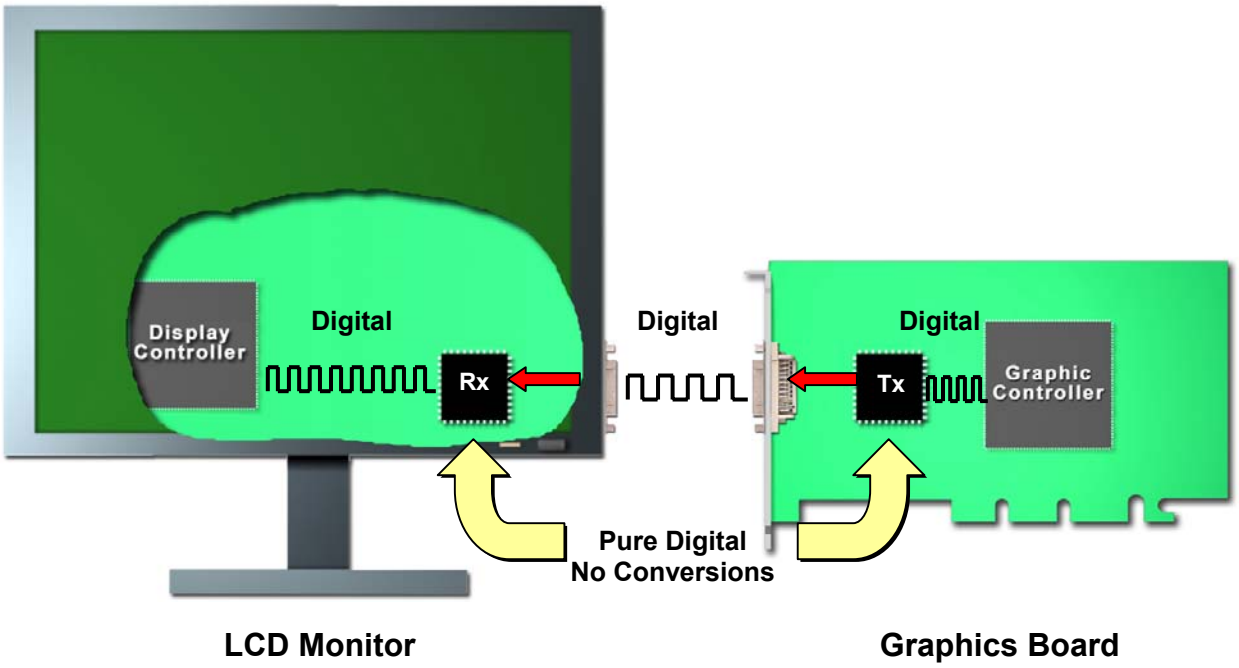


Figure 3: Digital-Only Interface

In summary, DVI ensures data integrity due to no data conversions. Further, DVI is an uncompressed digital signal providing the best image quality, while also reducing the cost of components and complexity required to support an analog signal. DVI is the only solution that supports very high-resolutions, such as 9.2 Megapixel (3840 x 2400) displays. DVI can support bandwidths higher than 330 MHz in a dual-link configuration. While VGA supports only analog displays, DVI also supports VGA (passed through) for legacy device support. DVI can also support High-bandwidth Content Protection (HDCP), which is discussed in more detail later in this paper.

One of the most popular uses for DVI is the digital interface between a graphics board and an LCD monitor **[Figure 4]**.

Figure 4: Major DVI Components

There are four main components to the DVI standard:

1. TMDS transmitter
2. TMDS receiver
3. DVI connector
4. DVI cable

The TMDS transmitter or receiver may be either integrated within the graphics/display controller or implemented as a discrete component. For the purposes of this white paper, we will always assume the TMDS capability is being provided by a discrete component.

Graphics Controller:

To drive an LCD and light up a pixel, three color components are required: Red, Green and Blue (RGB). Each color component has 8 bits that allow 256 different color shades to be selected. Using a combination of 256 shades for each color (RGB) allows up to 16 million colors to be displayed. The graphics controller outputs 24 bits in parallel with 8 bits representing each color component to the TMDS transmitter.

TMDS Transmitter:

The TMDS transmitter receives the 24 bits of parallel data and then prepares the data for transmission by encoding and serializing it. Each RGB color component and the clock are transmitted on separate channels in a process known as differential signaling. There are a total of four channels (differential pairs): three for RGB and the fourth for the clock.

TMDS Receiver

The TMDS receiver receives the serial data, including the clock, via the four channels and then decodes the data and outputs the data in parallel to the display controller.

Single Link vs. Dual Link:

The DVI standard defines a single-link bandwidth of 165 MHz, or support for resolutions up to 1600 x 1200 at 60 Hz **[Figure 5]**. For speeds greater than 165 MHz, dual-link DVI is an option **[Figure 6]**. Please note, these figures have been simplified and do not represent all of the inputs/outputs and control signals between the graphics controller, TMDS transmitter/receiver and the display controller. A dual-link solution uses two transmitters and two receivers to double the single-link DVI bandwidth to 330 MHz and greater, providing plenty of headroom for higher-resolution monitors than those currently available on the market.

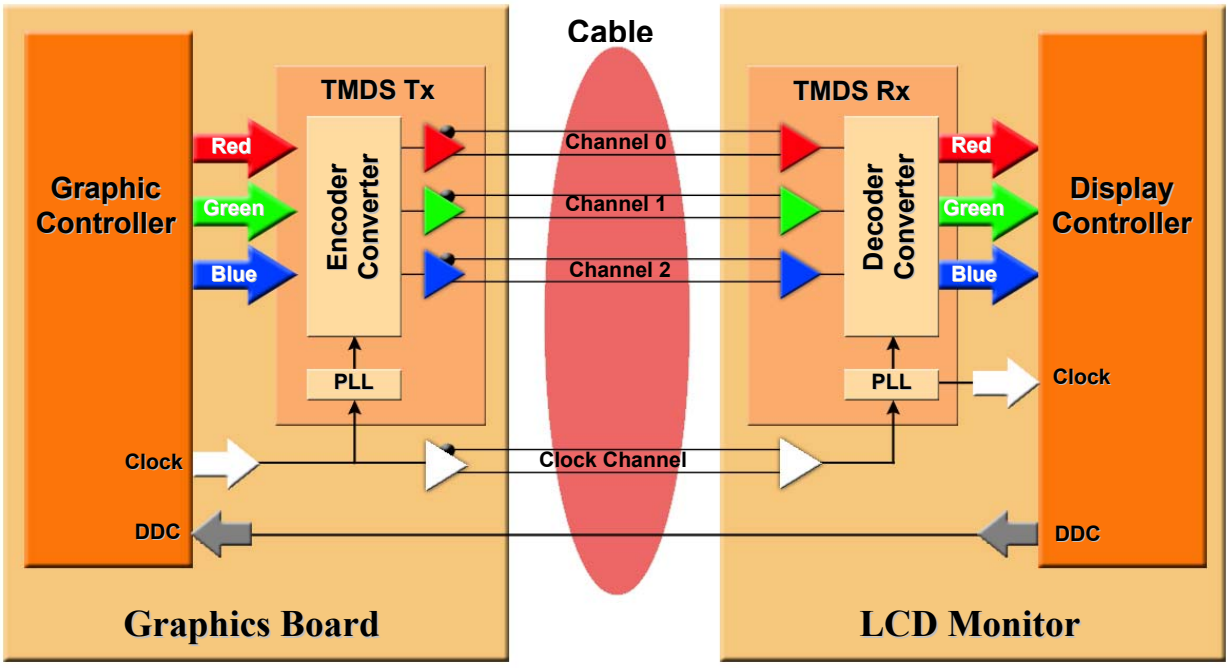


Figure 5: Single-Link DVI

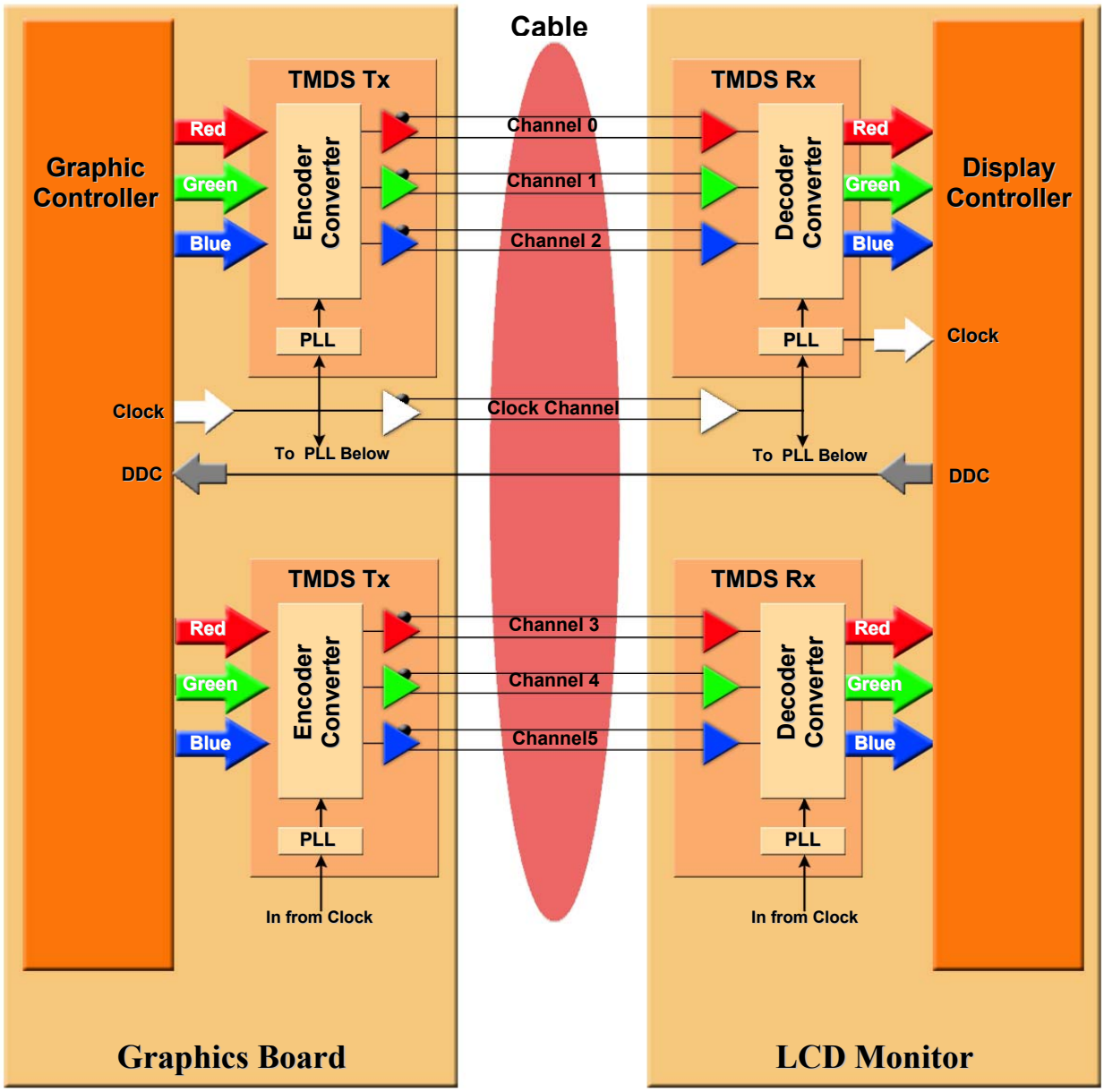


Figure 6: Dual-Link DVI. Although not shown, both transmitter PLLs are linked together, as are the receiver PLLs.

Silicon Image's TMDS technology serves as the underlying protocol for both the DVI and HDMI standards. TMDS is the key to transferring digital data from a TMDS transmitter to a TMDS receiver at high speeds up to 225 MHz, enabling support for resolutions up to 2048 x 1536 (QXGA) in a single-link configuration. The DVI standard supports speeds up to 165 MHz. TMDS also offers a cost-effective means of doubling bandwidth with the use of a second link to accommodate even higher-resolution PC displays. As discussed previously, a dual-link solution uses twice as many data channels to double the maximum bandwidth, currently 2x 225MHz = 450MHz. This number will continue to grow.

A TMDS link consists of a single clock channel and three data channels (for RGB). An advanced data-encoding algorithm, implemented on each of the three data channels, converts 8 bits of video or audio data into a 10-bit transition-minimized, DC-balanced sequence. This makes transmission very robust, while at the same time minimizing EMI over copper cables. Receiver data recovery is very reliable due to the advanced encoding algorithm and unique data clocking architecture, thus achieving greater skew-tolerance for transmission over longer cable lengths. More details on TMDS technology are below.

Transition Minimization: The 8- to 10-bit transition minimization and DC balancing performed by TMDS may at first seem counter-productive, increasing the data rate of the link while not carrying any more data. In actuality, this advanced algorithm creates a special 10-bit sequence that can more reliably be transmitted across long and inexpensive copper cables. Because each one of the 1-to-0 or 0-to-1 transitions in the original sequence of 8 bits causes generation of radio frequency emissions, reducing the number of transitions reduces the level of emissions. This, in turn, reduces the possibility of interference between a user's electronic devices.

Figure 7 below is an example of a graphics controller sending 8 bits of RED data in a parallel stream. To minimize transitions, the following steps are taken:

1st: A stream of 8 bits of parallel data for the RED component is sent into the TMDS transmitter

2nd: The data is serialized

3rd: The transitions are minimized, and a 9th bit is added to show the data was encoded

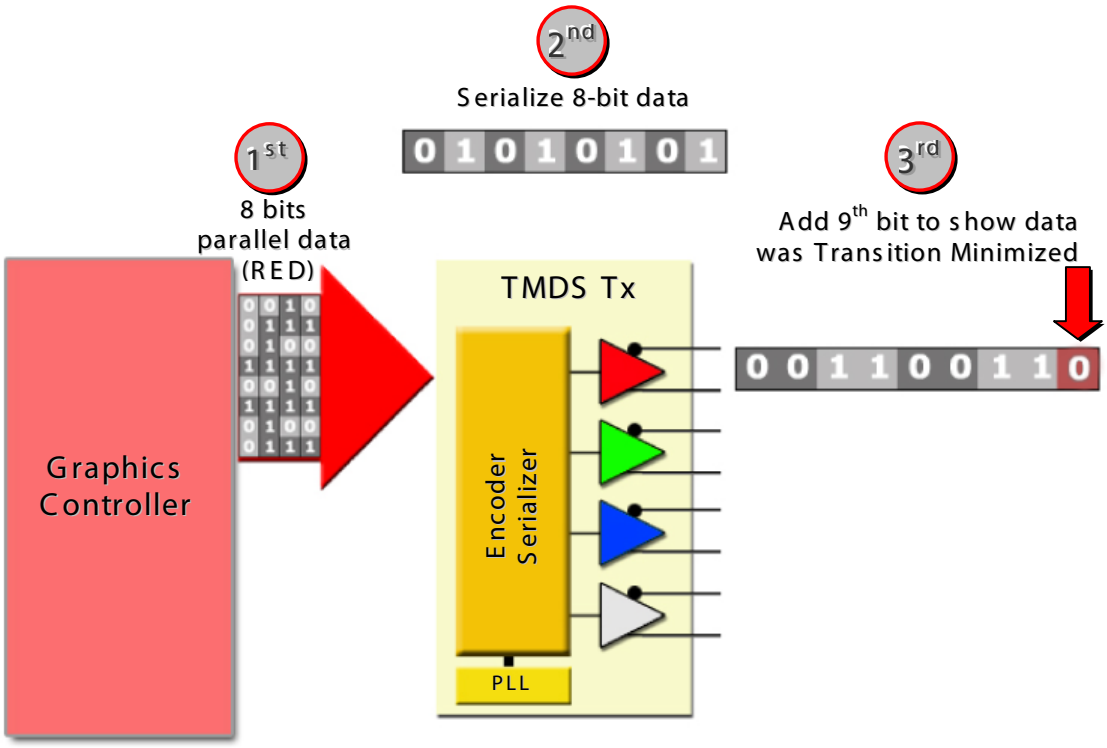


Figure 7: TMDS Transmitter

Figure 8 below explains in more detail how minimizing transitions is accomplished. In this example, we take the worst case senario (seven transitions), where each bit transitions to a different state in the 8-bit word.

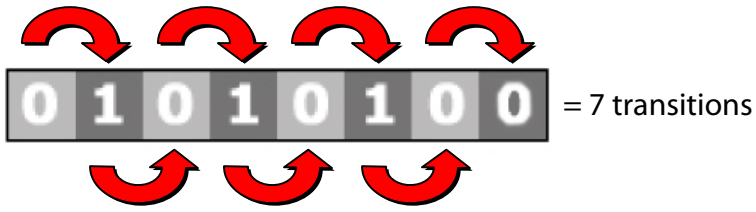


Figure 8: Too Many Data Transitions

The TMDS algorithm minimizes the transitions to three by doubling up on each transition, adding a 9th bit and clearing this to a 0 state to show this 8-bit word was encoded with ***Transitions Minimized***. This enables the transitions to be reduced from seven to three **[Figure 9]**.

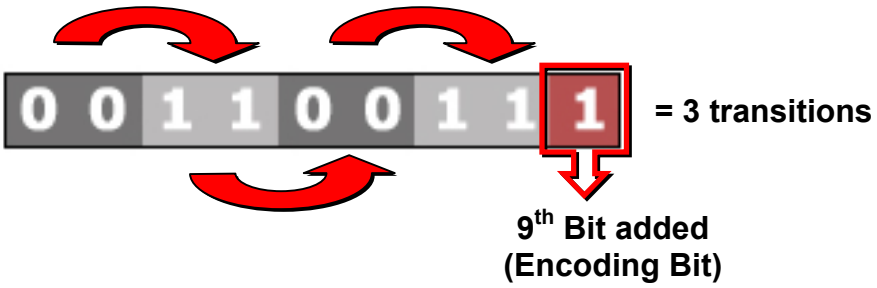


Figure 9: Minimizing Transitions

With 8b/10b encoding, there is an additional 10th bit added to every 8-bit word.

DC Balancing: One of the problems with transmitting a series of 1s or 0s over a cable at very-high speeds is the electrical characteristic of charging a line. This occurs when you send a long stream of 1s or 0s. **Figure 10** below is an example of a long stream of 1s being sent over the line. Note, the 9th and 10th encoding bits are left out to simplify the example.

Figure 10: Series of 1s Data Words

The charge on the cable tends to resist the subsequent change of data to the opposite state and will cause data errors. The method used to solve this problem is called DC balancing. DC balancing inverts (from 1 to 0 or 0 to 1) some of the bits in the sequence and then marks them as inverted.

The process for ensuring the data stream is DC balanced is very simple. In **Figure 11**, we pick one word (8-bits) from a series of words that have the same state.

Original 8-bit word

Figure 11: Original Data Word

The 9th bit indicates no encoding is required to minimize transitions, as there are no transitions between each bit **[Figure 12].**

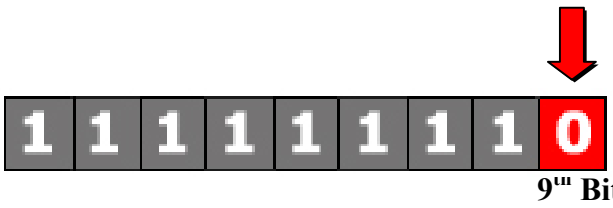


Figure 12: No TM Encoding Required

The 10th bit is turned "on" to indicate polarity reversal.

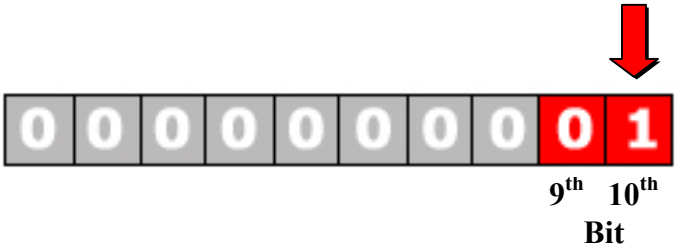


Figure 13: DC-Balanced Encoded Bit

In the above example **[Figure 13]**, the 9th bit is 0 to indicate the data word required no encoding to minimize transitions.

Below is the data stream that is now DC balanced. Note, the 9th and 10th encoding bits are left out to simplify the example **[Figure 14]**.

Figure 14: DC-Balanced Data Words

Differential Signaling: Besides minimizing transitions to help increase high speeds, the other critical factor is to increase the immunity to radio frequency and other electrical noise. A normal digital serial transmission consists of a series of 1s and 0s sent on one wire, which makes it susceptible to electrical impulses **[Figure 15]**.

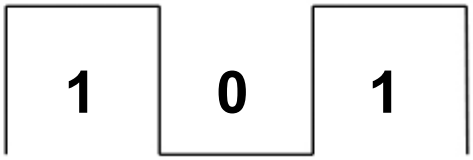


Figure 2: Digital Signal

Differential signaling uses two wires, with the second wire transmitting the opposite value of the first **[Figures 16 and 17]**.

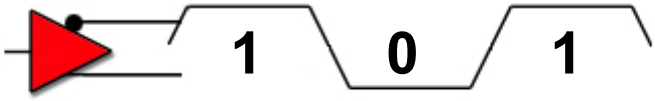


Figure 16: Differential Signal

Figure 17: Differential Signal (Two Wires)

The receiver can then subtract one signal from the other, thereby canceling out any noise that was picked up by both wires but still recovering the transmitted data **[Figure 18]**.

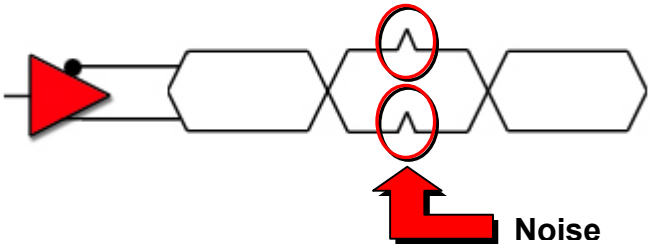


Figure 18: Noise on Line

DVI Signaling

There are three different types of DVI connectors that can be implemented: DVI-I supports both digital and analog; DVI-D supports digital only; and DVI-A supports analog only.

The most common DVI connector is DVI-I, as this offers the flexibility to drive either a digital or an analog display interface. A special adapter may be attached to the DVI-I connector on the graphics board to allow the user to attach a VGA cable to a display that supports an analog interface.

A DVI-I connector has a total of 29 pins available for use: 18 pins are used for TMDS, including the pins for a dual-link configuration; 6 pins are used for reserved for analog; and 5 pins are for Plug & Play **[Figures 19 and 20]**.

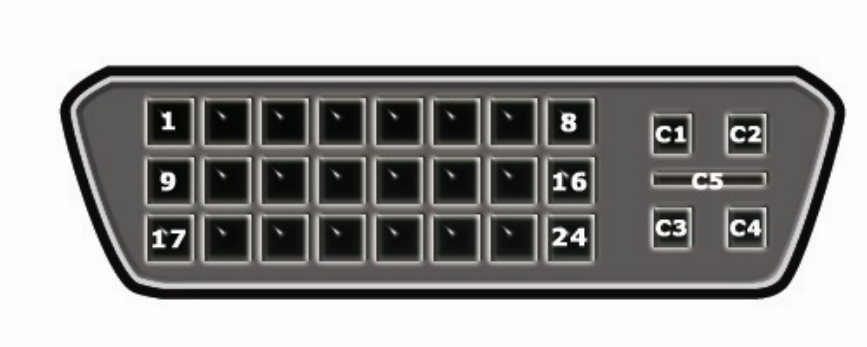


Figure 19: DVI-I Signal Pins

Pin	Signal	Pin	Signal	Pin	Signal
1	Data 2 -	9	Data 1 -	17	Data 0 -
2	Data 2 +	10	Data 1 +	18	Data 0 +
3	Shield (2 & 4)	11	Shield (1 & 3)	19	Shield (0 & 5)
4	Data 4 -	12	Data 3 -	20	Data 5 -
5	Data 4 +	13	Data 3 +	21	Data 5 +
6	Clock DDC	14	Power +5V	22	Shield Clock
7	Data DDC	15	Ground	23	Clock +
8	Analog Vertical Sync	16	Hot Plug	24	Clock -
C1	Analog Red				
C2	Analog Green				
C3	Analog Blue				
C4	Analog Horizontal Sync				
C5	Analog Ground				

TMDS
PLUG & PLAY
ANALOG

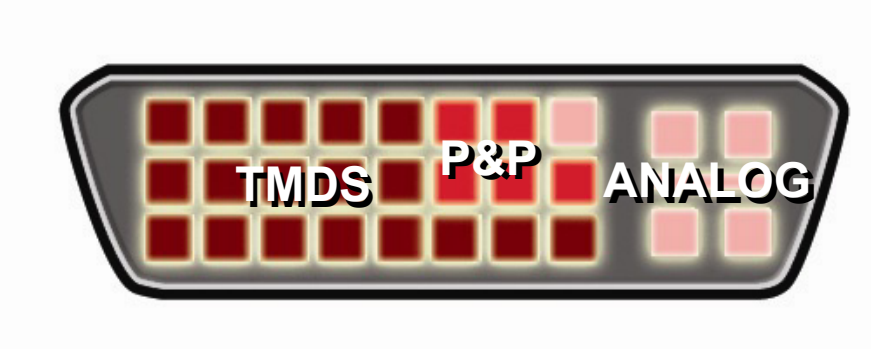


Figure 20: TMDS, Plug & Play and Analog Signals

EDID

EDID (Extended Display Identification Data) is a subset of Plug and Play and is the method used by the display to provide important information back to the host device via the Display Data Channel (DDC), or in our case the graphics board. A standard developed by VESA, EDID was designed to ensure the host device has the basic information about the attached display so the host can be properly configured and/or optimized for that display device. For example, the display would provide information to the host on all the resolutions supported.

Display Basics

One of the major differences between a CRT and an LCD monitor is that the LCD uses a fixed array of pixels. This is where the term ***native resolution*** is commonly used. While a CRT has the advantage of supporting multiple resolutions without affecting image quality, an LCD is best viewed at its ***native resolution***. Scaling is the method used to solve the problem of supporting multiple resolutions below the native resolution of an LCD monitor.

In **Figure 21** below, we have magnified an area of the LCD panel so you can see the pixels that compose the native resolution of the display. An LCD monitor with a native resolution of 1600 x 1200 (UXGA), or 1.9 megapixels, is used for the purposes of this example.

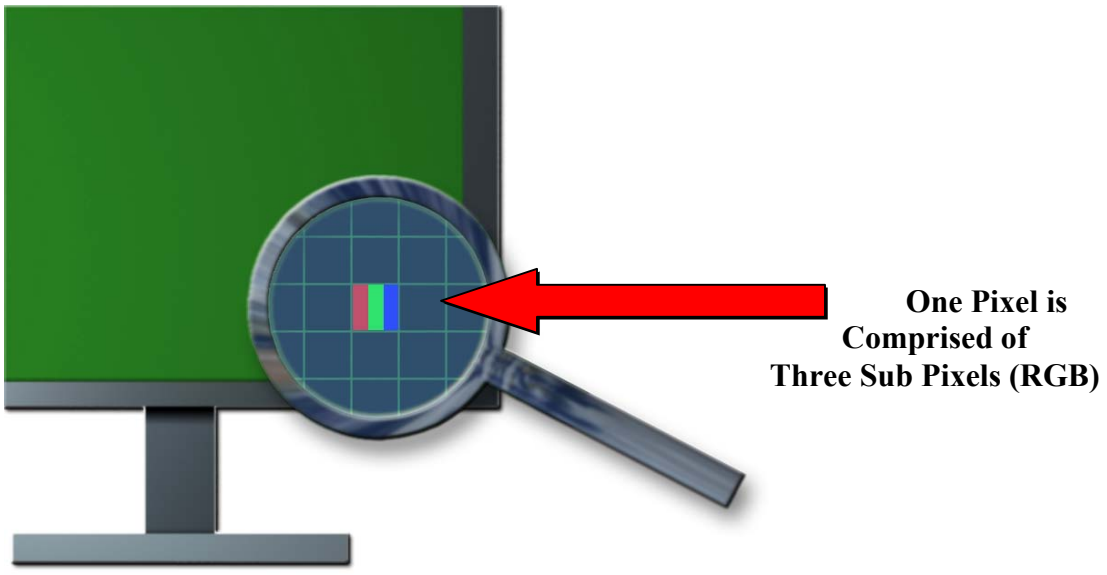


Figure 21: Sub Pixels

A graphics board must constantly send out a stream of pixel data to tell the display controller when and where a pixel needs to be turned on. This is coordinated via the pixel clock. The pixel data (24 bits) determines the color of the pixel by the 256 levels set for each RGB sub pixel.

Pixel Clock

The pixel clock provides the display controller with all the information required to light up a pixel, row-by-row, and frame-by-frame.

The pixel clock is approximately determined by calculating the total number of pixels multiplied by the refresh rate. For example, the pixel clock for 1600 x1200 (UXGA) at 60 Hz would be ~115 MHz, but there are also other factors like blanking time etc. that add much more overhead to the pixel clock time.

Figure 22 below represents the total pixel clock time (not pixels) it takes to display an image on a CRT or LCD monitor. The margin area is not used or viewable to the end user. The blanking area is especially important when driving a CRT display, as this is the time when the CRT gun is turned off at the end of a row, repositioned to the beginning of the next row, and turned on again. Also, when the CRT gun has completed one frame (bottom right-hand corner), it then needs to be repositioned to the first pixel in the first row (top left-hand corner).

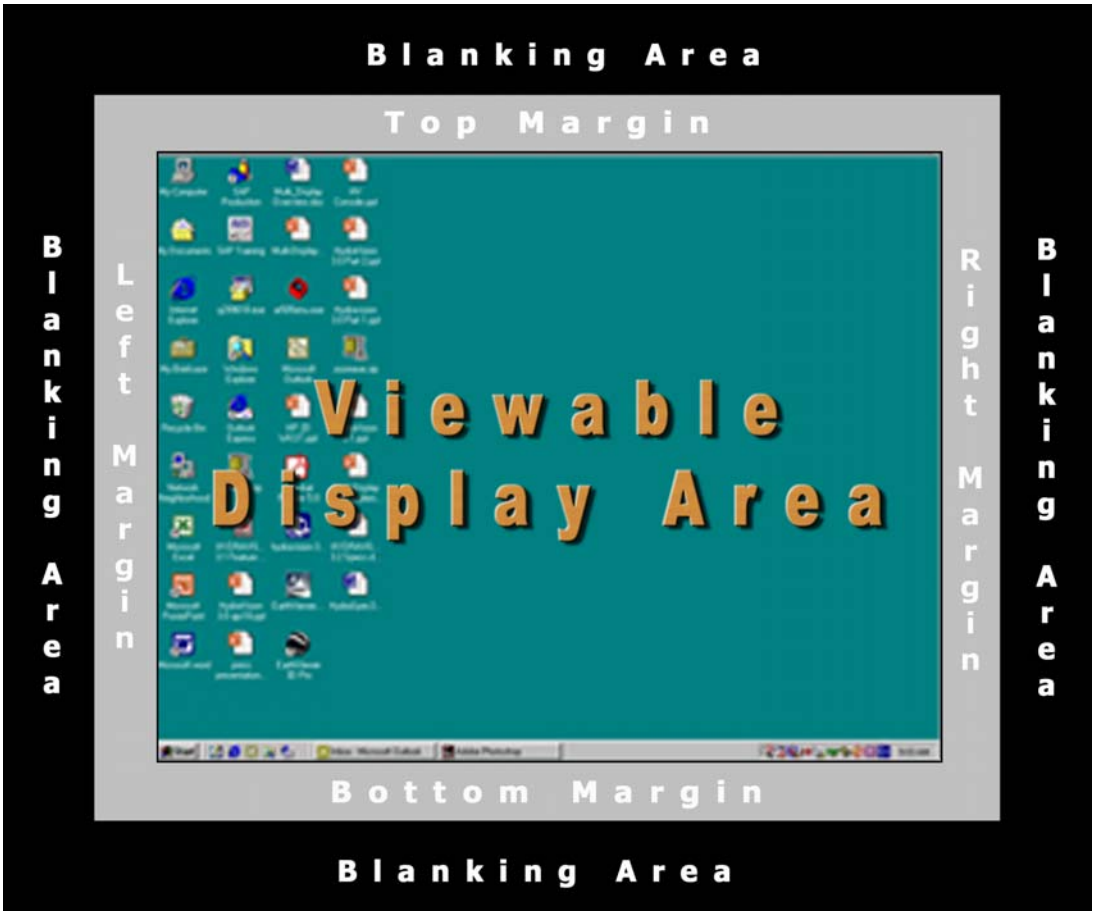


Figure 22: Blanking Area

As you can see, the blanking time can take up approximately 25 percent of the total pixel clock time and was implemented due to the time it takes to re-position a CRT gun in an analog display device. However, LCD technology requires no CRT gun, and thus most of the blanking time is wasted for a digital display device.

This is important because you normally need to increase your pixel clock time to achieve higher-resolution support. However, TMDS transmitters and receivers supporting the DVI standard only support a pixel clock of up to 165 MHz (single link), which equates to a resolution of 1600 x 1200 at 60 Hz. The problem arises if you need to support a resolution just a little higher, such as the HDTV resolution of 1920 x 1080 or a widescreen PC resolution of 1920 x 1200. Implementing dual link is an option, but an easier and more cost-effective method is called reduced blanking.

In theory, single- and dual-link support have a clear dividing line. Single-link DVI supports resolutions up to 1600 x 1200 (165 MHz), and dual link can support much higher resolutions (330 MHz and greater) **(Figure 23)**. But in reality, single link can support up to 3840 x 2400 **(Figure 24)**.

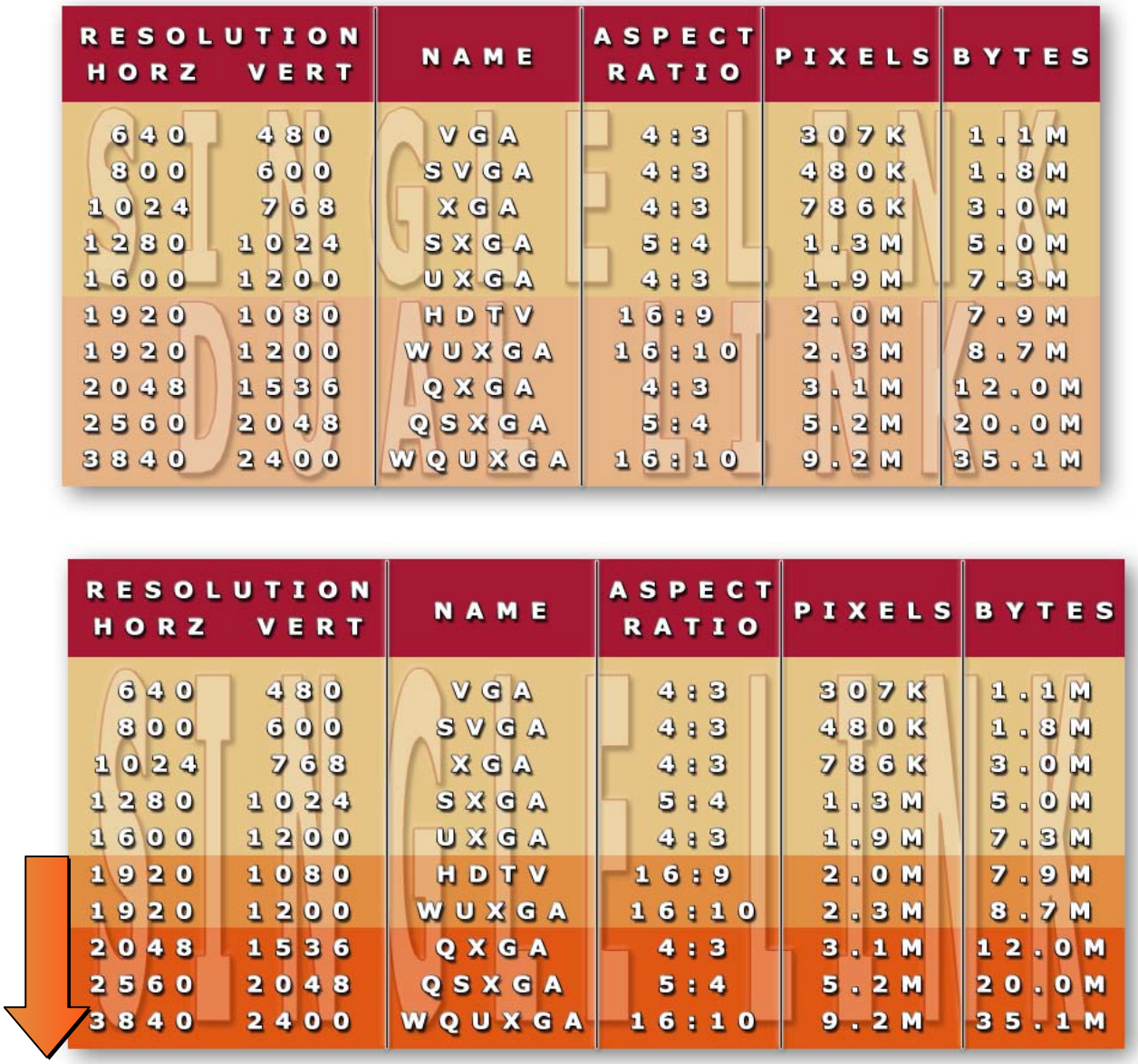


Figure 23: Increasing Single-link Support

There are two reasons why single link can support resolutions higher then 1600 x 1200. First, by using reduced blanking, LCD monitors can recapture much of the wasted pixel clock time used during the blanking period. Since there is no CRT gun required for repositioning, this valuable time can now be used to light up pixels without needing to implement a dual-link strategy. Reducing the refresh rate (Hz) is another method used to support higher resolutions like 3840 x 2400.

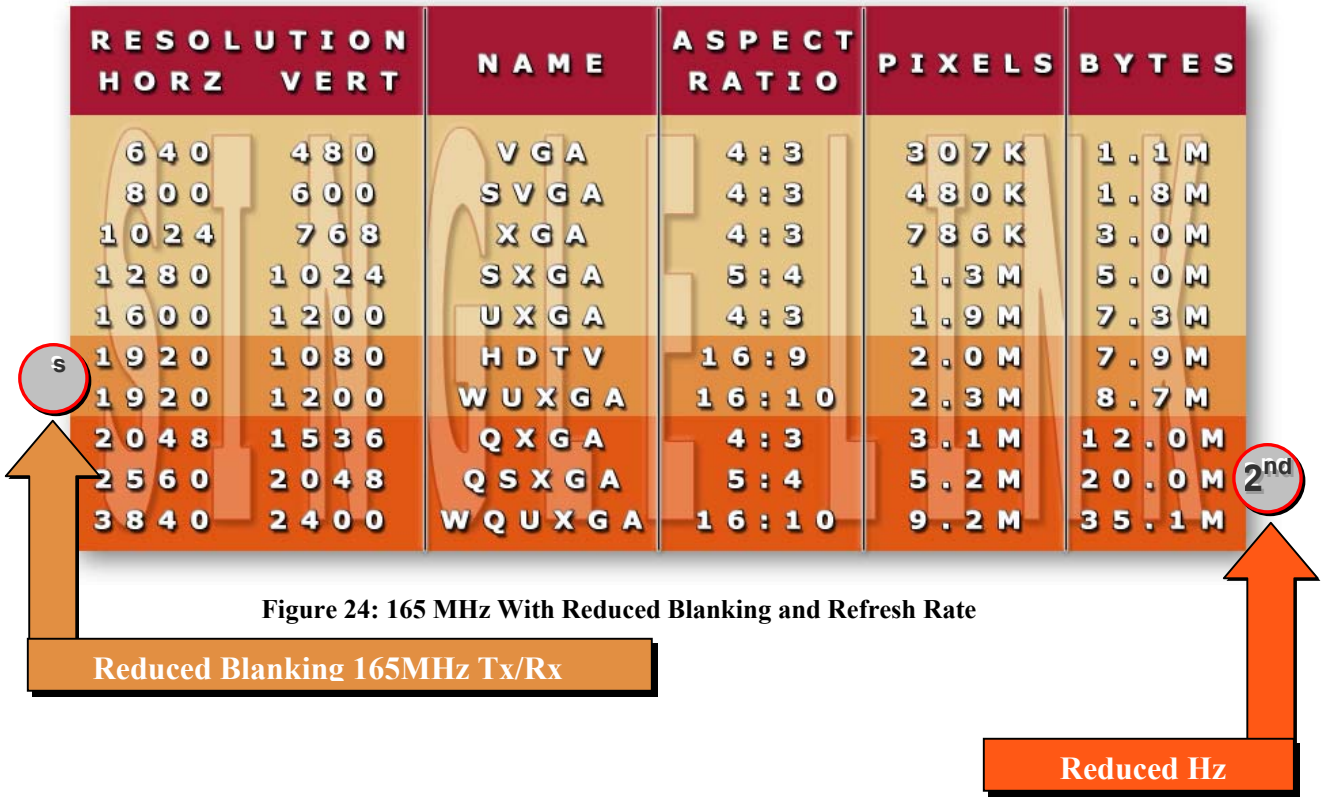


Figure 24: 165 MHz With Reduced Blanking and Refresh Rate

DVI Configurations

There are three ways to provide a DVI solution on a PC: via a graphics board; an ADD (AGP Digital Display) card; or a motherboard. The graphics board may feature either an integrated or a discrete transmitter. An ADD card is a board that features only a TMDS transmitter and no Graphics Processing Unit (GPU). This option would be used if you have integrated graphics on the PC motherboard, but want to have a DVI port without having to upgrade to a more expensive graphics board with DVI **(Figure 25)**.

Figure 25: Silicon Image ADD Card

In the case of a PC motherboard, a discrete TMDS transmitter can be located directly on the PC motherboard itself for the lowest cost solution, while the DVI connector is located on the chassis. Currently there are some OEM PCs shipping with this configuration as a standard feature. In addition, any motherboard using an integrated graphics chipset (i.e. ATI, Intel, or NVIDIA) and supporting a graphics expansion slot can drop in a DVI ADD card as a flexible DVI upgrade solution.

Graphics board vendors implement DVI in many different configurations, and below are a few examples **[Figures 26 and 27]**:

Board	Single Link Ports	Dual Link Ports	Connector
A	1	0	DVI & VGA
B	2	0	DVI x 2
C	1	1	DVI x 2
D	0	2	DVI x 2
E	4	0	High Density DVI x 2
F	2	0	High Density

Figure 26: Different DVI Configurations

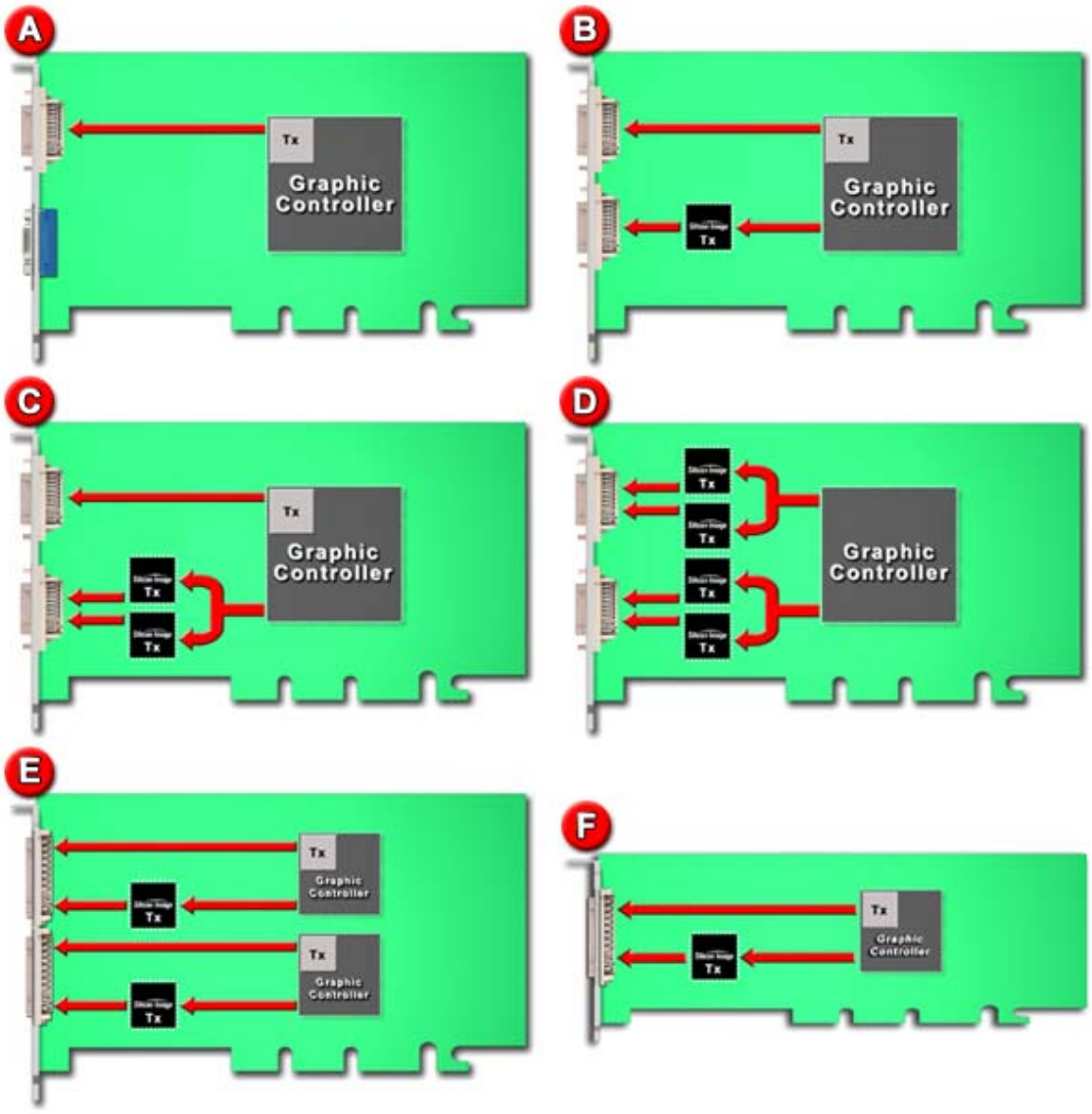


Figure 27: Board Configuration Examples

Single-link DVI is a very versatile, cost-effective and proven digital display interface. For this reason, it is also used to drive a high-resolution display known as the 9 megapixel display (3840 x 2400). Remember, the maximum speed for a DVI single-link transmitter is 165 MHz, which will drive resolutions up to1600 x 1200 at 60 Hz without reduced blanking. Even with reduced blanking, there is still not enough bandwidth in the pixel clock to drive a 9 megapixel display. However, the main factors that affect the pixel clock are resolution, blanking time and the refresh rate. The 9 megapixel display takes advantage of this by reducing the refresh rate and also has the option of using more than one DVI single link to drive the display.

Basically, a 9 megapixel display can be divided into four quadrants of 1920 x 1200, or two of 1920 x 2400. This allows the display to be driven by one, two or four single-link DVI ports.

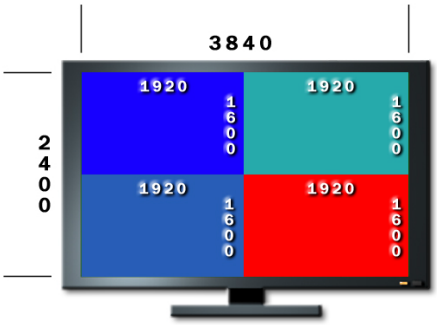


Figure 28: 9 Megapixel Display

The overall refresh rate of the display will increase along with the more DVI ports used. The refresh rate is important when using 3D applications like CAD or animation software. But the refresh rate is not as important when viewing high-resolution static images like maps or satellite photos.

Figure 29 below is an example of two single-link DVI ports driving one display. In this configuration, the approximate refresh rate would be 24 Hz.

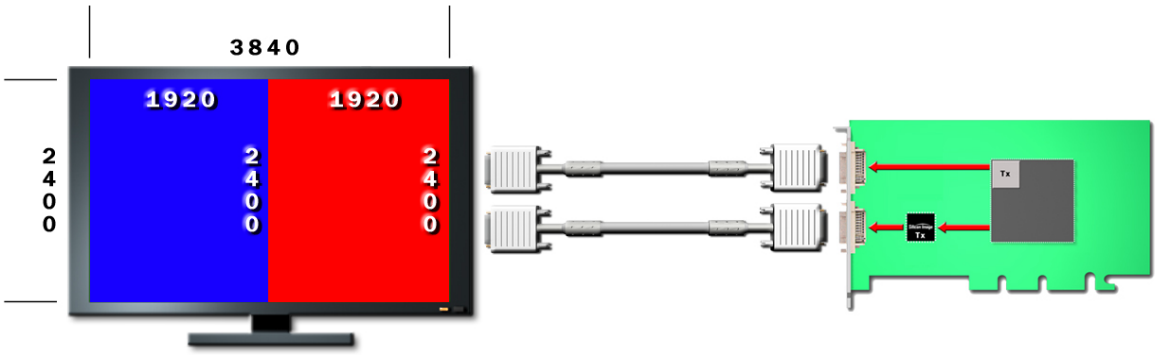


Figure 29: Two Single-Link DVI Ports Driving a 9 Megapixel Display

DMS-59 Connector

In March 2003, VESA introduced a new connector standard (DMS-59) based on a high-density connector **[Figure 30]**. The purpose of this connector was to solve the problem of driving two displays from one connector. This was required for two reasons:

Low-Profile (LP) graphic boards

LP boards have the advantage of being installed in a slim-line PC where space is always at a premium. However, a LP board is half the height of a standard graphics board, and therefore there is not enough room to install two DVI connectors. The DMS-59 connector solves this problem by

offering a single connector that can drive dual displays. The DMS-59 connector has 60 pins, of which 59 are available for use.

Quad Boards

A quad board is defined as a single graphics board that can drive up to four displays. Similar to the situation with the LP board, there is not enough space to install four DVI connectors due to the size of the DVI connector, so two DMS-59 connectors are used.

The DMS-59 connector requires the use of a special "Y" cable, which allows two displays to be attached via one connector on the graphics board.

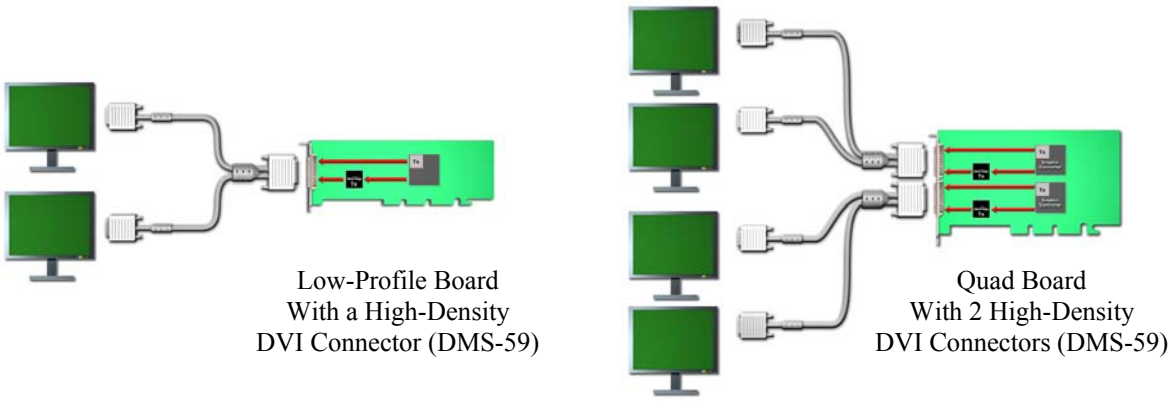


Figure 30: DMS-59 Connector

Why Dual Link?

Dual-link DVI ensures graphics board and display vendors have an easy upgrade path to higher-resolution displays without having to wait for a new technology to be introduced, tested and standardized. The DVI standard was developed by the DDWG with this goal in mind.

Originally, dual link was used to support very high-resolution displays found in specialized markets such as the medical display industry. The dual-link boards were bundled with these devices and normally not available to the mass market. In the last few years, more graphics board vendors are including one dual-link port as a standard feature on their workstation-class boards.

In fact, one vendor recently just announced a 30" high-resolution (2560 x 1600) LCD monitor for the consumer market that requires a board featuring two dual-link ports.

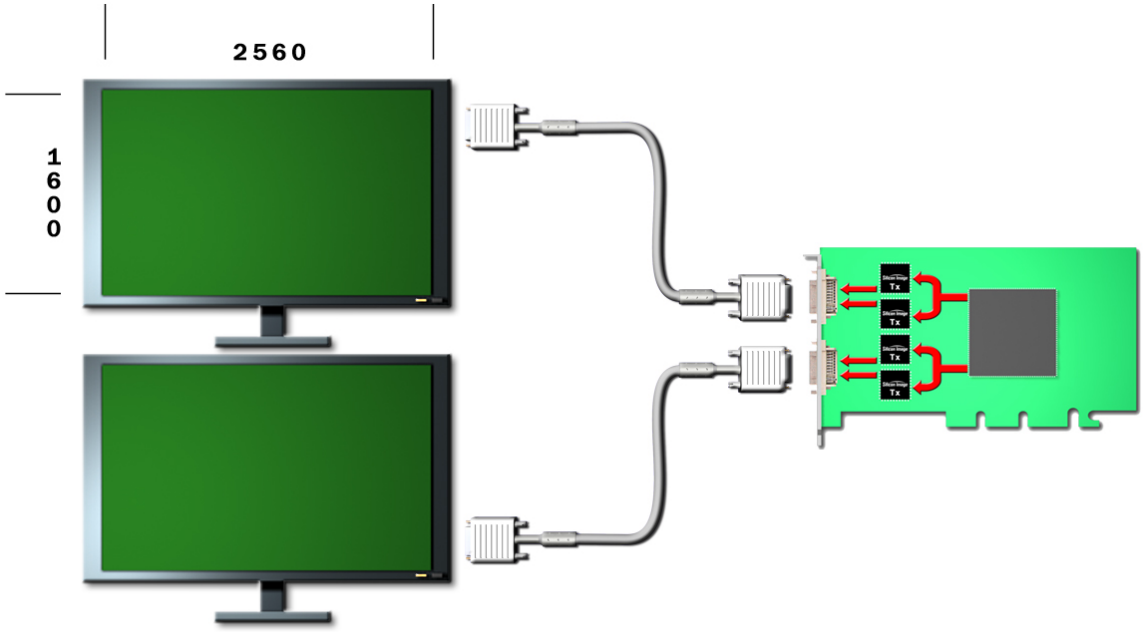


Figure 31: Dual DVI With Dual Links

High-bandwidth Digital Content Protection (HDCP)

A year after the DVI specification was released, Intel introduced High-bandwidth Digital Content Protection (HDCP) with contributions from Silicon Image. HDCP protects content on a digital link by adding encryption capability. Major motion picture providers became interested in DVI with HDCP, as it provides a means of protecting their high-value content from piracy and mass duplication over the Internet. Satellite and cable service providers, seeking a larger library of high-quality HD content for their customers, quickly supported DVI as an output on their STBs. DTV manufacturers responded in kind by incorporating DVI-HDCP inputs on their systems. In 2003, more than 500 consumer electronics devices had DVI-HDCP ports, and approximately 80 percent of new DTVs shipped to the U.S. market had DVI-HDCP inputs.

High-Definition Multimedia Interface

Building upon the success of DVI, High-Definition Multimedia Interface™ (HDMI™) was developed specifically to address the unique requirements of the consumer electronics market. HDMI is also based on Silicon Image's TMDS technology and is backward compatible with DVI. HDMI-enabled devices are backward compatible with the broad array of DVI based PCs so users can display PC gaming or entertainment content on their HDTV.

HDMI provides both uncompressed digital video and multi-channel audio over a single, sleek connector and cable. HDMI replaces the rat's nest of video and audio cables usually found behind a consumer electronics device such as an A/V receiver, dramatically simplifying the user experience. HDMI has quickly emerged as the standard for connecting HDTV, and as of September 2004, more than 25 CE manufacturers had introduced more than 240 systems with HDMI.

Figure 32 below represents a simplified version of an A/V receiver, where it is not uncommon to have five video and six audio cables (all analog). What is not shown are all the duplicate ports for attaching more than one CE device, such as a DVD, DTV or VCR, to an A/V receiver. HDMI replaces the need for all these legacy interfaces and multiple cables with a single cable **[Figure 33]**.

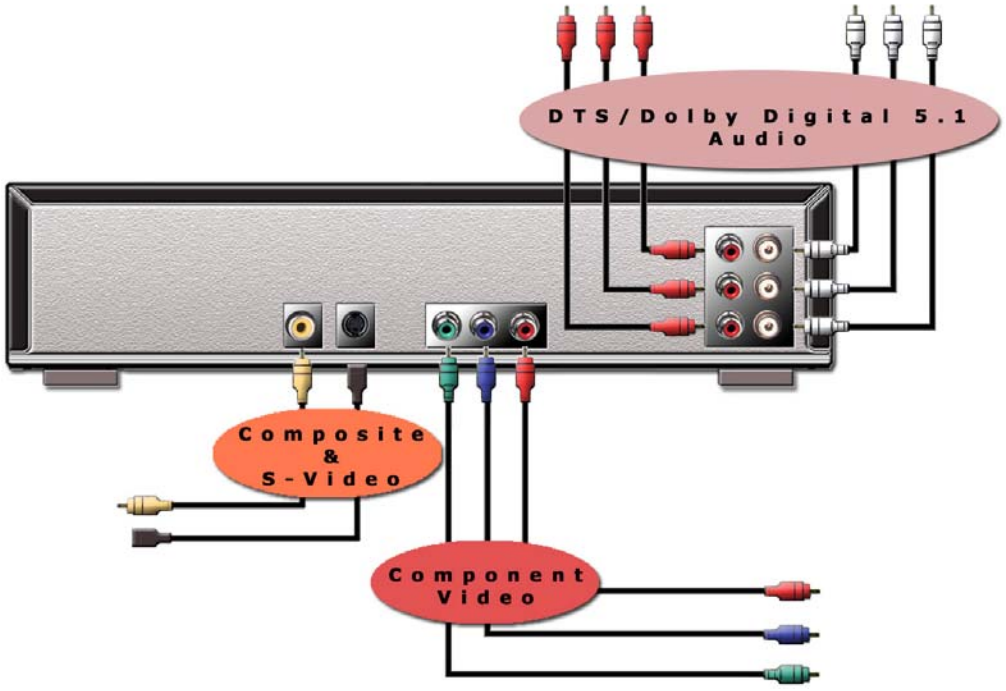


Figure 32: Without HDMI

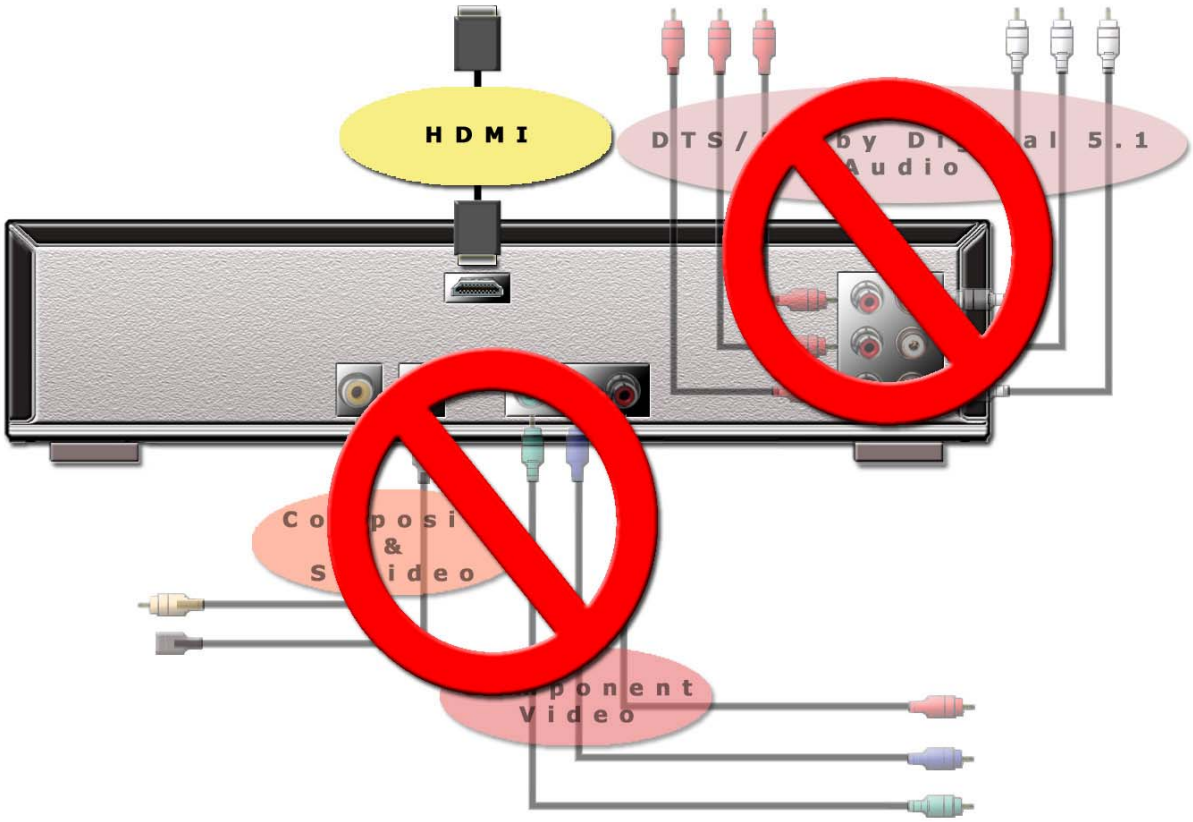


Figure 33: With HDMI

Because it was designed specifically for consumer electronics applications, HDMI offers additional consumer enhancements. Content comes in a variety of sizes, resolutions and formats, and HDMI systems will automatically configure to display content in the most effective format. HDMI also offers universal remote capability through the new Consumer Electronics Control protocol, which provides simple control of an HDMI-linked home theater system from a single remote control unit. This enables automatic configuration of the home theater system on demand, such as turning on or off the components necessary to view a DVD, listen to a CD or watch cable TV.

Internal LCD Architecture

The basic architecture of an LCD monitor includes four main components: (1) Display Board; (2) LCD interface board; (3) LCD panel; (4) backlight.

Many LCD monitors still provide support for VGA even though LCDs are digital devices. This leads to a complex architecture that is no longer required since all the major graphics board vendors have standardized on DVI as the digital interface, which is now widely available **[Figure 34]**.

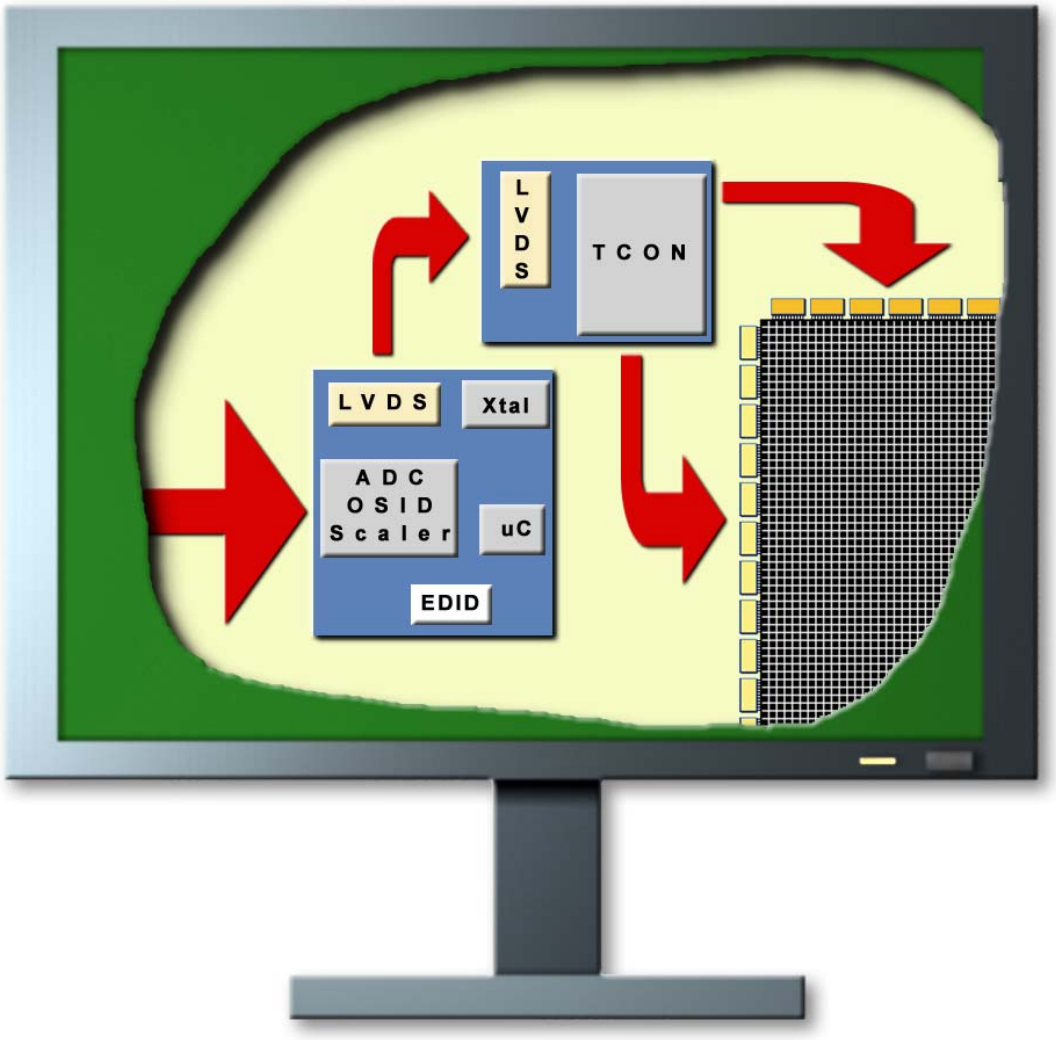


Figure 34: Internal LCD Architecture

Designing a digital-only architecture for an LCD offers a number of advantages **[Figure 35]**. It removes complexity, reduces components/cost and provides a pure-digital signal from host to display.

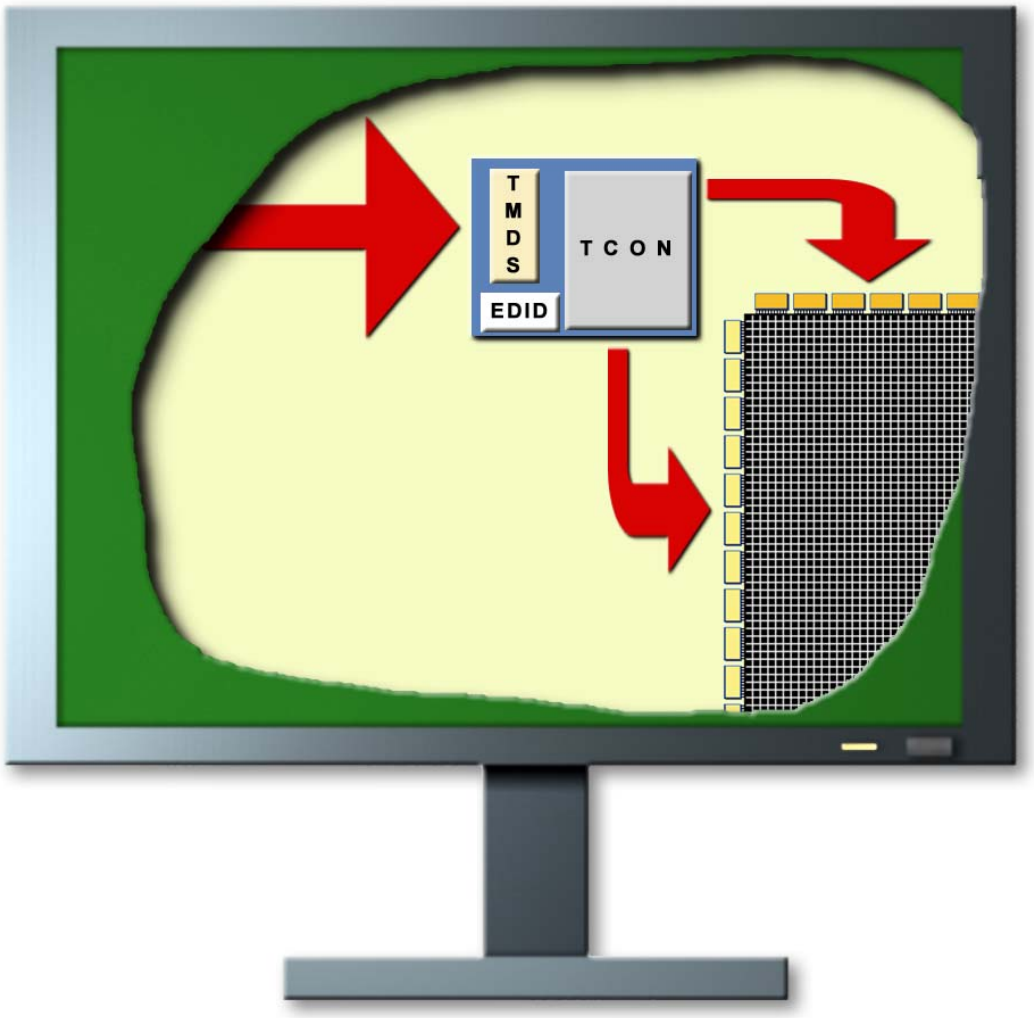


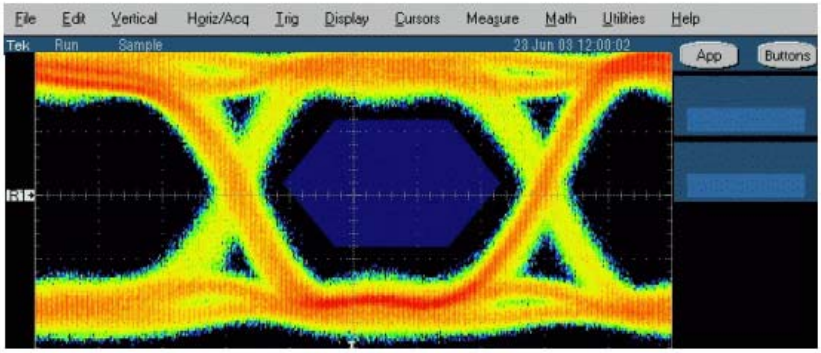
Figure 35: Digital-Only Internal LCD Architecture

DVI Compliance

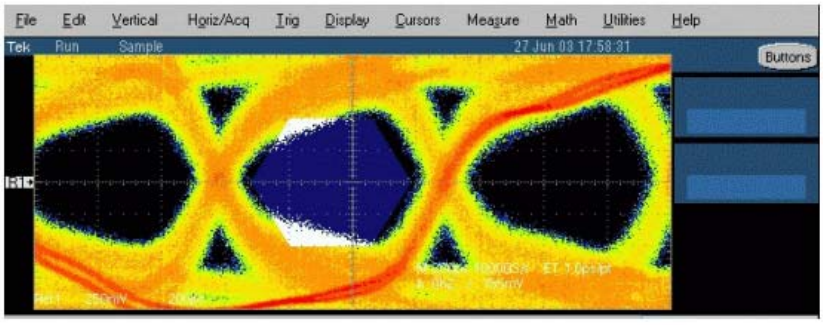
Compliance testing or certification is not a strict requirement of the DVI license. As a result, a number of non-compliant DVI products have entered the market. Until recently, limited options existed for companies wishing to evaluate the compliance of their DVI products. Manufacturers can self-test for DVI compliance, but the necessary equipment and software is expensive, making it prohibitive for many. Furthermore, testing accuracy is dependent upon the test engineer's skill level, so extensive experience and training are necessary. Until recently, the only alternative has been plug testing at VESA-sponsored PlugFests, which is limited to basic interoperability between DVI-enabled source and display devices provided by participating companies.

To address this problem, Silicon Image introduced a DVI Compliance Test Center (CTC) in December 2003 for host devices. The DVI CTC promotes greater interoperability among DVI-enabled devices by providing comprehensive and impartial compliance test services to manufacturers of DVI components and end-user products implementing DVI. The DVI CTC performs testing in accordance with the DVI Test and Measurement Guide Specification published by the DDWG. TMDS eye diagram performance is one of the tests performed as part of this specification, and **Figure 36** below shows examples of compliant and non-compliant DVI eye diagrams.

To ensure compliance testing is widely available to all manufacturers, Silicon Image is willing to assist other organizations that are interested in becoming a DVI CTC.



DVI-Compliant Eye Diagram



Non-compliant DVI Eye Diagram

Figure 36: DVI Eye Diagrams

1060 E. Arques Avenue
Sunnyvale, CA 94085
T 408.616.4000 F 408.830.9530
www.siliconimage.com