AUDIO MODULATED MATRIX LED DRIVER

July 2017

GENERAL DESCRIPTION

The IS31FL3732 is a compact LED driver for 144 single LEDs. The device can be programmed via an I2C compatible interface. The IS31FL3732 offers two blocks each driving 72 LEDs with 1/9 cycle rate. The required lines to drive all 144 LEDs are reduced to 18 by using the cross-plexing feature optimizing space on the PCB. Additionally each of the 144 LEDs can be dimmed individually with 8-bit allowing 256 steps of linear dimming.

To reduce CPU usage up to 8 frames can be stored with individual time delays between frames to play small animations automatically. LED frames can be modulated with audio signal.

IS31FL3732 is available in QFN-40 (5mm×5mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +85°C.

FEATURES

- Supply voltage range: 2.7V to 5.5V
- 1MHz I2C-compatible interface
- 144 LEDs in dot matrix
- Individual blink control
- Individual PWM control 256 steps
- Individual on/off control
- Global current control 256 steps
- Cascade for synchronization of chips
- 8 frames memory for animations
- Picture mode and animation mode
- Auto intensity breathing during the switching of different frames
- LED frames displayed can be modulated with audio signal intensity
- LED light intensity can be modulated with audio signal intensity
- QFN-40 (5mm×5mm) package

APPLICATIONS

- Mobile phones and other hand-held devices for LED display
- LED in home appliances

TYPICAL APPLICATION CIRCUIT

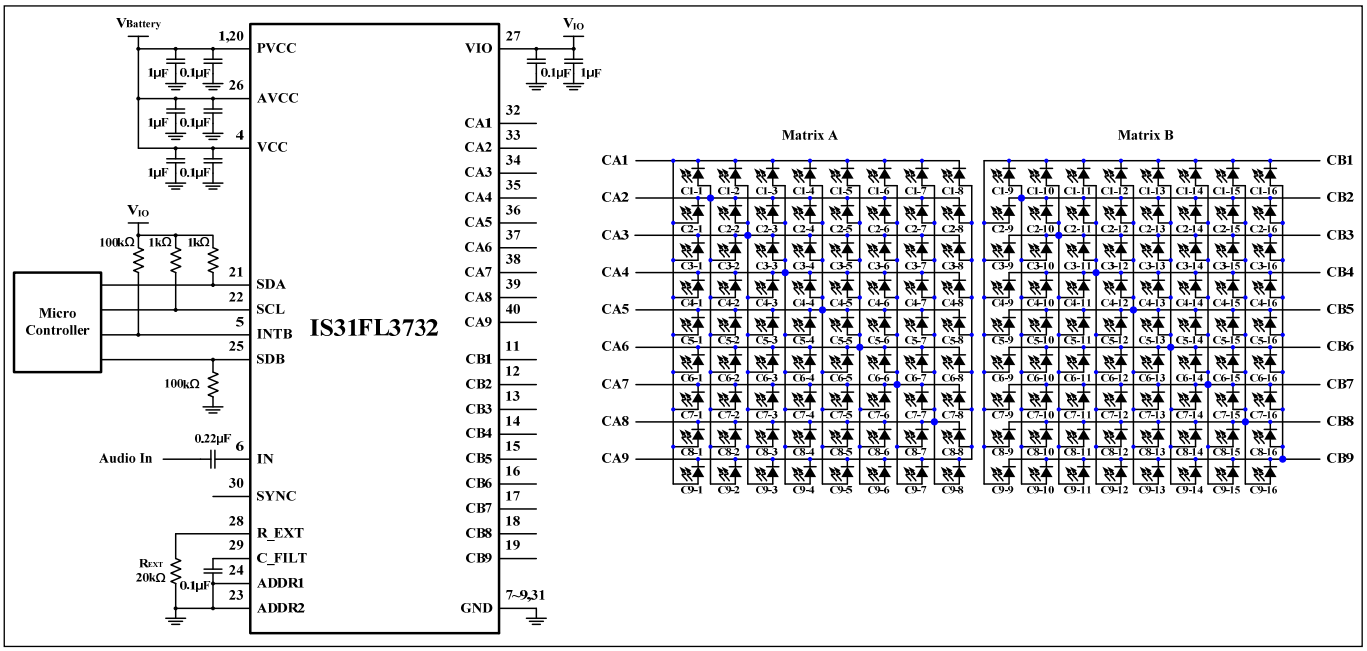


Figure 1 Typical Application Circuit

Note 1: For the mobile applications the IC should be placed far away from the mobile antenna in order to prevent the EMI.

Note 2: The average current of each LED is 3.2mA when R_{EXT} = 20kΩ. The LED current can be modulated by the R_{EXT}. Please refer to the detail information in Page 18.

Note 3: The thermal pad should be connected to GND.

Note 4: The V_{IO} should be 1.8V≤ V_{IO} ≤V_{CC}. And it is recommended to be equal to V_{OH} of the micro controller. For example, if V_{OH}=1.8V, set V_{IO}=1.8V is recommended.

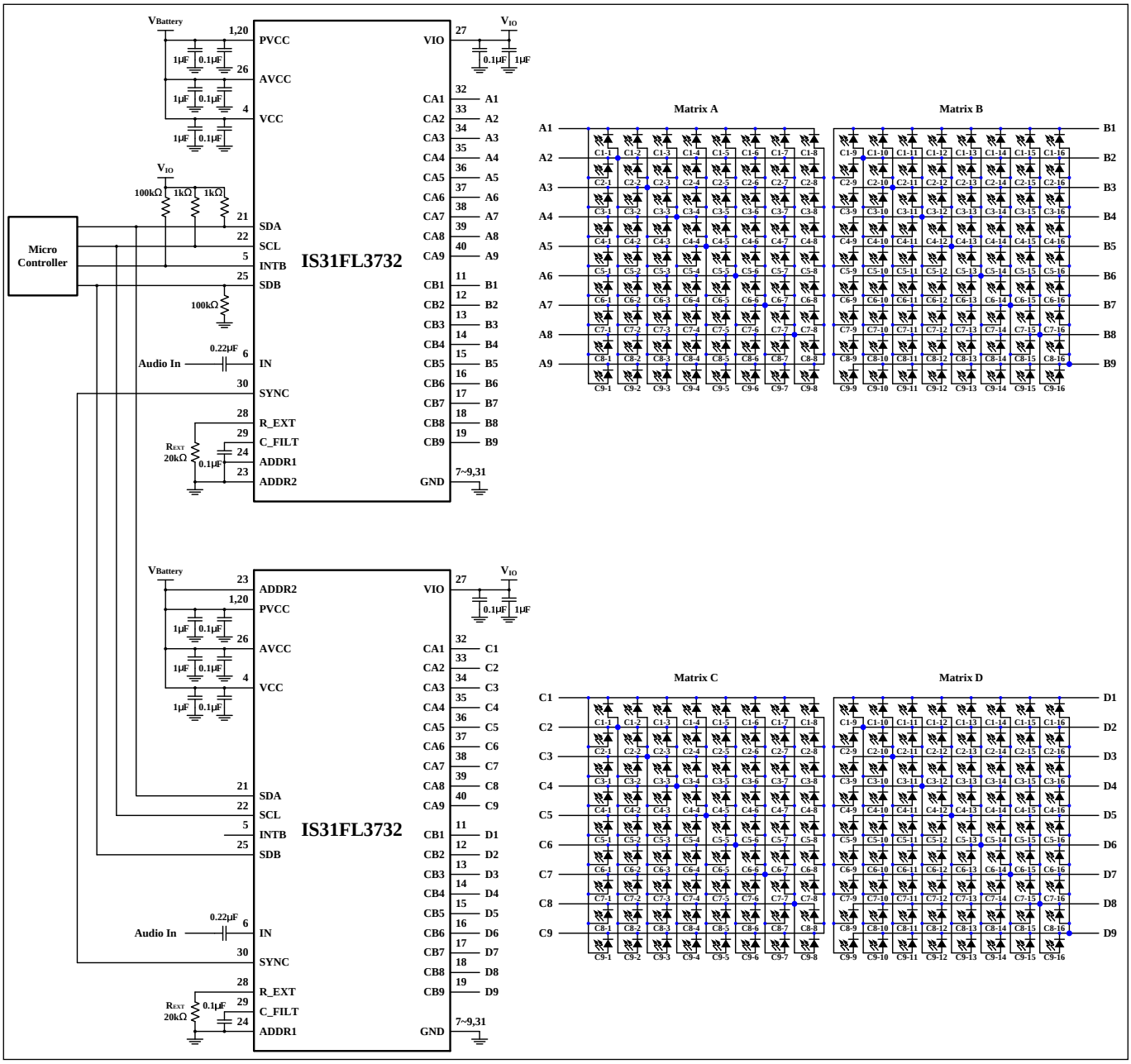


Figure 2 Typical Application Circuit (Two Parts Synchronization-Work)

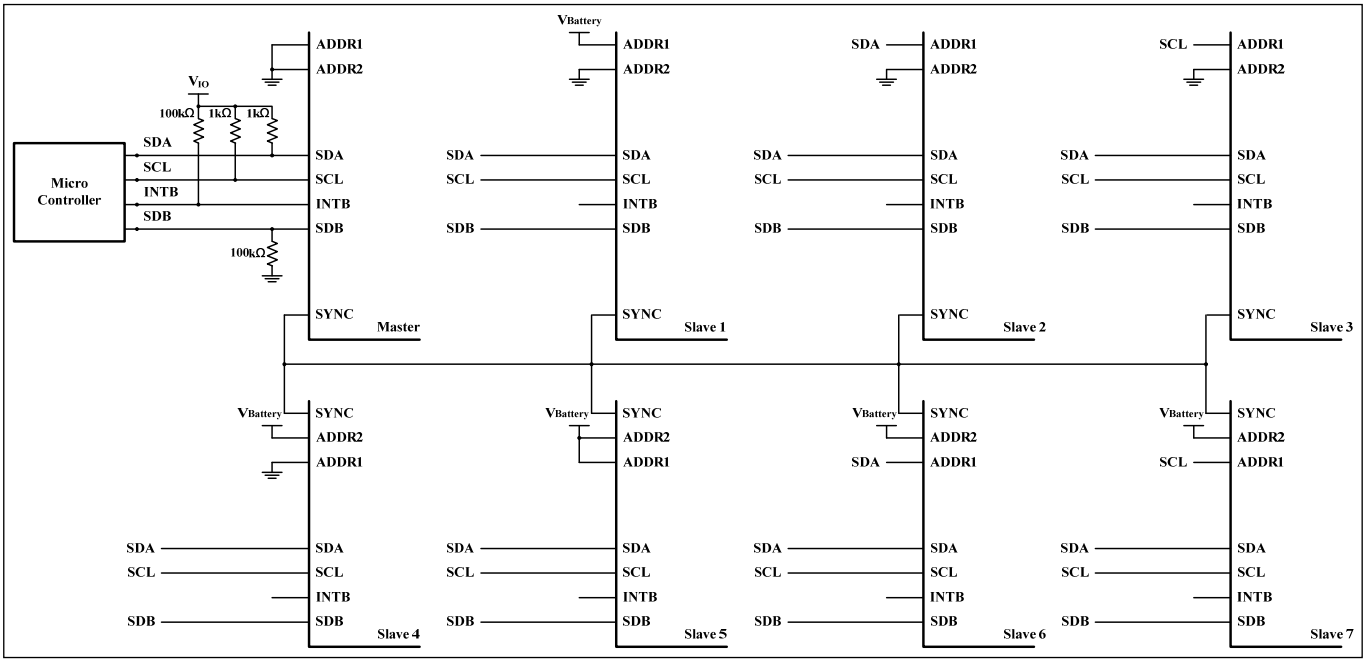
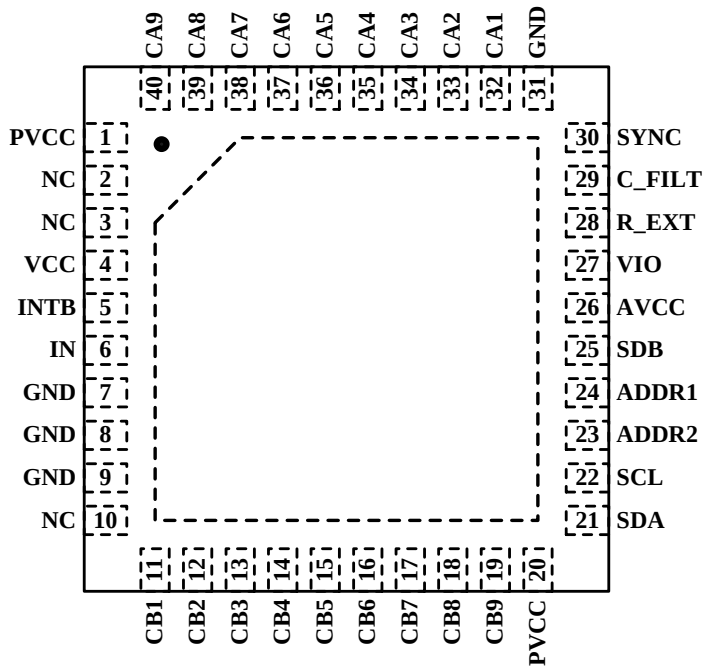


Figure 3 Typical Application Circuit (Eight Parts Synchronization-Work)

Note 5: One part is configured as master, all the other 7 parts configured as slave. Work as master or slave specified by Configuration Register (Function register, 00h), and the detail described in Page 14. Master part output master clock, and all the other parts which work as slave input this master clock. The master clock is used for all parts which are connected synchronize Breath /Blink/ Auto Frame Play Mode related timing spec.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-40	

PIN DESCRIPTION

No.	Pin	Description
1,20	PVCC	Power supply for internal power block.
2,3,10	NC	Not connect.
4	VCC	Digital power supply
5	INTB	Interrupt output. Active low when movie end in Auto Frame Play Mode. Detail information refers to Page 19.
6	IN	Audio input.
7~9,31	GND	Digital ground.
11~19	CB1 ~ CB9	LED Matrix B current output/input port.
21	SDA	I2C compatible serial data.
22	SCL	I2C compatible serial clock.
23	ADDR2	I2C address 2 setting.
24	ADDR1	I2C address 1 setting.
25	SDB	Shutdown the chip when pull to low.
26	AVCC	Analog power supply.
27	VIO	Input logic reference voltage.
28	R_EXT	Input terminal used to connect an external resistor. This regulates the global output current. Detail information refers to Page 18.
29	C_FILT	Filter capacitor for audio control.
30	SYNC	Synchronize signal. It is used for more than one part work synchronize. Detail information refers to Page 20. If it is not used please float this pin.
32~40	CA1 ~ CA9	LED Matrix A current output/input port.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31FL3732-QFLS2-TR	QFN-40, Lead-free	2500

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a.) the risk of injury or damage has been minimized;

b.) the user assume all such risks; and

c.) potential liability of Lumissil Microsystems is adequately protected under the circumstances

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, $T_A = T_J$	-40°C ~ +85°C
Thermal resistance, junction to ambient, θ_{JA}	24.96°C/W
ESD (HBM) ESD (CDM)	±8kV ±1kV

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC} = 3.6V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	Picture Mode, all LEDs off		2.17		mA
I_{SD}	Shutdown current	V_{SDB} = 0V		0.1	1	μA
		V_{SDB} = V_{CC}, Software Shutdown 1 Function Register 0Ah written "0000 0000".		230		
		V_{SDB} = V_{CC}, Software Shutdown 2 Function Register 0Ah written "0000 0010".		3		
I_{OUT}	Output DC current of CA1~CA9, CB1~CB9	Matrix display mode without audio modulation (Note 1)		34		mA
V_{HR}	Current sink headroom voltage C1~C9	I_{SINK} = 270mA (Note 1,2)		350		mV
	Current source headroom voltage C1~C9	I_{SOURCE} = 34mA (Note 1)		350		
t_{SCAN}	Period of scanning	(Figure 4)		100		μs
t_{SCANOL}	Non-overlap blanking time during scan	(Figure 4)		14		μs
I_{LED}	Average current of each LED	R_{EXT} = 20kΩ, PWM Register written "1111 1111" (Note 3)		3.2		mA
Logic Electrical Characteristics (SDA, SCL, ADDR1, ADDR2, SYNC, SDB)						
V_{IL}	Logic "0" input voltage	V_{IO}=3.6V	GND		0.2V_{IO}	V
V_{IH}	Logic "1" input voltage	V_{IO}=3.6V	0.75V_{IO}		V_{IO}	V
V_{OL}	Logic "0" output voltage for SYNC	I_{OL} = 8mA			0.4	V
V_{OH}	Logic "1" output voltage for SYNC	I_{OH} = 8mA	0.75V_{IO}			V
I_{IL}	Logic "0" input current	V_{INPUT} = 0V (Note 4)		5		nA
I_{IH}	Logic "1" input current	V_{INPUT} = V_{IO} (Note 4)		5		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 4)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-Clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	μs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	μs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	μs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	μs
$t_{HD, DAT}$	Data hold time	-		-	-		-	μs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	μs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	μs
t_R	Rise time of both SDA and SCL signals, receiving (Note 5)	-	$20+0.1C_b$	300	-	$20+0.1C_b$	120	ns
t_F	Fall time of both SDA and SCL signals, receiving (Note 5)	-	$20+0.1C_b$	300	-	$20+0.1C_b$	120	ns

Note 1: In case of R_{EXT} = 20kΩ, Global Current Control Register (Function Register, 04h) written "1111 1111".

Note 2: All LEDs are on.

Note 3: I_{LED} = 680/(10.5×R_{EXT}), R_{EXT} = 20kΩ is recommended. The recommended minimum value of R_{EXT} is 18kΩ.I_{LED}=I_{OUT}/10.5. Global Current Control Register (Function Register, 04h) written "1111 1111".

Note 4: Guaranteed by design.

Note 5: C_b = C_{I2C}+C_W, where C_W is the parasitic capacitance of SDA/SCL PCB wire and C_{I2C} (2pF, Typ.) is the capacitance of SDA or SCL pins. t_R and t_F measured between 0.3 × V_{IO} and 0.7 × V_{IO} and I_{SINK} ≤ 6mA.cv

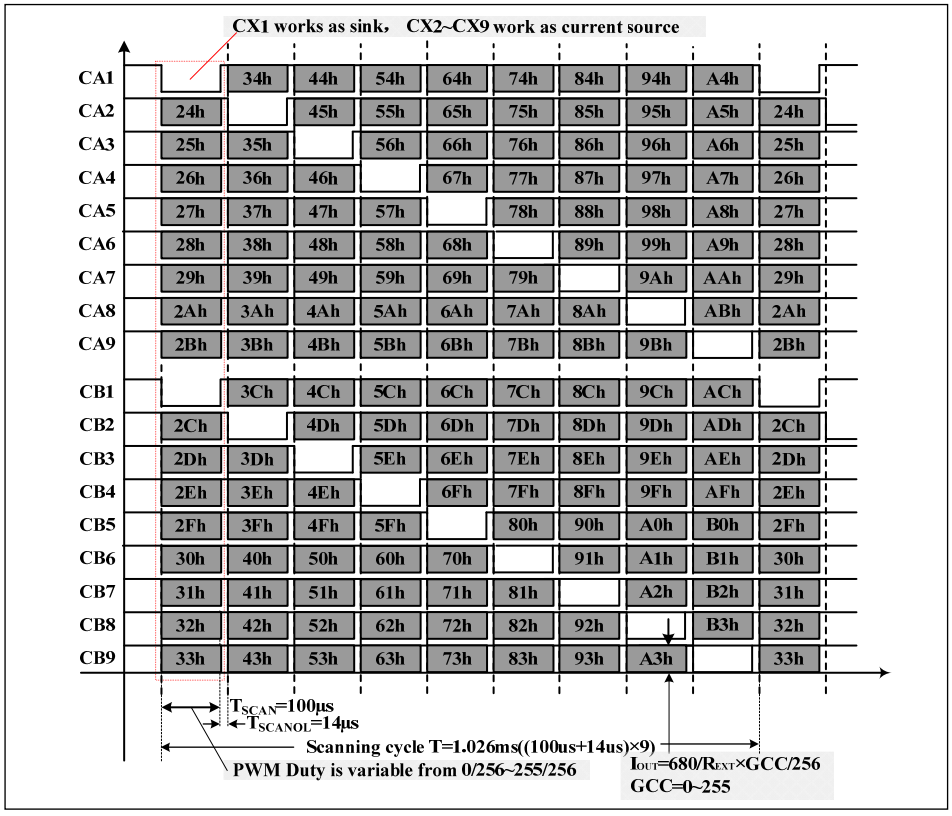


Figure 4 Scanning Timing

DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3732 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3732 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the ADDR1 pin. The value of bits A3 and A4 are decided by the connection of the ADDR2 pin.

The complete slave address is:

Table 1 Slave Address:

ADDR2	ADDR1	A7:A5	A4:A3	A2:A1	A0
GND	GND	101	00	00	0/1
GND	SCL		00	01	
GND	SDA		00	10	
GND	VCC		00	11	
SCL	GND		01	00	
SCL	SCL		01	01	
SCL	SDA		01	10	
SCL	VCC		01	11	
SDA	GND		10	00	
SDA	SCL		10	01	
SDA	SDA		10	10	
SDA	VCC		10	11	
VCC	GND		11	00	
VCC	SCL		11	01	
VCC	SDA		11	10	
VCC	VCC		11	11	

ADDR1/2 connected to GND, (A2:A1)/(A4:A3)=00;
ADDR1/2 connected to VCC, (A2:A1)/(A4:A3)=11;
ADDR1/2 connected to SCL, (A2:A1)/(A4:A3)=01;
ADDR1/2 connected to SDA, (A2:A1)/(A4:A3)=10;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 1kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3732.

The timing diagram for the I2C is shown in Figure 5. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3732's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3732 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3732, the register address byte is sent, most significant bit first. IS31FL3732 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3732 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3732, load the address of the data register that the first data byte is intended for. During the IS31FL3732 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3732 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3732 (Figure 8).

READING OPERATION

All of registers in IS31FL3732 can be read. But Frame Register can only be read in Software Shutdown 1 as SDB pin is high. The Function Register can be read in all modes.

To read the device data, the bus master must first send the IS31FL3732 address with the R/$\overline{W}$ bit set to "0", followed by the Command Register (FDh) then send command data which determines which response register is accessed. After a restart, the bus master must send the IS31FL3732 address with the R/$\overline{W}$ bit set to "0" again, followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3732 address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3732 to the master (Figure 9).

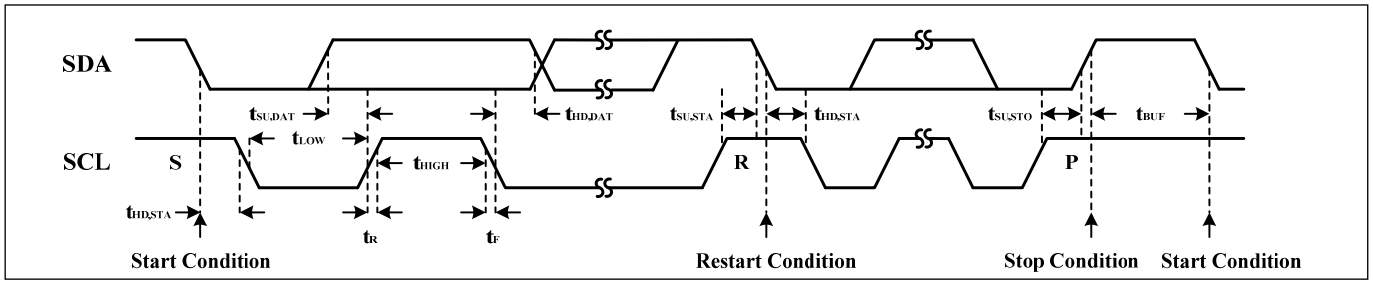


Figure 5 Interface timing

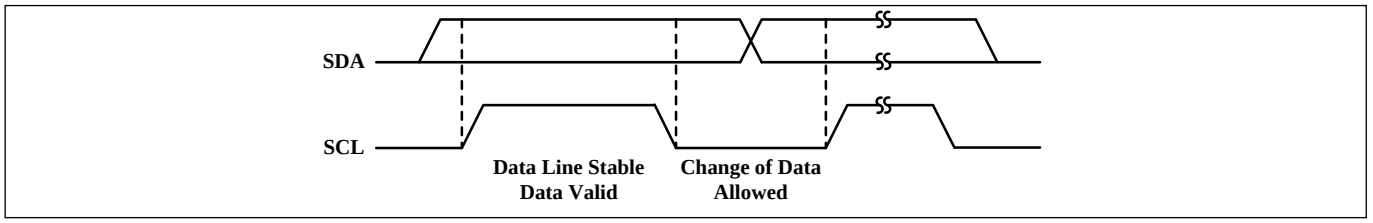


Figure 6 Bit transfer

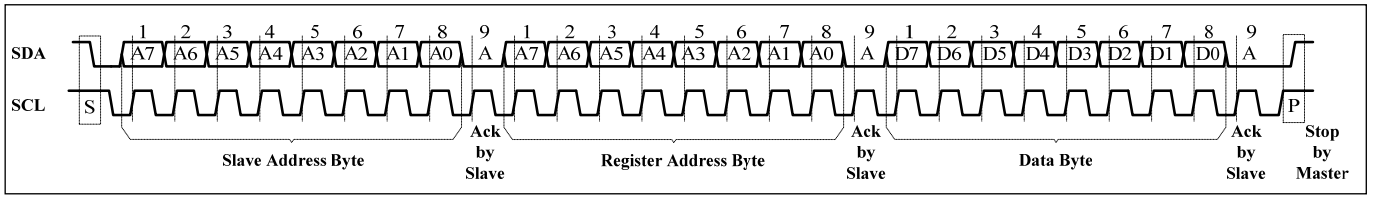


Figure 7 Writing to IS31FL3732 (Typical)

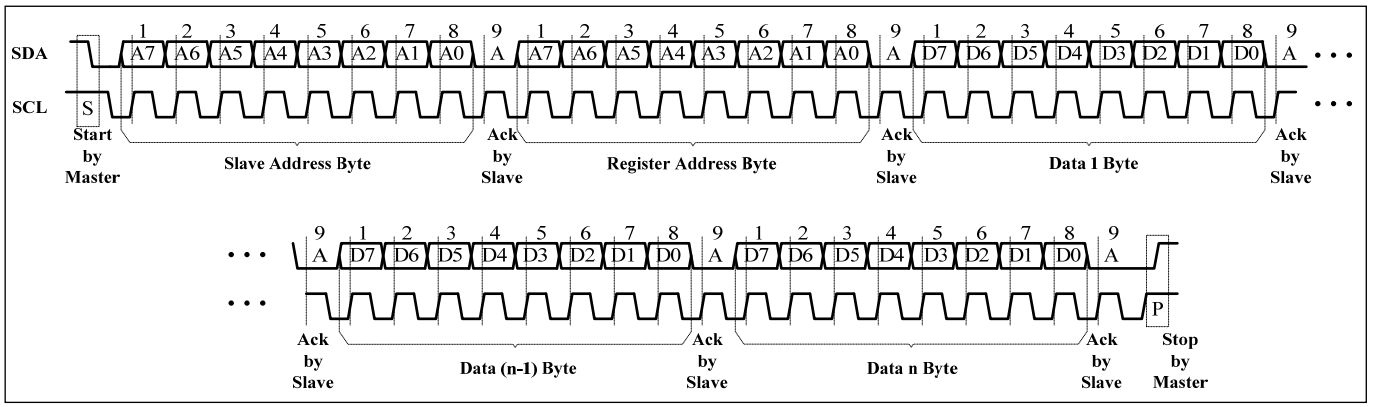


Figure 8 Writing to IS31FL3732 (Automatic address increment)

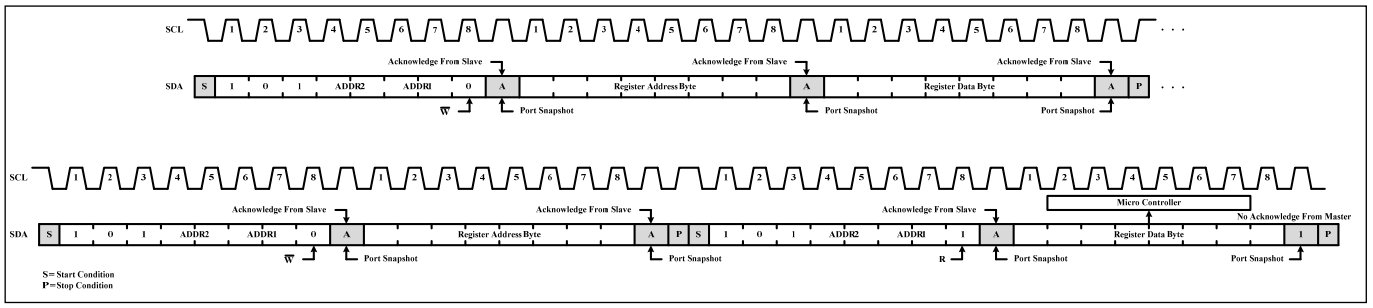


Figure 9 Reading from IS31FL3732

REGISTER DEFINITION

Table 2 FDh Command Register (Write Only)

Data	Function	Data	Function
0000 0000	Point to Page One (Frame 1 Register is available)	0000 0001	Point to Page Two (Frame 2 Register is available)
0000 0010	Point to Page Three (Frame 3 Register is available)	0000 0011	Point to Page Four (Frame 4 Register is available)
0000 0100	Point to Page Five (Frame 5 Register is available)	0000 0101	Point to Page Six (Frame 6 Register is available)
0000 0110	Point to Page Seven (Frame 7 Register is available)	0000 0111	Point to Page Eight (Frame 8 Register is available)
0000 1011	Point to Page Nine (Function Register is available)	Others	Reserved

Note: The Command Register should be configured first after writing in the slave address to choose the available register (Frame Register and Function Register). Then write data in the choosing register. Power up default state is "0000 0000".

For example, when write "0000 0011" in the Command Register (FDh), the data which writing after will be stored in the Frame 4 Register. Write new data can configure other registers.

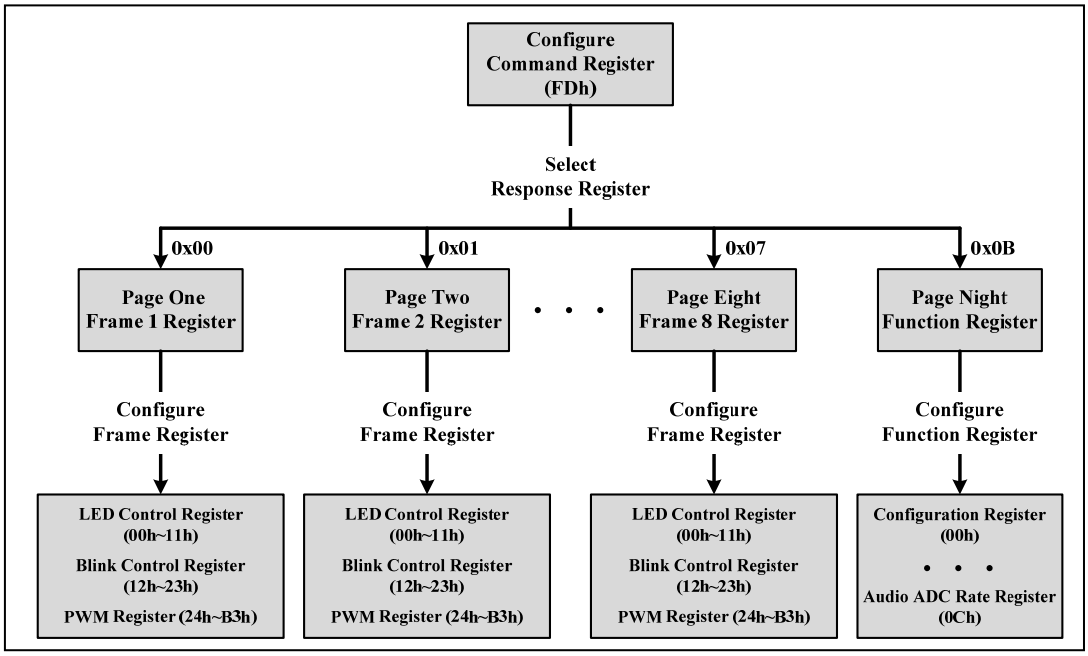
Table 3 Response Register Function
(The address of each Page is starting from 00h. Frame Registers have the same format.)

Address	Name	Function	Table	R/W	Default
Frame Register (Page One to Page Eight) (Note 6)					
00h ~ 11h	LED Control Register	Store on or off state for each LED	4	R/W	xxxx xxxx
12h ~ 23h	Blink Control Register	Control the blink function for each LED	5	R/W	
24h ~ B3h	PWM Register	144 LEDs PWM duty cycle data register	6	R/W	
Function Register (Page Night) (Note 7)					
00h	Configuration Register	Configure the operation mode	8	R/W	0000 0000
01h	Picture Display Register	Set the display frame in Picture Mode	9	R/W	
02h	Auto Play Control Register 1	Set the way of display in Auto Frame Play Mode	10	R/W	
03h	Auto Play Control Register 2	Set the delay time in Auto Frame Play Mode	11	R/W	
04h	Global Current Control	Set the global current for all LEDs	12	R/W	
05h	Display Option Register	Set the display option	13	R/W	
06h	Audio Synchronization Register	Set audio synchronization function	14	R/W	
07h	Frame State Register	Store the frame display information	15	R	
08h	Breath Control Register 1	Set fade in and fade out time for breath function	16	R/W	
09h	Breath Control Register 2	Set the breath function	17	R/W	
0Ah	Shutdown Register	Set software shutdown mode	18	R/W	
0Bh	AGC Control Register	Set the AGC function and the audio gain.	19	R/W	
0Ch	Audio ADC Rate Register	Set the ADC sample rate of the input signal	20	R/W	

Note 6: The data of Frame Registers are random after power up. Please initialize the Frame Registers first to ensure operate normally. Frame Register writing operation must be in case of SDB pin high and Function Register (0Ah) written "0000 0000" (Software Shutdown 1) or "0000 0001" (Normal operation). Read operation asks for SDB pin high and Function Register (0Ah) written "0000 0000" (Software Shutdown 1). Due to max address of Frame Registers is B3h, value '110' and '111' are prohibited for Frame Register address 3 MSB.

Note 7: Function registers can be written and read after power up. All function registers power up default state are '0000 0000', once V_{CC} drop to 1.75V (typical) all function registers are reset to their default state in case of SDB pin pulled high.

REGISTER CONTROL



For example, if write "0000 0001" into Command Register (FDh), it means choosing Page Two Frame 2 Register to configure. Then next address and data will take effect only for Frame 2 Register unless re-configure Command Register (FDh).

FRAME REGISTER

Table 4 00h ~ 11h LED Control Register

Bit	D7:D0
Name	C_{X-8} : C_{X-1} or C_{X-16} : C_{X-9}
Default	xxxx xxxx

The LED Control Registers store the on or off state of each LED in the Matrix A and B. Please refer to the detail information in Table 7.

C_{X-Y}	LED State Bit
0	LED off
1	LED on

Figure 10 in Page 13 shows the ordering of C_{X-Y}.

Table 5 12h ~ 23h Blink Control Register

Bit	D7:D0
Name	C_{X-8} : C_{X-1} or C_{X-16} : C_{X-9}
Default	xxxx xxxx

The Blink Control Registers configure the blink function of each LED in the Matrix A and B. Please refer to the detail information in Table 7.

C_{X-Y}	Blink Control Bit
0	Disable
1	Enable

Figure 10 in Page 13 shows the ordering of C_{X-Y}.

Table 6 24h ~ B3h PWM Register

Bit	D7:D0
Name	PWM
Default	xxxx xxxx

PWM Registers modulate the 144 LEDs average current in 256 steps.

The value of the PWM Registers decides the output average current of each LED noted I_{LED}.

I_{LED} computed by Formula (1):

$$I_{LED} = \frac{PWM}{256} \times I_{OUT} \times \frac{1}{10.5} \qquad (1)$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0 = 10110101,

$$I_{LED} = \frac{2^0 + 2^2 + 2^4 + 2^5 + 2^7}{256} \times I_{OUT} \times \frac{1}{10.5}$$

I_{OUT} is output DC current which can be set by the GCC bit of Global Current Control Register (04h) and R_{EXT}. Detail information refers to Table 12 in Page 15.

Table 7 Address of Frame Register

LED Location		LED Control Register		Blink Control Register		PWM Register	
Matrix A	Matrix B	**Matrix A**	Matrix B	**Matrix A**	Matrix B	**Matrix A**	Matrix B
CA1(C_{1-1}~C_{1-8})	CB1(C_{1-9}~C_{1-16})	**00h**	01h	**12h**	13h	**24h ~ 2Bh**	2Ch ~ 33h
CA2(C_{2-1}~C_{2-8})	CB2(C_{2-9}~C_{2-16})	**02h**	03h	**14h**	15h	**34h ~ 3Bh**	3Ch ~ 43h
CA3(C_{3-1}~C_{3-8})	CB3(C_{3-9}~C_{3-16})	**04h**	05h	**16h**	17h	**44h ~ 4Bh**	4Ch ~ 53h
CA4(C_{4-1}~C_{4-8})	CB4(C_{4-9}~C_{4-16})	**06h**	07h	**18h**	19h	**54h ~ 5Bh**	5Ch ~ 63h
CA5(C_{5-1}~C_{5-8})	CB5(C_{5-9}~C_{5-16})	**08h**	09h	**1Ah**	1Bh	**64h ~ 6Bh**	6Ch ~ 73h
CA6(C_{6-1}~C_{6-8})	CB6(C_{6-9}~C_{6-16})	**0Ah**	0Bh	**1Ch**	1Dh	**74h ~ 7Bh**	7Ch ~ 83h
CA7(C_{7-1}~C_{7-8})	CB7(C_{7-9}~C_{7-16})	**0Ch**	0Dh	**1Eh**	1Fh	**84h ~ 8Bh**	8Ch ~ 93h
CA8(C_{8-1}~C_{8-8})	CB8(C_{8-9}~C_{8-16})	**0Eh**	0Fh	**20h**	21h	**94h ~ 9Bh**	9Ch ~ A3h
CA9(C_{9-1}~C_{9-8})	CB9(C_{9-9}~C_{9-16})	**10h**	11h	**22h**	23h	**A4h ~ ABh**	ACh ~ B3h

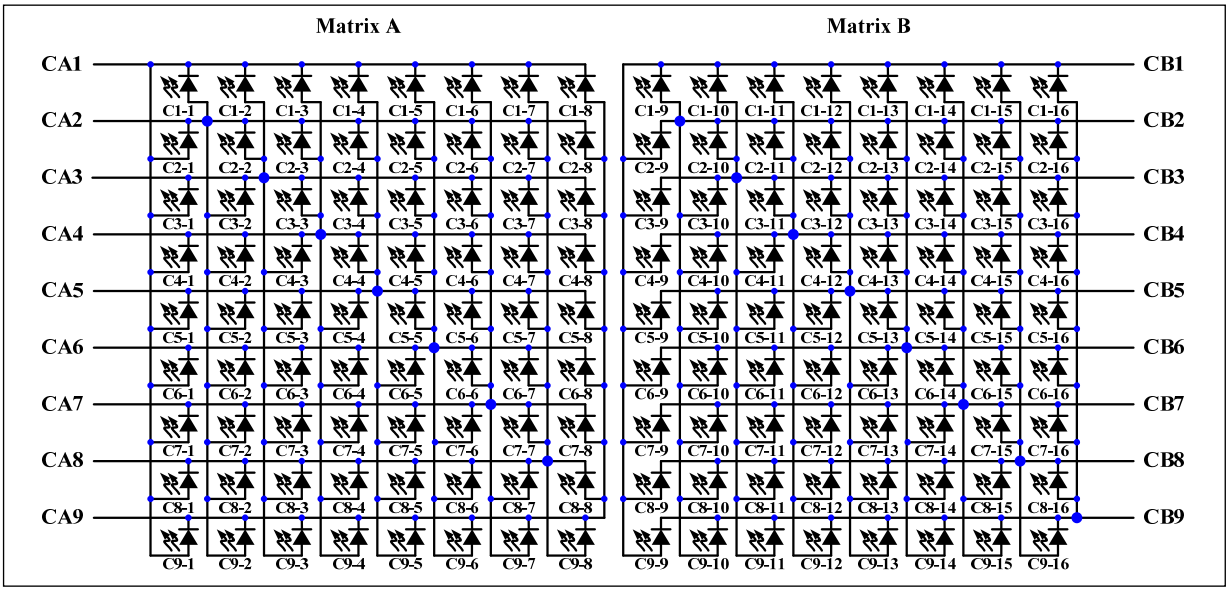


Figure 10 LED Array

FUNCTION REGISTER

Table 8 00h Configuration Register

Bit	D7:D6	D5	D4:D3	D2:D0
Name	SYNC	-	MODE	FS
Default	00	0	00	000

The Configuration Register sets operating mode of IS31FL3732.

SYNC Synchronize Configuration
00/11 High Impedance
01 Master
10 Slave

MODE Display Mode
00 Picture Mode
01 Auto Frame Play Mode
1x Audio Frame Play Mode

FS Frame Start
(Available in Auto Frame Play Mode)
000 Frame 1
001 Frame 2
010 Frame 3
011 Frame 4
100 Frame 5
101 Frame 6
110 Frame 7
111 Frame 8

FS bit sets the start frame in Auto Frame Play Mode. Movie starts from Frame 4 when the FS bit is set to "011". The FS bit is only available in Auto Frame Play Mode.

Table 9 01h Picture Display Register

Bit	D7:D3	D2:D0
Name	-	PFS
Default	00000	000

The Picture Display Register sets display frame in Picture Mode.

PFS Picture Frame Selection
(Available in Picture Mode)
000 Frame 1
001 Frame 2
010 Frame 3
011 Frame 4
100 Frame 5
101 Frame 6
110 Frame 7
111 Frame 8

Table 10 02h Auto Play Control Register 1

Bit	D7	D6:D4	D3	D2:D0
Name	-	CNS	-	FNS
Default	0	000	0	000

The Auto Play Control Register 1 sets the way of display in Auto Frame Play Mode.

CNS Number of Loops Playing Selection
(Available in Auto Frame Play Mode)
000 Play endless
001 1 loop
010 2 loops
011 3 loops
100 4 loops
101 5 loops
110 6 loops
111 7 loops

FNS Number of Frames Playing Selection
(Available in Auto Frame Play Mode)
000 All Frame
001 1 frame
010 2 frames
011 3 frames
100 4 frames
101 5 frames
110 6 frames
111 7 frames

Movie will be stop in the next frame of the cycle. For example, FS bit is set to "011", CNS bit is set to "011" and FNS bit is set to "011". Then the movie will play from Frame 4 to Frame 6 and play three times it stops in Frame 7.

Table 11 03h Auto Play Control Register 2

Bit	D7:D6	D5:D0
Name	-	A
Default	00	000000

The Auto Play Control Register 2 sets the delay time in Auto Frame Play Mode (Figure 14).

FDT Frame Delay Time

(Available in Auto Frame Play Mode)

If A = 0, FDT = τ×64;

If A = 1~63, FDT = τ×A;

A = 0~63 and τ = 11ms (Typ.);

For example, when A = 23, FDT is 11ms×23 = 253ms

Table 12 04h Global Current Control Register

Bit	D7:D0
Name	GCC
Default	0000 0000

The Global Current Control Register modulates all LEDs DC current which is noted as I_{OUT} in 256 steps.

I_{OUT} is computed by the Formula (2):

$$I_{OUT} = \frac{GCC}{256} \times \frac{680}{R_{EXT}} \quad (2)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0 = 10110101,

$$I_{OUT} = \frac{2^0 + 2^2 + 2^4 + 2^5 + 2^7}{256} \times \frac{680}{R_{EXT}}$$

R_{EXT} is the external resistor to set DC current, detail information please refers to Page 18.

Table 13 05h Display Option Register

Bit	D7:D6	D5	D4	D3	D2:D0
Name	-	IC	-	BE	A
Default	00	0	0	0	000

The Display Option Register sets display option of IS31FL3732.

IC Intensity Control

0 Set the intensity of each frame independently

1 Use intensity setting of frame 1 for all other frames

BE Blink Enable

0 Disable

1 Enable

BPT Blink Period Time

BPT = τ×A;

A = 0~7, τ = 0.27s (Typ.);

For example, when A = 5, BPT is 0.27s×5 = 1.35s.

The duty cycle for blink function is 50%.

Table 14 06h Audio Synchronization Register

Bit	D7:D1	D0
Name	-	AE
Default	0000000	0

The Audio Synchronization Register sets audio synchronization function.

AE Audio Synchronization Enable

0 Audio synchronization disable

1 Enable audio signal to modulate the intensity of the matrix

The intensity of matrix can be modulated by the audio input signal basing on each LED's current is set by PWM when the AE bit is set to "1".

Table 15 07h Frame State Register (Read Only)

Bit	D7:D5	D4	D3	D2:D0
Name	-	INT	-	CFD
Default	-			

The Frame State Register stores the frame display information.

INT Interrupt Bit

(Available in Auto Frame Play Mode)

0 Movie has not finished

1 Movie has finished

CFD Current Frame Display

000 Frame 1

001 Frame 2

010 Frame 3

011 Frame 4

100 Frame 5

101 Frame 6

110 Frame 7

111 Frame 8

The INT bit will be set to "1" automatically when movie is end in Auto Frame Play Mode. The INT bit can be cleared up by reading the Frame State Register.

Table 16 08h Breath Control Register 1

Bit	D7	D6:D4	D3	D2:D0
Name	-	A	-	B
Default	0	000	0	000

The Breath Control Register 1 sets fade in and fade out time for breath function.

FOT Fade Out Time
FOT = $\tau \times 2^A$
A = 0~7, τ = 26ms (Typ.)
For example, when A = 4, FOT is $26ms \times 2^4 = 416ms$

FIT Fade In Time
FIT = $\tau \times 2^B$
B = 0~7, τ = 26ms (Typ.)
For example, when A = 4, FIT is $26ms \times 2^4 = 416ms$

Table 17 09h Breath Control Register 2

Bit	D7:D5	D4	D3	D2:D0
Name	-	B_EN	-	A
Default	000	0	0	000

The Breath Control Register 2 sets the breath function.

B_EN Breath Enable
(Available in Picture Mode and Auto Frame Play Mode)
0 Disable
1 Enable

ET Extinguish Time
ET = $\tau \times 2^A$
A = 0~7, τ = 3.5ms (Typ.)
For example, when A = 4, ET is $3.5ms \times 2^4 = 56ms$

Table 18 0Ah Shutdown Register

Bit	D7:D2	D1:D0
Name	-	SSD
Default	000000	00

The Shutdown Register sets software shutdown.

SSD Software Shutdown Control
00 Software Shutdown 1
01 Normal Operation
1x Software Shutdown 2

Frame Register and Function Register all can be written and read during Software Shutdown 1.
Frame Register cannot be written during Software Shutdown 2.

Table 19 0Bh AGC Control Register

Bit	D7:D5	D4	D3	D2:D0
Name	-	AGCM	AGC	AGS
Default	000	0	0	000

The AGC Control Register sets the AGC function and the audio gain.

AGCM AGC Mode
0 Slow Mode
1 Fast Mode

AGC AGC Enable
0 Disable
1 Enable

AGS Audio Gain Selection
000 0dB
001 3dB
010 6dB
011 9dB
100 12dB
101 15dB
110 18dB
111 21dB

The AGS bit is available in Audio Frame Play Mode and audio synchronization mode.

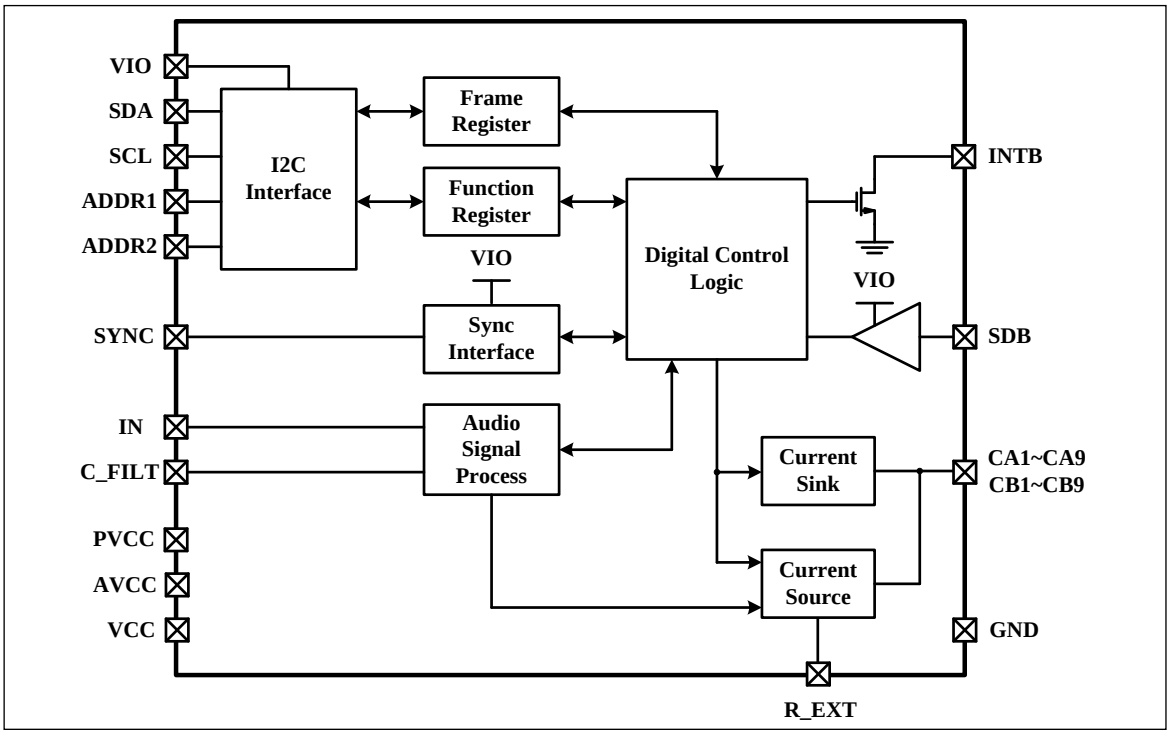
Table 20 0Ch Audio ADC Rate Register

Bit	D7:D0
Name	A
Default	0000 0000

The Audio ADC Rate Register sets the ADC sample rate of the input signal in Audio Frame Play Mode.

AAR Audio ADC Rate
(Available in Audio Frame Play Mode)
If A = 0, AAR = τ×256
If A = 1~255, AAR = τ×A
τ = 46μs (Typ.)
For example, when A = 14, AAR is 46μs×14 = 644μs

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION (The description below is for the Function Register unless otherwise noted.)

PWM CONTROL

The brightness of 144 LEDs can be modulated with 256 steps by PWM Register. For example, if the data in PWM Register is “0000 0100”, then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

EXTERNAL RESISTOR (R_{EXT})

The average output current of each LED can be adjusted by the external resistor, R_{EXT}, as described in Formula (3).

$$I_{LED} = \frac{PWM}{256} \times \frac{GCC}{256} \times \frac{680}{R_{EXT}} \times \frac{1}{10.5} \qquad (3)$$

Where PWM is PWM Register (Frame Register, 04h~B3h) data showing in Page 12 Table 6, and GCC is Global Current Control Register (Function Register, 04h) data showing in Page 15 Table 12.

For example, in Figure 1, R_{EXT} = 20kΩ,

And PWM=255, GCC=255.

So $I_{LED} = \frac{255}{256} \times \frac{255}{256} \times \frac{1}{10.5} \times \frac{680}{20k} = 3.21mA$

The recommended minimum value of R_{EXT} is 18kΩ.

LED CURRENT (I_{LED})

The LED average current can be set by 3 factors:

1. R_{EXT}, resistant which is connected R_EXT pin and GND. R_{EXT} set all LED DC current value.

2. Global Current Control Register (Function Register, 04h). This register control global current, set all LED DC current by 256 steps. Details refer to Page 15.

3. PWM Registers (Frame Register, 04h~B3h), every LED has an own PWM register. PWM Registers set individual LED current by 256 steps. Details refer to Page 12.

$$I_{LED} = \frac{PWM}{256} \times \frac{GCC}{256} \times \frac{680}{R_{EXT}} \times \frac{1}{10.5} \qquad (3)$$

GAMMA CORRECTION

In order to perform a better visual LED breathing effect we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3732 can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

Table 21 32 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	4	6	10	13	18
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
22	28	33	39	46	53	61	69
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
78	86	96	106	116	126	138	149
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
161	173	186	199	212	226	240	255

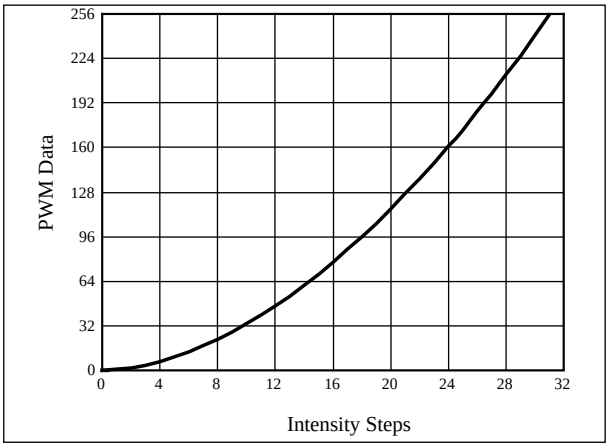


Figure 11 Gamma Correction (32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps, when T=2s, choose 64 gamma steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 22 64 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	3	4	5	6	7
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
8	10	12	14	16	18	20	22
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
24	26	29	32	35	38	41	44
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
47	50	53	57	61	65	69	73
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
77	81	85	89	94	99	104	109
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
114	119	124	129	134	140	146	152
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
158	164	170	176	182	188	195	202
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	C(63)
209	216	223	230	237	244	251	255

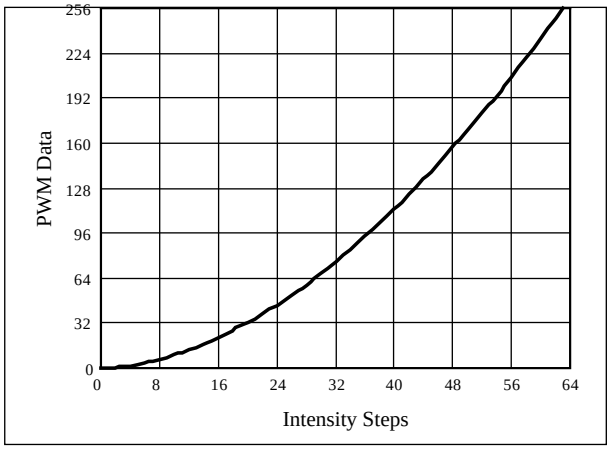


Figure 12 Gamma Correction (64 Steps)

Note: The data of 32 gamma steps is the standard value and the data of 64 gamma steps is the recommended value.

OPERATING MODE

IS31FL3732 has three operating modes, Picture Mode, Auto Frame Play Mode and Audio Frame Play Mode.

Picture Mode

By setting the MODE bit of the Configuration Register (00h) to "00", the IS31FL3732 operates in Picture Mode. Set the PFS bit of Picture Display Register (01h) to choose the display frame. The Picture Mode can be operating with breath function by configuring Breath Control Register 2 (09h).

Auto Frame Play Mode

By setting the MODE bit of the Configuration Register (00h) to "01", the IS31FL3732 operates in Auto Frame Play Mode. It stores data of 8 frames and automatically plays in order. Customers can configure the delay time between each two frames and the first playing frame by setting the FS bit of Configuration Register (00h). The Auto Play Control Register 1 (02h) can configure the display cycle and display frames.

Configure the Auto Play Control Register 2 (03h), Breath Control Register 1 (08h) and Breath Control Register 2 (09h) can set the breath time between two frames switching.

Audio Frame Play Mode

By setting the MODE bit of the Configuration Register (00h) to "1x", the IS31FL3732 operates in Audio Frame Play Mode. It stores data of 8 frames and the 8 frames playing follow the input signal. 0Ch register is used to set the ADC sample rate for the input signal to control frames playing. It plays the first frame when the value is the smallest and plays the eighth frame when the value is the biggest.

AUDIO MODULATED AND GAIN SETTING

By setting the AE bit of the Audio Synchronization Register (06h) to "1", IS31FL3732 operates with audio synchronization. The intensity of LEDs is adjusted by the input signal. The audio input gain can be set by the AGC Control Register (0Bh).

BLINK FUNCTION SETTING

By setting the BE bit of the Display Option Register (05h) to "1", blink function enable. If the BE bit is set to "1", each LED can be controlled by the Blink Control Registers (12h~23h in Page One to Page Eight). The Display Option Register (05h) is used to set the blink period time, BPT, and the duty cycle is 50% (Figure 13).

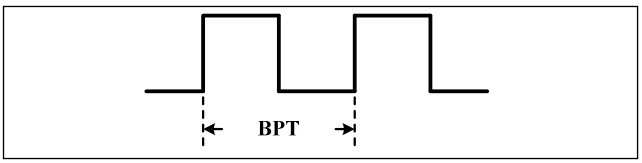


Figure 13 Blink Function

BREATHING FUNCTION SETTING

When IS31FL3732 switches playing frame, breath function is available. By setting the B_EN bit of the Breath Control Register 2 (09h) to "1", breath function enable. When set the B_EN bit to "0", breath function disables.

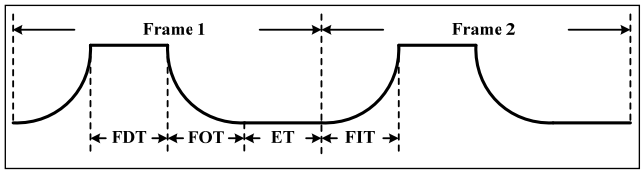


Figure 14 Breathing Function

INTERRUPT CONTROL

When IS31FL3732 is playing frame in the Auto Frame Play Mode, the INTB pin is high and the INT bit of Frame State Register (07h) is "0". It will be pulled low as movie end and the INT bit will be set to "1" at the same time.

The INTB pin will be pulled high after reading Frame State Register (07h) operation or it will be pulled high automatically after it stays low for 9ms (Typ.). The INT bit will be reset to “0” only after reading Frame State Register (07h) operation.

SYNCHRONIZE FUNCTION

SYNC bit of the Configuration Register (00h) sets SYNC pin input or output synchronize clock signal. It is used for more than one part working synchronize. When SYNC bit is set to “01”, SYNC pin output synchronize clock to synchronize other parts as master. When SYNC bit is set to “10”, SYNC pin input synchronize clock and work synchronization with this input signal as slave. When SYNC bit is set to “00/11”,SYNC pin is high impedance. Synchronize function is disabled. SYNC bit default state is “00” and SYNC pin is high impedance when power up.

LED MATRIX CIRCUIT

The IS31FL3732 can drive 144 LEDs totally. Part of LEDs can if there is no need to use all 144 LEDs (Figure 15). But the LEDs which are no connected must be off by LED Control Register (Frame Register) or it will affect other LEDs.

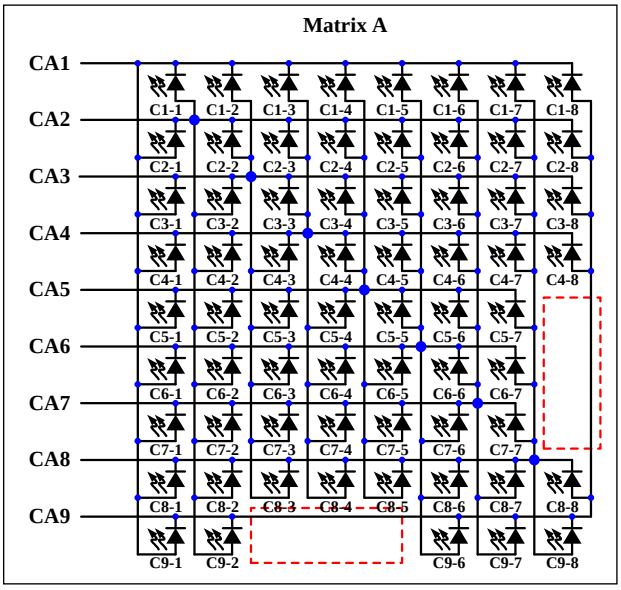


Figure 15 No C9-3~C9-5, C5-8~C9-8

DRIVE RGBS MATRIX

The IS31FL3732 can drive 32 common cathode / common anode RGBs at best (Figure 16 and 17). The location of red LED must follow the below circuit and the black location could connect single LED except red one, or the IC can’t work normally. Note, the LEDs which are no connected must be off by LED Control Register (Frame Register) or it will affect other LEDs.

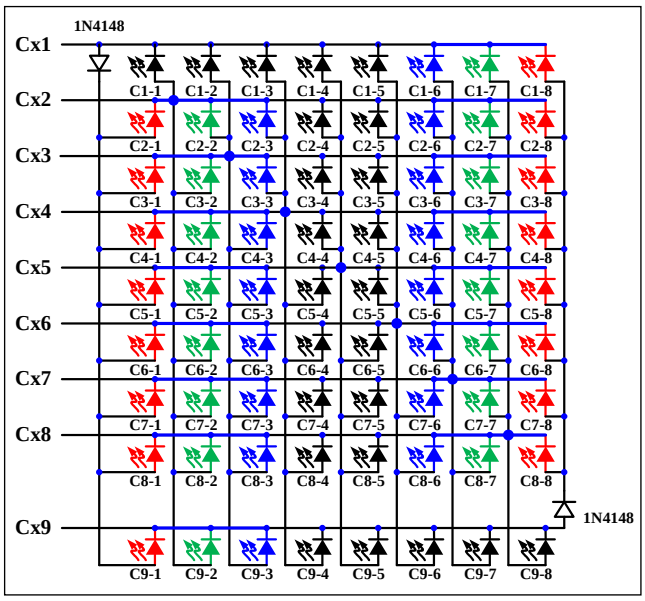


Figure 16 Common Cathode RGBs Connection

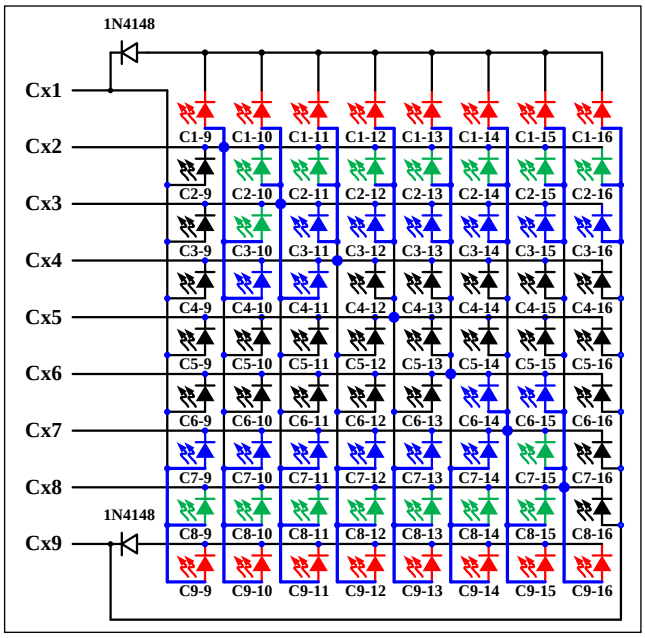


Figure 17 Common Anode RGBs Connection

MORE FRAMES DISPLAY

The IS31FL3732 can store 8 frames data at best. Each 4 frames writing in Frame Registers is recommended if there are more frames to play (Figure 18). First, store 8 frames data and play 4 frames in front. Then play last 4 frames and writing new data in the Frame Registers (1~4) at the same time. Play the new 4 frames (1~4) and write new data in the Frame Registers (5~8).

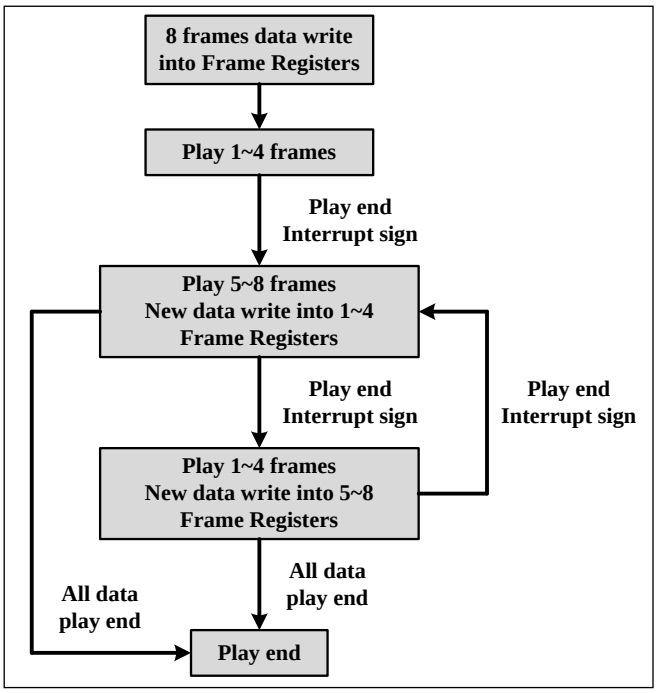


Figure 18 More Frame Data Writing In

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Shutdown Register (0Ah) to "00", the IS31FL3732 will operate in Software Shutdown 1. When the IS31FL3732 is in Software Shutdown 1, all current sources are switched off, so that the matrix is blanked. All registers (include Function Register and Frame Register) can be written or read when the SDB pin is pulled high. Typical current consume is 230μA.

By setting SSD bit to "10" or "11", the IS31FL3732 will operate in Software Shutdown 2. When the IS31FL3732 is in Software Shutdown 2, all current sources are turned off, the matrix is blanked. Function Register can be written or read. Frame Register can not be written or read. Typical current consume is 3μA.

Registers Reset

When SDB pin is pulled low, all registers won't be reset. During SDB pin pulled high, Function Registers are reset to "0000 0000" once V_{CC} drop below 1.75V (Typ.). SDB pin hold in low voltage state (Hardware Shutdown), all analog circuits are shutdown. The Function Register still can be reset in case of Hardware Shutdown when V_{CC} drops below 0.1V.

Frame Register constructed by SRAM. Frame Registers are random state after power up, and only can be changed by I2C writing operation.

Hardware Shutdown

The chip enters Hardware Shutdown when the SDB pin is pulled low. All analog circuits are disabled during Hardware Shutdown, typical current consume is 0.1μA.

The chip enters Hardware Enable when the SDB pin is pulled high. During Hardware Shutdown state Function Register can be written and read, but Frame Register cannot be written and read.

If V_{CC} has risk drop below 1.75V but above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

POWER DISSIPATION

The power dissipation of the IS31FL3732 can calculate as below:

$$P_{3732}=I_{PVCC}\times PV_{CC}+ I_{CC}\times V_{CC}(AV_{CC})-I_{PVCC}\times V_{F(AVR)} \quad (4)$$

$$\approx I_{PVCC}\times PV_{CC} - I_{PVCC}\times V_{F(AVR)}$$

$$= I_{PVCC}\times (PV_{CC} - V_{F(AVR)})$$

Where IPV_{CC} is the current of PV_{CC} and $V_{F(AVR)}$ is the average forward of all the LED.

For example, if R_{EXT}=20kΩ, GCC=255, PWM=255, PV_{CC}=5V, $V_{F(AVR)}$=3.4V@34mA, then the IPV_{CC}=(34mA×8×9/10.5)x2=466.29mA.

P3732=466.29mA×(5V-3.4V)=0.746W

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Formula (5):

$$P_{D(MAX)} = \frac{125°C - 25°C}{R_{\theta JA}} \quad (5)$$

So,

$$P_{D(MAX)} = \frac{125°C - 25°C}{24.96°C/W} \approx 4W$$

Figure 19, shows the power derating of the IS31FL3732 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

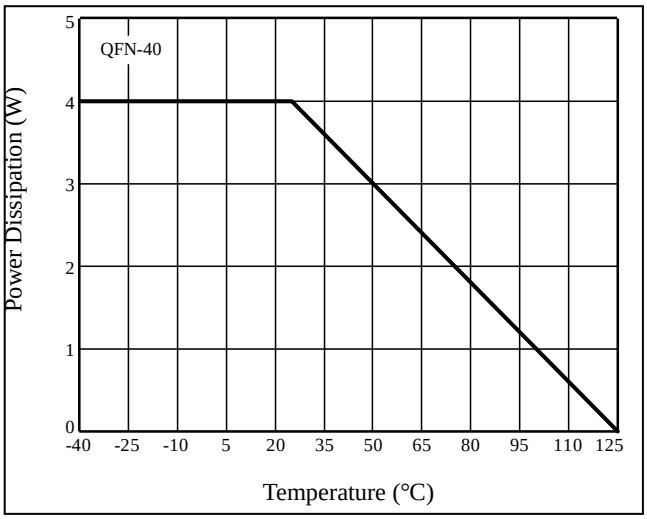
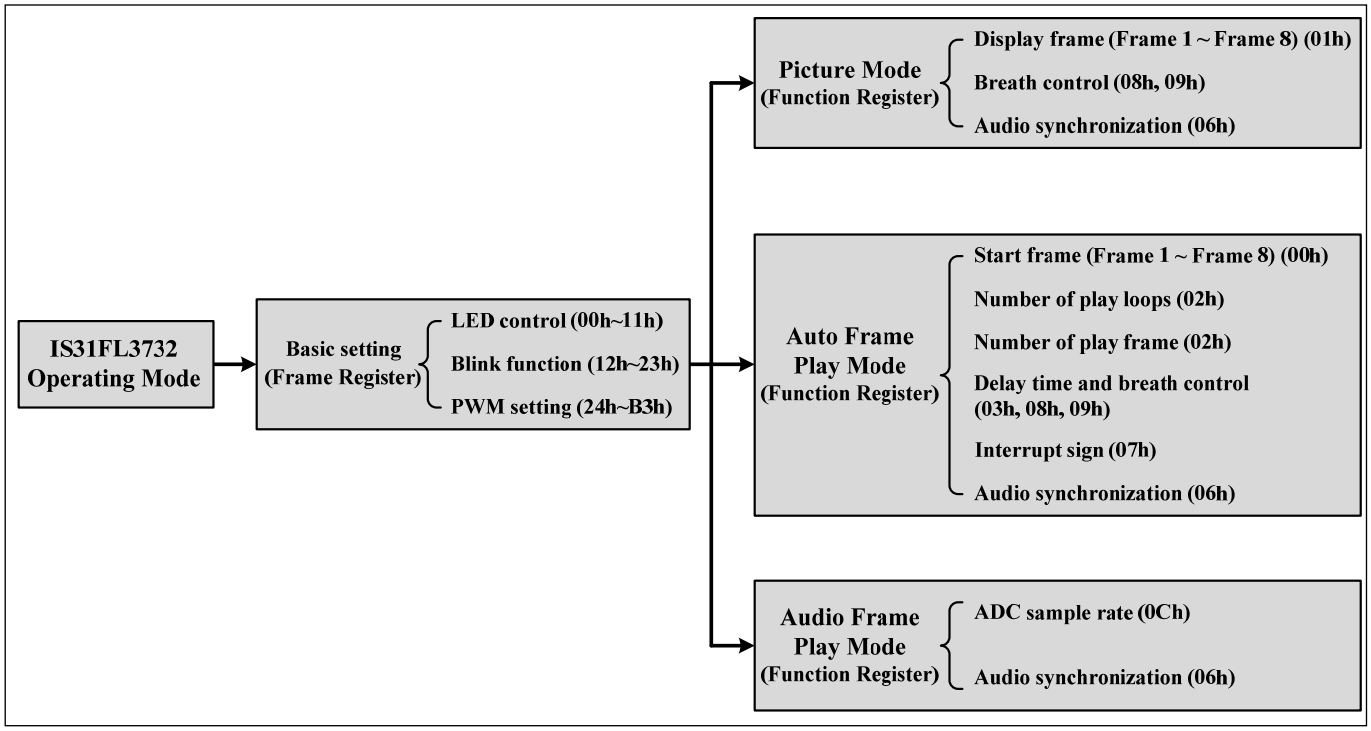


Figure 19 Dissipation Curve

APPLICATION DESIGN



CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

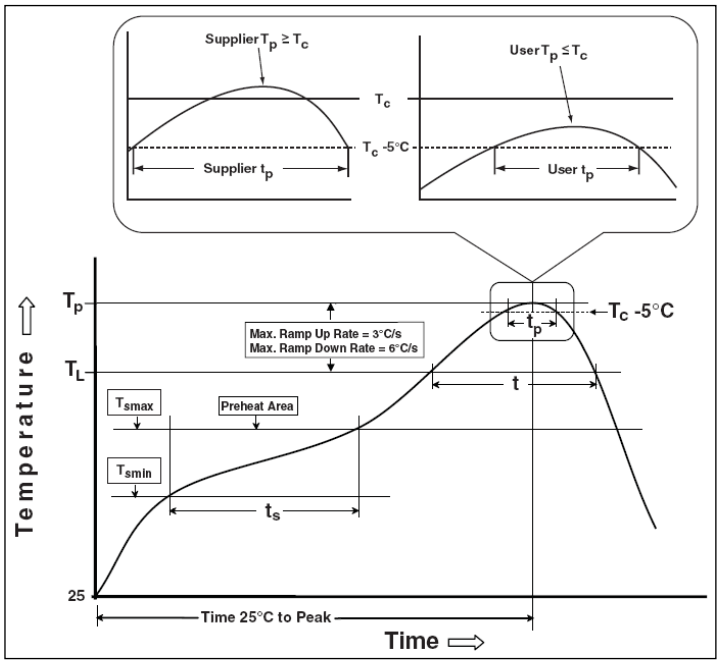
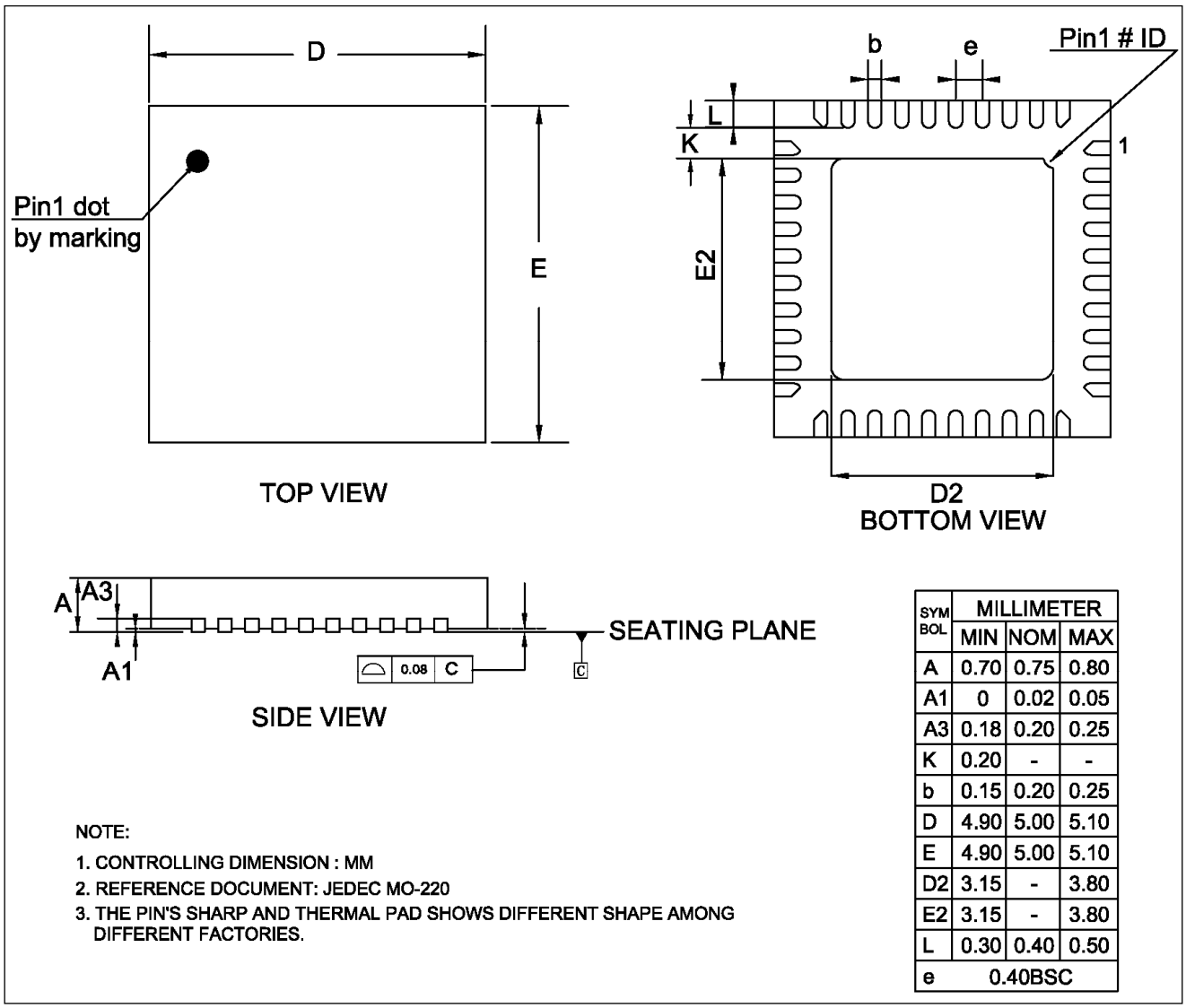


Figure 20 Classification Profile

PACKAGE INFORMATION

QFN-40

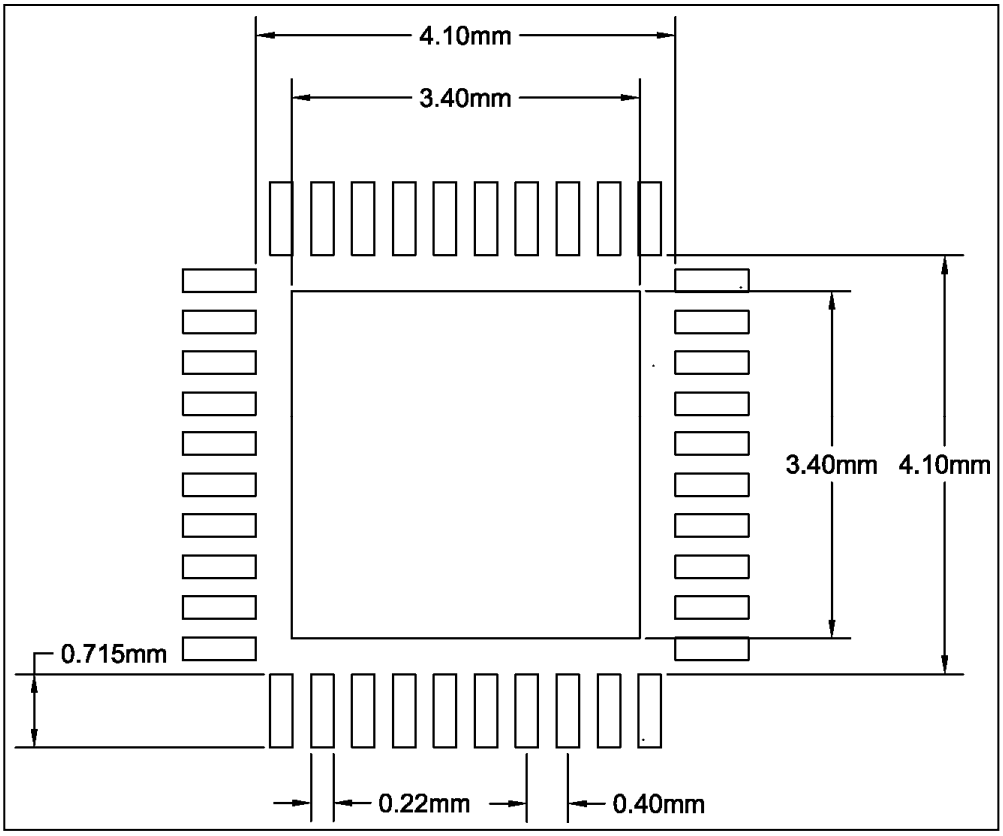


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.18	0.20	0.25
K	0.20	-	-
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.15	-	3.80
E2	3.15	-	3.80
L	0.30	0.40	0.50
e	0.40BSC		

NOTE:

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2015.09.06
B	1. Revise VCC MAXIMUM RATINGS from 5.5V to 6.0V 2. Update Figure 1, 2, 10, Formula(1)(2)(3) 3. Add θ_{JA} in ABSOLUTE MAXIMUM RATINGS table 4. Add POWER DISSIPATION section in APPLICATION INFORMATION	2016.06.22
C	Correct Figure 1 and 2.	2017.04.20
D	1. Update package POD 2. Update land pattern	2017.07.04

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