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Editors

Three-Dimensional Integration of Semiconductors

Processing, Materials, and Applications

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Morihiro Kada is an invited researcher of the National Institute of Advanced Industrial Science and Technology (AIST) and a part-time researcher at Osaka Prefecture University. Prior to joining AIST and the university, he headed the Japanese national research and development project on semiconductor 3D-Integration technology in the Association of Super-Advanced Electronics Technologies (ASET). He has also been the general manager of the Advanced Packaging Development Department in Sharp Corporation. He received his B.E. in applied physics from Fukui University, Japan in 1970. He has more than 40 years of experience in semiconductor packaging engineering, with major emphasis on developing chip scale, chip stack package, and three-dimensional-system-in-package (3D-SiP), and is the global pioneer of 3D-Integration technology in the world.

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Chapter 1
Research and Development History of Three-Dimensional Integration Technology

Morihiro Kada

1.1 Introduction

Semiconductor integrated circuits have been developed according to Moore's law; the conjecture made in 1965 was that the number of transistors in a dense integrated circuit (IC) will double every 2 years, and the industry has developed according to this trend [1]. Two different concepts have been proposed for future advancements. One is "More Moore," which suggests that technological progress will continue to follow scaling theory, and the other is termed "More than Moore," which emphasizes the evolution and diversification of function [2].

1.1.1 The International Technology Roadmap for Semiconductors

The international semiconductor research community gathered in 2005, at the abovementioned meeting (the International Technology Roadmap for Semiconductors, ITRS), which led to the concept of "More than Moore." Two years later, at ITRS 2007, a number of such ideas were formally defined. We elaborate on two of these: scaling and functional diversification with reference to Fig. 1.1.

1. Scaling: Fig. 1.1, vertical axis of "More Moore"
   a. *Geometrical scaling:* Also referred to as constant field scaling, this design methodology involves reducing the horizontal and vertical dimensions of physical features of the on-chip logic and memory storage components to

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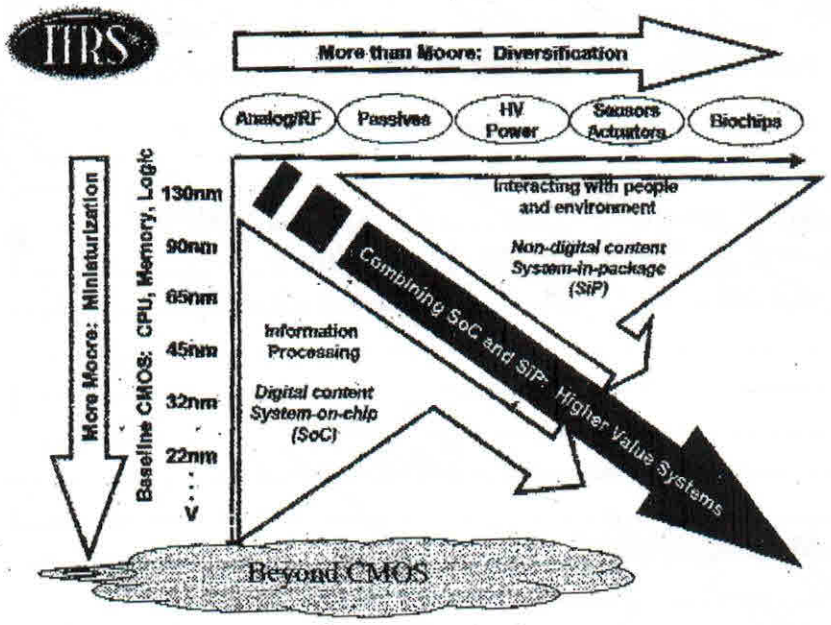


Fig. 1.1 A diagrammatic representation of the concepts of "Moore's law" and "More than Moore". (Reproduced with permission from Ref. [3], Fig. 4). *RF* radio frequency, *CPU* central processing unit, *CMOS* complementary metal–oxide–semiconductor

improve density (cost per function reduction), performance (speed, power), and reliability (Fig. 1.1).

b. *Equivalent scaling*: This approach refers to (a) three-dimensional (3D) device structure ("design factor") improvements as well as other nongeometric processing techniques and the use of new materials that affect the performance of the chip; (b) novel design techniques and technologies, such as multi-core design. Equivalent scaling occurs in conjunction with geometric scaling and aims for the continuation of "Moore's law."

2. Functional Diversification: Fig. 1.1, horizontal axis of "More than Moore."

Moore's law is not the only way to provide additional value to the end user. A complementary approach is that of functional diversification, which refers to the incorporation of new functionalities into devices that are not necessarily scalings of existing hardware or software. Typical of this "More than Moore" approach is the migration of non-digital functionalities (e.g., radio frequency (RF) communication, power control, passive components, sensors, and actuators) from the system board level into a particular chip-level (system on a chip; SoC) or package-level (system in package; SiP) implementation. As the need increases for evermore complex software to be embedded into SoCs and SiPs, the role of the software itself in performance scaling may also need to be considered. The objective of the "More than Moore" design methodology is to incorporate digital and non-digital functionalities into compact systems.

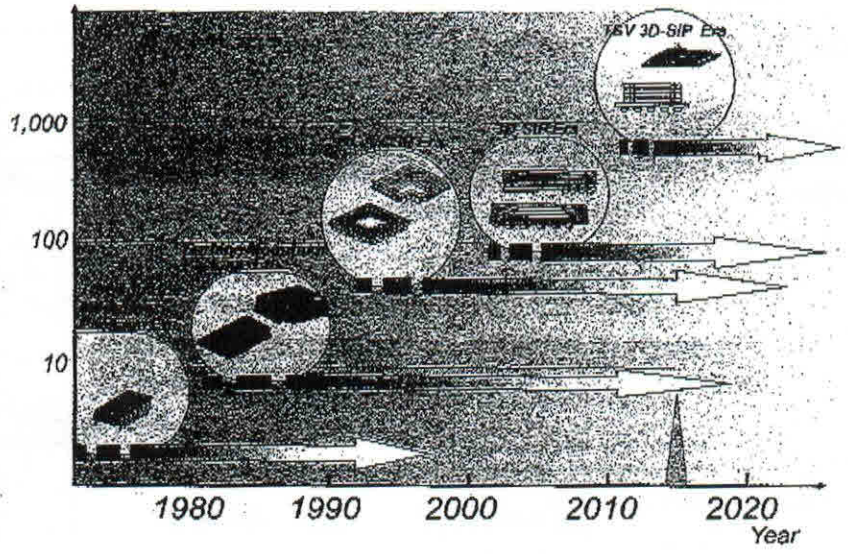


Fig. 1.2 Toward the new TSV 3D-SiP Era. *3D-SiP* three-dimensional system in package, *TSV* through-Si via, *BGA/CSP* ball grid array/chip-scale package

1.1.2 3D Integration Technology

Although 3D integration technology is not explicit in the definition of "More than Moore," it is generally considered to be one of the most important technology development strategies. The transistor scaling that has continued for more than 40 years is approaching the atomic level of silicon, and this physical limit will likely be reached in 10–15 years.

Entirely new device structures, such as carbon nanotubes, spintronics, and molecular switches are being developed to replace transistor technology. However, they will not be ready for 10–15 years. In the interim, 3D integration technology offers a viable solution for continued performance and economic advancement [4].

"More than Moore" is not just a solution to the limitation of "More Moore," it also recognizes the evolution and potential for improvements of packaging technology. Figure 1.2 illustrates the history of IC packaging technology. Every 10 years since the 1970s, packaging technology has undergone a technological revolution. The first decade of this century is the era of the 3D system in package (3D-SiP), and work has begun to develop new 3D technology termed through-Si via (TSV) that will define the present decade [5]. In TSV, the electrode passes completely through the silicon wafer (or chip). It represents the fusion of silicon wafer process technology (front end of line, FEOL) and semiconductor packaging technology (assembly/packaging).

3D integration using conventional technologies, such as with the wire bonding (WB) as shown in Fig. 1.3 (left), is referred to as 3D integration packaging technologies. In this book, we focus our attention on systems in which semiconductor chips are stacked and connected by TSV, as shown in Fig. 1.3 (right), which

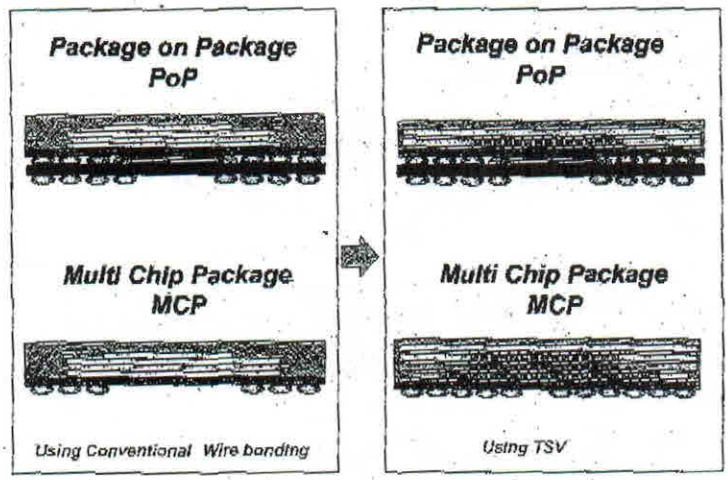


Fig. 1.3 3D integration packaging technology and 3D integration technology [6]

define 3D integration technology [6]. We do not discuss 3D integrated circuits (3D-IC) that use FEOL, such as 3D NAND in which transistors are stacked, nor the Intel tri-gate transistors that were introduced in the 22-nm generation ivy bridge CPU.

1.2 Motivation for 3D Integration Technology

The development impetus is accounted for in the following two points.

1. If semiconductor integrated circuit chips are connected using TSV, the interconnected distance is approximately 1/1000 of that using conventional WB (micrometers compared with millimeters). This results in dramatic reductions in electric resistance and capacitance, making possible high-speed operation and low power consumption.
2. It is difficult to make (wire) connections between the conventional packages on the mounting board on the order of thousands, but this task is straightforward, and on even grander scales, between Si chips using TSV. Thus, TSV-based systems that have several 1000 input/output (I/O) circuits are realizable, which also benefit from being lower power consumption devices with higher data transmission speeds.

3D integration need not be confined to like technologies. By combining semiconductor integrated circuits with, for example, micro-electro-mechanical systems (MEMS) devices, unique functionalities can be developed in what is termed heterogeneous 3D integration technology.

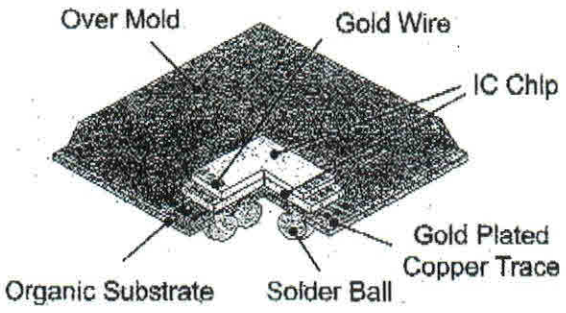


Fig. 1.4 Typical construction of S-CSP (MCP). *IC* integrated circuit

1.3 Research and Development History of 3D Integration Technology

1.3.1 3D Packaging Technology

Even as of 2015, the use of 3D-IC (TSV) is uncommon, with the exception of complementary metal–oxide–semiconductor imaging sensors (CIS). However, high-volume manufacturing of 3D integration packaging technology using WB continues.

In 1998, Sharp Corporation developed the world's first stacked two-chip chip-scale package (CSP) using WB [7]. Before that time, there was no notion of chip stacking in CSP. This led to its development for use in mobile phones, mostly by Japanese chip makers, such as Sharp; Mitsubishi, Hitachi, NEC, Toshiba, and Fujitsu. This technology was called stacked chip-scale (size) package (S-CSP) or multi-chip package (MCP). Figure 1.4 shows the typical construction of S-CSP (MCP).

S-CSP/MCP was first used to make combinations of NOR flash memory and of static random-access memory (SRAM), which are at the heart of all mobile phones. Consumer demand fuelled the development of smaller sizes and higher performance [8]. When Sharp developed the world's first stacked CSP, the combination memory development race was called the "East versus West War" over standardization by the Joint Electron Device Engineering Council. It became a demonstration of the strength of Japanese packaging technology.

Although, in the beginning, the interconnect technology was only WB, CSP stacking has given rise to the package on package (PoP) model, which also uses flip chip (FC) technology. Today, this approach is integral to modern smart phones and tablets; dynamic random access memory (DRAM) and application and/or baseband processors are stacked together using this technology. Upon these foundations, newer technologies continue to drive advances in telecommunications, such as through mold via (TMV) [9, 10]; see Fig. 1.5.

In the present-day flash memory, there are more than eight chips stacked into a single package [11]; see, for example, Fig. 1.6. This technology will likely continue being a mainstay of 3D integration packaging technology for some time yet. On the horizon are wireless interconnect technologies, such as capacitive and inductive 3D coupling [12].

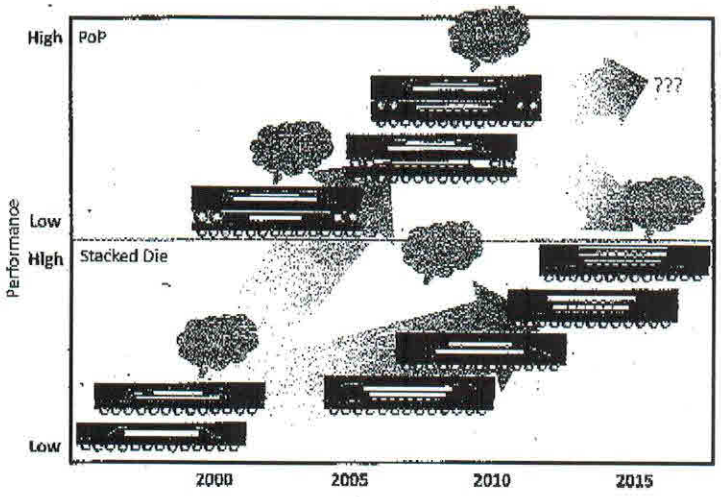


Fig. 1.5 3D integration packaging technology transition [10]. (With permission from Amkor Technology, Inc., Chandler AZ). *WB* wire bonding, *PoP* package on package, *FC* flip chip, *TMV* through-mold via, *TSV* through-Si via

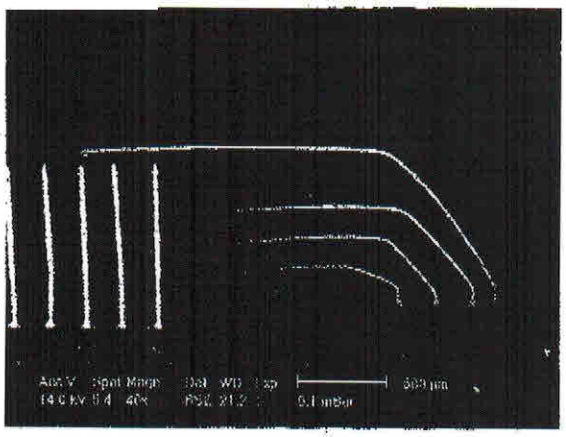
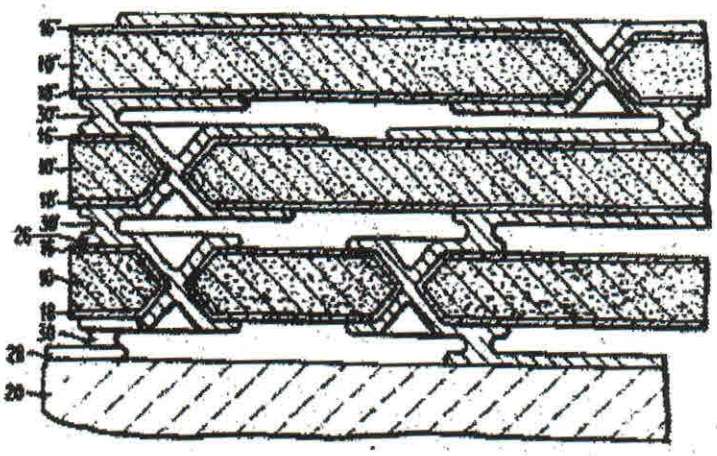


Fig. 1.6 World's first nine-chip stacked memory. (With permission from Toshiba Corporation)

1.3.2 Origin of the TSV Concept

The underlying concept of TSV technology is not new. International Business Machines Corporation filed the patent USP3,648,131 entitled, "Hourglass-shaped conductive connection through semiconductor structures" in November 1969, with the following abstract [13]:



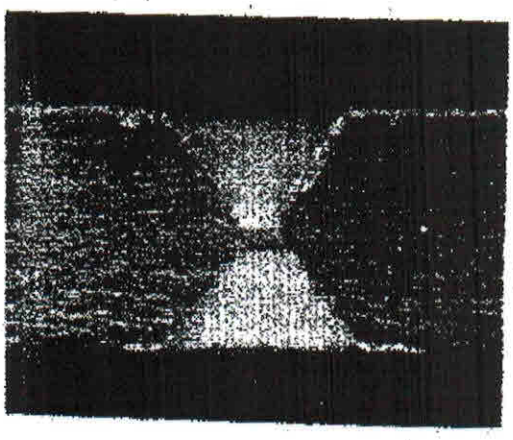


Fig. 1.7 US Patent 3,648,131 A [13]

"An integrated semiconductor structure including the fabrication thereof, and more particularly, an improved means for interconnecting the two planar surfaces of a semiconductor wafer. To provide the electrically conductive interconnections through the wafer, a hole is etched, insulated, and metallized. Active or passive devices may be formed on either or both sides of the wafer and connected to a substrate by solder pads without the use of beam leads or flying lead bonding." The drawings are shown in Fig. 1.7.

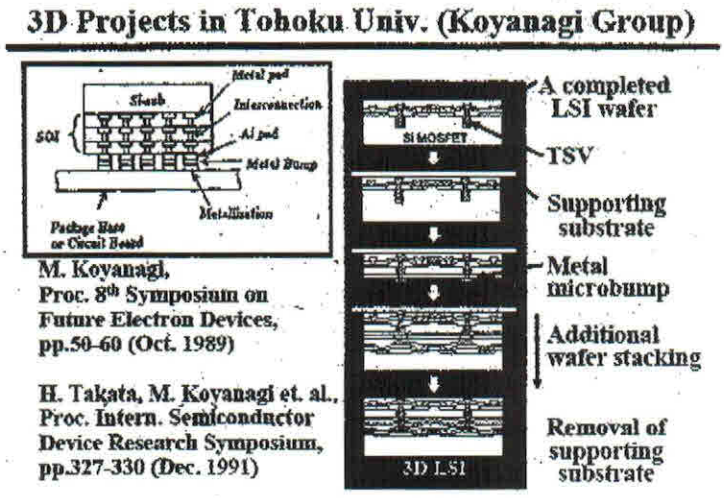


Fig. 1.8 Extracts from presentations by Tohoku University researchers in 1989 [14] and 1991 [15]. (With permission from Tohoku University, Japan). *TSV* through-Si via, *LSI wafer* large-scale integration wafer

Later on, patents JP (S59)1984-22954 (June 1, 1983) and patent JP (S61)1986–88546 (October 5, 1984) were filed by Hitachi Ltd. and Fujitsu Ltd, respectively. The patent JP (S63)1988–156348 (December 19, 1986), by Fujitsu, describes a stacked chip structure. Figure 1.8 shows key schematics of chip stacking techniques sourced from 1989 and 1991 conference presentations by Tohoku University, Japan [14, 15].

1.3.3 Research and Development History of 3D Technology in Organizations

Research and development of 3D integration technologies has been carried out through global efforts [16]. Some of the major contributions by region are summarized in Fig. 1.9 [17].

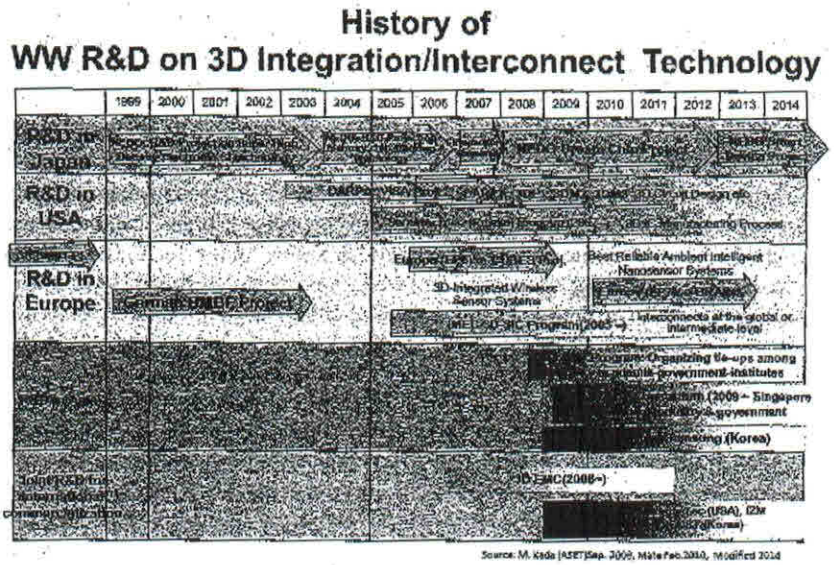


Fig. 1.9 History of global research and development on 3D integration technology. (Adapted from Ref. [16]). *NEDO* New Energy and Industrial Technology Development Organization, *DARPA* Defense Advanced Research Projects Agency, VISA vertically interconnected sensor arrays, *ADSTAC* Advanced Stacked-System Technology and Application Consortium, *TSV* through-silicon via, *ASSM* All Silicon System Module, *EMC* Equipment and Materials Consortium, *SiC* stacked integrated circuit, *German BMFT* German Ministry of Research, *BMBF* Federal Ministry of Education and Research, *FP7* Seventh Framework Programme

1.3.3.1 Japan

In Japan, research and development of the "Three-Dimensional Circuit Element R&D Project" by the Research and Development Association for Future (New) Electron Devices was conducted from 1981 to 1990, and the technology developed was termed "Cumulatively Bonded IC" (CUBIC): (in Japanese); TSV was not integral to the design. A thin film (approximately 2-μm thick) of electron channel metal–oxide–semiconductor field-effect transistor (nMOSFET) was laminated onto the bulk silicon device. The electrical interconnection of 1600 wiring contact arrays was checked, and the contact volume resistance of $5 \times 10^{-6}\ \Omega \cdot \mathrm{cm}^2$ did not adversely affect the operation [18].

In Japan, the Association of Super-Advanced Electronics Technologies (ASET) carried out a research and development project of 3D integration technology using TSV during the 5-year period 1999–2003. The project was entitled, "R&D on High Density Electronic System Integration Technology" (in Japanese). Its execution was entrusted to the New Energy and Industrial Technology Development Organization (NEDO) organization of the Japanese government's Ministry of Economy, Trade, and Industry (METI) [19]. Following on were the "Stacked Memory Chip

Technology Development Project" (in Japanese), 2004–2006 [20] and the "Development on Functionally Innovative 3D-Integrated Circuit (Dream Chip) Technology Project" (in Japanese), 2008–2012. In 2010, research was conducted with a focus on "Design Environmental Technology, Interposer Technology, Chip-Testing Technology, Three-dimensional Integration Basic Technology, Flex chip (FPGA) Technology, and RF MEMS."

The majority of the semiconductor-related businesses in Japan were involved in these projects. These included semiconductor companies Elpida, Toshiba, Renesas, and Rohm; electronic companies NEC, Sharp, Nac Image Tech., IBM, Panasonic, Hitachi, and Fujitsu; and material/equipment companies Advantest, DNP, Ibiden, Shinko, TEL, Toppan, Yamaichi, and Zycube. Furthermore, The University of Tokyo, Tohoku University, and the National Institute of Advanced Industrial Science and Technology represented the academic participation [21–23].

In 2010, an interim assessment led to a focus shift to thermal management/chip stacking technology, thin wafer technology, 3D integration technology, ultra-wide bus 3D-SiP, mixed signal (digital–analog) 3D integration technology, and heterogeneous 3D integration technology. The research outcomes are described in later sections of this book [24, 25].

However, despite the sizeable investment by the Japanese government over these long periods of time, the national semiconductor industry is presently in decline and future research and development remains uncertain.

The WOW alliance based at the Tokyo Institute of Technology (based at The University of Tokyo until 2014) was founded in 2008 [26], and the "Three-Dimensional Semiconductor Investigation Center" (translated from the Japanese) in Kyushu commenced operations in 2011 [27].

1.3.3.2 Japanese 3D Integration Technology Research and Development Project (Dream Chip)

The second full-scale national research and development (R&D) initiative of 3D integration technology using through-silicon via (TSV) was implemented over the 5-year period from 2008 to 2012. Super-Advanced Electronics Technologies (ASET) conducted the project "Development on Functionally Innovative 3D-Integrated Circuit (Dream Chip) Technology Project," and it was managed by the NEDO Organization that is based on "IT Innovation Program" of Japanese government's Ministry of Economy, Trade and Industry (METI). After the 2010 interim assessment, the two focus areas became 3D integration process basic technologies and application technologies using TSV. The former consisted of thermal management/chip-stacking technology, thin wafer technology, and 3D integration technology, while the latter focus area comprised ultra-wide bus 3D-SiP, mixed signal (digital–analog) 3D, and heterogeneous 3D; see Fig. 1.10. For details beyond research and development subjects and results, the reader is referred to Chapter 9 [17, 28].

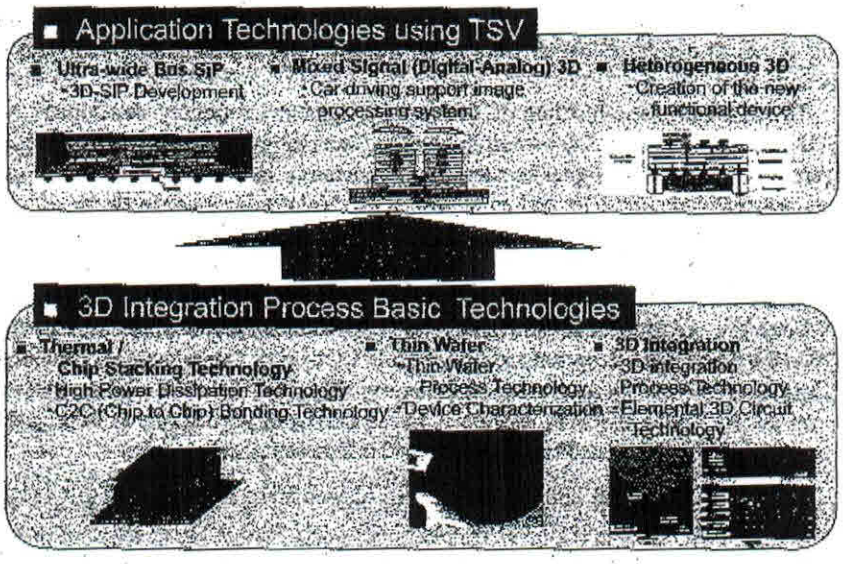


Fig. 1.10 Research and development subject of the Dream Chip Project. (With permission from the Electrochemical Society: ECS) [17]. *TSV* through-Si via

1.3.3.3 The USA

The US Defense Advanced Research Projects Agency (DARPA)'s work in microsystems technology has a long history. 3D-related research and development projects are controlled by the "Microsystems Technology Office (MTO)." These projects are:

1. Enhanced Digital (3D-IC Program)
   - Large amounts of cache memory
   - High memory bandwidth
2. Enhanced Analog (COSMOS Program)
   - Heterogeneous integration
   - Disparate process technologies (e.g., SiGe/Si, C.S./Si, SOI/Bulk)
3. Smart Focal Planes (Vertically Interconnected Sensor Arrays, VISA Program)
   - Processing at each pixel
   - High fill factors
4. Photonics (EPIC Program)
   - Optical and electronic tiers

DARPA funding and the Microelectronics Center of North Carolina Research and Development Institute (MCNC-RDI) supported a project that was started in 2003. The research and development device comprised VISA that implemented highly

parallel and densely interconnected architectures with micron-sized vias penetrating stacks of detectors, which were made from analog, digital, and mixed signal circuits.

The Massachusetts Institute of Technology Lincoln Laboratory developed "A SOI-Based Wafer-scale 3-D Circuit Integration Technology." Integral to this project were precision wafer aligner-bonder, low temperature oxide–oxide bonding, and concentric 3D via, all 3D-enabling technologies. Major milestones were the delivery of the 3DL1, 3DM2, and 3DM3 chips in April 2006, and November 2007 and 2010, respectively. Participants of the 3DM3 chip project were from universities, commercial laboratories, and the business sector.

They are Arizona State University (ASU), North Carolina State University (NCSU), The Naval Research Laboratory (NRL), the US Department of Defense (DoD), Fermi National Accelerator Laboratory, IBM, The State University of New York (SUNY), MIT Lincoln Laboratory, and so on. As for third 3D-IC Multiproject Run (3DM3)3D Circuits, 39 designs were submitted as follows:

3D Circuits Anti-tamper authentication chip, stacked memory (SRAM & DRAM), stacked microprocessor, hi-speed transmit/receive, one-chip GPS, network-on-chip, reconfigurable neural network, SAR processor elements, RF-switching power converter, power management for 3D-IC's, Integrated RF MEMS, implantable biosensors, and bio lab on chip.

3D Imaging Applications International Linear Collider (ILC) pixel readout, low-power pattern recognition 3D vision chip, multi-core processor with image recognition, focal plane image processor, and sub-l- sized pixel imaging array

3D Technology Characterization 3D radiation test structures, jitter-clock skew-propagation delay, hi-speed I/O, RF building block, meta-material inductors, and stacked MOSFET.

3D design software were also developed by PTC, NTSU, R3Logic, and the University of Minnesota (UMN) [29–32].

Following are the overview of press releases by International SEMATEC from 2004 to 2006. "June 10, 2004 they released its several top technical challenges for 2005, one of several top technical challenges was 3-D interconnect on the list for the first time" [33]. "Then aiming to expand the range of potential solutions to the challenges of continued CMOS scaling, they launched a project to explore the feasibility of 3D interconnect technology for the semiconductor industry, in February 9, 2006" [34]. Also, "December 13, 2010, SEMATECH, the Semiconductor Industry Association (SIA), and Semiconductor Research Corporation (SRC) announced they had established a new 3D Enablement program to drive cohesive industry standardization efforts and technical specifications for heterogeneous 3D integration" [35].

In September 13, 2011, members of SEMATEC were Hynix, IBM, Intel, Samsung, ADI, and ON Semiconductor as the IDMS. As for foundries, Global Foundries, TSMC, and UMC. As for Fabless, HP, Altera, LSI, and Qualcomm. As for

OSATs, ASE. As for Suppliers Atotech, COSAR, NEXX, TEL, R&D Partners, CNSE/FRMC, NIST, and SRC [36].

1.3.3.4 Europe

In Europe, 3D integration technology research has a long history, which was reviewed in the welcome presentation at the IEEE 3D System Integration Conference 2010 (3D-IC) in Munich, November 16–18 [37].

Siemens, AEG, Philips, and Fraunhofer IFT formed the 1987–1989 consortium for developing 3D integration technology. From the 1980s through to the early 2000s, projects were supported by the German Ministry of Research (German BMFT) and the Federal Ministry of Education and Research (BMBF). Subsequent projects were supported by the European Committee: From 2006 to 2009, the European ICT Project "e-CUBES (6th European Framework ICT)—3D-Integrated Wireless Sensor Systems, Technology Platform for 3D Heterogeneous Integration" was conducted. They said four optimized 3D integration technologies were successfully used in the development of three e-CUBES application demonstrators: thin-chip-integration technology (TCI/UTCS) for Philips' Health & Fitness demonstrator, TSV technology ICV-SLID, HoViGo for Infineon's Automotive demonstrator (TPMS) and Package-in-Package technology HiPPiP for Thales' Aeronautic demonstrator [38, 39].

And the latest was the Seventh Framework Programme (FP7: 2007–2013) of the European Union for research, technological R&D, and demonstration activities. "e-BRAINS"—Best Reliable Ambient Intelligent Nanosensor Systems for developing 3D Heterogeneous System Integration.

The project members were Infineon, Fraunhoer, Siemens, SINTEF, sensonor, imec, SORIN Group, CEA, IQE, FPFL, 3D plus, Tyndall, DMCE, TU, Vermon, ITE, MaganaDiagnositics, TECHNICHE UNIVERSITAT CHEMNITZ, and eesy-id. Applications are smart biosensor grain, Infrared imager, active medical implant, air quality system, and smart ultra-sound imaging probe [40, 41]. Following are the overview of press releases by IMEC from 2005 and CEA-Leti from 2011.

July 2005, "IMEC announced that IMEC launched advanced Packaging and Interconnect Center (APIC) and started to develop 3D Stacked IC "3D-SIC." APIC grouped more than 30 partners worldwide including integrated device manufacturers (IDMs), system houses, packaging, assembly and test houses and so on. The programs were based on interconnects at the global or intermediate level of the chip wiring hierarchy." [42].

Then "IMEC developed another R&D subject "3D-WLP," wafer level packaging, and "3D-SIP," traditional packaging interconnect technology. These were the part of IMEC's Industrial Affiliation Program (IIAP) on advanced interconnect technology for future technology node" [43].

And, "Qualcomm announced to participate in IMEC's industrial affiliation program (IIAP) on 3D-integration 2008 and also extends 3D research agreement with Qualcomm focusing on advanced technologies and devices 2011 [44, 45].

Also, "IMEC and TSMC announced 2009 that they have forged an Innovation Incubation Alliance to create a platform enabling the R&D of innovative product solutions using emerging More-than-Moore technology options [46].

Partners of IMEC 3D System Integration Program in 2011, were for Logic IDM, Panasonic, Intel, Fujitsu, Sony. As for Memory IDM Micorn, As for foundries TSMC, GlobalFamundries. As for fabless Quacomm, Xilinx, Nvidea, Altera. As for OSAT Amkor UTAC. As for EDA Synopsys, Acdnxe, Atrenta. As for Material suppliers Hitachi Chemical, ThinMaterials, Henkel, BASF. As for Equipment Suppliers Applied Material, Lam, TEL, Suss Screen, Ultratec, CascadeMicortech, Disco, Nanda Tech PVA Tepla, Smart Equipment Technology (Set) [47].

Followings are the announcement of CEA-Leti. "January 2011, they significantly expand its technology offering this month when it ramps up one of Europe's first 300 mm lines dedicated to 3D-integration applications." [48].

And "CEA-Leti announced January 2012 that the launch of a major new platform that provides industrial and academic partners with a global offer of mature 3D innovative technologies for their advanced products and research projects" [49].

1.3.3.5 Asia

The research and development project entitled, "Advanced Stacked-System Technology and Application Consortium" (Ad-STAC), centering on ITRI, has been supported by the Taiwanese government since 2008. The initial announcement was as follows:

"Formed on July 23, 2008, Ad-STAC provides a unique platform for both technical exchanges and information sharing among the partners distributed worldwide." "The purpose of Ad-STAC is to unify companies in different field but not limited academia, government industries, and institute, to co-operate and improve the 3D IC technology [50].

Members were 22 companies in October 2010. Applied Materials Inc of Taiwan, Atotech, Deutschland GmbH, Brewer Science Inc., Cadence Design Systems, Inc. Graduate School of Engineering, the University of Tokyo, Hermes Epitek Corp., SUSS MicroTec AG., Tazmo Co., Ltd, Unimicron Corporation, IV Technologies, Air Products, GPT, Disco, ASE, Leading Precision, Dupont, BASF, SPTS, UMC, SPIL, Cabot Microelectronics, and Cisco.

The full 300 mm line for 3D development was installed by the end of 2009 [51].

In South Korea, there has been speculation of a national project led by Hynix and Amkor but details presently remain confidential [52].

The Institute of Microelectronics (IME) Agency for Science, Technology, and Research (A*STAR) has been active since 2011. They announced, "Dec 6, 2011, IME and Tezzaron Semiconductor announced a research collaboration agreement to develop and exploit advanced Through Silicon Interposer (TSI) technology" [53].

June 5, 2012-IME and United Microelectronics Corporation agreed to develop Through-Silicon Via (TSV) technology for backside illuminated CMOS image sensors (CIS). [54] Aug 17, 2012-IME and Huawei Technologies, signed MOU to develop and advance Through Silicon Interposer (TSI) technology. The two organizations will collaborate on advanced packaging with TSI, 2.5D/3D-IC research and development, and demonstrate heterogeneous 2.5D design and manufacturing flow. [55]

1.3.3.6 International

Press releases of international 3D integration technology research and development consortia are as follows:

"Semiconductor 3D Equipment and Materials Consortium (EMC-3D) is a new consortium created to address the technical and cost issues of creating 3D interconnects using TSV technology for chip stacking and MEMS/sensors packaging. Equipment companies initiating the consortium are Alcatel, EV Group, Semitool and XSiL. Associate research members include Fraunhofer IZM, SAIT (Samsung Advanced Institute of Technology), KAIST (Korea Advanced Institute of Science and Technology) and TAMU (Texas A&M University). Material members include Rohm and Haas, Honeywell, Enthone, and AZ with wafer service support from Isonics [56].

Another international consortium's announcement was as follows: "The Microsystems Packaging Research Center (PRC) at Georgia Tech, in partnership with Fraunhofer IZM (Germany) and the Korea Advanced Institute of Science and Technology (KAIST) launched a global industry consortium titled"3D All Silicon System Module (3DASSM)" in October, 2008 [57].

1.4 Research and Development History of 3D Integration Technology for Applications

1.4.1 CMOS Image Sensor and MEMS

Toshiba, Aptina, STMicroelectronics, and several other companies commercialized the complementary metal–oxide–semiconductor (CMOS) image sensor during 2007–2008, which used TSV as the target electrode formation technology. The advantage of using TSV was its compactness, permitting the design of miniature devices.

Toshiba named the new application of penetration electrode technology "Through Chip Via" (TCV). This space-saving technology made it possible to mount an assembly of camera module components in a wafer state. For example, the conventional substrates and wire bonding spaces were reduced by forming a solder ball in the back side of the chip.

STMicroelectronics' multi-chip MEMS devices, such as smart sensors and multi-axis inertial modules, enable a higher level of functional integration and performance in a smaller form factor [58–60].

1.4.2 DRAM

DRAM is anticipated to be the principle application driving volume manufacturing of full-scale 3D integration technology.

In June 2011, Elpida Memory shipped the world's first 8 GB DRAM sample. It consisted of four 2 GB (double data rate type 3; DDR3) modules stacked using TSV technology [61]. Then in August of the same year, Samsung Electronics announced that they had developed 30-nm-class 32 GB Green DDR3 DRAM using TSV package technology for next-generation servers [62].

Hynix became a member of SEMATECH's 3D Interconnect program at the College of Nanoscale Science and Engineering (CNSE) of the University at Albany [63].

Smart phone and tablet SoCs have reached impressive levels of performance in the past few years. However, limited memory bandwidth has become a bottleneck for further advancements, and the continued growth of the display resolution only exacerbates this problem. Despite their size difference, tablets have now overtaken laptop computers in display resolution.

JEDEC Solid State Technology Association, the global leader in the development of standards for the microelectronics industry, announced the availability of a new standard for wide I/O mobile DRAM: JESD229 Wide I/O Single Data Rate (SDR). They said "Widely anticipated by the industry, Wide I/O mobile DRAM is a breakthrough technology that will meet industry demands for increased levels of integration as well as improved bandwidth, latency, power, weight and form factor; providing the ultimate in performance, energy efficiency and small size for smartphones, tablets, handheld gaming consoles and other mobile devices." JESD229 using TSV was standardized in December 2011 in JEDEC [64, 65].

However, wide I/O memory, which has a bandwidth of 12.8 GB/s for mobile applications, has not been adopted because of the significant improvements of classical DDR memory. It is now possible to achieve the desired bandwidth using more traditional 2D-IC integration in both PC/server and mobile DRAM applications. JEDEC more recently moved to standardize Wide I/O2

One of the primary challenges facing DRAM engineers is the memory bandwidth required by high-performance computers and next-generation networking equipment. Conventional DDR is not suitable for these architectures. To address these needs, in October 2011, Samsung Electronics and Micron Technology announced a collaboration to implement as an open interface the Hybrid Memory Cube (HMC). They said "The Hybrid Memory Cube Consortium (HMCC) will work closely with fellow developers Altera, IBM (added by another announcement), Open-Silicon and Xilinx to collectively accelerate industry efforts in bringing to market a broad set of technologies. The consortium will initially define a specification to enable

applications ranging from large-scale networking to industrial products and high-performance computing."

Then, in May 2012, HMCC announced that Microsoft Corp. has joined the consortium and in June 2012, they also announced that new members ARM, HP, and SK hynix, Inc. have joined the global effort to accelerate widespread industry adoption of HMC technology.

In August 2012, they announced that its developer members have released the initial draft of the HMC interface specification to a rapidly growing number of industry adopters [66–70].

1.4.3 2.5D with Interposer

The technology of mounting IC chips side by side, using a Si Interposer, rather than 3D stacking with TSV, has gained popularity. Because the Si interposer is technically a silicon chip with the wiring layer only, the IC is also referred to as being 2.5 dimensional.

Xilinx announcement in October 2010 for 2.5D is as follows. "The industry's first stacked silicon interconnect technology for delivering breakthrough capacity, bandwidth and power savings using multiple FPGA die in a single package for applications that require high-transistor and logic density, as well as tremendous levels of computational and bandwidth performance" [71, 72].

Then, just 1 year later, in 2011, Xilinx announced the progression. "First shipments of its Virtex®-7 2000T Field Programmable Gate Array (FPGA), the world's highest-capacity programmable logic device built using 6.8 billion transistors, providing customers access to an unprecedented 2 million logic cells, equivalent to 20 million ASIC gates, for system integration, ASIC replacement, and ASIC prototyping and emulation." [73].

One and a half years later, the competition started. Taiwan Semiconductor Manufacturing Co. Ltd. (TSMC) and Altera Corp, on March 22, 2012, announced "The joint development of a heterogeneous 3-D IC test vehicle using TSMC's chip-on-wafer-on-substrate (CoWoS) integration process. TSMC said the technology is an integrated process technology that attaches device silicon chips to a wafer through a chip-on-wafer bonding process [74].

1.4.4 Others

Many other semiconductor companies, such as IBM [75] and Qualcomm [76], have also been developing 3D integration technology.

In September 2006, Intel announced at their developer forum, the promise of an 80-core chip within 5 years based on the innovation of connecting memory directly to processor cores. They also showcased TSV alongside the 80-core chip prototypes, which piggybacked 256 MB of SRAM directly to each chip's 80 cores [77].

But, in June 2010, they said as follows. "There are several problems with TSV technology: Lack of EDA design tools; complexity of designs; integration of

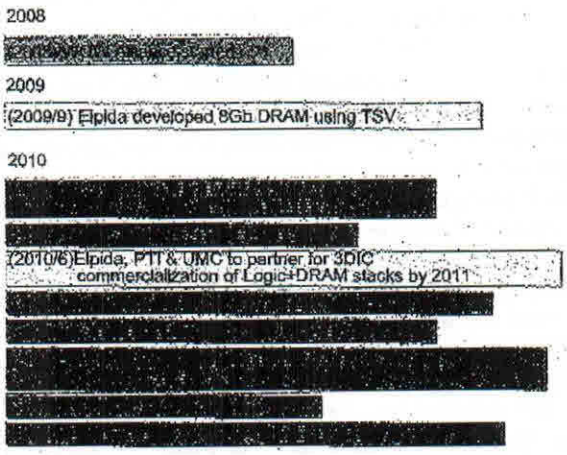


Fig. 1.11 Worldwide research and development activities in 2008–2010. *DRAM* dynamic random access memory, *TSV* through-silicone via, *TSMC* Taiwan Semiconductor Manufacturing Co. Ltd, *AD-STAC* Advanced Stacked-System Technology and Application Consortium, *UMC* United Microelectronics Corporation, *MPW* multi-project wafer, *MOSIS* metal–oxide–silicon implementation service, *CMP* circuits multi-projects, *SEMI* semiconductor equipment and materials international, *I/O* input/output

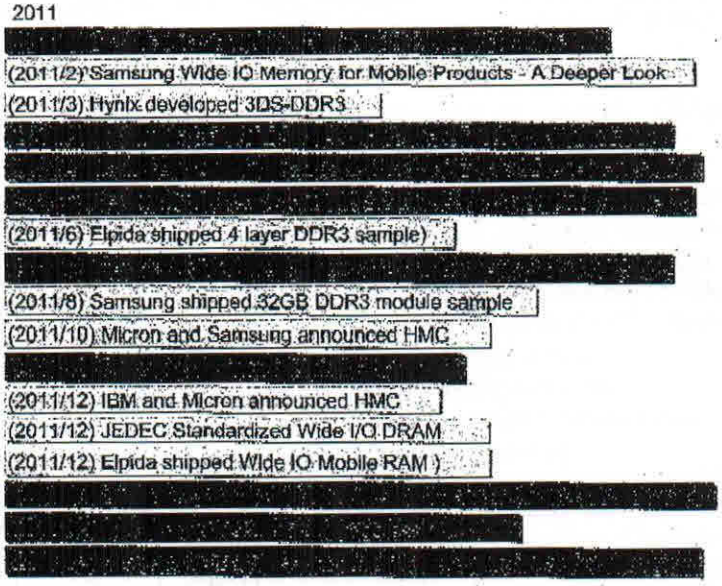


Fig. 1.12 Worldwide research and development activities in 2011. *DDR3* double data rate type 3, *CNSE* College of Nanoscale Science and Engineering, *3D-IC* three-dimensional integrated circuit, MOSIS metal–oxide–silicon implementation service, *DRAM* dynamic random access memory, *TSV* through-silicone via, *HMC* hybrid memory cube, *FPGA* field-programmable gate array, *I/O* input/output, *RAM* random access memory, *SoC* system on chip, *TSMC* Taiwan Semiconductor Manufacturing Co. Ltd, *TSI* through silicon interposer, *A*STAR* Agency for Science, Technology, and Research

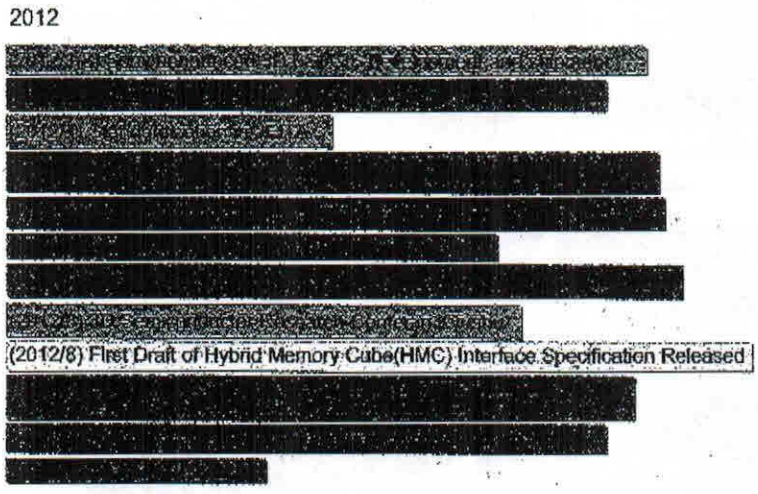


Fig. 1.13 Worldwide research and development activities in 2012. *BIS* back-illuminated sensor, *CIS* complementary metal–oxide–semiconductor imaging sensors, *TSMC* Taiwan Semiconductor Manufacturing Co. Ltd, *JEITA* Japan Electronics and Information Technology Industries Association, *TSV* through-silicone via, *FPGA* field-programmable gate array, *A*STAR* Agency for Science, Technology, and Research, *UMC* United Microelectronics Corporation, *SIP* system in package

assembly and test; cost; and lack of standards. As previously reported, Intel Corp. is still searching for an application for TSVs. It does not make sense for Intel to go to 3D with CPU cache memory" [78].

A summary of worldwide research and development activities from 2008 to 2012 are shown in Figs. 1.11, 1.12, and 1.13.

The 3D integration technology using TSV has not yet reached high-volume manufacturing despite the sizeable global investment in research and development. There are several reasons for this. Standardization is difficult because of the diversity of architectures, such as Via Size and TSV, process order, for example, Via First/Last/Front/Back, and issues with the supply chain for high-volume manufacturing and high component costs.

However, the 3D integration technology in which TSV is used and the arguments surrounding its application and forecasted use is actively being discussed.

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