FinFET Scaling to 10nm Gate Length

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Abstract

While the selection of new "backbone" device structure in the era of post-planar CMOS is open to a few candidates, FinFET and its variants show great potential in scalability and manufacturability for nanoscale CMOS. In this paper we report the design, fabrication, performance, and integration issues of double-gate FinFET with the physical gate length being aggressively shrunk down to 10nm and the fin width down to 12nm. These MOSFETs are believed to be the smallest double-gate transistors ever fabricated. Excellent short-channel performance is observed in devices with a wide range of gate lengths (10~105nm). The subthreshold slopes of the 10nm gate length FinFETs are 125mV/dec for n-FET and 101mV/dec for p-FET, respectively. The DIBL's are 71mV/V for n-FET and 120mV/V for p-FET, respectively. At 55nm gate length, the subthreshold slopes are 64mV/dec for n-FET and 68mV/dec for p-FET, which is very close to the ideal MOSFET behavior (at room temperature). The DIBL's are 11mV/V for n-FET and 27mV/V for p-FET, respectively. All measurements were performed at a supply voltage of 1.2V. The observed short-channel behavior outperforms any reported single-gate silicon MOSFETs. Due to the (110) channel crystal orientation, hole mobility in the fabricated p-channel FinFET remarkably exceeds that in a traditional planar MOSFET. At 105nm gate length, p-channel FinFET shows a record-high transconductance of $633\mu S/\mu m$ at a V_{dd} of 1.2V. At extremely small gate lengths, parasitic R_{sd} in the narrow fin (proportionally scaled with L_g) influences the device performance. Working CMOS FinFET inverters are also demonstrated.

Introduction

Si CMOS has been the main stream IC fabrication technology for three decades. In the last few years, the industry has witnessed a striking progress in downsizing the planar CMOS. Despite many fabrication challenges, 15nm physical gate length bulk MOSFETs have been recently demonstrated. However, scaling planar CMOS to 10nm-and-below would be exceptionally difficult, if not completely impossible, due to electrostatics, excessive leakages, mobility degradation, and many realistic fabrication issues. Particularly, control of leakage (hence power) in a nanoscale transistor would be critical to high-performance chips such as microprocessors.

Non-planar MOSFETs provide potential advantages in packing density, carrier transport, and device scalability. Double-gate and surround-gate MOSFETs have been researched for a decade, they were not seriously considered by the industry due to their complicated fabrication process. These structures have regained attentions in deep-sub-100nm CMOS due to many scaling limits associated with the planar CMOS. While a dozen of device structures have been invented in the last 5~6 years, the industry's focus has been pointing to FinFET, a double-gate device proposed in 1999 [1] (initially named folded-channel FET [2]), due to its quasi-planar structure and relatively simple fabrication.

Fabrication

Figure 1 (a)-(f) show the schematic diagram of the double-gate FinFET fabrication process. Figure 1 (g)-(h) are the top- and tilted-view SEM of a FinFET in the middle of fabrication (after gate etching). Figure 2 is the layout design of a FinFET with single-fin structure. Multiple-fin devices were also fabricated in this experiment. A major distinction between a FinFET and a traditional planar FET is an appreciably narrowed active region (fin). Reduction of the fin width (i.e., body thickness), T_{fin}, is important to the scaling of double-gate FinFET. In addition, the overlay of the gate to the active layer should be effectively controlled to reduce the transistor performance variation.

The FinFETs were fabricated on bonded SOI wafers with a modified planar CMOS process. Dual doped (n^+/p^+) poly-Si gates were used as gate electrodes. The poly-Si gates were doped by ion implantations and subsequently activated with RTA. 193nm and 248nm wavelength optical lithography were used to pattern the Si fin and the gate, respectively. A pattern reduction technique was able to produce both fin width and gate length down to sub-10nm dimensions. A nitrided oxide with 17Å physical thickness was used as the gate insulator. Other process features include low-temperature source/drain annealing, NiSi, and Cu metalization. The CMOS FinFET inverters (built from multiple-fin transistors) were also fabricated.

The conducting channels were formed on the two vertical sidewalls of the silicon fin, which are in the (110) crystal orientation. This channel crystal orientation is different from that in a conventional planar CMOS device, which is (100). A thin sacrificial oxide was formed and later stripped completely to remove the Si surface damage caused during the plasma etching of the fin stack. A thin insulating cap layer is retained on top of the Si fin.

Device Characteristics

A. Scaling Performance

Figure 3 is the TEM of a FinFET with a 10nm-long poly-Si gate. NiSi was formed on top of the poly-Si gate electrode. Figure 4 is the TEM of a narrow Si fin etched from the SOI wafer. Figure 5 is the I_d-V_d characteristics of the 10nm gate length CMOS FinFETs. The drive currents are 446μA/μm for n-channel FinFET and 356μA/μm for p-channel FinFET, both measured at a gate over-drive of 1V and a V_{dd} of 1.2V. All the currents are normalized by two times the fin height (i.e., the total channel width of a double-gate device). A large V_{dd} is selected due to the thick gate oxide used. Figure 6 is the subthreshold I_d-V_g behavior for the same devices. In this experiment the threshold voltages are shifted from the desired values due to the use of poly-Si gate and lightly doped channels. The threshold voltage can be fixed by proper channel implant and/or using alternative gate materials with appropriate workfunction. Figure 7 is the gate C-V characteristics measured from a multiple-fin device with large gate area ($10x10μm^2$).

At 10nm gate length, the sub-threshold slopes are 125mV/dec for n-channel FinFET and 101mV/dec for p-channel FinFET, respectively. The DIBL's are 71mV/V for n-channel FinFET and 120mV/V for p-channel FinFET, respectively. Despite the relatively thick fin body used (17~26nm), the good short-channel performance is observed because of the dual gate control and the significant grading of the source/drain junction. A largely graded source/drain junction helps reducing the electrical coupling from the drain biasing, relaxing the strict requirement on fin width scaling. Figure 8 shows the sub-threshold slopes and DIBL's measured from a group of FinFETs with different gate lengths but the same fin width. Table-1 summarizes the short-channel effects of several recently published FinFETs from different sources.

B. Parasitics and Carrier Transport

Figure 9 is the TEM of a 12nm-wide silicon fin (patterned by optical lithography). The fin aspect ratio is determined by circuit design and fabrication considerations as illustrated in Figure 10. The short-channel performance of the FinFET could be further improved by reducing the fin width. However, this introduces a large parasitic source/drain resistance, degrading the device drive current. With a wide fin (hence less parasitics), FinFETs with longer channel show good DC performance (Figure 11-12). In particular, the peak transconductance (at V_{dd} =1.2V) of the p-channel FinFET is very high (633μS/μm) measured from a device with 105nm gate length (Figure 13), which is consistent with the large hole mobility observed. While the electron mobility in a (110) FinFET channel is decreased as compared with that in a (100) channel (conventional planar FET) (Figure 14), the hole mobility in a (110) FinFET channel is remarkably improved from that in a (100) channel (Figure 15). Hole mobility in a p-channel FinFET is roughly 100% higher than that in a planar FET (measured at the same gate over-drive of 0.8V) due to the significantly reduced vertical electric field in the inversion layer and the different channel crystal orientation. Both conditions of sacrificial oxidation resulted in comparable mobility, suggesting that a clean gate oxide interface can be obtained with a sacrificial oxidation of 50Å (Figure 16). The direct tunneling leakage through thin gate oxide (formed on sidewalls of the etched silicon) in the FinFET is comparable to what was measured in a planar FET with the same gate oxide physical thickness (Figure 17).

C. Gate Delay and CMOS Inverter

Figure 18 shows the intrinsic gate delay (CV/I) of the fabricated CMOS FinFETs as compared with that of the published planar devices. Gate delays of 0.34ps for n-FET and 0.43ps for p-FET, respectively, were achieved for the 10nm gate length FinFETs at V_{dd}=1.2V. Figure 19 is the schematic layout of a FinFET CMOS inverter with multiple-fin device configuration. Figure 20 is the voltage transfer characteristic measured from the fabricated CMOS FinFET inverter at a supply voltage of 1V.

Summary

Double-gate CMOS FinFETs were fabricated with the smallest physical gate length ever reported. With the demonstrated scalability and potential performance benefit (under the penalty of adding some fabrication complexity to the existing planar process), the FinFET would be a strong competitor or successor to classical CMOS. While a few non-show-stopper issues (e.g., gate material engineering and parasitics reduction) need to be addressed, the FinFET is promising for the extremely scaled CMOS in which the packing density, scalability, performance, and power dissipation would be among the vital challenges.

References

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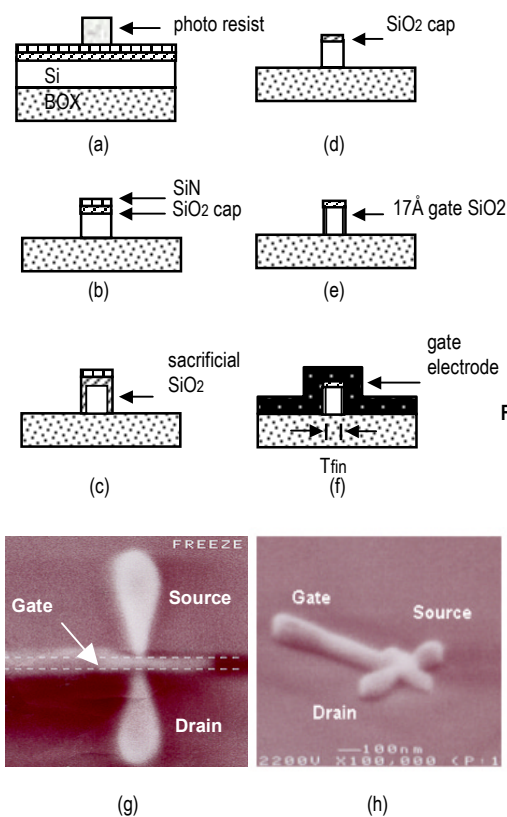
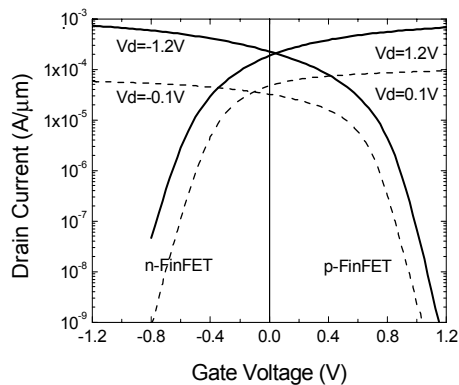**Fig.1** (a-f) FinFET fabrication flow. (g) Top view and (h) tilted view of FinFET right after gate etching.

Fig.2 Layout of FinFET with single fin structure.

Fig.3 Cross-section TEM of 10nm polysilicon gate with NiSi formed on top.

Fig.4 Cross-section TEM of a narrow silicon fin with 17A nitrided oxide formed on both sidewalls.
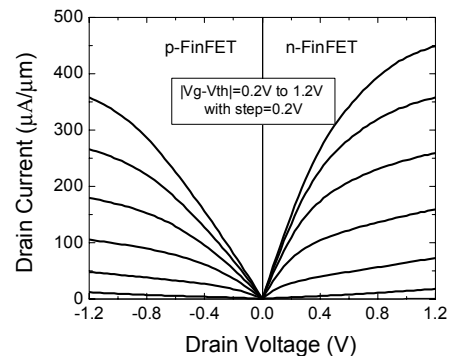
Fig.5 Id-Vd characteristics of 10nm gate length CMOS FinFET transistors.

Fig.6 Subthreshold Id-Vg behavior of 10nm gate length CMOS FinFET transistors.

Fig.7 Gate C-V curves of FinFET (Tox(phys)=17A).
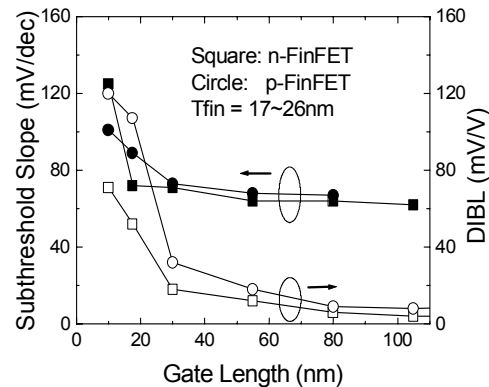
Fig.8 Short-channel effects of CMOS FinFET.

Transistor Parameter	This Work FinFET	This Work FinFET	Ref. [5] FinFET (IEDM'01)	Ref. [7] FinFET (VLSI'02)	Ref. [3] FinFET (DRC'01)	Ref. [6] FinFET (IEDM'01)	Ref. [4] FinFET (DRC'01)
Lg (nm)	10	55	20	35	60	60	100
Vdd (V)	1.2	1.2	1	1	1	1.5	1.5
Tox(phys) (A)	17	17	21	24	25	16	22
Gate Electrode	Poly-Si	Poly-Si	N+ SiGe	in-situ N+	N+ SiGe	Poly-Si	Poly-Si
Swing, N (mV/dec)	125	64	75	78	70	66	72
Swing, P (mV/dec)	101	68	90	96	80	65	N/A
DIBL, N (mV/V)	71	11	100	N/A	40	N/A	57
DIBL, P (mV/V)	120	27	140	N/A	90	N/A	N/A

Table 1 Summary of FinFET scaling performance.
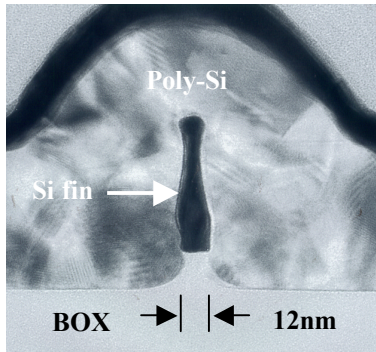
Fig.9 12nm wide fin patterned by optical lithography.
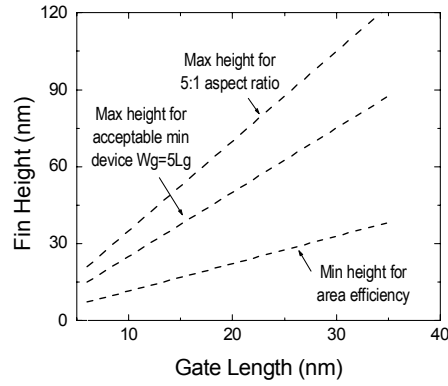

Fig.10 Fin height is determined by process and circuit design considerations.
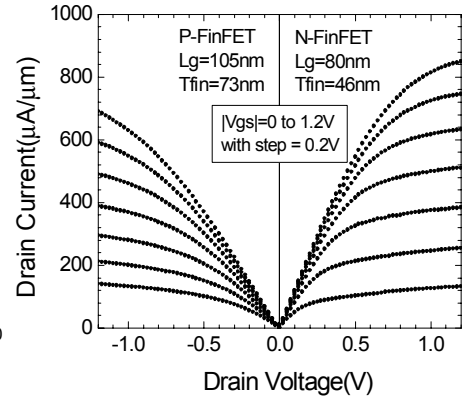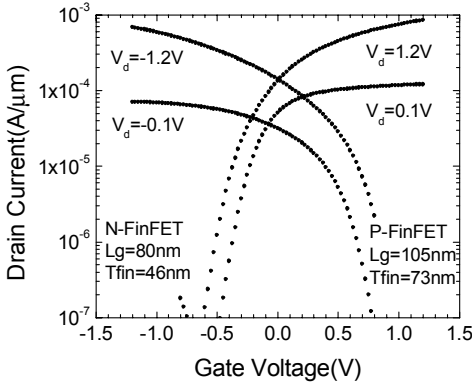

Fig.11 Long-channel FinFET Id-Vd characteristics.

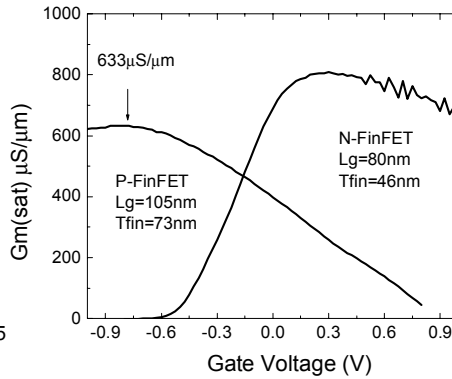**Fig.12** Long-channel FinFET subthreshold behavior.

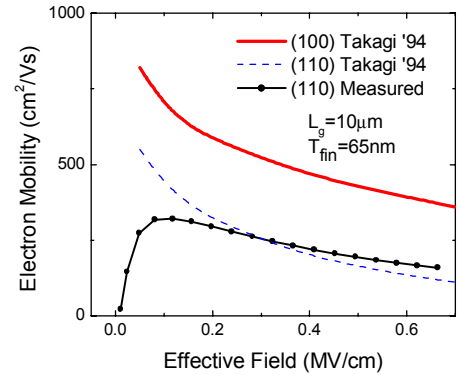**Fig.13** Long-channel FinFET transconductance measured at |Vd|=1.2V.

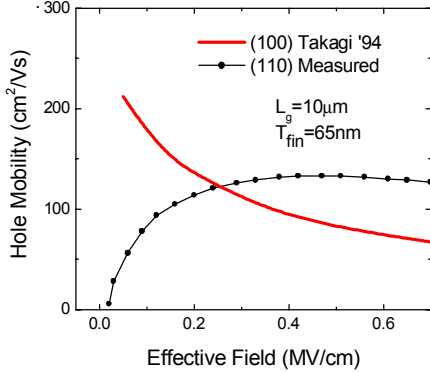**Fig.14** Electron mobility is reduced as the channel orientation is changed from (100) to (110) direction.

Fig.15 Hole mobility is increased as the channel orientation is changed from (100) to (110) direction.
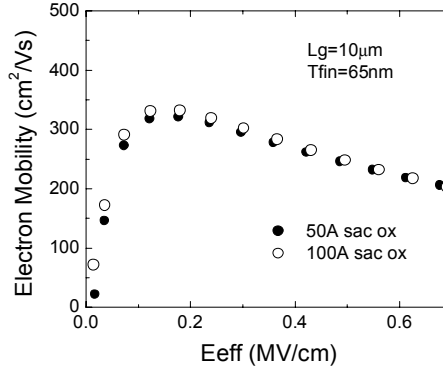
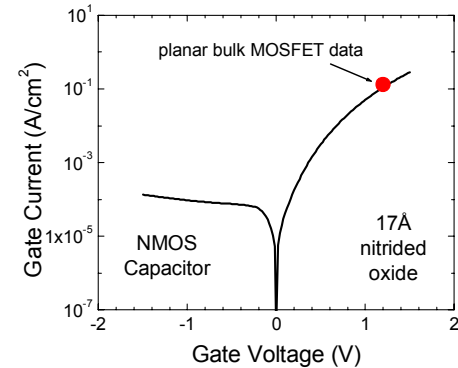**Fig.16** A 50Å sacrificial oxidation is enough to creat a clean gate oxide interface.

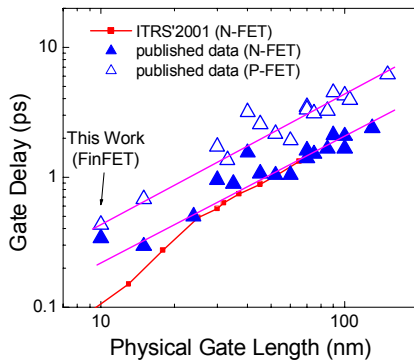**Fig.17** Direct tunneling leakage through ultra-thin gate oxide in n-channel FinFET.

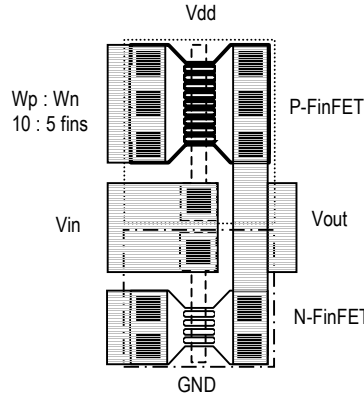**Fig.18** Gate intrinsic delay (CV/I) of FinFET compared with published planar CMOS transistors.

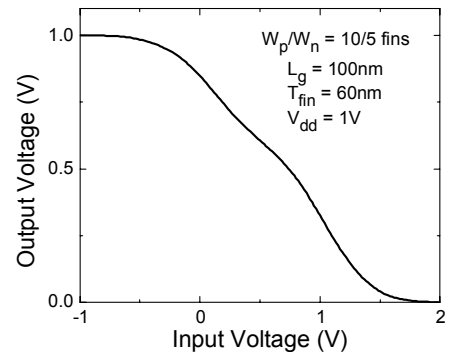**Fig.19** CMOS inverter made by FinFET with multiple-fin configuration.

Fig.20 Voltage transfer characteristics of CMOS FinFET inverter at a supply voltage of 1V.