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INTERRELATIONSHIPS OF TECHNOLOGY, SYSTEM PERFORMANCE, AND PRICE--ETC(U)
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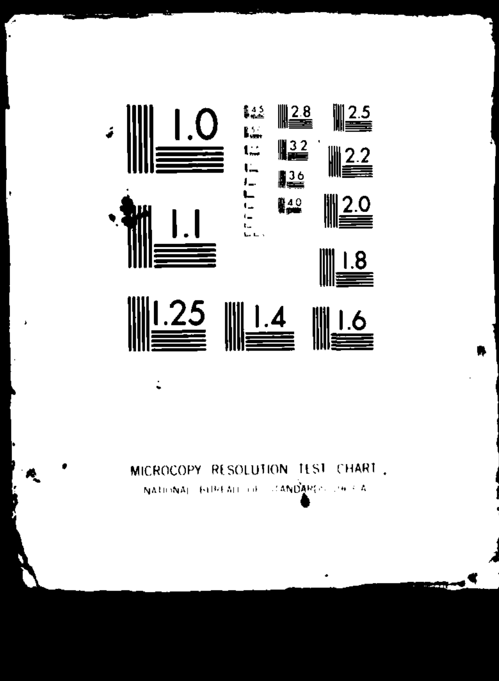

LEVEL II

INTERRELATIONSHIPS OF TECHNOLOGY, SYSTEM PERFORMANCE, AND PRICES FOR MINI/MIDICOMPUTERS

Edward H. Yates

August 1980

Presented at the Sixteenth Annual
DOD Cost Analysis Symposium,
5 October 1981, Arlington VA

Sponsored by: Office of the Secretary of the Army, Washington, D.C.

Held at: Sheraton Hotel, Arlington, VA

The views, opinions, and findings contained in this report are those of the author and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.

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1 SUMMARY

A study has been performed on the interrelationships of technology, prices, and performance of mini/midicomputers. The key functional characteristics and prices of 203 commercial and 13 military processors from 46 different manufacturers were compiled and analyzed. Multiple correlations among technology, performance characteristics, and prices were conducted by using a RAND Corporation multi-form regression analysis program called Curves. Although the variance statistics were somewhat poor, cost estimating relationships were developed from the data which can be used to estimate the "industry average" price of new mini-midicomputer configurations.

Differences between commercial and military versions are discussed. Typical military specifications are presented which show why military computers cost from 2 to 2.5 times more than their commercial counterparts.

The effect of technology on prices over the time period 1965 to 1980 is derived for both commercial and military processors. The results showed that technology did reduce prices of commercial computers approximately 15 to 26 percent annually, depending on the assumptions made about inflation and statistical manipulation. The corresponding results for military computers showed 20 to 43 percent annually.

2 INTRODUCTION AND STUDY OBJECTIVES

2.1 OBJECTIVES

Because technological advances in small computers have significantly reduced prices in data processing, it is necessary for BMDO* to update its assessment of state-of-the-art and technology projections for this type of equipment for incorporation in new BMD concepts and potential deployments. It is also necessary to assess the price differences between commercial and military equipment, because commercial equipment is often used as the baseline design for military counterparts. The objective of this study is to provide this information for use by the BMDO when examining new BMD concepts or systems.

In summary, this is a study of the interrelationships of small computer prices, technology, and performance.

2.2 TASKS

In order to accomplish the above objectives, the following tasks have been identified:

a. Review other survey efforts of small scientific-oriented computers to avoid duplication of study effort.
b. Collect available information on small computer capabilities and costs for both commercial and military versions.
c. Develop generalized cost estimating relationships (CERs) based on the tabulated data, identifying the relationships among processor and memory prices, performance, and technology.
d. Define cost factor differences between commercial and military computers.
e. Assess the technology impact on computer prices over the past 15 years.

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* Ballistic Missile Defense Organization (BMDO) is meant to include both the BMD Systems Command (BMDSCOM) and the Advanced Technology Center (ATC).

2.3 REPORT ORGANIZATION

The presentation of this report is organized to respond to the tasks identified in Section 2.2 above. Task a (survey review) and Task b (data collection) are discussed in this report's Section 4 (collection of data), while Task c (CER development), Task d (military versus commercial) and Task e (technology trends) are discussed in Section 5 (analysis of data). Section 6 of this report presents the study conclusions and recommendations.

2.4 CAVEAT

The reader should be cautioned that it would be unwise to rely solely on the information contained in this report except in a general way, i.e., this information should be regarded as a general data base on which selected price and technology trends can be identified. There is not universal agreement on some of the performance characteristics persented in this report, and it should be remembered that prices are peculiar to any specific situation and time period. Other causes of uncertainty are due to manufacturers' secrecy about their system performance and prices of their equipment, and inconsistent definitions and classifications of systems. Any serious consideration of selecting a particular computer configuration should be based on a detailed investigation of price and performance from the manufacturer.

However, on the positive side, an attempt has been made to record values as accurately as possible from more reliable sources and to engage in "cross-checking" values from alternate sources. In many cases, value judgements had to be made among conflicting estimates of physical, performance and economic characteristics.

3 DEVELOPMENT OF HYPOTHESES

3.1 CLASSIFICATION

The first issue to address is what types of computers should be included in this study. It was generally agreed that the emphasis should be on smaller computers because the larger types are better defined and well known, while the smaller ones with innovations in technology and manufacturing may offer better cost-effectiveness solutions for BMD. Unfortunately, classification schemes are plentiful but not universal. There is disagreement within the industry itself as to how to classify computers. Rigid definitions can be made on the basis of price, equipment complement, software support, applications support, flexibility, peripheral availability, work size, purpose, physical size, or combinations of these.

For purposes of this study of BMD computer technology, the classification problem was simplified so as to include a broad data base of available general purpose, digital, ground-based computers classified loosely as minicomputers and midicomputers. The main classification would be arbitrary price ranges where the central processor unit* (CPU) would, in most cases, cost less than $100,000. Although not important to the study results, arbitrary subgroupings could be made where: (a) minicomputer CPUs would usually have prices between $1,000 and $50,000 and usually have word lengths less than 32-bits, and (b) midicomputer CPUs would generally cost between $50,000 to $100,000 and usually have at least 32-bit word lengths.

Excluded from this study would be personal computers, special purpose microprocessors, space or airborne computers, and small business computers that would be inefficient for scientific or engineering applications, as well as the large-scale computers costing over $100,000.

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* A more precise hardware definition is presented in Section 3.2.

3.2 SCOPE

Before the scope of equipment covered by this study can be described, it is necessary first to discuss the definitions of terms in the next paragraph.

Processors are devices which perform or control a sequence of operations on data, and are closely tied to the main memory. Included in this category are central processing units (CPUs), input-output processors, and a variety of processor options such as floating point arithmetic units. The memory stores information, received through an input unit or developed during the processing of data, so that it can be brought from storage for use without being destroyed. Although classification schemes are many, there appears to be agreement on categorization into two kinds. One is main memory, also called working storage or internal memory/storage, and the other is mass storage or auxiliary memory/storage. The main memory holds the data directly manipulated by the arithmetic unit of the processor. Because of the speed of processing, the data must be readily available, so they are moved from mass storage into main memory.

Peripherals are the input-output devices (and auxiliary memory units) designed to provide the processors with data. Included in this category are magnetic tape units, line printers, punched card equipment, and moving-head and head-per-track disks and drums (and their controllers). Terminals, which are input-output devices connected to the processor, are sometimes classified as peripherals and sometimes in a separate category. Similarly, auxiliary memory or storage units can be classified separately or as peripherals.

For the purposes of this study, the major cost emphasis is on the processors (sometimes inaccurately abbreviated as "CPU" in this report) and its internal main memory. The price data which was collected not only included all types of processors (i.e., CPU, I/O, and hardware floating point) but also power supply, front panel, and minimum memory in the chassis.

Mass storage, peripherals, and terminals have been excluded from the scope. Multiprocessor configurations are also excluded. Most BMD tactical applications do not require vast amounts of peripherals, but when specific requirements are identified, this equipment would be costed on an ad hoc basis.

The time period considered for this analysis of prices, technology, and performance is between 1965 and 1980, with the major emphasis on the 1970 to 1980 decade.

3.3 PERFORMANCE EVALUATION

In selecting CPU performance measures for this study, it was necessary to conduct a library search. Several of the alternatives are discussed below:

a. Phister's Raw Speed. As noted in his recent publication*, Phister observes that "although it is hard to pick a single parameter to characterize CPU performance, the best choice is probably addition time, including memory access."

b. Knight's Performance Measure. Although quite old, this measure devised by K. Knight at Carnegie-Mellon Institute is still being discussed. It is somewhat more sophisticated as it simultaneously attempts to take into account arithmetic speed, memory size, memory word-length, and the degree of overlap permitted between the CPU and the I/O system. It also has different instruction mixes for commercial and scientific systems.

* Page 60, Data Processing Technology and Economics, Second Edition, by Montgomery Phister, Jr., Digital Press, 1979.

c. Other analytical techniques include those known as Grosch's Law, the Whetstone Technique, an approach by the Institute of Software Engineering, and a series of weighted MIP equations developed by Rein Turn of TRW for BMD applications.

d. Benchmarks for performance evaluation have been synthesized by a number of organizations including Auerbach and more recently TRW* for the Army BMDSCOM.

All of the analytical techniques mentioned in a. through c. appear to exclude such basic factors as the type of operating system and the job workload size and complexity. The most satisfying evaluation process would be to take the particular application required and run it on all the alternative computer systems, i.e., to use a benchmark representing the real application. Thus, a rational decision could be made on the time and cost to handle this specific type of workload and compare the performance of the alternate systems being considered. Although this approach is theoretically possible, it is impractical for this type of study emcumbered with limited resources.

Therefore, it seemed most practical and relevant to modify and use Turn's MIP equations, and these are discussed in the definitions in subsection 4.3 and in Appendix D.

3.4 SELECTION OF IMPORTANT CER VARIABLES

The question now is to hypothesize which independent variables have a "first-order" effect on processor price with a size-normalized internal main memory. Based on previous studies and discussions with experts, the following variables are selected for primary analysis:

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* Burns, I.F., et. al., Advanced Data Processing Technology, CDRL A004, TRW Report 32 304-6921-001, 16 January 1978.

a. First Delivery, year (Technology Surrogate)

b. Word Length, bits

c. Main Memory Type, core or semiconductor

d. Millions of Instructions Per Second (MIPS) which is a function of:

- Instruction Execution Times, microseconds
  - . Add
  - . Multiply/Divide
- Memory Cycle Time, microseconds

e. Maximum Memory Capacity, bits, which is a function of:

- Word Length, bits
- Maximum Memory Capacity, words

f. Floating Point Hardware, yes or no

So, there are six independent variables (later identified as X1 through X6) to be tested for correlation to processor price as the dependent variable (Y). The analysis is presented in Subsection 5.2.

Data was collected on additional variables which were hypothesized to only have "second-order" effects on price. These are:

g. Number of Accumulators

h. Direct Memory Access

i. Number of I/O Channels

j. Vector Interrupt

k. Minimum Memory Capacity, words

Definitions of all of the above variables are included in Subsection 4.3.

There was an additional set of features or options which are included as standard in some of the mini/midicomputers. They are listed below but not explicitly accounted for in this study because they are hypothesized to have "third order" effects on processor cost.

- Memory Management
- Hardware Memory Protection
- Memory Interleave Capability
- Cache Memory
- Microprogrammable
- Power Fail/Auto Restart
- Real Time Clock/Timer
- Battery Backup Power
- Multiprocessor Capability

3.5 MILITARIZATION PRICE DIFFERENTIALS

It is hypothesized that military specifications make military computers cost more than commercial computers. To test this hypothesis, the relevant military specifications will be identified, and a quantitative analysis will be made of price differentials, using both the general CER equations and case examples. This analysis in Subsection 5.4 should determine if the hypothesis is supported.

3.6 IMPACT OF TECHNOLOGY

The cost of a mini/midicomputer is influenced by a large number of factors as discussed in Subsection 3.4. The traditional CER development would attempt to relate cost to one or several of the equipment's physical and/or performance characteristics. However, in the case of mini/midicomputers, it is well known that innovations in design and manufacturing technology (and the competitive market place) are resulting in the availability of mini/midicomputers with steadily lower prices and increased capabilities. This leads to the hypothesis that technology must be a key variable in determining price and performance. It is further hypothesized that the first year of delivery of a new computer configuration would be the surrogate variable for technology.

In addition to including technology as a variable in the CER, a more detailed analysis is conducted on technology trends, i.e., how technology affects prices quantitatively over the 1965 to 1980 time period. It is hypothesized that technology reduces prices over time, and this is analyzed in Subsection 5.5.

4 COLLECTION OF DATA

4.1 REVIEW PREVIOUS SURVEYS

Many inquiries were made in the research community about available surveys that may be related to this investigation. Investigations were made, with the conclusion drawn that the other surveys did not include (a) all of the desired physical and performance characteristics data, (b) a clear enough explanation of the cost assumptions, or (c) a complete set of mini/midi computers of the relevant type for the time period of interest. The surveys investigated included those made by TRW, GRC, Aerospace Corporation, SDC, The RAND Corporation, Datamation, Byte, Auerbach, DataPro, and GML.

4.2 SOURCE OF DATA

The task of conducting a quantitative survey of mini/midicomputer costs and characteristics proved to be quite challenging as well as difficult. About 75 percent of the data was readily available but, in many cases, the missing data had to be painfully obtained from the designers or manufacturers. In some cases, estimates had to be made by manufacturers' representatives or by this study investigator, using the techniques of analogy or interpolation/extrapolation of similarly known information.

Consequently, it should be realized by users of this data that: (1) much of the data was obtained from secondary sources (DataPro's EDP Buyer's Bible, Auerbach Buyer's Guide, GML Minicomputer Review, and Datamation) and not always accurate, (2) some of the data was based on informed estimates from knowledgeable individuals, and again, not always completely accurate.

It is in this context that the data was assembled and tabulated. Large work sheets were designed which allowed space for recording input values from alternate sources (sometimes quite contradicting). Then, in some cases, judgements had to be made (with the assistance of experts) on which value was the most realistic.

The data sets were stratified into two groups -- 203 commercial and 13 militarized mini/midicomputers, for a total population of 216 data sets.

4.3 DEFINITION OF DATA AND VARIABLES

The data base which was collected and used to develop the cost/technology estimating relationships is presented in Appendix A. The key functional characteristics and costs of 203 commercial and 13 military mini/midicomputers from 46 different manufacturers are presented in these tables. For each CPU and system listed, complete sets of data were compiled except where noted as "optional." The optional data sets were incomplete and excluded from the regression analyses. These data should be regarded as supplementary information which might be utilized in future cost/technology investigations.

Definitions for the data tables follow:

1. Manufacturer. This is a 3-letter code to indicate the present manufacturer. Product lines and equipment acquired from prior owners are listed under the new owner's coding, e.g., Interdata computers are listed under Perkin Elmer, and Varian computers under Sperry Univac. The systems are grouped together by manufacturer, and their code symbols are defined in Appendix C.

2. Model. The particular computer system model name and number is listed in this column. Where a choice of CPU models was possible, its model designator is also given in parenthesis following the system designator.

3. First Year Delivery. This indicates the year when the first production model was delivered to a customer. The date of announcement is usually one to six months prior to that date. It is used as an important variable in this study as a surrogate for design and production technology. The last 2 digits of

the year are used as the input, e.g., "76" would be the equation input value to represent the year 1976.

4. Word Length. This is the computer's fundamental word length, expressed in bits. It is sometimes called data format size, memory bandwidth, or input/output bus width. It is the number of binary digits (bits) that can be stored in or retrieved from main storage during a single (clock) cycle. To this basic length has been added any parity bits or ERCC (error-correcting) bits. Parity checking usually requires the addition of one more bit to each main storage location. This added bit is set to the appropriate value whenever a word is written into main storage and checked each time the word is read out, permitting detection of most read and write errors. ERCC is a rather new form of error correction. It involves appending five or six check bits to each word of memory. The check bits, often called a Hamming code, and special algorithms allow a system to detect and correct single-bit errors and also to detect most multiple-bit errors that occur. In general, the longer the total word length, the greater the efficiency and accuracy of a computer's internal architecture and operations.

5. Add Time. This is the first of three possible variables which represent instruction execution times, expressed in microseconds. These are average timings for a full basic word, single precision, fixed point arithmetic-operands. In general, the indicated add times are the times required to retrieve a one-word operand from main storage and add it to another operand already contained in an accumulator, with no indexing or indirect addressing. It should be cautioned that even these times are not always directly comparable, due to the way the manufacturer performed the test, or because of differences in word lengths, instruction repertoires, or hardware architecture. It should also be noted that instruction execution speed depends on memory cycle time as well as the CPU's internal logic.

6. Multiply Time. This is the second of three possible variables which represent instruction execution times in microseconds. Many minicomputer applications impose little or no need for multiplication (or division) operations and therefore contain no multiply/divide hardware. In these cases, multiplication (and division) must be performed by means of programmed subroutines at a significant reduction in execution speeds. For machines with no hardware multiplication (or division), the time required for a programmed multiplication (or division) is recorded, if available.

7. Division Time. This is the last of three possible variables which represent instruction execution times in microseconds. The previous explanation in Variation 6 (above), Multiple Time, also applies here. These data are not used in the MIPS calculation.

8. MIPS. Millions of *Instructions Per Second.* The speed or rate at which adds, multiplies, or divides and memory cycles can be performed is the inverse of their execution times, converted to millions of instructions per second. By modifying the instruction mix formulas for BMD applications given by Dr. Rein Turn of TRW*, MIPS were calculated for each computer system. The choice of which formula to use depended upon the computer architecture (hardware multiply?; look ahead?) and upon the data available. The alternative formulas are presented in Appendix D.

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* See Appendix D for derivation and modification of these formulas.

9. Floating Point. A coding system has been devised to distinguish between those computer systems which hardware floating point is built-in and included in the CPU price, and those which do not have floating point or it is a cost-plus option. The coding is:

1. = No or Optional (no floating point)
2. = Yes (floating point included in CPU price)

Hardware floating point has not been included in the standard instruction repertoires of most of the currently available minicomputers, despite the fact that floating-point arithemtic is highly desirable, if not essential, in many scientific and BMD applications. However, there is an increasing tendency to include this feature as standard on many of the recent minicomputers, and while this feature now is rather costly*, the trend of including it as standard firmware may eliminate the differential cost as an option in the future.

10. DMA. The coding system is:

1. = No DMA capability or optional at extra cost
2. = Yes (DMA capability included in CPU price).

Direct Memory Access (DMA) is a method of data transfer using a hardware device that establishes a high-speed data path to link memory with peripheral devices. When a DMA channel is used, the I/O data bypasses the computer's main hardware registers and the I/O operation proceeds independently of program control once it has been initiated by the program. There is a growing trend to include this feature as standard. Although it is an important factor, it is considered to have a "second order" price effect, and therefore classified as an optional (no primary cost effect) variable in this study.

* Roughly $2,000 to $10,000 incremental cost.

11. Accumulators. The number of accumulators is considered an optional variable in this study because of its hypothesized "second order" cost effect, and also because the values could not be obtained for the complete data set without a costly investigation into each processor's internal architecture. However, it is recognized that the number of accumulators can have a significant effect upon internal flexibility and processing power. An accumulator is defined as a special type of hardware register which holds one operand and permits various arithmetic and logical operations to be performed upon it. In computers with multiple accumulators, instructions involving operands in two of the accumulators can often be executed more rapidly than instructions which require the retrieval of an operand from main storage.

12. I/O Channels. The number of I/O channels or ports is considered an optional variable in this study because of its hypothesized "second order" cost effect and because of the relative ease of expanding the number of I/O channels with I/O expanders and buses. For any particular computer system, the design goal is to have a balanced system which is neither I/O-limited or CPU computation-limited. For specific types of applications, one would add I/O channels (in buffered modes) until system throughput is maximized.* Further, it is rationalized that other considerations reduce the need to consider the number of I/O channels as a key cost-determining variable, e.g.,
    - DMA is a type of I/O channel which greatly facilitates I/O operations
    - I/O rate is equally as important as number of I/O channels
    - Maximum memory/storage capacity might be interrelated to number of channels.

* For a thorough discussion of I/O design, see: Phister, Montgomery, Jr., Data Processing Technology and Economics, Second Edition, Digital Press, December 1979.

13. Memory Type. The type of memory or storage generally falls into one of two basic categories, and the coding is as follows:

1. = Semiconductor (MOS or Bipolar)
2. = Core (or other)

Semiconductor memories are generally of two types -- metal oxide semiconductor (MOS) or bipolar transister (bipolar). MOS appears to be more popular for commercial applications because of its compactness, producability, and price. However, bipolar technology, a type of transistor-transistor logic, offers a classic tradeoff -- higher speed at the expense of more space, greater power consumed, and usually higher price. The type of MOS main memory considered in this study is Random-Access Memory (RAM), but other types are also often used in small systems and controllers, such as Read-Only Memory (ROM) and Programmable ROM (PROM). ROM is a memory containing permanently available, frequently used programs and data. It is designed and sequenced as it is manufactured and cannot be changed. With PROM, the programmer can decide on the subroutines, which are entered electronically at the beginning but are not easily changed.

Magnetic core storage has been widely used for the past ten years and has proved to be sufficiently fast, flexible, and reliable. Also, there are several advantages for using core for military applications, e.g., it is nonvolatile, i.e., if power is lost, the contents remain stable. Also included in this category is an older memory technology called "plated wire" used in a few of the early (pre-1970) small computers.

14. Memory Cycle Time. This is the minimum time interval, in microseconds, between two successive accesses to any one particular storage location. It is the time to read (and restore) a single word in memory.

Cycle times are directly related to the type (core versus MOS) and size (8K, 16K, etc.) of memory selected for the computer system. The cycle time values included in this study are those directly related to the type of memory selected, if this option was available.

15. Minimum Memory. This is the minimum capacity of the main memory/storage, in thousands of full words, of each particular computer. In most cases, this information was expressed in terms of bytes and had to be transformed to words to account for computers that do not utilize an 8-bit byte. The price for this memory is included in the unadjusted CPU price.

16. Maximum Memory. This is the maximum capacity of the main storage capacity of the main storage, expressed in thousands of full words, and is used as an indicator of minicomputer capability. The main memory is described by its word size and capacity. The word length is the amount of data that can be stored in one memory location, and the capacity is the total number of memory locations or words available. For this study, the maximum number of words is recorded, but this is later multiplied by word length to obtain the total cost impact in bits of a computer's capability, and used as variable X 5.

17. Memory Cost. This set of information provides data on memory economics, expressed in terms of cents per bit by type of memory. For some systems, processors are offered in several configurations, each having a different memory size. For these systems, cost per bit was calculated by examining the prices for various memory increments. In other cases, memory is offered as a separate increment or add-on memory, and the cost per bit was derived in this fashion. Memory cost is shown for each computer configuration and classified by type (semiconductor versus core) and time period (manufacturing technology).

18. Typical System Cost. The values shown are in thousands of "then year" dollars. This is an optional variable because of its peculiar nature, i.e., each application and customer may have unique preferences and requirements, so that any cost generalizations become difficult. The reason for including this "typical system cost" in the survey data is that it indicates the importance (and cost) of the peripherals. For BMD applications, the ratio of peripherals to CPU would be considerably smaller, and a "shopping list" approach would be used to selecte and price them.

19. CPU Cost. The values shown are in thousands of "then year" dollars. An attempt was made to normalize these figures to account for the same scope of costs for each system, i.e., the price to include CPU*, power supply, front panel, and minimum memory in the chassis (as identified in data set variable number 15). In general, an attempt was made to record the prices quoted during the first several years after a model was introduced. This is imprecise since there are two (but luckily countervailing) trends. First, inflation would tend to raise the prices as time progresses. But, secondly, the intense competitive market place would tend to force the manufacturers to lower their prices of the older models. The prices collected are associated with quantity buys of around 10 for identical configurations. Subsection 5.3 discusses how to make price-quantity adjustments.

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* And any other processors, e.g., I/O, floating point.

20. Adjusted CPU Cost*. This is an adjustment of the CPU cost shown in data set number 19 to normalize such that each CPU would have the same minimum memory of 8K words. This figure will act as the dependent variable in the regression analysis, along with tis word length acting as one of the independent variables. The adjusted CPU prices are analyzed and presented in 2 different ways -- non-inflated (then year dollars) and inflated (constant 1980 dollars). This is discussed further in Subsection 5.2.

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* The terms "cost" and "price" are used interchangeably in this report. The manufacturer's price is the Government's cost.

5 ANALYSIS OF DATA

5.1 CORRELATION ANALYSIS

The next step in the scientific method process is to test the hypotheses developed in Section 3 using the data described in Section 4 and contained in Appendix A.

After an assessment of available correlation analysis techniques, it was decided to utilize a multiple regression (curve-fitting) program* called "Curves" developed by H. E. Boren, Jr., and Captain G. W. Corwin at The RAND Corporation in 1976. "Curves" was designed as a cost analysis tool, although its potential scope of application goes far beyond this. The program provides least-squares fits for eight equations representing alternative functional forms, most of which permit up to seven independent variables. These equations are listed below:

1. <u>Linear</u>

   Y = A + B*X1 + C*X2 + ... + H*X7

2. <u>Quadratic</u>

   Y = A + B*X1 + C*X1**2

3. <u>Power</u>

   Y = A*(X1**B) * (X2**C) * ... * (X7**H)

4. <u>Asymptotic-Power</u>

   Y = A + B* (X1**C)

5. <u>Exponential</u>

   Y = EXP(A + B*X1 + C*X2 + ... + H*X7)

6. <u>Logarithmic-Linear</u>

   ALOG(Y) = ALOG(A) + B*ALOG(X1) + ... + H*ALOG(X7)

7. <u>Semilog-Linear - Log of dependent versus independent</u>

   ALOG(Y) = A + B*X1 + C*X2 + ... + H*X7

8. <u>Semilog-Linear - Dependent versus log of independent</u>

   Y = A + B*ALOG(X1) + [illegible]G(X2) + ... + H*ALOG(X7)

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* A full description and listing of the program appears in RAND Report R-1753-1-PR.

where:

Y = dependent variable

X1,X2,...,X7 = independent variables

A,B,...,H = parameters estimated by program

EXP = exponential function (e^X)

ALOG = natural logarithm function

It should be noted that only Equations 2 (Quadratic) and 4 (Asymptotic-Power) restrict the user to less than seven independent variables. Although Equation 6 (Log-linear) can be derived from Equation 3 (Power) by taking the log of both sides of 3, and likewise Equation 7 (Semilog-linear with log of dependent) can be derived from Equation 5 (Exponential), the parameters estimated by the equations will not be the same (except possibly for the case of perfect fit).

In addition to the estimates of the regression parameters, Curves calculates and prints various statistical measures of variance. The Curves report lists and defines these statistics. Included are the standard error of the estimate, standard deviation of the input variables, students' T-ratio, and Durbin-Watson statistic. Samples of the output sheets are presented in Appendix B.

Some of the statistical concerns stem from the fact that good statistical fits (e.g., high R^2 values) may not guarantee that the resulting CER will be meaningful and useful. The regression only reveals the best "mathematical fit." Therefore, in selecting the "best" CER among alternative equations, several factors have to be checked, including:

a. Are the mathematical signs ($\pm$) correct?

b. Are the CER coefficients meaningful?

c. Does the CER functional form support the hypotheses?

5.2 CER DEVELOPMENT

Separate multiple regressions were run for the commercial and military computers. As referenced before, the data for the regressions are contained in Appendix A. The statistical analyses and variance parameters for each of the selected regressions are presented in Appendix B.

Of the 150 total regression analyses run, the preferred 20 CERs are presented next, followed by an explanation of the alternative cases.

<u>COMMERCIAL PROCESSORS:</u>

a. 6 variables, uninflated $, semi-log, R^2 = .42

$\ell n\ C = 5.29 - .0643\ (X\ 1) + .01469\ (X\ 2) + .0691\ (X\ 3) + .774\ (X\ 4) + .00000241\ (X\ 5) + .717\ (X\ 6)$

$C^* = 12.5$

b. 6 variables, constant 80$, semi-log, R2 = .42

$\ell n\ C = 7.61 = .0908\ (X\ 1) + .0455\ (X\ 2) + .0813\ (X\ 3) + .731\ (X\ 4)$

$+ .0000023\ (X\ 5) + .708\ (X\ 6)$

$C^* = 16.9$

c. 5 variables, constant 80$, linear, R^2 = .43

$C = 118 - 2\ (X\ 1) + 1.53\ (X\ 2) + 18.4\ (X\ 4) + .0000336\ (X\ 5) + 19.8\ (X\ 6)$

$C^* = 25.6$

**d. 5 variables, constant 80$, power, R^2 = .46

$C = 1.4 \times 10^{12}\ (X\ 1)^{-6.56}\ (X\ 2)^{1.08}\ (X\ 4)^{.109}\ (X\ 5)^{.0476}\ (X\ 6)^{.974}$

$C^* = 26.7$

e. 4 variables, all with flt. pt. hdw., constant 80$, linear, R^2 = .36

$C = 138 - 1.94\ (X\ 1) + 1.65\ (X\ 2) + 25\ (X\ 4) + .0000705\ (X\ 5)$

$C^* = 30.6$

f. 4 variables, all with flt. pt. hdw., constant 80$, power, R^2 = .36

$C = 1.31 \times 10^{11}\ (X\ 1)^{-5.98}\ (X\ 2)^{.966}\ (X\ 4)^{.0845}\ (X\ 5)^{.113}$

$C^* = 34.4$

See Footnote on Page 5-6.

MILITARY PROCESSORS:

a. 6 variables, uninflated $, log-linear, $R^2 = .84$

$\ell n\, C = 36.1 - 11.1\, (\ell n\, X\, 1) + 4.61\, (\ell n\, X\, 2) + .489\, (\ell n\, X\, 3)$

$+ .175\, (\ell n\, X\, 4) + .351\, (\ell n\, X\, 5) + .498\, (\ell n\, X\, 6)$

$C^* = 33.5$

b. 6 variables, constant 80$, log-linear, $R^2 = .86$

$\ell n\, C = 51.6 - 14.8\, (\ell n\, X\, 1) + 4.9\, (\ell n\, X\, 2) + .414\, (\ell n\, X\, 3)$

$+ .237\, (\ell n\, X\, 4) + .340\, (\ell n\, X\, 5) + .768\, (\ell n\, X\, 6)$

$C^* = 43.1$

**c. 5 variables, constant 80$, power, $R^2 = .87$

$C = 7.05 \times 10^{25}\, (X\, 1)^{-17.6}\, (X\, 2)^{6.11}\, (X\, 4)^{.0174}\, (X\, 5)^{.437}\, (X\, 6)^{1.02}$

$C^* = 64.1$

d. 4 variables, all with flt. pt. hdw., constant 80$, linear, $R^2 = .60$

$C = 499 - 7.79\, (X\, 1) + 7.94\, (X\, 2) + 18.9\, (X\, 4) + .00359\, (X\, 5)$

$C^* = 54.4$

e. 4 variables, all with flt. pt. hdw., constant 80$, power, $R^2 = .57$

$C = 1.41 \times 10^{18}\, (X\, 1)^{-10.5}\, (X\, 2)^{1.92}\, (X\, 4)^{.0872}\, (X\, 5)^{.310}$

$C^* = 67.9$

f. 4 variables, all with flt. pt. hdw., constant 80$, log-linear, $R^2 = .69$

$\ln C = 46.3 - 13\, (\ell n\, X\, 1) + 4.33\, (\ell n\, X\, 2) + .405\, (\ell n\, X\, 4) + .324\, (\ell n\, X\, 5)$

$C^* = 48.4$

See Footnote on Page 5-6.

COMMERCIAL MEMORY (SEMICONDUCTOR):

a. 2 variables, uninflated \$, semi-log, $R^2 = .38$

$\ln C_m = 13.5 - .179\ (X\ 1) - .0655\ (X\ 2_m)$

$C_m^* = .85$

b. 2 variables, constant 80\$, linear, $R^2 = .33$

$C_m = 25.6 - .316\ (X\ 1) - .0636\ (X\ 2_m)$

$C_m^* = 1.48$

c. 2 variables, constant 80\$, semi-log, $R^2 = .46$

$\ln C_m = 16.6 - .216\ (X\ 1) - .0849\ (X\ 2_m)$

$C_m^* = 1.08$

COMMERCIAL MEMORY (CORE):

a. 2 variables, uninflated \$, exponential, $R^2 = .67$

$C_m = \text{Exp}\ [28 - .359(X1) - .996(X2_m)]$

$C_m^* = 2.16$

b. 2 variables, constant 80\$, linear, $R^2 = .39$

$C_m = 186 - 2.41\ (X\ 1) - 2.83\ (X\ 2_m)$

$C_m^* = 6.69$

c. 2 variables, constant 80\$, exponential, $R^2 = .68$

$C_m = \text{Exp}\ [28.9 - .365(X1) - .986(X2_m)]$

$C_m^* = 3.27$

See Footnote on Page 5-6.

MILITARY MEMORY (CORE):

a. 2 variables, constant 80$, linear, R^2 = .06

$C_m = 29.6 - .253\ (X\ 1) - 4.97\ (X\ 2_m)$

$C_m^* = 4.88$

b. 2 variables, constant 80$, exponential, R^2 = .09

$C_m = \text{Exp}\ [10.2 - .0879(X1) - 1.75(X2_m)]$

$C_m^* = 4.74$

where:

C = CPU Cost including power supply, front panel, and 8K words internal main memory, $thousands, for either uninflated or constant '80$ case.

C_m = Memory Cost per bit, cents, for either uninflated or constant '80$ case.

X1 = First Delivery, year (last 2 digits), where $65 \leq X1 \geq 80$.

X2 = Word Length, bits

$X2_m$ = Memory Cycle, microseconds

X3 = Memory Type, where 1 = semiconductor; 2 = core

X4 = Millions of Instructions Per Second (MIPS)

X5 = Maximum Memory (K words x word length), thousands of bits

X6 = Floating Point Hardware, where 1 = No or option; 2 = Yes

---

* C values are calculated using the "mean" X values shown in Appendix B.

** Preferred CERs to use; for add-on memory costs, use Table 1 instead of the CERs.

TABLE 1

DIFFERENTIAL MEMORY PRICES

	Typical Prices (cents per bit)		Differentials	
Year	Core	Semiconductor	Uninflated	Inflated
1964	4.5	2.5	2.0	3.3
1965	4.3	2.3	2.0	3.2
1966	4.0	2.2	1.8	2.8
1967	3.7	2.0	1.7	2.6
1968	3.6	2.0	1.6	2.5
1969	3.5	1.9	1.6	2.5
1970	3.2	1.8	1.4	2.2
1971	3.0	1.6	1.4	2.1
1972	2.7	1.5	1.2	1.8
1973	2.4	1.3	1.1	1.6
1974	2.1	1.2	0.9	1.4
1975	1.9	1.0	0.9	1.2
1976	1.6	0.9	0.7	0.9
1977	1.3	0.7	0.6	0.8
1978	1.1	0.5	0.6	0.7
1979	1.0	0.4	0.6	0.7
1980	1.0	0.4	0.6	0.7

The descriptors for the 20 preferred CERs will now be explained. The 6 variable case means that there were 6 independent variables (X1, X2, X3, X4, X5 and X6) correlated to the one dependent variable, C. Since many of these regression results were unsatisfying, it was then decided to search for better fits by eliminating certain variables that could be "normalized" by adjusting the data base properly. Hence, for the 5 variable cases, X3 (memory type) was dropped, and the memory was normalized such that all commercial computers had 8K words semiconductor memory, and all military computers had 8K words core memory. The adjustments were computerized by using the differential costs shown in Table 1 which were to be added or subtracted as appropriate. For the 4 variable cases, both X3 and X6 were dropped. The memory type (X3) was normalized as just described, and, in addition, the floating point option (X6) was normalized such that all computers had the hardware floating point capability. The algorithm used to add floating point is shown in Figure 1. The function, FPH$ = 3 + .067 (CPU$), is an "eyeball" fit to the data consisting of 16 commercial and military computer cases. This same cost function can be used to subtract floating point cost from the 4 variable cases, if desired.

The second descriptor is whether the case is uninflated or inflated (i.e., in constant 1980 dollars). Nornally, one would prefer the "constant dollar" case, but both cases are shown here because there is a price index problem; there appears to be no accurate price index series to properly adjust for inflation. Table 2 shows candidate price index series published by the Bureau of Labor Statistics (BLS) and Department of Defense (DOD). It is believed that the series in columns 4 and 5 are based on output factor prices*. It is hoped that column 3 (BLS Series 11.78) indexes are based on input factor (in the economic theory sense) differentials. As shown in

---

* In economic terms, output factors are finished goods prices, while input factors are prices of the basic resources used in production such as hourly labor cost, cost per pound of material, etc. In adjusting for price inflation, it would be preferable to use an index series based on input factors.

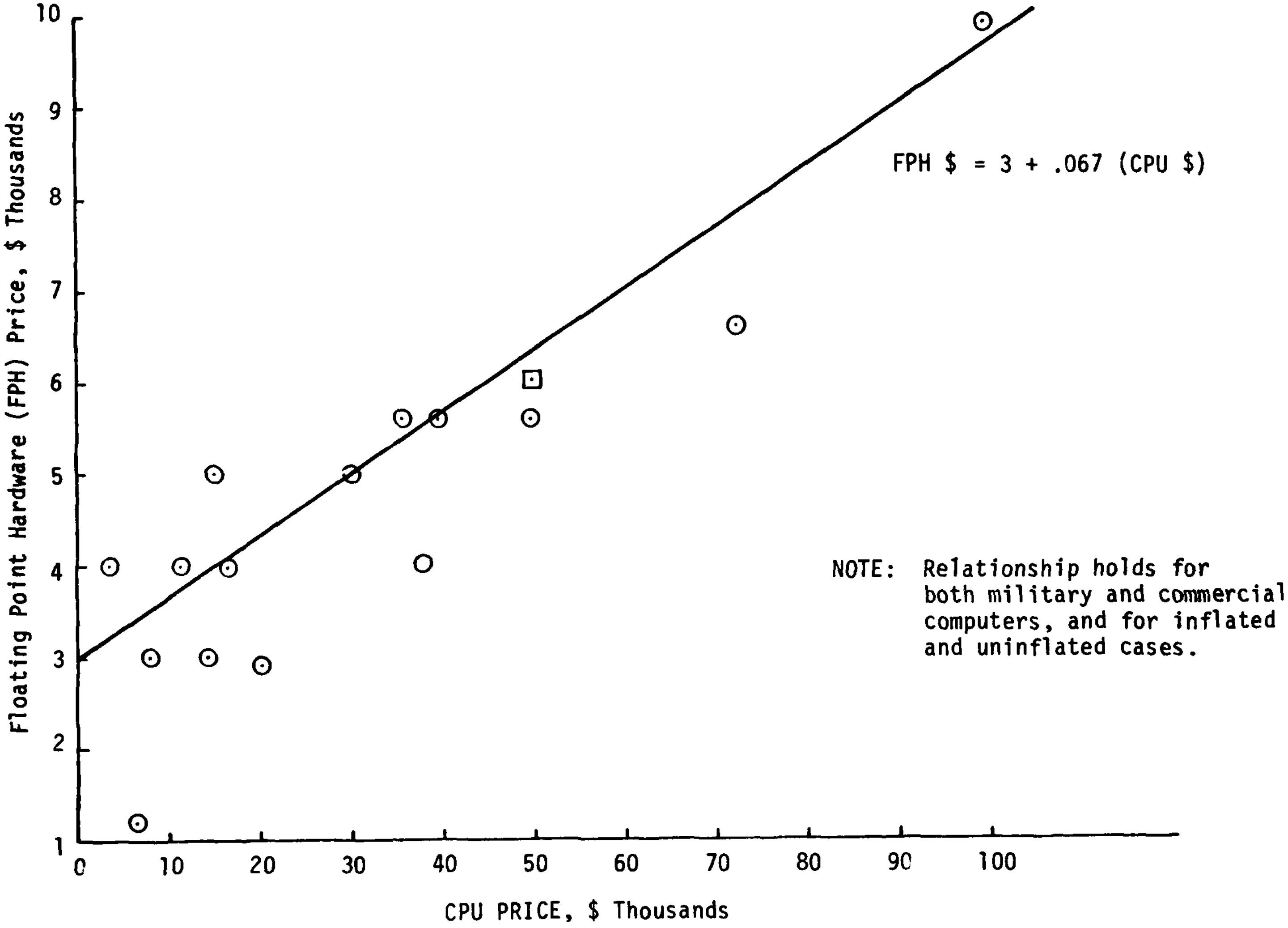


Figure 1. Floating Point Hardware Price Vs. CPU Price (Unadjusted $ Thousands)

TABLE 2

ALTERNATIVE PRICE INDEX SERIES

(1)	(2)	(3)	(4)	(5)	(6)
	BLS COMMODITY CODE			DOD	BLS
	11.7	11.78	11.7842		11.78
CAL. YEAR	ELECTRICAL MACH + EQPT	ELECTRONIC COM + ACCES	DIGITAL MOS ICs	COMPUTER PURCHASES(FY)	ADJUSTED TO 1980=0
1965	95.1	97.5(est)		36.3	62.4
1966	97.2	99.7		38.0	63.8
1967	100.0	100.0		39.9	64.0
1968	101.3	99.2		41.9	63.5
1969	102.9	100.7		42.8	64.5
1970	106.4	101.0		44.7	64.7
1971	109.2	102.4		46.8	65.6
1972	110.4	103.4		48.7	66.2
1973	112.4	104.4		50.4	66.8
1974	125.0	111.4		55.2	71.3
1975	140.7	115.5	77.7	62.9	73.9
1976	146.7	115.8	63.4	67.3	74.1
1977	154.1	119.5	59.4	72.1	76.5
1978	164.9	126.9	53.7	77.1	81.2
1979	178.9	135.8	51.2	84.0	86.9
1980	205.7(est)	156.2(est)	58.9(est)	91.8(est)	100.0

Table 3, the inflated results are particularly sensitive to the inflation rate selected. The BLS Series 11.78 was considered to be the most appropriate index, so it was normalized to where 1980 = 100 (column 6 of Table 2) and used for the inflated (constant 1980 dollar) cases.

The next descriptor stipulates the mathematical form of the equation (linear, power, exponential, etc.), and the last descriptor shows the value for R^2, Coefficient of Determination, on the statistical fit.

Care must be taken to interpret the proper independent variables when examining the computerized regression output sheets in Appendix B. For example, in the 5 variable cases, X5 is floating point option -- while in the 6 variable cases, X6 represents this variable. These variables have been standardized, however, in the equations stipulated in this Subsection.

Among the 20 equations presented in this Subsection, the two preferred CERs (for commercial processors and military processors) are marked with double asterisks. Also, these two preferred cases have complete computer printouts with all the related statistical information in Appendix B.

It should also be noted that complete definitions for the independent variables (X1 through X6) are presented in Subsection 4.3.

5.3 PRICE-QUANTITY ADJUSTMENTS

The CERs yield cost estimates for the same quantities implied in the data base. An attempt was made to collect price data that applied to single-buy procurements of around ten. According to the military manufacturers, the military equipments are seldom ordered in lots of much over ten of the exact same configuration. Whatever the quantity, the Government would probably receive their 9-10 percent GSA discount. For large purchases of like commercial equipment, substantial discounts (or quantity savings) are available, perhaps as high as 40 percent. In any event, the unit costs can be adjusted quite easily to reflect various types of procurements.

TABLE 3

VARYING INFLATION RATES

PRICE INDEX SERIES		1965→1979	1965→1980
DOD	COMPUTER PURCHASES	231%	253%
BLS	ELECTRONICS COMPONENTS & ACCESSORIES, SERIES 11.78	138%	160%
BLS	ELECTRICAL MACHINERY & EQUIPMENT, SERIES 11.7	188%	216%

5.4 MILITARIZATION REQUIREMENTS AND PRICES

Military computers are usually designed to meet a long list of environmental extremes which would seriously impact operation of a commercial mini/midicomputer. Although the military equipment is usually software and media-compatible with their Mil-Spec commercial counterparts, their design, packaging, production processes, and testing procedures are quite different. Additionally, the military versions are designed and packaged in such a way to be easily supportable in the field.

Most of the militarized computer systems are designed to meet all three of the key military specifications:

MIL-E-5400	Airborne
MIL-E-16400	Shipboard
MIL-E-4158	Land

A typical set of Mil-Specs might be as listed below:

<u>Standard Configuration - Case Temperature</u>

Standard:	0°C to +65°C
Wide:	-25°C to +75°C
Extreme:	-55°C to +95°C

<u>Vibration</u>

10g, 5-2000 Hz, with vibration isolators (MIL-E-5400, Curve 1Va); 2g, 5-2000 Hz, hard-mounted (MIL-E-5400, Curve 11a).

<u>Shock</u>

15g, 11ms operating; 30g, 11ms crash safety (MIL-E-5400).
High Impact shipboard equipment, (400 lb Hammer blow) per MIL-S-901, Grade A, Range 1 (Hardmount) (MIL-E-16400)

<u>Humidity</u>

95% relative

EMI Characteristics

MIL-STD-461 (400 Hz supply only)

Altitude

50,000 ft pressure altitude

Bench Handling, Explosive Atmosphere, Sand and Dust, Salt Spray and Salt Fog, and Fungus

per MIL-STD-810B

Power

+28 ± 8 Vdc ≤ 90 watts standard. Optional 400 Hz 115 Vac (per MIL-STD-704A, Category B)

Chassis Size

1/2 ATR (or 1 Full ATR)

Weight

____ lb with __K memory less I/O interfaces

In addition to the above, special electromagnetic pulse (EMP) and transient radiation effects (TRE) requirements may have to be met. Typical nuclear environment specifications might include the following elements and levels:

Radiation

Gamma dose rate: 10^8 Rad/Sec
Neutron fluence: 10^{12} n/cm^2
Total ionizing dose: 3000 Rad(Si)

EMP

Damped sine wave (500 V, 10 kHz to 100 MHz, Q = 25)

The differences in cost between commercial and military computers can be derived by using several different approaches:

(a) to use the separate CERs for commercial and military computers and to input the (differing) "mean" industry average values into the equations for various time periods;

(b) to, again, use the separate CERs for commercial and military computers but to input the same performance values into the equations for the mean year 1976; and

(c) to examine specific case examples and calculate an average factor differential.

All three of these approaches were used and the results are shown in Table 4. Using the alternative approaches, the resulting average factors were 2.2, 1.4, and 2.9. The simple average (mean) of these three is 2.2. It must be remembered that there are shortcomings in using any of these approaches. A conclusion might be drawn that a factor differential of 2 to 2.5 does not seem unreasonable.

5.5 TECHNOLOGY ANALYSIS

Since the euqations developed in Subsection 5.2 relate technology with prices and performance, it becomes possible to insert the performance values (industry means) into the estimating equations and calculate the resulting processor price separately for each year. This shows the effect that technology has on prices.

The problem is: what set of assumptions and which set of equations best represent the situation? Since there is a basic uncertainty about the inflation index, and several equation forms to consider, it was decided to calculate technology time versus price under varying conditions and regard the concomitant results as boundaries (i.e., calculate a range of possible values).

TABLE 4

COMMERCIAL VS. MILITARY COMPUTER PRICES

a. GENERALIZED EQUATIONS USING LINEAR, 6 VARIABLE, UNINFLATED EQUATIONS WITH SEPARATE "INDUSTRY AVERAGE" INPUTS:

	1965		1980
COMMERCIAL	$32K		$14K
MILITARY	$82K		$27K
DIFFERENTIAL PRICE FACTOR	2.6		1.9
AVERAGE MEDIAN FACTOR		2.2	

b. GENERALIZED EQUATIONS USING LINEAR, 6 VARIABLE, UNINFLATED EQUATIONS WITH COMMON "INDUSTRY AVERAGE" INPUTS:

	1976
COMMERCIAL	$32K
MILITARY	$44K
DIFFERENTIAL PRICE FACTOR	1.4

TABLE 4 (Con't)

c. CASE EXAMPLES USING CPU NORMALIZED PRICES (WITH 8KW MEMORY), INFLATED-CONSTANT 1980$:

	COMMERCIAL	MILITARY	FACTOR
DEC 11-34A	$11.7K		
UT NORDEN 11-34M		$53.2K	
PRICE DIFFERENTIAL			4.5
HONEYWELL 6/36	$8.9K		
HONEYWELL 6/36		$34.8K	
PRICE DIFFERENTIAL			3.9
DATA GENERAL ECLIPSE S-230	$16.2K		
ROLM MSE-20		$39.5K	
PRICE DIFFERENTIAL			2.4
DEC 11-70	$85.2K		
UT NORDEN M2-11/70A		$116.3K	
PRICE DIFFERENTIAL			1.4
DATA GENERAL NOVA 3/12	$5.7K		
ROLM 1603A (UYK-12)		$14.0K	
PRICE DIFFERENTIAL			2.4
AVERAGE MEAN FACTOR, $\frac{14.6}{5}$ =			2.9

Examples of results which can be calculated from the equations are shown in Figures 2, 3, and 4. Note that each figure shows results for both the uninflated and inflated (constant 1980$) cases. In Figure 2, the 4 variable case (top line) has floating point and semiconductor (MOS) memory for the commercial processors. It can be seen how the power functional form equation "crosses" the linear function at the mean year, 1976. As shown, the reduction in price from technology averages about 15 to 26 percent per year for these size computers.

Figure 3 shows similar results for the military processors but with the reduction in price from 20 to 43 percent annually. However, it should be kept in mind that there were no data for this curve prior to 1972.

Figure 4 is an example for commercial memory of the MOS type. Since the memory CERs were not statistically sound, it is recommended that the typical memory price values shown in Table 1 be used for technology analysis in lieu of the CER results.

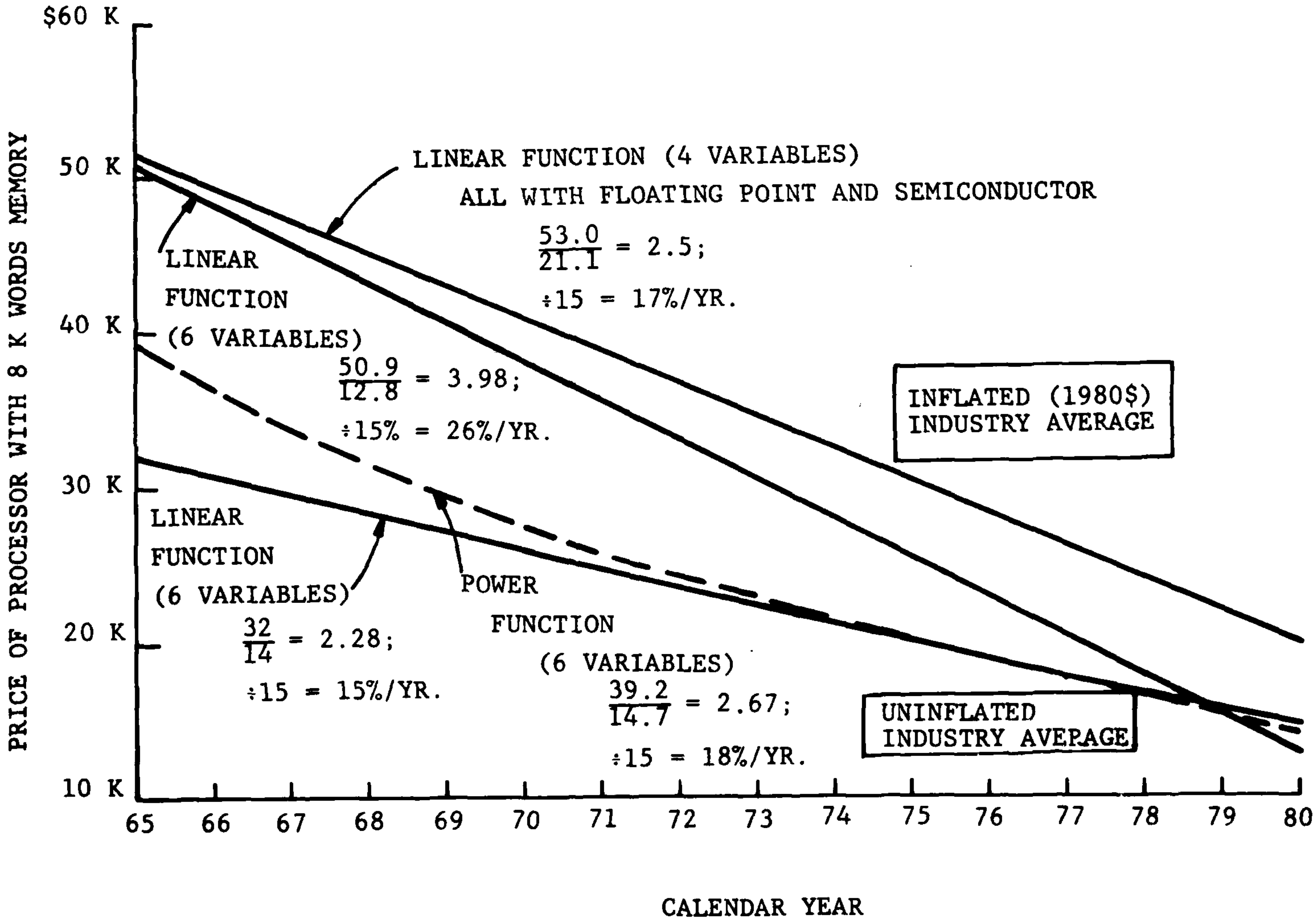


Figure 2. Technology Effect on Commercial CPU Price

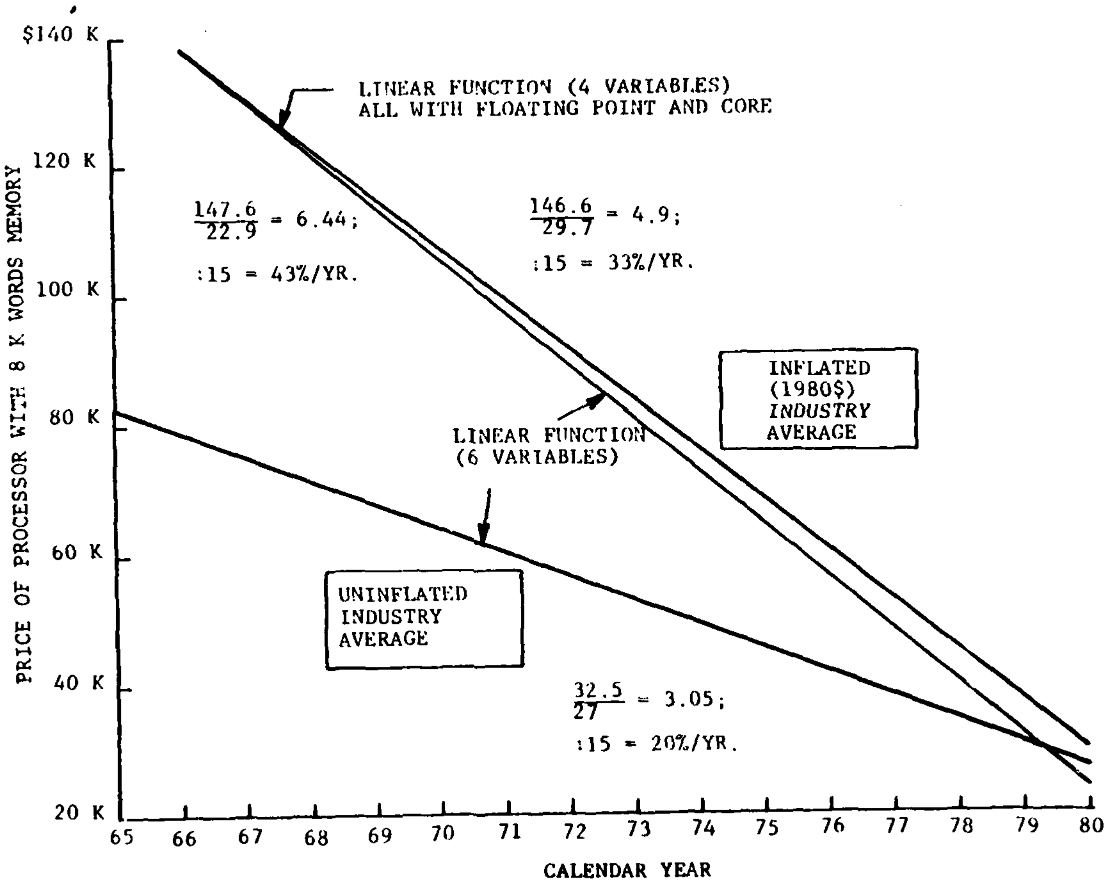


Figure 3. Technology Effect on Military CPU Price

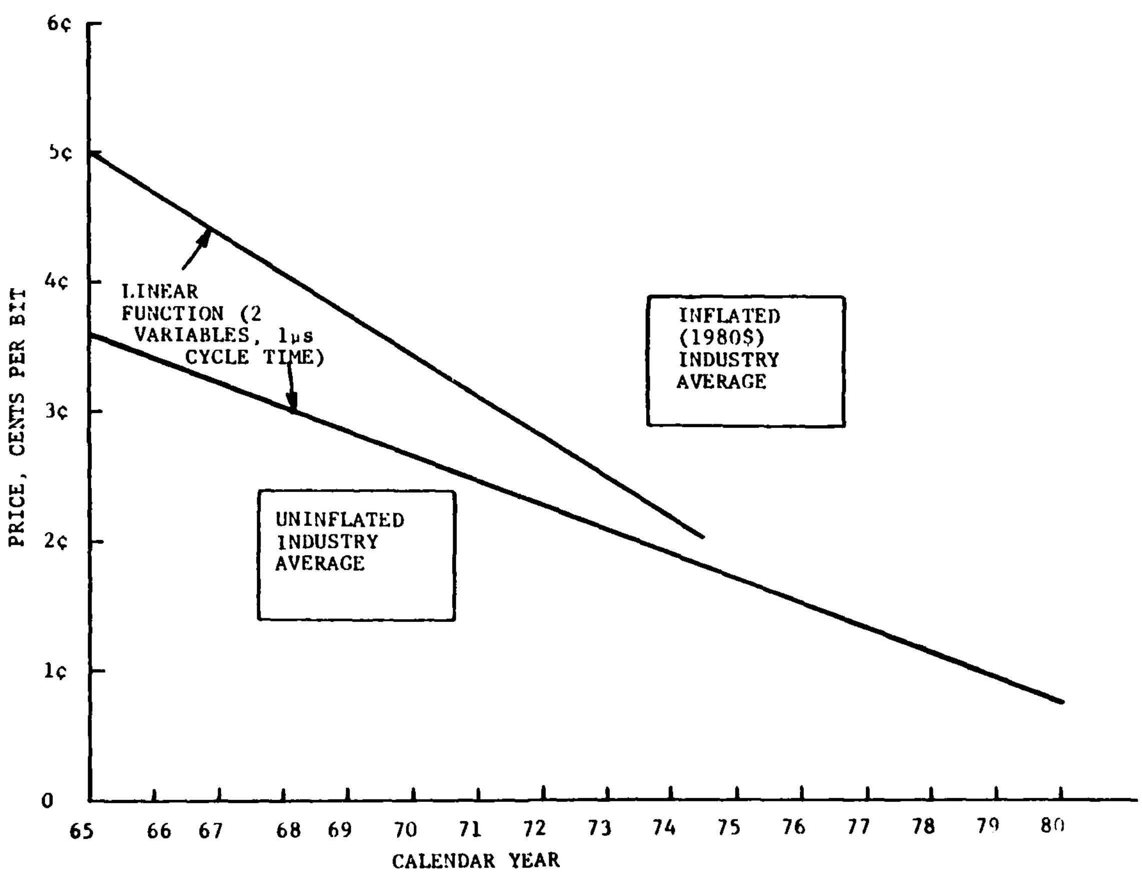


Figure 4. Technology Effect on Commercial Semiconductor Memory Price

6 CONCLUSIONS AND RECOMMENDATIONS

6.1 DATA BASE UPDATING

The key functional characteristics, technology year, and costs have been collected for 203 commercial and 13 military mini/midicomputers from 46 different manufacturers for the time period 1965 to 1980 and this data are included as Appendix A. This data should prove useful to the Army BMDO, and it is recommended that the data base be continuously improved and updated as newer configurations and models are introduced.

6.2 CER DEVELOPMENT

Cost Estimating Relationships have been developed for both commercial and military mini/midicomputers, and they are presented in Section 5.2. These can be used when a general purpose computer is needed in a technology or advanced concept study where precise computer specifications and performance criteria have not been completely defined.

The statistics of variance were adequately high for the military equipment (R^2 = .57 to .87) but quite low for the commercial mini/midicomputers (R^2 = .38 to .46). Although this was quite disappointing, it was not surprising considering the large number of different manufacturers that have become involved over the past decade in this complex market place. There is a very wide range of cost-performance ratios for equipment in the commercial market, ranging from low to high. This accounts for some of the disparity in the data. In either case, the estimating equations reflect the averages in the industry.

6.3 MILITARIZATION EFFECTS

From the set of military specifications included in Subsection 5.4, it can be seen why military computer versions cost more than their commercial counterparts. Several different approaches have been taken to quantify the price differential which ranged from 1.4 to 2.9. It was felt that a factor differential of 2 to 2.5 would not be unreasonable for early planning purposes, until specific designs and pricing have been accomplished.

6.4 TECHNOLOGY TRENDS

A number of different assumptions and approaches were taken. The results showed that technology reduced the price of commercial computers about 15 to 26 percent annually. The corresponding results for military computers showed 20 to 43 percent annually.

APPENDIX A

DATA BASE FOR COMMERCIAL AND MILITARY MINI/MIDICOMPUTERS

COMPUTER MFG. AND MODEL	FIRST DELIV YEAR	WORD LENGTH (BITS)	MICROSECS PER INSTRUCTION ADD	MULT.	DIVIDE	MIPS	FLOAT	DMA	NO. OF ACCUMS	NO. OF I/O CHNLS
AID SYSTEM 2000	75	16	1.2			.177	NO	YES	16	
AJI 1500	77	8	4.0			.061	NO	YES	128	
BUR B1705	76	24	.5	2.5		.522	NO	NO		10
BUR B1720-1	76	24	.33	1.6		.483	NO	NO		10
CAD SYSTEM 20	78	8	6			.037	NO	YES	1	
CAD SYSTEM 40/4	78	8	3.9			.059	NO	YES	1	
CDI CONCEPT 2	70	16	6.8			.041	NO	YES	15	
CDI CONCEPT 3	77	16	7.5			.034	NO	YES	16	
COP X1/35	74	16	4.2	12.9		.120	NO	YES	8	
COP CO135	73	16	2			.114	NO	YES	8	
CCC 200	69	8	1.6			.167	NO	YES	16	
CCC 300	71	8	2.6			.130	YES	NO	16	4
CCC 1000	77	16	2.6			.112	YES	YES	16	
CMC CIP/2200	71	8	12.5	65.5		.026	NO		32	
CMC CIP/2200B	74	8	10			.025	NO			
CAI LSI-2/10	73	18	4.1	14.8		.082	NO	YES	1	4
CAI LSI-3/05	75	16	6.2			.039	NO	YES	1	4
CAI LSI-4/90(MINI 4)	77	16	1.5	11.9	12.3	.175	NO	NO	2	8
CAI SYFA(15010)	76	16	2.4	12.8	15.1	.126	NO			
CDI OPUS 3	70	8	2	19.4		.108	NO			
CHI 2130	74	16	1.6			.178	NO	YES	8	32
CHI 3230	76	16	2.7			.106	NO	YES	8	32
CHI 4210	77	16	4.7			.079	NO	YES	16	4
CHI 4250	76	16	5.5			.103	NO	YES	16	16
CDC CYBER 18-17A	73	17	1.8	17.4	17.4	.121	YES	YES	2	
CDC CYBER 18-20	76	21	1.76	6.6	10.5	.202	NO	YES	6	
CDC CYBER 18-10M	75	17	1.76	6.6	10.5	.212	NO	YES	6	
CDC SYSTEM 17	75	17	1.8			.164	NO	YES		

COMPUTER MFG. AND MODEL	MEMORY CHARACTERISTICS TYPE	CYCLE (USECS)	SIZE(K WORDS) MIN	MAX	COST (¢/BIT)	SYSTEM COST ($K)	CPU COST ($K)	ADJUSTED CPU COST ($K) THEN YEAR $	1980 $
AIU SYSTEM 2000	SEMI	.6	4	32	.62		2.8	3.20	4.33
AJI 1500	CORE	.8	32	64	1.25		18.2	15.80	20.65
BUR B1705	SEMI	1	8	24	.23	126	26	26.00	35.09
BUR B1720-1	SEMI	.68	16	68	.23	150	67	66.56	89.82
CAD SYSTEM 20	SEMI	2.5	6	10	.5		5	5.08	6.26
CAD SYSTEM 40/4	SEMI	1.3	20	48	.5		7	6.52	8.03
CDI CONCEPT 2	CORE	1.2	16	64	.94	30	22	20.80	32.14
CDI CONCEPT 3	CORE	1	16	64	.94		26.9	25.70	33.59
COP X1/35	CORE	.76	8	64	.78		9	9.00	12.62
COP CD135	CORE	.68	8	128	.78		9	9.00	13.47
CCC 200	SEMI	1	32	512	2		16.5	12.66	19.63
CCC 300	SEMI	.6	8	32	1.25	32	17	17.00	25.91
CCC 1000	SEMI	1.2	64	256	.5		20	15.52	20.29
CMC CIP/2200	SEMI	1.1	8	64	3.4		6.7	6.70	10.21
CMC CIP/22003	SEMI	1.1	4	64	3.4		2.8	3.69	5.45
CAI LSI-2/10	CORE	.98	4	512	1.54	33	2.7	3.81	5.70
CAI LSI-3/05	SEMI	1.2	4	512	.86		.7	1.25	1.69
CAI LSI-4/90(MINI 4)	SEMI	.55	4	256	.36	12	1	1.24	1.63
CAI SYFA(15010)	CORE	1.2	32	524	.97	102	29	25.28	34.11
CDI OPUS 3	CORE	1	4	16	.94		3.5	3.60	5.87
CHI 2130	SEMI	.8	8	2048	.58		32	32.00	44.88
CHI 3230	SEMI	1.6	8	64	.58		15	15.00	20.24
CHI 4210	SEMI	.47	16	26	.6	17	13	12.23	15.99
CHI 4250	SEMI	.47	48	1024	.63		25	20.97	25.82
CDC CYBER 18-17A	SEMI	.9	4	64	3.69	65	11.2	13.71	20.52
CDC CYBER 18-20	SEMI	.75	16	128	1.95	137	15.3	12.02	16.23
CDC CYBER 18-10M	SEMI	.75	8	32	1.95	60	13.7	13.70	18.54
CDC SYSTEM 17	SEMI	.8	8	64	3.69		17.3	17.30	25.90

COMPUTER MFG. AND MODEL	FIRST DELIV YEAR	WORD LENGTH (BITS)	MICROSECS PER INSTRUCTION ADD	MULT.	DIVIDE	MIPS	FLOAT	DMA	NO. OF ACCUMS	NO. OF I/O CHNLS
CDC 3100(3114)	65	24	3.25			.086	NO			4
CSP CSP-30 (SIGNAL PROC)	69	16	.2			1.430	YES		32	
DGC NOVA 800	71	17	.8			.219	NO	YES	4	
DGC NOVA 820	71	17	.8			.219	NO	YES	4	
DGC NOVA 830	74	17	.8			.202	NO	YES	4	
DGC NOVA 840	74	17	.8			.219	NO	YES	4	
DGC NOVA 1200	70	17	1.2			.146	NO	YES	4	
DGC NOVA 1210	72	17	1.2			.146	NO	YES	4	
DGC NOVA 1220	72	17	1.2			.146	NO	YES	4	
DGC MICRONOVA 8560	77	16	2.4	41.28	59.04	.063	NO	YES	4	
DGC MICRONOVA 8561	77	16	2.4	41.28	59.04	.063	NO	YES	4	
DGC MICRONO MP/100 8520A	79	16	2.4	41.28	59.04	.063	NO	YES	4	
DGC MICRONO MP/200 8670D	79	16	.84	4.92	5.52	.326	NO	YES	4	
DGC NOVA 2/4	73	17	.8			.219	NO	YES	4	
DGC NOVA 2/10	73	17	.8			.219	NO	YES	4	
DGC NOVA 3/4(8478)	76	17	.7	5.8	6.5	.135	NO	YES	4	
DGC NOVA 3/12(8466)	76	17	.7	5.8	6.5	.135	NO	YES	4	
DGC NOVA 3/D(8584)	76	17	.7	5.8	6.5	.275	NO	YES	4	
DGC NOVA 4/C(8350G)	79	17	.2	4.4	5.4	.182	NO	YES	4	128
DGC NOVA 4/S(8352G)	79	17	.2	4.4	5.4	.182	NO	YES	4	128
DGC NOVA 4/X(8394K)	79	17	.2	4.4	5.4	.182	NO	YES	4	128
DGC ECLIPSE S/100	75	21	.2			1.110	NO		4	
DGC ECLIPSE S/200	75	21	.2			1.110	NO		4	
DGC ECLIPSE C/300	75	21	.2			1.110	NO		4	
DGC ECLIPSE S/130(8610G)	77	21	.6	7.2	8.2	.251	NO	YES	4	
DGC ECLIPSE S/230(8597G)	76	21	.6	7.2	8.2	.239	NO	YES	4	
DGC ECLIPSE C/330(8599H)	76	21	.6	7.2	8.2	.239	YES	YES	4	
DGC ECLIPSE M/600(8630N)	76	21	.6	7.2	8.2	.279	YES	YES	4	

COMPUTER MFG. AND MODEL		MEMORY CHARACTERISTICS TYPE	CYCLE (USECS)	SIZE (K WORDS) MIN	MAX	COST (¢/BIT)	SYSTEM COST ($K)	CPU COST ($K)	ADJUSTED CPU COST ($K) THEN YEAR $	1980 $
CDC	3100(3114)	CORE	1.75	4	32	9.66	726	45	54.27	86.90
CSP	CSP-30 (SIGNAL PROC)	CORE	.1	4	128	37.2	160	35	58.81	91.18
DGC	NOVA 800	CORE	.8	8	32	1.95	66	7.4	7.40	11.28
DGC	NOVA 820	CORE	.8	8	64	1.55	70	7.5	7.50	11.43
DGC	NOVA 830	CORE	1	16	128	.69		12.65	11.73	16.44
DGC	NOVA 840	CORE	.8	16	128	.68	55	16.53	15.81	21.89
DGC	NOVA 1200	CORE	1.2	4	32	2.81	44	5.1	7.01	10.84
DGC	NOVA 1210	CORE	1.2	4	32	1.41	43	4	4.96	7.49
DGC	NOVA 1220	CORE	1.2	4	48	1.41	44	4.9	5.86	8.85
DGC	MICRONOVA 8560	SEMI	.96	2	32	.74		2.6	3.31	4.33
DGC	MICRONOVA 8561	SEMI	.96	2	32	.74	12	2	2.71	3.54
DGC	MICRONO MP/100 8520A	SEMI	.96	4	64	.74		1.7	2.17	2.50
DGC	MICRONO MP/200 8670C	SEMI	.5	16	32	.74		3.7	2.75	3.17
DGC	NOVA 2/4	CORE	.8	4	32	1.56	42	3.5	4.56	6.83
DGC	NOVA 2/10	CORE	.8	8	64	1.56	43	4.4	4.40	6.59
DGC	NOVA 3/4(8478)	SEMI	.7	4	32	.93	35	2.6	3.23	4.36
DGC	NOVA 3/12(8466)	SEMI	.7	4	128	.93	44	3.6	4.23	5.71
DGC	NOVA 3/D(8564)	CORE	.7	32	128	.53	60	14.4	10.61	14.31
DGC	NOVA 4/C(83906)	SEMI	.4	16	32	.27		2.8	2.43	2.80
DGC	NOVA 4/S(8392G)	SEMI	.4	16	32	.23		5.8	5.49	6.31
DGC	NOVA 4/X(8394K)	SEMI	.4	64	128	.26		10.4	7.92	9.12
DGC	ECLIPSE S/100	CORE	.2	8	64	2.89	70	11.2	11.20	15.16
DGC	ECLIPSE S/200	CORE	.2	16	128	2.89	78	19.3	14.44	19.55
DGC	ECLIPSE C/3[illegible]	CORE	.2	32	128	2.89	125	37.7	23.13	31.31
DGC	ECLIPSE S/130(8610G)	CORE	.7	8	128	1.76	60	9.2	9.20	12.03
DGC	ECLIPSE S/230(8597G)	CORE	.8	16	256	1.76	135	15	12.09	16.25
DGC	ECLIPSE C/330(8559H)	CORE	.8	32	256	1.76	110	30	21.13	28.51
DGC	ECLIPSE M/600(8630H)	SEMI	.5	32	1024	1.17	275	62	56.10	69.09

COMPUTER MFG. AND MODEL		FIRST DELIV YEAR	WORD LENGTH (BITS)	MICROSECS PER INSTRUCTION ADD	MULT.	DIVIDE	MIPS	FLOAT	DMA	NO. OF ACCUMS	NO. OF I/O CHNLS
DGC	C/150 ECLIPSE	79	21	.6	4	5.85	.495	YES	YES	4	
DGC	S/250 ECLIPSE	79	21	.54	6.5	7.4	.366	YES	YES	8	
DGC	C/350 ECLIPSE	79	21	.6	4	5.85	.495	YES	NO	8	
DGC	MV/8000 ECLIPSE	80	39	.22			1.190	YES	YES	8	57
DPC	1500	77	8	1.8			.126	NO	NO	2	
DPC	1800	70	8	3.8			.065	NO	YES	2	
DPC	2200	72	8	3.2			.066	NO	YES	14	
DCC	D-116H	72	16	1.0	3.0	3.2	.250	NO	YES	4	62
DEC	PDP-8/A	74	12	4.5	7.4		.122	NO	YES	1	64
DEC	PDP-11/03	76	18	3.5			.090	NO	YES	6	
DEC	PDP-11/04	75	18	3.17	9.9	11.3	.140	NO	YES	6	
DEC	PDP-11/35	74	18	1.07	9.16	11.58	.183	NO	YES	6	4096
DEC	PDP-11/44	80	18	.87			.363	NO	YES	8	
DEC	PDP-11/45	72	18	.97	3.89	8.39	.263	NO	YES	12	
DEC	PDP-11/60	77	18	2.2			.134	YES	YES	8	
DEC	PDP-11/70	75	18	.4	3.4	7.9	.307	NO	YES	8	
DEC	PDP-11/34A	76	18	2.03	8.9	12.6	.180	NO	YES	8	
DEC	VAX-11/780	78	32	.4			.735	YES	YES	16	
DGI	SYSTEMS	76	8	2.5			.070	NO	YES	16	
DSC	4030	70	18	2.9			.066	YES	YES	14	
DSC	5010	72	18	1.44			.217	NO	YES	2	
DSC	META 4	70	18	1.37			.226	NO	YES		
DSY	MODEL 130	76	8	.3			.571	NO	YES	10	
FAI	F6400	79	64	6.0			.043	YES	YES	256	
GAI	16/40	70	16	1.4	12.6	23.1	.132	NO	NO	3	
GAI	16/110	76	17	2.4	19.5	19.5	.117	NO	YES	6	
GAI	16/220	76	18	2.1	19.5	19.5	.115	NO	YES	6	
GAI	16/330	76	18	1.9	18.45	18.45	.120	NO	YES	6	

COMPUTER MFG. AND MODEL	MEMORY CHARACTERISTICS					SYSTEM COST ($K)	CPU COST ($K)	ADJUSTED CPU COST ($K)	
	TYPE	CYCLE (USECS)	SIZE (K WORDS) MIN	SIZE (K WORDS) MAX	COST (¢/BIT)			THEN YEAR $	1980 $
DGC C/150 ECLIPSE	CORE	.2	64	512	1.17	75	34	20.24	23.29
DGC S/250 ECLIPSE	CORE	.2	32	1024	1.17	140	30	24.10	27.74
DGC C/350 ECLIPSE	CORE	.2	32	1024	1.17	133	49	43.10	49.60
DGC MV/8000 ECLIPSE	SEMI	.145	128	512	.34	165	106.4	90.49	90.49
DPC 1500	SEMI	.65	32	32	.75	17	5.95	4.51	5.90
DPC 1800	SEMI	.63	64	64	.6	19	5.5	2.81	3.46
DPC 2200	SEMI	1.6	4	16	2.0	40	8.6	9.24	13.96
DEC D-116H	SEMI	1.2	8	64	1.5	20	7.0	7.00	10.57
DEC PDP-8/A	CORE	1.4	1	16	2.97	10	1.84	4.33	6.08
DEC PDP-11/05	CORE	1.15	4	32	.77	15	2.0	2.55	3.45
DEC PDP-11/04	CORE	.98	8	32	.66	20	4.0	4.00	5.41
DEC PDP-11/35	CORE	.98	16	128	.43	30	19.8	19.18	26.90
DEC PDP-11/44	SEMI	.29	256	1024	.29		23.9	10.95	10.95
DEC PDP-11/45	CORE	.98	32	128	.43	42	39.6	37.74	57.01
DEC PDP-11/60	CORE	.98	32	256	.65	100	35.7	32.69	43.00
DEC PDP-11/70	CORE	.98	64	1024	.43	120	67.3	62.97	85.20
DEC PDP-11/34A	SEMI	.98	16	128	.625	51.9	9.1	6.20	11.07
DEC VAX-11/780	SEMI	.5	32	512	.625	180	99.7	94.90	116.87
DGI SYSTEMS	SEMI	2.5	16	64	.27		2.0	1.96	2.64
DSC 4030	CORE	4.0	8	128	3.12		33.85	33.85	52.32
DSC 5010	SEMI	.5	4	32	1.56		18.0	19.12	28.89
DSC META 4	SEMI	.5	8	64	1.56	55	21.25	21.25	32.84
DSY MODEL 130	SEMI	.5	64	128	1.76	57	34.7	26.82	36.19
FAI F6400	SEMI	.5	32	3750	.4		68.7	62.56	71.99
GAI 16/40	CORE	1.4	4	32	3.12	36	5.55	7.55	11.66
GAI 16/110	SEMI	.5	2	64	1.27		2.1	3.40	4.58
GAI 16/220	SEMI	.7	2	32	1.41	10	2.29	3.81	5.15
GAI 16/330	CORE	.72	4	32	1.27	36	4.45	5.36	7.24

COMPUTER MFG. AND MODEL	FIRST DELIV YEAR	WORD LENGTH (BITS)	MICROSECS PER INSTRUCTION ADD	MULT.	DIVIDE	MIPS	FLOAT	DMA	NO. OF ACCUMS	NO. OF I/O CHNLS
GAI 16/550	77	18	.48			.454	NO	YES	6	
GAI 16/460	78	18	.78			.285	NO	YES	6	
GAI 16-60/65	71	16	.96	5.28		.239	NO			64
GAI 16-80/85	71	16	.8	4.4		.287	NO			64
GRI 99/50	76	18	1.76	68.0		.040	NO	YES	8	4096
GRI 99/30	72	16	1.76	68.0		.040	NO			4096
HCP SLASH 4-1	73	26	1.5			.230	NO	NO	5	
HCP SLASH 6	76	29	1.2			.320	NO	NO	5	
HCP SLASH 7	75	26	1.1			.377	NO	NO	5	
HCP H600	80	48	.135			1.090	YES	YES	5	128
HCP H100(110-SLASH 4)	77	26	1.5			.190	NO	YES	5	32
HCP H200(210-SLASH 7)	77	26	1.12			.241	YES	YES	5	
HPC HP2100A/S	71	16	1.96	10.8		.152	NO			14
HPC HP21MX	74	16	1.94	13		.152	YES			14
HPC HP1000M(2108)	74	17	1.9	12.5	16	.157	NO	NO	2	56
HPC HP300	79	22	1.98			.166	YES	YES		16
HPC HP3000-III	78	22	.55	5.25	6.12	.298	YES	YES	20	9
HPC HP3000-33	79	22	.45			.351	YES	NO	13	7
HPC HP3000-30	80	22	.45			.351	YES	NO		2
HON 115(116)	70	30	66			.006	NO	NO	6	3
HON 2020(2021-1)	72	30	47.5			.008	NO	NO	15	3
HON 6/33	76	18	1.9	12.7	17	.155	NO	YES	7	160
HON 6/43	77	18	1			.263	NO	YES	7	160
HON 6/57	78	18	.79			.505	NO	YES	7	160
HON 6/23	78	18	1.9	12.7	17	.140	NO	YES	7	12
HON 6/4X	76	18	1			.263	YES	YES		
HON 6/47	76	18	.4			.435	NO	YES		160
HON 6/53	78	18	1.4			.206	NO	YES		160

COMPUTER MFG. AND MODEL		MEMORY CHARACTERISTICS TYPE	CYCLE (USECS)	SIZE (K WORDS) MIN	SIZE (K WORDS) MAX	COST (¢/BIT)	SYSTEM COST ($K)	CPU COST ($K)	ADJUSTED CPU COST ($K) THEN YEAR $	ADJUSTED CPU COST ($K) 1980 $
GAI	16/550	SEMI	.5	64	1024	1.86	100	43.	24.25	31.70
GAI	16/460	SEMI	.76	16	1024	1.86	40	6.8	4.12	5.08
GAI	16-60/65	CORE	.56	4	128	3.3	12	6.6	8.71	13.28
GAI	16-80/85	CORE	.8	4	128	3.6	15	8.6	10.90	16.62
GRI	99/50	SEMI	1.76	8	32	1.52	40	6.41	6.41	8.65
GRI	99/30	CORE	1.76	8	32	1.52		5.5	5.50	8.31
HCP	SLASH 4-1	CORE	.75	8	256	3.64		24	24.00	35.93
HCP	SLASH 6	SEMI	.45	16	256	1.43		20.5	17.18	23.19
HCP	SLASH 7	CORE	.675	32	256	3.91		55	30.60	41.41
HCP	H600	SEMI	.29	64	512	.19	384	165.9	160.79	160.79
HCP	H100(110-SLASH 4)	CORE	.75	32	256	3.18	85	45	25.16	32.88
HCP	H200(210-SLASH 7)	CORE	.675	64	256	3.91	179	161	104.07	136.04
HPC	HP2100A/S	CORE	.98	4	32	3.12	45	7.2	9.20	14.02
HPC	HP21MX	SEMI	.65	4	64	.55		5.95	6.30	8.84
HPC	HP1000M(2108)	SEMI	.65	8	1024	.55	51	7.4	7.40	10.38
HPC	HP300	SEMI	.5	64	256	.24	75	35	32.04	36.87
HPC	HP3000-III	SEMI	.7	128	1024	.28	115	75.9	68.51	84.37
HPC	HP3000-33	SEMI	.86	128	512	.39	76	37.2	26.90	30.96
HPC	HP3000-30	SEMI	.86	128	1024	.39	50	28.5	16.20	18.20
HON	115(116)	CORE	2.75	3	6	2.7	166	50	54.05	83.54
HON	2020(2021-1)	CORE	2.5	5	13	2.7	116	30	32.43	48.99
HON	6/33	SEMI	.65	8	64	.68	47	5.86	5.86	7.91
HON	6/43	SEMI	.65	16	1024	.68	97	9.79	8.81	11.52
HON	6/57	SEMI	.65	16	1024	.68	217	45.74	44.76	55.12
HON	6/23	SEMI	1	16	64	.57	22	5.55	4.73	5.82
HON	6/4X	SEMI	.65	8	1024	.5	29	6.4	6.40	8.64
HON	6/47	SEMI	.65	16	1024	.5	209	21.74	21.02	25.89
HON	6/53	SEMI	.65	16	1024	.5	147	21	20.28	24.98

COMPUTER MFG. AND MODEL	FIRST DELIV YEAR	WORD LENGTH (BITS)	MICROSECS PER INSTRUCTION ADD	MULT.	DIVIDE	MIPS	FLOAT	DMA	NO. OF ACCUMS	NO. OF I/O CHNLS
HON 6/06	76	18	2	8.8	10	.187	NO	YES		
HON 6/34	76	16	1.9	12.7	17	.133	NO	YES	7	
HON 6/36	76	16	1.9	12.7	17	.133	NO	YES	7	
IBM SYSTEM/34(5340)	78	16	68.5			.075	NO	YES		64
IBM SYSTEM/32(5320)	75	8	150.0			.004	NO	YES	16	
IBM 5100	75	16	1000			.001	YES	YES		1
IBM 360 MOD 20(2020,B1)	64	16	473			.001	NO	YES	8	
IBM 360 MOD 20(2020,B3)	68	16	739			.001	NO		8	
IBM 360 MOD 20(2020,C5)	68	16	160			.004	NO		8	
IBM 360 MOD 20(2020,C6)	71	16	289			.002	NO		8	
IBM 1800-2	66	16	4.5	15.25		.082	NO		8	
IBM 1130	65	18	6	15.7	76	.068	NO	NO	1	
IBM 8130	79	32	3.2			.091	NO		19	
IBM 8140	80	32	1.6			.178	NO		19	
IBM SYSTEM/7(5010,A8)	71	18	800			.001	NO		1	
IBM SYS/3-8(5408)	75	8	24.32			.027	NO	YES	8	
IBM SYS/3-12(5412)	76	8	24.32			.027	NO	YES		
IBM SYS/3-6(5406)	71	8	24.32			.055	NO	YES	1	
IBM SYS/3-10(5410)	70	8	24.32			.027	NO	YES	8	
IBM SYS/3-4(5404)	76	8	24.32			.037	NO	YES		
IBM SERIES1 MOD2(4952)	79	16	9.4			.075	NO	NO	8	
IBM SERIES1 MOD3(4953A)	76	16	8.4	13.2	15.6	.087	NO	NO	8	
IBM SERIES1 MOD5(4955A)	76	16	2.64	10.79	17.16	.156	NO	YES	8	
LEC MAC/LEC 16	69	17	2	10		.156	NO	YES	1	256
LEC SLE 1110	72	16	2.79	15.4		.098	NO	YES	7	
LEC SYSTEM 3	73	16	2.85			.120	NO	YES	7	
MDC 3200	74	16	5.2			.378	YES			
MDC 1600	72	16	66.5	92.7		.039	NO	NO	2	32

COMPUTER MFG. AND MODEL	TYPE	MEMORY CHARACTERISTICS CYCLE (USECS)	SIZE (K WORDS) MIN	MAX	COST (¢/BIT)	SYSTEM COST ($K)	CPU COST ($K)	ADJUSTED CPU COST ($K) THEN YEAR $	1980 $
HON 6/06	SEMI	.65	8	32	.5	46	7.1	7.10	9.58
HON 6/34	CORE	1.2	8	32	1.6	22	4.4	4.40	5.94
HON 6/36	CORE	1.2	8	64	1.6	110	6.6	6.60	8.91
IBM SYSTEM/34(5340)	SEMI	.6	16	64	.94	60	26.3	25.10	30.91
IBM SYSTEM/32(5320)	SEMI	.6	16	32	.92	32	23.5	22.91	31.00
IBM 5100	SEMI	.533	8	32	.92		6.3	6.30	8.53
IBM 360 MOD 20(2020,B1)	CORE	3.6	2	16	13.9	80	11.7	25.04	41.06
IBM 360 MOD 20(2020,B3)	CORE	3.6	2	16	10.7	42	8.2	18.47	29.09
IBM 360 MOD 20(2020,C5)	CORE	2	4	32	16	120	19	29.24	46.05
IBM 360 MOD 20(2020,C6)	CORE	3.6	4	16	17.8	104	11.2	22.59	34.44
IBM 1800-2	CORE	2.25	4	64	9.3	43	38.7	44.65	69.99
IBM 1130	CORE	2.2	4	32	6.86		8.63	13.57	21.75
IBM 8130	SEMI	1.5	64	128	.6	92	22.	11.25	12.94
IBM 8140	SEMI	.8	64	128	.6	182	31.	20.25	20.25
IBM SYSTEM/7(5010,A8)	CORE	.4	2	64	4.8	17	12.19	17.57	26.48
IBM SYS/3-8(5408)	SEMI	1.52	16	64	.92	66	27.1	26.51	35.87
IBM SYS/3-12(5412)	SEMI	1.52	32	64	.92	110	50.6	48.83	65.90
IBM SYS/3-6(5406)	CORE	1.52	8	256	5.16	50	22.4	22.40	34.15
IBM SYS/3-10(5410)	CORE	1.52	8	48	5.16	64	17.6	17.60	27.20
IBM SYS/3-4(5404)	SEMI	1.52	64	64	1.33	34	19.2	13.24	17.87
IBM SERIES1 MOD2(4952)	SEMI	.2	16	64	.175	30	4.6	4.38	5.04
IBM SERIES1 MOD3(4953A)	SEMI	.8	8	32	1.18	30	4.6	4.60	6.21
IBM SERIES1 MOD5(4955A)	SEMI	.66	8	64	1.18	40	6.5	6.50	8.77
LEC AAC/LEC 16	CORE	1	8	64	3.27	14	7.6	7.60	11.78
LEC SUE 1110	CORE	1.8	16	496	1.52	10	6	4.05	6.12
LEC SYSTEM 3	SEMI	.6	16	132	.7	30	12.2	11.30	16.92
MDC 3200	SEMI	.9	4	64	.94		9.5	10.10	14.17
MDC 1600	CORE	1	4	32	2.19		5.6	7.00	10.58

COMPUTER MFG. AND MODEL	FIRST DELIV YEAR	WORD LENGTH (BITS)	MICROSECS PER INSTRUCTION ADD	MULT.	DIVIDE	MIPS	FLOAT	DMA	NO. OF ACCUMS	NO. OF I/O CHNLS
MOC MICRO-ONE	74	8	73.2	1020		.036	NO	NO	2	32
MOD MODCOMP II(10)	72	17	.8	6.1	8.8	.251	NO	YES	15	64
MOD MODCOMP IV(35-8)	74	17	.64	3.5	8.6	.400	NO	YES	240	64
MOD MODCOMP I	71	16	.5	10.3		.190	NO	YES		64
MOD CLASSIC 7830	79	16	.5	1.3		1.180	NO	YES	15	256
MOD CLASSIC 7860	80	16	.2			1.330	YES	YES	240	256
MOD CLASSIC 7870	70	16	.2	1.2		1.330	YES	YES	15	256
NOI 812	71	12	2	10.7		.116	NO		2	
PEC 50	72	16	3.25	19.4		.099	NO		16	255
PEC 70	72	16	3.25	10.2		.136	YES		16	255
PEC 74	73	16	1.5	34		.075	NO		16	255
PEC 7/16	74	17	1.5	34		.075	NO			255
PEC 7/16HS	74	17	.75	5.5		.240	YES		32	255
PEC 1610	79	16	1			.262	NO	YES		
PEC 1620	79	16	.825			.296	NO	YES		
PEC 1630	79	16	.75			.313	NO	YES		
PEC 6/16	75	17	.9	6.6	12	.262	NO	YES	16	
PEC 8/16E	77	17	.75	9.25	12.5	.208	NO	YES	16	
PEC 7/32C	74	34	1	21.75	21.75	.115	NO	YES	32	
PEC 8/32C	75	34	.4	2.7	5.5	.386	NO	YES	256	
PEC 5/16	76	16	1.2	24.9	31.5	.105	NO	YES	16	
PEC 3220	79	34	.5	8.5	11.15	.218	NO	YES		
PEC 3240	80	34	.85	3.84	5.76	.364	NO	YES		
P3S P330	77	8	1.2			.134	NO	YES	16	
P3S P350	70	64	1.5			.117	NO	YES	1	
PPS SYST-1	77	16	3.5			.072	NO	YES	8	
PPS SYST-04	77	16	3.17			.078	NO	YES	8	
PCI 550	79	32	.56	4.2	4.76	.274	YES	YES		71

COMPUTER MFG. AND MODEL	MEMORY CHARACTERISTICS						SYSTEM COST ($K)	CPU COST ($K)	ADJUSTED CPU COST ($K)	
		TYPE	CYCLE (USECS)	SIZE(K WORDS) MIN	MAX	COST (¢/BIT)			THEN YEAR $	1980 $
MDC	MICRO-ONE	SEMI	1.1	8	32	.94		3.5	3.50	4.91
MOD	MODCOMP II(10)	CORE	.8	16	64	1.56	34	11.5	9.38	14.17
MOD	MODCOMP IV(35-8)	CORE	.5	64	1024	1.5	175	42.5	28.22	39.58
MOD	MODCOMP I	CORE	.8	8	16	2.2		7.4	7.40	11.28
MOD	CLASSIC 7830	SEMI	.125	64	256	.98		23.8	15.02	17.28
MOD	CLASSIC 7860	SEMI	.125	64	624	.98	75	37	28.22	28.22
MOD	CLASSIC 7870	SEMI	.125	256	2048	.98		61	22.11	34.18
NDI	812	CORE	2	8	16	5.2		10	10.00	15.24
PEC	50	CORE	1	4	32	1.4	46	7.4	8.30	12.53
PEC	70	CORE	1	4	32	1.4	46	7.4	8.30	12.53
PEC	74	CORE	1	4	32	1.3	43	4.6	5.43	8.13
PEC	7/16	CORE	1	4	32	1.6		4.2	5.29	7.42
PEC	7/16HS	CORE	1	4	32	1.2		9	9.62	13.77
PEC	1610	SEMI	.66	8	32	.55		5.4	5.40	6.21
PEC	1620	SEMI	.66	16	128	.55		9	8.30	9.55
PEC	1630	SEMI	.66	16	128	.55		11	10.30	11.85
PEC	6/16	CORE	.6	4	32	.78	8	4	4.53	6.13
PEC	8/16E	CORE	.75	16	131	.98	30	9.33	8.00	10.45
PEC	7/32C	CORE	.75	16	256	1.28	50	14.4	10.92	15.31
PEC	8/32C	CORE	.75	32	256	.92	180	51.9	44.39	60.07
PEC	5/16	SEMI	.6	4	32	.94		2.1	2.70	3.65
PEC	3220	SEMI	.7	64	1024	.46		33.5	24.74	28.47
PEC	3240	SEMI	.5	64	4096	.56	185	85	74.34	74.34
PBS	P330	CORE	1.5	24	32	2.34		16.99	15.99	20.91
PBS	P350	CORE	1.5	8.	12.	17.97		13.5	36.50	56.42
PPS	SYST-1	SEMI	.5	16	32	.41		3.54	3.02	3.94
PPS	SYST-04	SEMI	.5	16	32	.34		7.09	6.40	8.36
PCI	550	SEMI	1	64	512	.61	70	63.5	52.57	60.49

COMPUTER MFG. AND MODEL	FIRST DELIV YEAR	WORD LENGTH (BITS)	MICROSECS PER INSTRUCTION ADD	MULT.	DIVIDE	MIPS	FLOAT	DMA	NO. OF ACCUMS	NO. OF I/O CHNLS
PCI 450	79	32	.56	4.2	4.76	.274	YES	YES		36
PCI 350	78	16	.56			.385	YES	YES		
PCI 100	73	16	2.44			.091	NO	YES	1	
PCI 200	72	18	1.96			.114	NO	YES	1	
PCI 300	74	18	1.56			.138	NO	YES	1	
PCI 400	76	22	.56			.342	YES	YES	1	
PCI 650	79	32	.56	4.2	4.70	.274	YES	YES		71
PCI 750	79	32	.24	1.38	4.56	.561	YES	YES		71
RDS RDS-500	73	18	1.4			.204	NO	YES	8	
RDS RDS-5000	77	18	1.4			.204	NO	YES	8	
SUD 9200	66	32	40.8			.023	NO		8	
SUD 9200II	66	32	40.8			.023	NO		8	
SUD 9300II	66	32	20.4			.046	NO		8	
SUD 90/30	74	32	5.4	39.6	65.4	.152	NO		16	
SUD V620/L-100	72	16	1.9	9.5		.164	NO			32
SUD V77-400/410	77	16	1.32	5.94	7.92	.248	NO	YES	2	
SUD V73	72	18	1.32			.216	NO	YES	3	
SUD V76	76	18	1.32			.216	NO	YES	8	
SUD V77-600/610	77	16	.74	4.79	5.28	.305	NO	YES	2	
SUD 90/25	77	32	5.4	42	67.8	.057	NO	YES	16	
SUD V77-800	79	48	.45			.430	NO	YES	2	
SUD V77-200/210	77	16	2.31	5.11	7.67	.224	NO	YES	2	
SEL 32/55	75	36	1.2	5.5	9.2	.271	YES	YES	8	16
SEL 32/75	78	36	1.2	5.5	9.2	.271	YES	YES	8	64
SEL 32/77-60	78	36	.6			.303	NO			
SEL 32/35	76	36	1.8	6.2	9.5	.203	YES	YES	8	
TAN T16/1102(M)	76	17	.5	3.4	3.1	.422	NO	YES	8	
TAN T16/1102(C)	76	17	.6	3.4	3.1	.314	NO	YES	8	

COMPUTER MFG. AND MODEL	MEMORY CHARACTERISTICS TYPE	CYCLE (USECS)	SIZE (K WORDS) MIN	MAX	COST (¢/BIT)	SYSTEM COST ($K)	CPU COST ($K)	ADJUSTED CPU COST ($K) THEN YEAR $	1980 $
PCI 450	SEMI	1	64	256	.61	70	40	29.07	33.45
PCI 350	SEMI	.6	16	128	.61	125	35	34.22	42.14
PCI 100	SEMI	1	8	64	2.66		5.5	5.50	6.23
PCI 200	SEMI	.75	8	64	3.05		6.8	6.80	10.27
PCI 300	SEMI	.75	8	64	1.66	75	17.6	17.60	24.68
PCI 400	SEMI	.76	64	4000	1.66		65.1	44.65	60.25
PCI 650	SEMI	1	64	1024	.61	200	68.5	77.57	89.26
PCI 750	SEMI	.6	128	2048	.61	240	123.5	100.08	115.16
RDS RDS-500	SEMI	.7	16	64	1.46		12.05	9.95	14.89
RDS RDS-5000	SEMI	.7	16	448	1.46	140	18.3	16.20	21.17
SUD 9200	CORE	1.2	2	4	32.9	46	12	75.17	117.82
SUD 9200II	CORE	1.2	2	8	32.9	165	15	78.17	122.52
SUD 9300II	CORE	.6	4	8	35.7	325	30	75.70	118.65
SUD 90/30	SEMI	.6	8	131	4.72	189	66	66.00	92.57
SUD V620/L-100	CORE	.95	8	32	2.73		7.7	7.70	11.63
SUD V77-400/410	SEMI	.66	16	1024	1.13	75	5.1	3.65	4.78
SUD V73	SEMI	.66	8	256	2.73		15.53	15.53	23.46
SUD V76	SEMI	.66	16	1024	1.13		8.4	6.77	9.14
SUD V77-600/610	SEMI	.66	16	1024	1.13	115	6.5	5.05	6.61
SUD 90/25	SEMI	.65	16	32	5.57	136	50	35.74	46.72
SUD V77-800	SEMI	.6	42	342	.44	150	41	33.82	38.92
SUD V77-200/210	SEMI	.66	8	32	1.13	25	3.5	3.50	4.58
SEL 32/55	CORE	.6	16	256	2.05	105	49	43.10	58.32
SEL 32/75	CORE	.6	32	2040	.83	153	72.3	65.13	80.21
SEL 32/77-60	CORE	.9	128	4056	.83	110	46	10.14	12.49
SEL 32/35	CORE	.9	8	128	1.27	74	25	25.00	33.74
TAN T16/1102(M)	SEMI	.5	48	256	.54	84	22	15.61	21.06
TAN T16/1102(C)	CORE	.8	32	128	1.56	99	20.4	14.04	18.94

COMPUTER MFG. AND MODEL	FIRST DELIV YEAR	WORD LENGTH (BITS)	MICROSECS PER INSTRUCTION ADD	MULT.	DIVIDE	MIPS	FLOAT	DMA	NO. OF ACCUMS	NO. OF I/O CHNLS
TEK 4051	75	8	2			.135	NO	NO	2	
TII 960A	74	22	3.6	8.6	10.9	.152	NO	YES	16	
TII 960B	74	22	1.75	2.65	6.25	.284	NO	YES	2	256
TII 990/4	76	17	4.7			.076	NO	NO		
TII 990/10	76	17	3.6			.097	NO	YES		
WLI 2200VP	77	8	15			.030	YES	NO	32	9
WEC 2500	72	16	1.7	24.4		.098	NO	YES	1	2

COMPUTER MFG. AND MODEL	MEMORY CHARACTERISTICS					SYSTEM COST ($K)	CPU COST ($K)	ADJUSTED CPU COST ($K)	
	TYPE	CYCLE (USECS)	SIZE(K WORDS) MIN	MAX	COST (¢/BIT)			THEN YEAR $	1980 $
TEK 4051	SEMI	1.2	8	32	2.19		6	6.00	8.12
TII 960B	SEMI	.75	8	64	1.09	12	4.5	4.50	6.31
TII 960B	SEMI	.75	8	64	1.09	47	5.15	5.15	7.22
TII 990/4	SEMI	.67	1	32	.9	14	2.28	3.35	4.52
TII 990/10	SEMI	.65	8	1024	.7	13	3.45	3.45	4.66
WLI 2200VP	SEMI	.6	16	64	2.34	25	8	6.50	8.50
NEC 2500	CORE	.85	8	1024	1.56	60	13.7	13.70	20.69

COMPUTER MFG. AND MODEL	FIRST DELIV YEAR	WORD LENGTH (BITS)	MICROSECS PER INSTRUCTION ADD	MULT.	DIVIDE	MIPS	FLOAT	DMA	NO. OF ACCUMS	NO. OF I/O CHNLS
AUT D216	72	16	2.5	13.8	23.8	.112	NO	YES	16	16
MON 6/36(MILITARIZED)	78	18	1.9	12.7	17	.133	NO	YES	7	
PPS PA-1150/SRP	76	16	2.03			.116	NO	YES	8	
ROL MSE-30	80	16	.65	4.7		.259	YES	YES	8	64
ROL 1602A/UYK-19	77	16	1	5.3	9.2	.233	NO	YES	4	56
ROL 1603A/UYK-12	76	16	5.9			.120	NO		4	56
ROL 1606/UYK-19	78	16	1			.333	NO		4	56
ROL 1650/UYK-19	76	16	1.05			.327	NO		4	12
ROL 1664/UYK-19	76	16	1			.333	YES		12	56
ROL 1666/UYK-19	77	16	1			.333	NO		4	56
ROL 1602B/UYK-19	76	16	1.05			.216	NO			56
UTN 11/34 M	76	16	1.9	9	13	.172	YES	YES		
UTN M2-11/70 A	78	16	.3	3.2	7.7	.337	YES			

COMPUTER MFG. AND MODEL	MEMORY CHARACTERISTICS TYPE	CYCLE (USECS)	SIZE (K WORDS) MIN	MAX	COST (¢/BIT)	SYSTEM COST ($K)	CPU COST ($K)	ADJUSTED CPU COST ($K) THEN YEAR $	1980 $
AUT D216	CORE	1.5	2	64	2.7	100	50	52.59	79.44
HON 6/36(MILITARIZED)	CORE	1.2	8	64	6.9	476	28.3	26.30	34.85
PPS PM-1150/5KP	SEMI	.55	16	128	.58		19.5	16.76	25.31
ROL MSE-30	CORE	1	128	1024	2.7	200	135	83.16	83.16
ROL 1602A/UYK-19	CORE	1	16	64	2.73		25.25	21.76	28.44
ROL 1603A/UYK-12	CORE	1.2	16	32	2.34		13.4	10.40	14.04
ROL 1606/UYK-19	CORE	1	16	1024	2.73		43.9	40.41	49.76
ROL 1650/UYK-19	CORE	1	16	32	2.73		26.25	22.76	30.71
ROL 1664/UYK-19	CORE	1	16	64	2.73		39.45	35.96	46.52
ROL 1666/UYK-19	CORE	1	16	1024	2.73		48.9	45.41	59.35
ROL 1602B/UYK-19	CORE	1	16	64	2.73		26.3	22.81	28.09
UTN 11/34 #	CORE	.9	32	128	7.32		67.5	39.39	53.16
UTN M2-11/70 A	CORE	.9	64	1024	7.32		160	94.41	116.27

APPENDIX B

COST ESTIMATING RELATIONSHIPS

AND

REGRESSION ANALYSES

COMMERCIAL COSTS - 6 INDEPENDENT VARIABLES - UNINFLATED - SEMI-LOG (LN Y) DATE: 06/19/80 TIME: 11.54.58. PAGE: 29

SEMILOG REGRESSION -- LN Y = A + B * X1 + C * X2 + D * X3 + E * X4 + F * X5 + G * X6

SUMMARY TABLE

NOTE -- STATISTICS ARE BASED ON LOGARITHMS

PARAMETER		VALUE	STANDARD ERROR	T-RATIO	SIGNIF LEVEL	BETA COEFF
A	(CONSTANT)	5.29450	1.53795	3.44282	.00070	
B	DELIV YR	-.64292D-01	.01957	-3.28516	.00121	-.22115
C	WRD LNTH	.46935D-01	.00756	6.20743	.00000	.40337
D	MEM TECH	.69065D-01	.12705	.54544	.58744	.03480
E	MIPS	.77535	.23524	3.28396	.00121	.19595
F	MAX MEMO	.24146D-05	.00000	.90708	.36548	.05295
G	FLOAT PT	.71665	.15171	4.72387	.00000	.28422

CORRELATION MATRIX

VARIABLE		MEAN	STANDARD DEVIATION	LN ADJ. CPU	DELIV YR	WRD LNTH	MEM TECH	MIPS	MAX MEMO	FLOAT PT
LN Y	ADJ. CPU	2.52476	.98596	1.00000	-.04478	.51847	.12930	.32652	.29961	.41721
X1	DELIV YR	74.85222	3.39158	-.04478	1.00000	.15543	-.50829	.24214	.26887	.24120
X2	WRD LNTH	19.14286	8.47327	.51847	.15543	1.00000	.06146	.21145	.50256	.26960
X3	MEM TECH	1.43350	.49678	.12930	-.50829	.06146	1.00000	-.05852	-.10657	-.08850
X4	MIPS	.22413	.24769	.32652	.24214	.21145	-.05852	1.00000	.13129	.33465
X5	MAX MEMO	8495.14778	24871.43011	.29961	.26887	.50256	-.10657	.13129	1.00000	.26607
X6	FLOAT PT	1.16749	.39103	.41721	.24120	.26960	-.08850	.33465	.26607	1.00000

COEFFICIENT OF DETERMINATION (ENADJ), R SQ	.42311	MEAN OF ABSOLUTE RELATIVE DEVIATIONS (LN	.08824
STANDARD ERROR OF ESTIMATE	.76025	COEFF VARIATION (STD ERR EST / MEAN Y OBS)	.30111
SUM OF SQUARES OF RESIDUALS (LN	113.28322	SUM OF SQUARES TOTAL (LN	196.26502
F VALUE	23.95885	DURBIN-WATSON STATISTIC	1.52470
DEGREES OF FREEDOM FOR ERROR	196	DEGREES OF FREEDOM DUE TO REGRESSION	6
TOTAL DEGREES OF FREEDOM	202	NUMBER OF DATA POINTS	203

VARIANCE-COVARIANCE MATRIX

	A	B	C	D	E	F	G
A	.22653D+01	-.10619D-01	-.76285D-03	-.16620D-01	-.10505D-01	-.41939D-07	-.22216D-01
B	-.10619D-01	.36239D-03	-.84095D-05	.12521D-02	-.79803D-03	-.78446D-05	-.31462D-03
C	-.76285D-03	-.84095D-05	.57173D-04	-.15225D-03	-.21332D-03	-.92295D-08	-.13725D-03
D	-.16620D-01	.12521D-02	-.15225D-03	.16151D-01	-.14311D-02	.16505D-07	.12067D-03
E	-.10505D-01	-.79803D-03	-.21332D-03	-.14311D-02	.55528D-01	.30736D-07	-.94699D-02
F	-.41939D-07	-.78446D-08	-.92295D-08	.16505D-07	.30736D-07	.76657D-11	-.50159D-07
G	-.22216D-01	-.31462D-03	-.13725D-03	.12067D-03	-.94699D-02	-.50159D-07	.23016D-01

SEMILOG REGRESSION -- LN Y = A + B * X1 + C * X2 + D * X3 + E * X4 + F * X5 + G * X6

SUMMARY TABLE

NOTE -- STATISTICS ARE BASED ON LOGARITHMS

PARAMETER		VALUE	STANDARD ERROR	T-RATIO	SIGNIF LEVEL	BETA COEFF
A	(CONSTANT)	7.60541	1.52399	4.99243	.00000	
B	DELIV YR	-.90756D-01	.01939	-4.68604	.00001	-.31449
C	WRD LNTH	.45456D-01	.00749	6.07210	.00000	.39386
D	MEM TECH	.81031D-01	.12593	.64582	.51915	.04128
E	MIPS	.73142	.23351	3.13234	.00200	.18464
F	MAX MEMO	.22018D-05	.00000	.87265	.38393	.05861
G	FLOAT PT	.70737	.15033	4.70546	.00000	.26284

CORRELATION MATRIX

VARIABLE		MEAN	STANDARD DEVIATION	LN ADJ. CPU	DELIV YR	WRD LNTH	MEM TECH	MIPS	MAX MEMO	FLOAT PT
LN Y	ADJ. CPU	2.02021	.97877	1.00000	-.14610	.49154	.18355	.29147	.28531	.38645
X1	DELIV YR	74.05222	3.39158	-.14610	1.00000	.15543	-.50829	.24214	.28887	.24120
X2	WRD LNTH	19.14222	8.47327	.49154	.15543	1.00000	.06166	.21145	.50288	.28980
X3	MEM TECH	1.43350	.49576	.18355	-.50829	.06166	1.00000	-.05852	-.10657	-.08850
X4	MIPS	.22415	.24709	.29147	.24214	.21145	-.05852	1.00000	.13180	.33465
X5	MAX MEMO	8493.14776	24071.43011	.28531	.28887	.50288	-.10657	.13180	1.00000	.26607
X6	FLOAT PT	1.19711	.39103	.38645	.24120	.28980	-.08850	.33465	.26607	1.00000

COEFFICIENT OF DETERMINATION (UNADJ), R SQ	.42519	MEAN OF ABSOLUTE RELATIVE DEVIATIONS (LN	.27559
STANDARD ERROR OF ESTIMATE	.75354	COEFF VARIATION (STD ERR EST / MEAN Y OBS)	.26833
SUM OF SQUARES OF RESIDUALS (LN	111.23557	SUM OF SQUARES TOTAL (LN	193.51399
F VALUE	24.16336	DURBIN-WATSON STATISTIC	1.54383
DEGREES OF FREEDOM FOR ERROR	196	DEGREES OF FREEDOM DUE TO REGRESSION	6
TOTAL DEGREES OF FREEDOM	202	NUMBER OF DATA POINTS	203

VARIANCE-COVARIANCE MATRIX

	A	B	C	D	E	F	G
A	.23225D+01	-.10285D-01	-.74910D-03	-.16215D-01	-.10315D-01	-.41181D-07	-.21614D-01
B	-.10285D-01	.37607D-03	-.61592D-05	.12295D-02	-.76360D-03	-.77028D-08	-.30895D-05
C	-.74910D-03	-.61592D-05	.56146D-04	-.14979D-03	-.20946D-03	-.90921D-06	-.13477D-03
D	-.16215D-01	.12295D-02	-.14979D-03	.15859D-01	-.14053D-02	.16206D-07	.11049D-03
E	-.10315D-01	-.76360D-03	-.20946D-03	-.14053D-02	.54525D-01	.30180D-07	-.93184D-02
F	-.41181D-07	-.77028D-08	-.90921D-06	.16206D-07	.30180D-07	.69577D-11	-.49253D-07
G	-.21614D-01	-.30895D-05	-.13477D-03	.11049D-03	-.93184D-02	-.49253D-07	.22599D-01

CURVES REGRESSION ANALYSIS COMPUTER PROGRAM
(JULY 1976)

COMMERCIAL COSTS - MEMORY TYPE ELIMINATED - LINEAR FIT   DATE: 07/23/83 TIME: 13.59.24. PAGE: 1

LINEAR REGRESSION -- Y = A + B * X1 + C * X2 + D * X3 + E * X4 + F * X5

SUMMARY TABLE

PARAMETER		VALUE	STANDARD ERROR	T-RATIO	SIGNIF LEVEL	BETA COEFF
A	(CONSTANT)	116.36640	35.50851	3.32600	.00105	
B	DELIV YR	-1.99508	.48153	-4.15149	.00005	-.23957
C	WRD LNTH	1.52734	.21260	7.18421	.00000	.45785
D	MIPS	18.45096	6.70292	2.75357	.00645	.16134
E	MAX MEMO	.33623E-04	.00008	.44406	.65747	.02862
F	FLOAT PT	19.80215	4.32018	4.58365	.00001	.27394

CORRELATION MATRIX

VARIABLE		MEAN	STANDARD DEVIATION	ADJ. CPU	DELIV YR	WRD LNTH	MIPS	MAX MEMO	FLOAT PT
Y	ADJ. CPU	25.90246	28.28299	1.00000	-.05586	.54299	.29552	.26854	.40123
X1	DELIV YR	74.65222	3.39158	-.05586	1.00000	.15543	.24214	.26867	.24120
X2	WRD LNTH	19.14286	8.47727	.54299	.15543	1.00000	.21145	.50268	.26960
X3	MIPS	.22415	.24709	.29552	.24214	.21145	1.00000	.13180	.35465
X4	MAX MEMO	6493.14776	24071.43011	.26854	.26867	.50268	.13180	1.00000	.26607
X5	FLOAT PT	1.13715	.39103	.40123	.24120	.26960	.35465	.26607	1.00000

COEFFICIENT OF DETERMINATION (UNADJ), R SQ	.42786	MEAN OF ABSOLUTE RELATIVE DEVIATIONS	1.14262
STANDARD ERROR OF ESTIMATE	21.64998	COEFF VARIATION (STD ERR EST / MEAN Y OBS)	.83585
SUM OF SQUARES OF RESIDUALS	92338.16201	SUM OF SQUARES TOTAL	161391.26677
F VALUE	29.46446	DURBIN-WATSON STATISTIC	1.49599
DEGREES OF FREEDOM FOR ERROR	197	DEGREES OF FREEDOM DUE TO REGRESSION	5
TOTAL DEGREES OF FREEDOM	202	NUMBER OF DATA POINTS	203

VARIANCE-COVARIANCE MATRIX

	A	B	C	D	E	F
A	.12266D+04	-.15100D+02	-.61266D+00	-.25192D+01	-.34012D-04	-.18016D+02
B	-.15100D+02	.23187D+00	.28519D-02	-.55720D+00	-.73994D-05	-.26274D+00
C	-.61266D+00	.28519D-02	.45196D-01	-.16395D+00	-.73826D-05	-.11638D+00
D	-.25192D+01	-.55720D+00	-.16395D+00	.44929D+02	.26112D-04	-.76674D+01
E	-.34012D-04	-.73994D-05	-.73826D-05	.26112D-04	.57327D-08	-.40778D-04
F	-.18016D+02	-.26274D+00	-.11638D+00	-.76674D+01	-.40778D-04	.18664D+02

POWER REGRESSION -- Y = A * X1**B * X2**C * X3**D * X4**E * X5**F

SUMMARY TABLE

PARAMETER	VALUE	INITIAL GUESS	STANDARD ERROR	T-RATIO	SIGNIF LEVEL
A (CONSTANT)	.15975D+13	.50557[illegible]***************		.20658	.83655
B DELIV YR	-6.55610	-6.97995	1.16494	-5.62956	.00000
C WRD LNTH	1.08346	.67732	.11110	9.75191	.00000
D MIPS	.10944	-.56793D-01	.04532	2.41494	.01665
E MAX MEMO	.47613D-01	.18672	.03957	1.20338	.23027
F FLOAT PT	.97451	1.13300	.17312	5.62898	.00000

CORRELATION MATRIX

VARIABLE	MEAN	STANDARD DEVIATION	ADJ. CPU	DELIV YR	WRD LNTH	MIPS	MAX MEMO	FLOAT PT
Y ADJ. CPU	25.90246	28.28599	1.00000	-.05586	.54299	.29552	.28854	.40123
X1 DELIV YR	74.65222	3.39158	-.05586	1.00000	.15543	.24214	.26867	.24120
X2 WRD LNTH	19.14286	6.47327	.54299	.15543	1.00000	.21145	.50268	.26980
X3 MIPS	.22415	.24769	.29552	.24214	.21145	1.00000	.13160	.63465
X4 MAX MEMO	8453.14776	24671.43011	.28854	.26867	.50268	.13160	1.00000	.26607
X5 FLOAT PT	1.16719	.39103	.40123	.24120	.26980	.63465	.26607	1.00000

COEFFICIENT OF DETERMINATION (UNADJ), R SQ	.45569	MEAN OF ABSOLUTE RELATIVE DEVIATIONS	1.12608
STANDARD ERROR OF ESTIMATE	21.11293	COEFF VARIATION (STD ERR EST / MEAN Y OBS)	.81509
SUM OF SQUARES OF RESIDUALS	87815.93283	SUM OF SQUARES TOTAL	161391.20677
F VALUE	33.01235	DURBIN-WATSON STATISTIC	1.53601
DEGREES OF FREEDOM FOR ERROR	197	DEGREES OF FREEDOM DUE TO REGRESSION	5
TOTAL DEGREES OF FREEDOM	202	NUMBER OF DATA POINTS	203

VARIANCE-COVARIANCE MATRIX

	A	B	C	D	E	F
A	.43790D+26	-.78618D+13	-.54506D+10	.68859D+11	.14271D+12	.11520D+12
B	-.78618D+13	.13571D+01	-.54149D-02	-.11184D-01	-.25608D-01	-.17695D-01
C	-.54506D+10	-.54149D-02	.12344D-01	.12991D-02	-.13638D-02	.48116D-03
D	.68859D+11	-.11184D-01	.12991D-02	.20537D-02	-.17056D-03	-.15493D-02
E	.14271D+12	-.25608D-01	-.13638D-02	-.17056D-03	.15655D-02	-.24917D-02
F	.11520D+12	-.17695D-01	.48116D-03	-.15493D-02	-.24917D-02	.29972D-01

TABLE OF RESIDUALS

COMPUTER		OBSERVED ACQ. CPU	DELIV YR	WRD SIZE	MIPS	MAXIMUM MEM SIZE	FLOAT PT	COMPUTED ACQ. CPU	RESIDUAL ACQ. CPU	RELATIVE DEVIATION
A AIU	SYS	4.300	75.000	16.000	.177	512.000	1.000	15.848	-11.548	-2.686
A ADI	150	20.100	77.000	8.000	.081	512.000	1.000	5.600	14.500	.721
A BUR	817	35.000	76.000	24.000	.322	576.000	1.000	24.205	10.795	.308
A BUR	817	89.800	76.000	24.000	.953	2112.000	1.000	22.918	62.882	.700
A CAD	SYS	6.200	76.000	8.000	.057	64.000	1.000	4.460	1.740	.281
A CAD	SYS	8.200	76.000	8.000	.059	384.000	1.000	5.057	3.143	.383
B CDI	CCN	29.300	78.000	16.000	.041	1024.000	1.000	21.942	7.358	.251
B CDI	CCN	32.500	77.000	16.000	.034	1024.000	1.000	11.506	20.994	.646
B CDP	X17	11.000	74.000	16.000	.120	1024.000	1.000	17.142	-6.142	-.558
B CDP	CDI	11.300	75.000	16.000	.114	2048.000	1.000	19.262	-7.962	-.705
B CCC	200	19.600	69.000	8.000	.187	4096.000	1.000	24.175	-5.425	-.277
B CCC	300	25.900	71.000	8.100	.130	256.000	2.000	19.691	6.209	.240
C CCC	100	20.200	77.000	16.100	.112	4096.000	2.000	27.518	-7.318	-.362
C CMC	CIP	10.200	71.000	8.000	.026	512.000	1.000	8.684	1.516	.149
C CMC	CIP	5.400	74.000	8.000	.025	512.000	1.000	6.592	-1.192	-.221
C CAI	LSI	3.300	72.000	16.000	.082	9216.000	1.000	22.878	-19.578	-5.871
C CAI	LSI	2.600	75.000	16.000	.039	8192.000	1.000	15.325	-12.725	-4.878
C CAI	LSI	1.600	77.000	16.000	.175	4096.000	1.000	14.705	-13.105	-8.191
D CAI	STP	32.900	76.000	16.000	.128	6384.000	1.000	16.992	15.908	.484
D CDI	CPU	4.400	70.000	8.000	.106	128.000	1.000	10.427	-6.027	-1.370
D CHI	215	45.800	74.000	16.000	.176	32768.000	1.000	21.109	24.691	.539
D CHI	323	20.200	76.000	16.000	.106	1024.000	1.000	14.197	6.003	.297
D CHI	421	15.900	77.000	16.000	.079	414.000	1.000	12.088	3.812	.240
D CHI	425	25.800	78.000	16.000	.105	16384.000	1.000	13.620	12.180	.472
E CLC	CYB	20.500	73.000	17.000	.121	1024.000	2.000	39.476	-18.976	-.926
E CDC	CYB	16.200	78.000	21.000	.202	2208.000	1.000	21.417	-5.217	-.322
E CLC	CYB	18.500	75.000	17.000	.212	544.000	1.000	17.311	1.189	.064
E CLC	SYS	25.900	75.000	17.000	.164	1024.000	1.000	20.770	5.130	.198
E CDC	310	80.800	65.000	24.000	.086	768.000	1.000	59.241	21.559	.267
E CSP	CSP	88.000	69.000	16.000	1.450	2048.000	2.000	72.239	15.761	.179
F DGC	NOV	8.500	71.000	17.000	.219	544.000	1.000	24.087	-15.587	-1.834
F DGC	NOV	8.500	71.000	17.000	.219	1024.000	1.000	25.722	-17.222	-2.026
F DGC	NOV	14.700	74.000	17.000	.202	2176.000	1.000	20.087	-5.387	-.366
F DGC	NOV	20.100	74.000	17.000	.219	2176.000	1.000	20.288	-.188	-.009
F DGC	NOV	7.600	70.000	17.000	.146	544.000	1.000	20.127	-12.527	-1.648
F DGC	NOV	5.000	72.000	17.000	.146	544.000	1.000	21.720	-16.720	-3.344
G DGC	NOV	6.300	72.000	17.000	.146	816.000	1.000	22.143	-15.843	-2.515
G DGC	MIC	4.300	77.000	16.000	.065	512.000	1.000	11.910	-7.610	-1.770
G DGC	MIC	3.500	77.000	16.000	.065	512.000	1.000	11.910	-8.410	-2.403
G DGC	MIC	2.500	77.000	16.000	.065	1024.000	1.000	10.404	-7.904	-3.162

TABLE OF RESIDUALS (CONTINUED)

COMPUTER		OBSERVED AVG. [illegible]	DELIV YR	[illegible]	[illegible]	[illegible]	[illegible]	COMPUTED AVG. [illegible]	RESIDUAL AVG. [illegible]	RELATIVE [illegible]
G DGC	MIC	3.100	79.000	16.000	.026	512.000	1.000	12.050	-8.950	-[illegible]
G DGC	NOV	1.500	75.000	17.000	.219	544.000	1.000	20.792	-19.292	-[illegible]
H DGC	NOV	4.300	75.000	17.000	.219	1088.000	1.000	21.426	-17.126	-[illegible]
H DGC	NOV	4.300	75.000	17.000	.155	544.000	1.000	17.166	-13.066	-[illegible]
H DGC	NOV	5.700	76.000	17.000	.155	2176.000	1.000	20.157	-14.457	-2.[illegible]
H DGC	NOV	13.500	76.000	17.000	.275	2176.000	1.000	17.945	-4.445	-.[illegible]
H DGC	NOV	2.800	79.000	17.000	.182	544.000	1.000	12.108	-9.308	-[illegible]
H DGC	NOV	6.300	79.000	17.000	.182	544.000	1.000	12.108	-5.808	-.922
I DGC	NOV	9.100	79.000	17.000	.182	2176.000	1.000	12.584	-3.484	-.[illegible]
I DGC	ECL	13.100	75.000	21.000	1.110	1376.000	1.000	27.256	-14.156	-1.075
I DGC	ECL	17.500	75.000	21.000	1.110	2752.000	1.000	28.150	-10.650	-.[illegible]
I DGC	ECL	29.20	75.000	21.000	1.110	2752.000	1.000	28.150	1.050	.[illegible]
I DGC	ECL	16.700	77.000	21.000	.251	2688.000	1.000	26.131	-9.431	-.[illegible]
I DGC	ECL	14.600	76.000	21.000	.239	5376.000	1.000	22.547	-7.947	-.[illegible]
J DGC	ECL	26.900	76.000	21.000	.239	5376.000	2.000	44.365	-17.465	-.647
J DGC	ECL	69.600	76.000	21.000	.279	21504.000	2.000	40.597	28.403	.41[illegible]
J DGC	C/1	22.100	79.000	21.000	.495	10752.000	2.000	3[illegible].470	-1[illegible]	-.74[illegible]
J DGC	S/2	26.500	79.000	21.000	.366	21504.000	2.000	[illegible].469	-11.[illegible]9	-.45[illegible]
J DGC	C/3	46.496	79.000	21.000	.495	21504.000	2.000	39.761	6.[illegible]	.17[illegible]
J DGC	MV/	90.400	80.000	39.000	1.190	19968.000	2.000	7[illegible].537	11.[illegible]	.1[illegible]
K DPC	150	5.900	77.000	8.000	.126	256.000	1.000	5.86[illegible]	.034	.006
K DPC	180	3.400	76.000	8.000	.065	512.000	1.000	5.1[illegible]	-1.7[illegible]	-.[illegible]
K DPC	220	13.900	72.000	8.000	.066	128.000	1.000	[illegible]	[illegible]7	[illegible]
K DEC	D-1	10.500	72.000	16.000	.250	1024.000	1.000	22.252	-11.752	-1.1[illegible]
K DEC	PDP	4.800	74.000	12.000	.122	192.000	1.000	11.011	-6.211	-1.415
K DEC	PDP	2.009	76.000	16.000	.090	576.000	1.000	15.415	-13.415	-[illegible]
L DEC	PDP	3.600	75.000	16.000	.140	576.000	1.000	17.647	-14.047	-3.[illegible]
L DEC	PDP	25.000	74.000	16.000	.185	2304.000	1.000	21.198	3.[illegible]02	.15[illegible]
L DEC	PDP	19.950	80.000	16.000	.565	18432.000	1.000	15.129	4.[illegible]	.[illegible]
L DEC	PDP	54.400	72.000	16.000	.265	2304.000	1.000	28.[illegible]	26.[illegible]	.[illegible]
L DEC	PDP	41.800	77.000	16.000	.134	4608.000	2.000	32.062	9.7[illegible]	.[illegible]
L DEC	PDP	83.400	75.000	16.000	.307	18432.000	1.000	2[illegible]	[illegible].719	.7[illegible]
M DEC	PDP	11.000	76.000	16.000	.180	2304.000	1.000	17.765	-[illegible].76[illegible]	-.[illegible]
M DEC	VAX	119.500	76.000	32.000	.735	18304.000	2.000	7[illegible].025	4[illegible].475	.[illegible]
M DCI	SYS	2.600	76.000	8.000	.070	512.000	1.000	[illegible].154	-[illegible]	-1.[illegible]
M DSC	403	49.200	76.000	16.000	.066	2304.000	2.000	5[illegible]	-4.[illegible]	-.[illegible]
M DSC	501	25.000	72.000	16.000	.217	576.000	1.000	2[illegible]	[illegible]	.1[illegible]
M DSC	MLT	32.000	70.000	16.000	.226	1152.000	1.000	3[illegible]	[illegible]	.[illegible]
N DSY	MCD	56.100	76.000	8.000	.571	1024.000	1.000	5.[illegible]	[illegible].045	.777
N FAI	F64	71.900	79.000	64.000	.043	240000.000	2.000	114.175	-42.275	-.[illegible]

TABLE OF RESIDUALS (CONTINUED)

COMPUTER		OBSERVED ADJ. CPC	CELLS [illegible]	[illegible] UNIT	MIPS	MAXIMUM MEM [illegible]	[illegible]	COMPUTED ADJ. CPC	RESIDUAL ADJ. CPC	RELATIVE DEVIATION
N GAI	16/	6.035	79.000	16.000	.152	512.000	1.000	26.125	-18.5[illegible]	-2.74[illegible]
N GAI	16/	4.500	76.000	17.000	.117	1024.000	1.000	15.376	-10.876	-2.416
N GAI	16/	5.100	76.000	15.000	.115	576.000	1.000	15.824	-10.724	-2.105
N GAI	16/	5.800	76.000	16.000	.120	576.000	1.000	15.962	-10.1[illegible]	-1.745
O GAI	16/	31.700	77.000	16.000	.454	16432.000	1.000	19.921	11.779	.372
O GAI	16/	5.000	76.000	16.000	.265	16432.000	1.000	17.555	-12.555	-2.475
O GAI	16-	16.500	71.000	16.000	.259	2048.000	1.000	21.001	-14.201	-1.287
O GAI	16-	13.000	71.000	16.000	.277	2048.000	1.000	25.000	-11.763	-.753
O GRI	99/	5.595	75.000	15.000	.040	576.000	1.000	14.184	-8.589	-.640
O GRI	99/	5.900	72.000	16.000	.040	512.000	1.000	17.601	-11.701	-1.983
P HCP	SLA	32.500	75.000	26.000	.250	6656.000	1.000	37.250	-4.750	-.146
P HCP	SLA	20.100	76.000	25.000	.325	7424.000	1.000	30.537	-10.437	-.492
P HCP	SLA	36.000	75.000	26.000	.377	6656.000	1.000	32.515	3.385	.152
P HCP	F80	160.700	80.000	48.000	1.090	24576.000	2.000	98.579	62.121	.386
P HCP	H10	31.200	77.000	26.000	.190	6656.000	1.000	25.696	5.504	.176
P HCP	F20	134.405	77.000	26.000	.241	6656.000	2.000	51.624	82.976	.614
Q HFC	FF2	11.200	71.000	16.000	.152	512.000	1.000	22.327	-11.127	-.993
Q HFC	FF2	8.500	74.000	16.000	.152	1024.000	2.000	34.266	-25.766	-3.024
Q HFC	FF1	10.300	74.000	17.000	.157	17408.000	1.000	21.574	-11.274	-1.095
Q HFC	FF3	36.000	79.000	32.000	.166	5632.000	2.000	34.456	1.544	.152
Q HFC	HP3	84.300	76.000	22.000	.296	22528.000	2.000	43.100	41.200	.489
Q HFC	HP3	30.900	79.000	22.000	.351	11264.000	2.000	39.051	-8.151	-.264
R HFC	HP3	18.200	80.000	22.000	.351	22528.000	2.000	37.166	-18.966	-1.042
R HON	115	78.300	70.000	30.000	.006	128.000	1.000	32.543	45.757	.547
R HON	202	44.800	72.000	30.000	.008	256.000	1.000	28.788	16.012	.355
R HON	6/3	7.500	76.000	16.000	.155	1152.000	1.000	16.569	-9.069	-1.140
R HON	6/4	11.500	77.000	16.000	.265	16432.000	1.000	18.765	-7.265	-.632
R HON	6/5	55.100	76.000	17.000	.305	16432.000	1.000	17.324	37.776	.686
S HON	6/2	5.600	76.000	16.000	.140	1152.000	1.000	14.165	-8.565	-1.491
S HON	6/4	8.600	76.000	16.000	.265	16432.000	2.000	40.174	-31.574	-3.671
S HON	6/4	25.600	76.000	16.000	.455	16432.000	1.000	18.219	7.381	.294
S HON	6/5	24.900	76.000	16.000	.265	16432.000	1.000	16.805	8.095	.325
S HON	6/0	9.500	76.000	16.000	.067	576.000	1.000	16.700	-7.200	-.758
S HON	6/3	4.500	76.000	16.000	.155	576.000	1.000	16.068	-11.568	-2.575
T HON	6/3	7.500	76.000	16.000	.155	1152.000	1.000	16.623	-9.123	-1.217
T IBM	SYS	30.900	76.000	16.000	.075	1024.000	1.000	11.529	19.371	.627
T IBM	SYS	31.000	75.000	8.000	.004	256.000	1.000	4.779	26.221	.846
T IBM	513	8.500	75.000	16.000	.001	512.000	2.000	17.675	-9.175	-1.079
T IBM	360	36.600	64.000	16.000	.001	256.000	1.000	24.623	12.177	.331
T IBM	360	25.800	65.000	16.000	.001	256.000	1.000	16.545	9.255	.359

TABLE OF RESIDUALS (CONTINUED)

COMPUTER			OBSERVED AVG. CPU	DELIV YR	WORD LENGTH	MIPS	MEMORY SIZE	PERIPH FUNCT	COMPUTED AVG. CPU	RESIDUAL AVG. CPU	RELATIVE DEVIATION
U	IBM	360	42.500	66.000	16.000	.004	512.000	1.000	19.302	23.198	[illegible]
U	IBM	360	31.700	71.000	16.000	.002	[illegible]	1.000	13.448	18.252	[illegible]
U	IBM	160	66.300	66.000	[illegible]	.002	1024.000	1.000	34.819	31.481	.475
U	IBM	113	17.100	65.000	12.000	.088	576.000	1.000	41.950	-24.850	[illegible]
U	IBM	813	12.500	79.000	32.000	.041	[illegible]	1.000	24.320	-11.820	-.901
U	IBM	814	29.200	80.000	32.000	.178	4096.000	1.000	24.298	[illegible]	[illegible]
V	IBM	SYS	[illegible]	71.000	16.000	.001	[illegible]	1.000	13.214	[illegible]	[illegible]
V	IBM	SYS	35.400	75.000	8.000	.027	512.000	1.000	6.087	29.713	.830
V	IBM	SYS	62.500	76.000	8.000	.027	512.000	1.000	5.581	[illegible]	[illegible]
V	IBM	SYS	22.700	71.000	8.000	.055	[illegible]	1.000	10.070	12.630	[illegible]
V	IBM	SYS	25.000	70.000	8.000	.027	384.000	1.000	9.449	[illegible]	[illegible]
V	IBM	SYS	17.000	76.000	8.000	.037	512.000	1.000	5.777	11.223	.673
W	IBM	SER	[illegible]	79.000	16.000	.075	1024.000	1.000	15.505	-8.605	-1.121
W	IBM	SER	6.200	76.000	16.000	.007	512.000	1.000	13.445	-7.245	[illegible]
W	IBM	SER	8.700	76.000	16.000	.130	1024.000	1.000	14.815	-6.115	-.702
W	ELC	PAC	8.400	69.000	17.000	.136	1024.000	1.000	29.292	[illegible]	[illegible]
X	ELC	SCE	3.000	72.000	16.000	.096	7934.000	1.000	22.121	-19.321	-4.921
W	ELC	SYS	18.900	73.000	16.000	.120	2112.000	1.000	15.099	-2.499	-.140
X	MDC	320	14.100	74.000	16.000	.378	1024.000	2.000	[illegible]	[illegible]	[illegible]
X	MDC	160	8.200	72.000	16.000	.059	512.000	1.000	17.532	-9.332	-1.140
X	MOD	MIC	4.900	74.000	16.000	.055	224.000	1.000	6.636	[illegible]	[illegible]
X	MOD	MOD	11.700	72.000	17.000	.251	1368.000	1.000	23.820	-12.120	-1.036
X	MOD	MOD	37.000	74.000	17.000	.400	17408.000	1.000	23.900	13.900	.500
X	MOD	MOD	8.500	71.000	16.000	.190	256.000	1.000	22.135	[illegible]	-1.604
Y	MOD	CLA	17.200	75.000	16.000	1.160	4096.000	1.000	15.316	1.884	.110
Y	MOD	CLA	25.200	80.000	16.000	1.830	9904.000	2.000	29.294	-4.094	[illegible]
Y	MOD	CLA	34.100	76.000	16.000	1.830	32768.000	2.000	74.413	-40.313	-1.182
Y	MDI	8.2	13.200	71.000	12.000	.110	192.000	1.000	15.147	-1.947	-.193
Y	PEC	50	10.200	72.000	16.000	.099	512.000	1.000	19.496	-9.296	[illegible]
Y	PEC	70	10.200	72.000	16.000	.130	512.000	2.000	39.543	-29.343	-2.877
Z	PEC	74	6.000	73.000	16.000	.075	512.000	1.000	17.224	-11.224	-1.871
Z	PEC	7/1	5.700	74.000	17.000	.375	544.000	1.000	16.872	-11.172	[illegible]
Z	PEC	7/1	12.000	74.000	17.000	.246	544.000	2.000	37.053	-25.053	[illegible]
Z	PEC	101	6.200	75.000	16.000	.262	512.000	1.000	11.766	-5.566	[illegible]
Z	PEC	102	9.500	75.000	16.000	.296	2048.000	1.000	12.737	-3.237	-.341
Z	PEC	103	11.000	79.000	16.000	.313	2048.000	1.000	12.015	-1.015	[illegible]
1	PEC	6/1	4.400	75.000	17.000	.262	544.000	1.000	17.717	-13.317	-3.027
1	PEC	6/1	9.600	77.000	17.000	.206	2227.000	1.000	15.845	-6.245	-.672
1	PEC	7/3	15.400	74.000	34.000	.115	6784.000	1.000	42.755	-26.955	-2.223
1	PEC	8/3	56.700	75.000	34.000	.386	3704.000	1.000	44.498	12.202	.212

TABLE OF RESIDUALS (CONTINUED)

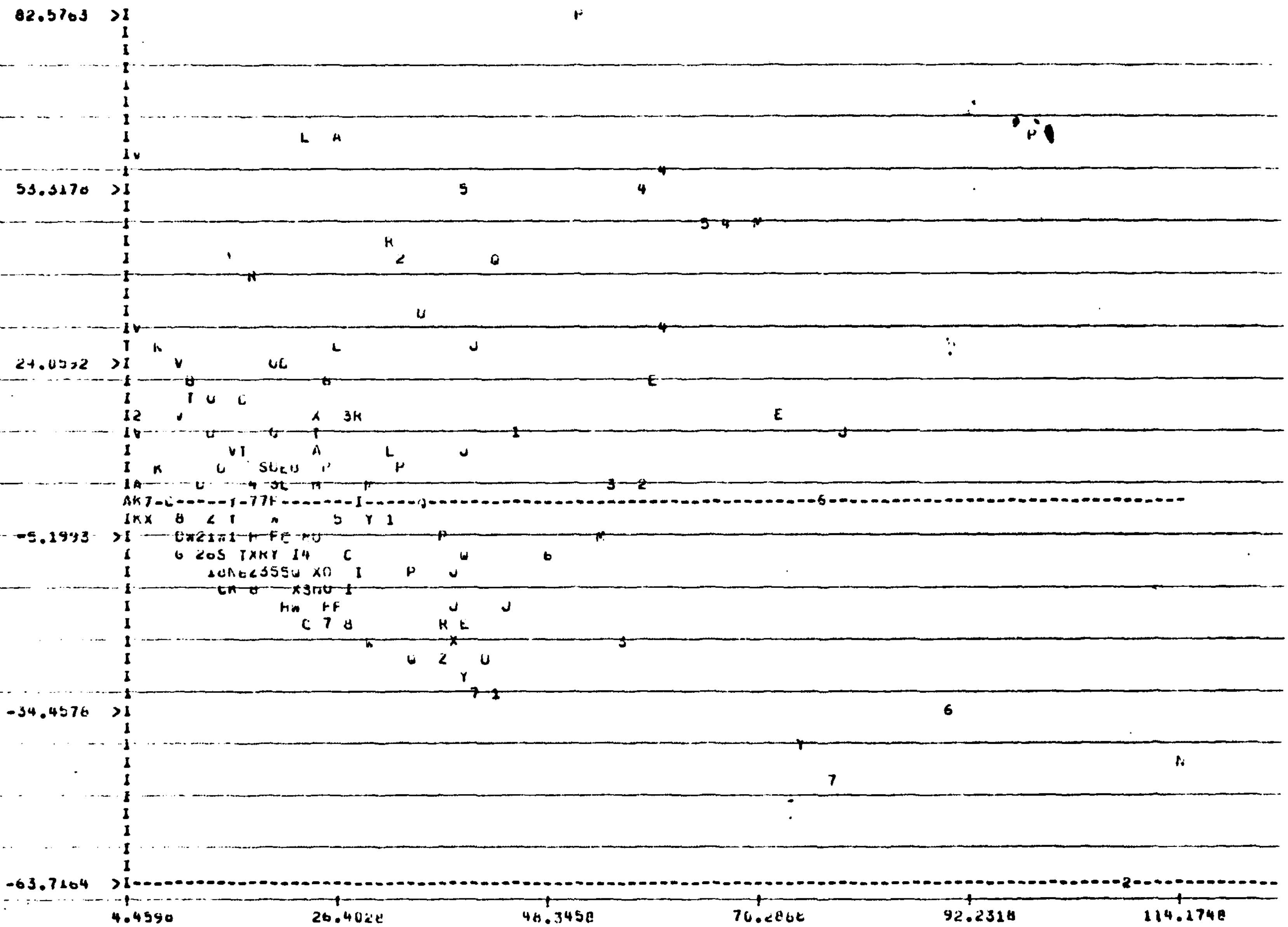
COMPUTER	OBSERVED ADJ. CPU	DELIV YR	WRD LNTH	MIPS	MODIFIED MAX MEMO	FLOAT PT	COMPUTED ADJ. CPU	RESIDUAL ADJ. CPU	RELATIVE DEVIATION
1 PDC 5/1	3.600	78.000	16.000	.105	512.000	1.000	13.722	-10.122	-2.812
1 PLC 322	26.400	73.000	34.000	.218	34816.000	1.000	31.902	-5.502	-.123
2 PLC 324	74.300	80.000	34.000	.364	139264.000	1.000	33.191	41.109	.553
2 PES P33	20.400	77.000	8.000	.134	256.000	1.000	5.906	14.494	.710
2 PES P35	45.300	70.000	64.000	.117	768.000	1.000	109.016	-63.716	-1.407
2 PPS SYS	3.900	77.000	16.000	.072	512.000	1.000	12.065	-8.165	-2.049
2 PPS SYS	8.300	77.000	16.000	.078	512.000	1.000	12.192	-3.892	-.469
2 PCI 550	60.400	79.000	32.000	.274	16384.000	2.000	58.066	2.334	.039
3 PCI 450	33.400	79.000	32.000	.274	8192.000	2.000	56.161	-22.761	-.682
3 PCI 350	42.100	78.000	16.000	.385	2048.000	2.000	28.004	14.096	.335
3 PCI 100	8.200	73.000	16.000	.051	1024.000	1.000	18.103	-9.903	-1.217
3 PCI 200	10.200	72.000	18.000	.114	1152.000	1.000	23.308	-13.108	-1.285
3 PCI 300	24.600	74.000	18.000	.138	1152.000	1.000	19.886	4.714	.192
3 PCI 400	60.200	76.000	22.000	.342	80000.000	2.000	55.357	4.843	.080
4 PCI 650	89.200	79.000	32.000	.274	32768.000	2.000	60.015	29.165	.227
4 PCI 750	115.100	79.000	32.000	.561	65536.000	2.000	67.089	48.011	.417
4 RCS RCS	14.800	75.000	18.000	.204	1152.000	1.000	22.693	-7.893	-.533
4 RCS RCS	21.100	77.000	18.000	.204	8064.000	1.000	17.546	3.554	.168
4 SDD 920	119.600	66.000	32.000	.023	128.000	1.000	56.151	52.449	.474
4 SDD 920	115.300	66.000	32.000	.023	256.000	1.000	60.102	55.198	.479
5 SDD 930	111.400	66.000	32.000	.046	256.000	1.000	64.838	46.562	.418
5 SDD 907	92.500	74.000	32.000	.152	4152.000	1.000	39.865	52.635	.569
5 SDD V62	9.300	72.000	16.000	.164	512.000	1.000	20.540	-11.240	-1.209
5 SDD V77	4.700	77.000	16.000	.248	16384.000	1.000	16.519	-11.819	-2.472
5 SDD V73	23.400	72.000	18.000	.216	4608.000	1.000	26.702	-3.302	-.141
5 SDD V76	9.100	76.000	16.000	.216	16432.000	1.000	20.009	-10.909	-1.199
6 SEL V77	6.600	77.000	16.000	.305	16384.000	1.000	16.693	-10.093	-1.529
6 SDD 907	46.700	77.000	32.000	.057	1024.000	1.000	25.801	20.899	.448
5 SDD V77	38.900	79.000	48.000	.460	16416.000	1.000	44.175	-5.275	-.134
6 SDD V77	4.500	77.000	16.000	.224	512.000	1.000	13.684	-9.164	-2.041
6 SEL 327	54.800	75.000	36.000	.271	9216.000	2.000	96.140	-35.340	-.645
6 SEL 327	78.000	76.000	36.000	.271	72000.000	2.000	76.863	1.137	.015
7 SEL 327	10.300	78.000	36.000	.303	147456.000	1.000	40.972	-30.672	-2.978
7 SEL 327	31.000	76.000	36.000	.203	4608.000	2.000	77.469	-46.469	-1.499
7 TAD T16	21.000	76.000	17.000	.422	4352.000	1.000	18.894	2.106	.100
7 TAP T16	17.600	76.000	17.000	.314	2176.000	1.000	17.698	-.098	-.006
7 TEP 405	8.100	75.000	8.000	.135	256.000	1.000	7.024	1.076	.133
7 TII 960	6.300	74.000	22.000	.152	1408.000	1.000	25.219	-18.919	-3.003
8 TII 980	7.200	74.000	22.000	.284	1408.000	1.000	27.004	-19.804	-2.751
8 TII 990	4.500	76.000	17.000	.076	544.000	1.000	14.185	-9.685	-2.152

TABLE OF RESIDUALS (CONTINUED)

COMPUTER	OBSERVED ADJ. CPU	DELIV YR	WRD LNTH	MIPS	MODIFIED MAX MEMO	FLOAT PT	COMPUTED ADJ. CPU	RESIDUAL ADJ. CPU	RELATIVE DEVIATION
B TII 990	4.600	76.000	17.000	.097	17408.000	1.000	17.183	-12.583	-2.735
B KLI 220	6.500	77.000	8.000	.030	512.000	2.000	10.182	-1.682	-.198
B KLC 250	18.300	72.000	16.000	.098	16384.000	1.000	22.898	-4.598	-.251

MINIMUM RELATIVE DEVIATION = -8.57818. MEAN ABSOLUTE RELATIVE DEVIATION = 1.12686. MAXIMUM RELATIVE DEVIATION = .91531

TRANSFORMATION FACTORS -- Y: 0.00000 X1: 0.00000 X2: 0.00000 X3: 0.00000 X4: 12.00000 X5: 0.00000



RESIDUAL ADJ. CPU VERSUS COMPUTED ADJ. CPU

CURVES REGRESSION ANALYSIS COMPUTER PROGRAM
(JULY 1976)

COMMERCIAL COSTS - NO MEMORY TYPE OR FLOATING POINT - LINEAR FIT DATE: 07/23/80 TIME: 18.41.32. PAGE: 1

LINEAR REGRESSION -- Y = A + B * X1 + C * X2 + D * X3 + E * X4

SUMMARY TABLE

PARAMETER	VALUE	STANDARD ERROR	T-RATIO	SIGNIF LEVEL	BETA COEFF
A (CONSTANT)	137.84114	37.46726	3.67898	.00030	
B DELIV YR	-1.93955	.50292	-3.85659	.00016	-.23291
C WRD LNTH	1.64953	.22221	7.42328	.00000	.49487
D MIPS	24.96586	6.80392	3.66933	.00031	.21841
E MAX MEMO	.705440-04	.00008	.89191	.37353	.06012

CORRELATION MATRIX

VARIABLE	MEAN	STANDARD DEVIATION	ADJ. CPU	DELIV YR	WRD LNTH	MIPS	MAX MEMO
Y ADJ. CPU	30.43300	28.24355	1.00000	-.08694	.53509	.27458	.27515
X1 DELIV YR	74.85222	3.39158	-.08694	1.00000	.15543	.24214	.26887
X2 WRD LNTH	19.14286	8.47327	.53509	.15543	1.00000	.21145	.50288
X3 MIPS	.22415	.24709	.27458	.24214	.21145	1.00000	.13180
X4 MAX MEMO	8495.14778	24071.43011	.27515	.26887	.50288	.13180	1.00000

COEFFICIENT OF DETERMINATION (UNADJ), R SQ	.36156	MEAN OF ABSOLUTE RELATIVE DEVIATIONS	.78081
STANDARD ERROR OF ESTIMATE	22.79409	COEFF VARIATION (STD ERR EST / MEAN Y OBS)	.74899
SUM OF SQUARES OF RESIDUALS	102874.96345	SUM OF SQUARES TOTAL	161134.96867
F VALUE	28.03277	DURBIN-WATSON STATISTIC	1.44422
DEGREES OF FREEDOM FOR ERROR	198	DEGREES OF FREEDOM DUE TO REGRESSION	4
TOTAL DEGREES OF FREEDOM	202	NUMBER OF DATA POINTS	203

VARIANCE-COVARIANCE MATRIX

	A	B	C	D	E
A	.140380+04	-.167380+02	-.685800+00	-.944340+01	-.377010-04
B	-.167380+02	.252930+00	.143890-02	-.737600+00	-.883840-05
C	-.685800+00	.143890-02	.493770-01	-.254310+00	-.845100-05
D	-.944340+01	-.737600+00	-.254310+00	.462930+02	.103270-04
E	-.377010-04	-.883840-05	-.845100-05	.103270-04	.625590-08

COMMERCIAL COSTS - NO MEMORY TYPE OR FLOATING POINT - POWER FIT DATE: 07/23/80 TIME: 18.41.32. PAGE: 8

POWER REGRESSION -- Y = A * X1**B * X2**C * X3**D * X4**E

SUMMARY TABLE

PARAMETER		VALUE	INITIAL GUESS	STANDARD ERROR	T-RATIO	SIGNIF LEVEL
A	(CONSTANT)	.131480D+12	.930558	************	.20353	.83893
B	DELIV YR	-5.97508	-5.36356	1.17366	-5.09099	.00000
C	WRD LNTH	.96585	.62362	.10754	8.98094	.00000
D	MIPS	.844690D-01	-.394070D-01	.04706	1.79484	.07421
E	MAX MEMO	.11318	.18527	.03643	3.10669	.00217

CORRELATION MATRIX

VARIABLE		MEAN	STANDARD DEVIATION	ADJ. CPU	DELIV YR	WRD LNTH	MIPS	MAX MEMO
Y	ADJ. CPU	30.43300	28.24355	1.00000	-.08694	.53509	.27458	.27515
X1	DELIV YR	74.85222	3.39158	-.08694	1.00000	.15543	.24214	.26887
X2	WRD LNTH	19.14286	8.47327	.53509	.15543	1.00000	.21145	.50288
X3	MIPS	.22415	.24709	.27458	.24214	.21145	1.00000	.13180
X4	MAX MEMO	8493.14778	24071.43011	.27515	.26887	.50288	.13180	1.00000

COEFFICIENT OF DETERMINATION (UNADJ), R SQ	.35889	MEAN OF ABSOLUTE RELATIVE DEVIATIONS	.76057
STANDARD ERROR OF ESTIMATE	22.84165	COEFF VARIATION (STD ERR EST / MEAN Y OBS)	.75056
SUM OF SQUARES OF RESIDUALS	103304.68639	SUM OF SQUARES TOTAL	161134.96887
F VALUE	27.71025	DURBIN-WATSON STATISTIC	1.53397
DEGREES OF FREEDOM FOR ERROR	198	DEGREES OF FREEDOM DUE TO REGRESSION	4
TOTAL DEGREES OF FREEDOM	202	NUMBER OF DATA POINTS	203

VARIANCE-COVARIANCE MATRIX

	A	B	C	D	E
A	.417320+24	-.756140+12	-.647290+10	.897500+10	.142150+11
B	-.756140+12	.137750+01	.555810-02	-.150490-01	-.268550-01
C	-.647290+10	.555810-02	.115660-01	.917610-03	-.127270-02
D	.897500+10	-.150490-01	.917610-03	.221490-02	-.300570-03
E	.142150+11	-.268550-01	-.127270-02	-.300570-03	.132710-02

LOG-LINEAR REGRESSION -- LN Y = LN A + B * LN X1 + C * LN X2 + D * LN X3 + E * LN X4 + F * LN X5 + G * LN X6

SUMMARY TABLE

NOTE -- STATISTICS ARE BASED ON LOGARITHMS

PARAMETER	VALUE	STANDARD ERROR	T-RATIO	SIGNIF LEVEL	BETA COEFF
A	.48925D+16				
LN A (CONSTANT)	36.12647	21.06777	1.71477	.13721	
B DELIV YR	-11.14925	5.54318	-2.01135	.09098	-.45141
C WRD LNTH	4.61162	3.75512	1.22809	.26540	.24847
D MEM TECH	.48772	.60495	.80622	.44981	.15376
E MIPS	.17538	.33558	.52262	.61997	.12686
F MAX MEMO	.35127	.09254	3.79597	.00901	.79603
G FLOAT PT	.79780	.32872	2.42699	.05137	.43463

CORRELATION MATRIX

VARIABLE	MEAN	STANDARD DEVIATION	LN ADJ. CPU	LN DELIV YR	LN WRD LNTH	LN MEM TECH	LN MIPS	LN MAX MEMO	LN FLOAT PT
LN Y ADJ. CPU	3.51033	.61121	1.00000	.21024	-.08233	.28601	.44768	.74163	.61821
LN X1 DELIV YR	4.34052	.02475	.21024	1.00000	.19651	.11887	.47457	.52472	.26713
LN X2 WRD LNTH	2.78165	.08267	-.08233	.19651	1.00000	.08333	-.31610	-.18148	-.19245
LN X3 MEM TECH	.65983	.15224	.28601	.11887	.08333	1.00000	.40762	.03666	.19245
LN X4 MIPS	-1.54508	.94698	.44768	.47457	-.31610	.40762	1.00000	.50279	.34069
LN X5 MAX MEMO	7.75564	1.38506	.74163	.52472	-.18148	.03666	.50279	1.00000	.34939
LN X6 FLOAT PT	.21526	.33298	.61821	.26713	-.19245	.19245	.34069	.34939	1.00000

COEFFICIENT OF DETERMINATION (UNADJ), R SQ	.84551	MEAN OF ABSOLUTE RELATIVE DEVIATIONS (LN	.05793
STANDARD ERROR OF ESTIMATE	.33975	COEFF VARIATION (STD ERR EST / MEAN Y OBS)	.09678
SUM OF SQUARES OF RESIDUALS (LN	.69257	SUM OF SQUARES TOTAL (LN	4.48298
F VALUE	5.47297	DURBIN-WATSON STATISTIC	2.08139
DEGREES OF FREEDOM FOR ERROR	6	DEGREES OF FREEDOM DUE TO REGRESSION	6
TOTAL DEGREES OF FREEDOM	12	NUMBER OF DATA POINTS	13

VARIANCE-COVARIANCE MATRIX

	LN A	B	C	D	E	F	G
LN A	.443856D+03	-.881706D+02	-.250736D+02	-.166553D+00	.737270D-01	-.390770D-01	-.185030D-01
B	-.881706D+02	.307270D+02	-.996890D+01	.548500D+00	-.789690D+00	-.180450D+00	-.234170D+00
C	-.250736D+02	-.996890D+01	.141010D+02	-.697420D+00	.557700D+00	.351570D-01	.215960D+00
D	-.166553D+00	.548500D+00	-.697420D+00	.365960D+00	-.100850D+00	.947450D-02	-.321710D-01
E	.737270D-01	-.789690D+00	.557700D+00	-.100850D+00	.112620D+00	-.799820D-02	-.194350D-02
F	-.390770D-01	-.180450D+00	.351570D-01	.947450D-02	-.799820D-02	.856340D-02	-.557780D-02
G	-.185030D-01	-.234170D+00	.215960D+00	-.321710D-01	-.194350D-02	-.557780D-02	.108060D+00

LOG-LINEAR REGRESSION -- LN Y = LN A + B * LN X1 + C * LN X2 + D * LN X3 + E * LN X4 + F * LN X5 + G * LN X6

SUMMARY TABLE

NOTE -- STATISTICS ARE BASED ON LOGARITHMS

PARAMETER		VALUE	STANDARD ERROR	T-RATIO	SIGNIF LEVEL	BETA COEFF
A		.24722D+23				
LN A	(CONSTANT)	51.56213	19.24749	2.67890	.03659	
B	DELIV YR	-14.77575	5.06425	-2.91766	.02671	-.63045
C	WRD LNTH	4.65781	3.43060	1.42766	.20330	.27596
D	MEM TECH	.41655	.55266	.75366	.47956	.15607
E	MIPS	.23721	.30659	.77371	.46848	.18363
F	MAX MEMO	.33566	.08454	4.01763	.00698	.61116
G	FLOAT PT	.76768	.30032	2.55613	.04313	.44072

CORRELATION MATRIX

VARIABLE		MEAN	STANDARD DEVIATION	LN ADJ. CPU	LN DELIV YR	LN WRD LNTH	LN MEM TECH	LN MIPS	LN MAX MEMO	LN FLOAT PT
LN Y	ADJ. CPU	3.76222	.37959	1.00000	.07068	-.11037	.27553	.41150	.68717	.59175
LN X1	DELIV YR	4.34052	.02475	.07068	1.00000	.19651	.11867	.47457	.52472	.26713
LN X2	WRD LNTH	2.76165	.03267	-.11037	.19651	1.00000	.06333	-.31610	-.16148	-.19245
LN X3	MEM TECH	.65763	.13224	.27553	.11867	.06333	1.00000	.40762	.03666	.19245
LN X4	MIPS	-1.54366	.44036	.41150	.47457	-.31610	.40762	1.00000	.50279	.34069
LN X5	MAX MEMO	7.73564	1.38598	.68717	.52472	-.16148	.03666	.50279	1.00000	.34939
LN X6	FLOAT PT	.21526	.33256	.59175	.26713	-.19245	.19245	.34069	.34939	1.00000

COEFFICIENT OF DETERMINATION (CHANGE), R SQ	.85680	MEAN OF ABSOLUTE RELATIVE DEVIATIONS (LN	.04951
STANDARD ERROR OF ESTIMATE	.31039	COEFF VARIATION (STD ERR EST / MEAN Y OBS)	.08249
SUM OF SQUARES OF RESIDUALS (LN	.57806	SUM OF SQUARES TOTAL (LN	4.03664
F VALUE	5.98306	DURBIN-WATSON STATISTIC	2.08003
DEGREES OF FREEDOM FOR ERROR	6	DEGREES OF FREEDOM DUE TO REGRESSION	6
TOTAL DEGREES OF FREEDOM	12	NUMBER OF DATA POINTS	13

VARIANCE-COVARIANCE MATRIX

	LN A	B	C	D	E	F	G
LN A	.37047D+03	-.96904D+02	-.20926D+02	-.13699D+00	.61537D-01	-.32616D-01	-.15444D-01
B	-.96904D+02	.25647D+02	-.83207D+01	.45782D+00	-.65913D+00	-.15062D+00	-.19545D+00
C	-.20926D+02	-.83207D+01	.11770D+02	-.56211D+00	.49888D+00	.29545D-01	.18027D+00
D	-.13699D+00	.45782D+00	-.56211D+00	.30545D+00	-.84156D-01	.79681D-02	-.26652D-01
E	.61537D-01	-.65913D+00	.49888D+00	-.84156D-01	.93997D-01	-.66758D-02	-.16220D-02
F	-.32616D-01	-.15062D+00	.29545D-01	.79681D-02	-.66758D-02	.71476D-02	-.46555D-02
G	-.15444D-01	-.19545D+00	.18027D+00	-.26652D-01	-.16220D-02	-.46555D-02	.90191D-01

MILITARY COSTS - MEMORY TYPE ELIMINATED - POWER FIT

POWER REGRESSION -- Y = A * X1**B * X2**C * X3**D * X4**E * X5**F

SUMMARY TABLE

PARAMETER		VALUE	INITIAL GUESS	STANDARD ERROR	T-RATIO	SIGNIF LEVEL
A	(CONSTANT)	.70547D+26	.10263D+24	************	.05774	.95557
B	DELIV YR	-17.59904	-15.74196	4.85266	-3.62668	.00843
C	WRD LNTH	6.10981	6.12636	4.23557	1.44250	.19237
D	MIPS	.17447D-01	.41432	.27091	.06440	.95045
E	MAX MEMO	.43703	.32257	.10010	4.36561	.00329
F	FLOAT PT	1.01948	.82432	.24751	4.11900	.00447

CORRELATION MATRIX

VARIABLE		MEAN	STANDARD DEVIATION	ADJ. CPU	DELIV YR	WRD LNTH	MIPS	MAX MEMO	FLOAT PT
Y	ADJ. CPU	49.75385	29.00277	1.00000	.09542	-.15490	.37448	.65008	.60931
X1	DELIV YR	76.76923	1.87767	.09542	1.00000	.19695	.40996	.54693	.27005
X2	WRD LNTH	10.15385	.55470	-.15490	.19695	1.00000	-.31951	-.19208	-.19245
X3	MIPS	.23262	.09374	.37448	.40996	-.31951	1.00000	.59511	.31561
X4	MAX MEMO	5850.76923	7331.38339	.65008	.54693	-.19208	.59511	1.00000	.29541
X5	FLOAT PT	1.30769	.48038	.60931	.27005	-.19245	.31561	.29541	1.00000

COEFFICIENT OF DETERMINATION (UNADJ). R SQ	.87077	MEAN OF ABSOLUTE RELATIVE DEVIATIONS	.23362
STANDARD ERROR OF ESTIMATE	13.65261	COEFF VARIATION (STD ERR EST / MEAN Y OBS)	.27440
SUM OF SQUARES OF RESIDUALS	1304.75609	SUM OF SQUARES TOTAL	10096.71231
F VALUE	9.43375	DURBIN-WATSON STATISTIC	2.65553
DEGREES OF FREEDOM FOR ERROR	7	DEGREES OF FREEDOM DUE TO REGRESSION	5
TOTAL DEGREES OF FREEDOM	12	NUMBER OF DATA POINTS	13

VARIANCE-COVARIANCE MATRIX

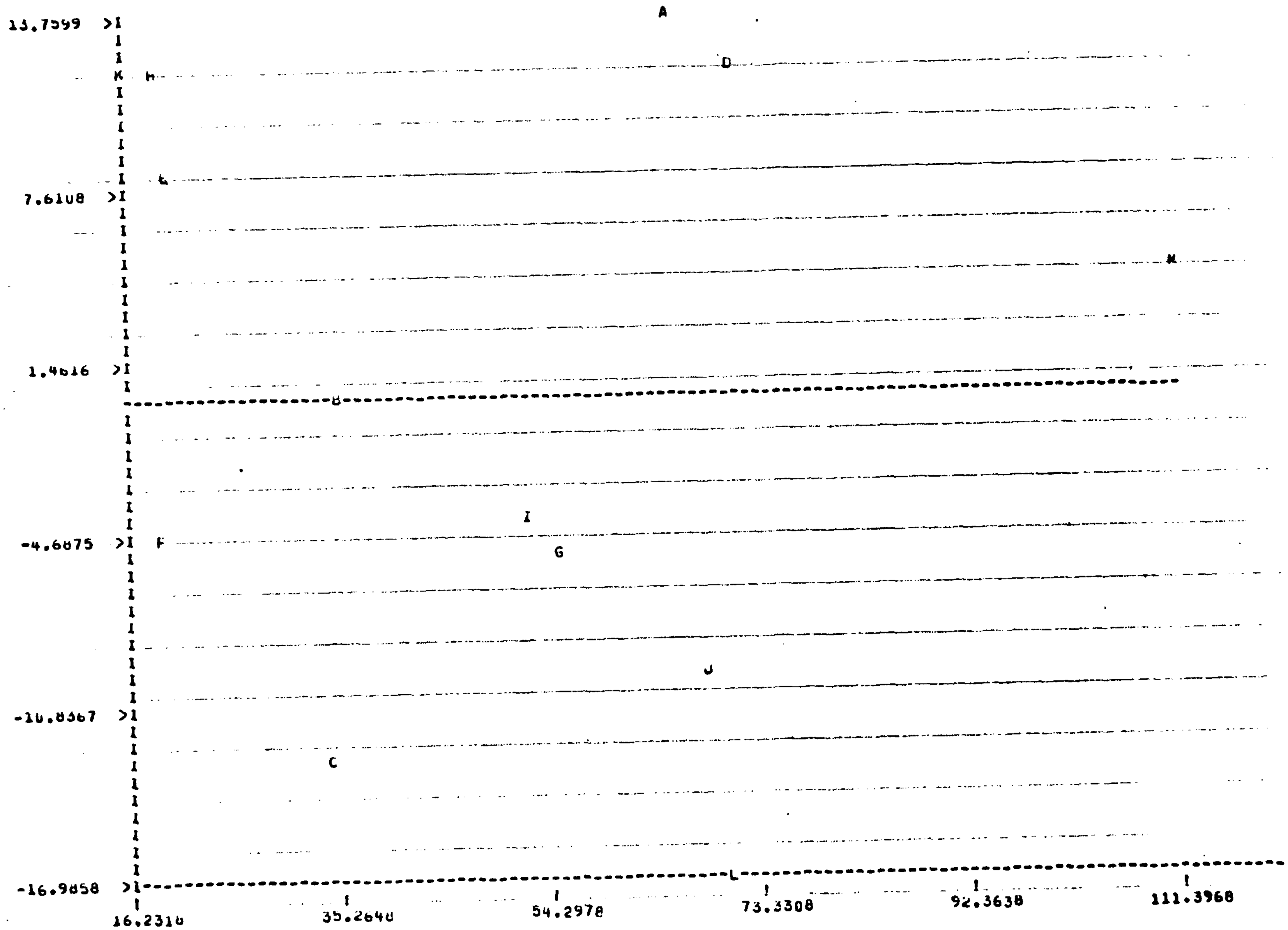
	A	B	C	D	E	F
A	.14925D+55	-.48613D+26	-.14903D+27	.80633D+26	.50368D+26	.95447D+26
B	-.48613D+26	.23548D+02	-.11235D+02	-.40141D+00	-.28682D+00	-.57709D+00
C	-.14903D+27	-.11235D+02	.17940D+02	.28405D+00	.15595D+00	.38043D+00
D	.80633D+26	-.40141D+00	.28405D+00	.73390D-01	-.99224D-02	-.42995D-02
E	.50368D+26	-.28682D+00	.15595D+00	-.99224D-02	.10021D-01	.75161D-02
F	.95447D+26	-.57709D+00	.38043D+00	-.42995D-02	.75161D-02	.61260D-01

TABLE OF RESIDUALS

COMPUTER	OBSERVED ADJ. CPU	DELIV YR	WRD LNTH	MIPS	MODIFIED MAX MEMO	FLOAT PT	COMPUTED ADJ. CPU	RESIDUAL ADJ. CPU	RELATIVE DEVIATION
A AGT 621	79.400	72.000	16.000	.112	1024.000	1.000	65.640	13.760	.173
B MCD 673	34.600	78.000	18.000	.133	1152.000	1.000	34.600	.000	.000
C PPS PA-	21.800	76.000	16.000	.116	2048.000	1.000	34.536	-12.736	-.590
D RCL MSE	83.100	80.000	16.000	.259	16384.000	2.000	71.018	12.082	.145
E RCL 160	28.400	77.000	16.000	.233	1024.000	1.000	20.397	8.003	.282
F RCL 160	14.000	76.000	16.000	.120	512.000	1.000	18.745	-4.745	-.339
G RCL 160	49.700	78.000	16.000	.333	16384.000	1.000	54.940	-5.240	-.105
H RCL 165	30.700	76.000	16.000	.327	512.000	1.000	19.076	11.624	.379
I RCL 166	48.500	76.000	16.000	.333	1024.000	2.000	52.369	-3.869	-.080
J RCL 166	59.300	77.000	16.000	.333	16384.000	1.000	68.946	-9.646	-.163
K RCL 160	28.000	73.000	16.000	.216	1024.000	1.000	16.232	11.768	.420
L UTN 117	53.100	76.000	16.000	.172	2048.000	2.000	70.086	-16.986	-.320
M UTN M2-	116.200	78.000	16.000	.337	16384.000	2.000	111.397	4.803	.041

MINIMUM RELATIVE DEVIATION = -.58963. MEAN ABSOLUTE RELATIVE DEVIATION = .23362. MAXIMUM RELATIVE DEVIATION = .42029

TRANSFORMATION FACTORS -- Y: 0.00000 X1: 0.00000 X2: 0.00000 X3: 0.00000 X4: 12.00000 X5: 0.00000



RESIDUAL ADJ. CPU VERSUS COMPUTED ADJ. CPU

CURVES REGRESSION ANALYSIS COMPUTER PROGRAM
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MILITARY COSTS - NO MEMORY OR FLOATING POINT - LINEAR FIT

LINEAR REGRESSION -- Y = A + B * X1 + C * X2 + D * X3 + E * X4

SUMMARY TABLE

PARAMETER		VALUE	STANDARD ERROR	T-RATIO	SIGNIF LEVEL	BETA COEFF
A	(CONSTANT)	499.16020	311.71685	1.60134	.14797	
B	DELIV YR	-7.79425	4.39550	-1.77320	.11413	-.52524
C	WRD LNTH	7.94124	13.04058	.60896	.55944	.15209
D	MIPS	10.87064	50.33930	.21371	.83612	.06351
E	MAX MEMO	.35051E-02	.00116	3.03252	.01625	.94331

CORRELATION MATRIX

VARIABLE		MEAN	STANDARD DEVIATION	ADJ. CPU	DELIV YR	WRD LNTH	MIPS	MAX MEMO
Y	ADJ. CPU	54.41538	27.66347	1.00000	.04786	-.14602	.35907	.66347
X1	DELIV YR	76.76923	1.87767	.04786	1.00000	.19695	.40996	.54693
X2	WRD LNTH	16.15385	.55470	-.14602	.19695	1.00000	-.31931	-.19208
X3	MIPS	.23222	.09374	.35907	.40996	-.31931	1.00000	.59511
X4	MAX MEMO	5030.76923	7601.[illegible]	.66347	.54693	-.19208	.59511	1.00000

COEFFICIENT OF DETERMINATION (UNADJ), R SQ	.60051	MEAN OF ABSOLUTE RELATIVE DEVIATIONS	.28317
STANDARD ERROR OF ESTIMATE	21.57458	COEFF VARIATION (STD ERR EST / MEAN Y OBS)	.39648
SUM OF SQUARES OF RESIDUALS	3723.69944	SUM OF SQUARES TOTAL	9316.47692
F VALUE	3.00580	DURBIN-WATSON STATISTIC	1.41753
DEGREES OF FREEDOM FOR ERROR	8	DEGREES OF FREEDOM DUE TO REGRESSION	4
TOTAL DEGREES OF FREEDOM	12	NUMBER OF DATA POINTS	13

VARIANCE-COVARIANCE MATRIX

	A	B	C	D	E
A	.97[illegible]E+05	-.[illegible]E+03	-.203[illegible]E+04	-.10269E+04	-.42136D-02
B	-.[illegible]E+03	.19321[illegible]E+02	-.23947[illegible]E+02	-.95605E+02	-.23270D-02
C	-.20364[illegible]E+04	-.23947[illegible]E+02	.170[illegible]E+03	.38218E+03	.29180D-02
D	-.10269[illegible]E+04	-.95605[illegible]E+02	.38218[illegible]E+03	.76038[illegible]E+04	-.40431D-01
E	-.42136[illegible]-02	-.23270[illegible]-02	.29180[illegible]-02	-.40431[illegible]-01	.13977D-05

POWER REGRESSION -- Y = A * X1**B * X2**C * X3**D * X4**E

SUMMARY TABLE

PARAMETER	VALUE	INITIAL GUESS	STANDARD ERROR	T-RATIO	SIGNIF LEVEL
A (CONSTANT)	.14115D+19	.13262D***************		.04127	.96809
B DELIV YR	-10.47764	-12.99086	6.16530	-1.69379	.12876
C WRD LNTH	1.92502	4.32562	5.49090	.35022	.73522
D MIPS	.87285D-01	.40144	.40383	.21584	.83451
E MAX MEMO	.30986	.32577	.12436	2.48599	.03776

CORRELATION MATRIX

VARIABLE	MEAN	STANDARD DEVIATION	ADJ. CPU	DELIV YR	WRD LNTH	MIPS	MAX MEMO
Y ADJ. CPU	54.41356	27.66347	1.00000	.04786	-.14682	.35907	.66347
X1 DELIV YR	76.76923	1.87767	.04786	1.00000	.19695	.40996	.54693
X2 WRD LNTH	16.15385	.55470	-.14682	.19695	1.00000	-.31931	-.19208
X3 MIPS	.23262	.05374	.35907	.40996	-.31931	1.00000	.59511
X4 MAX MEMO	5830.76923	7331.33339	.66347	.54693	-.19208	.59511	1.00000

COEFFICIENT OF DETERMINATION (CRADJ), R S.	.57101	MEAN OF ABSOLUTE RELATIVE DEVIATIONS	.25782
STANDARD ERROR OF ESTIMATE	22.35146	COEFF VARIATION (STD ERR EST / MEAN Y OBS)	.41076
SUM OF SQUARES OF RESIDUALS	3996.70033	SUM OF SQUARES TOTAL	9316.47652
F VALUE	2.66204	DURBIN-WATSON STATISTIC	1.77729
DEGREES OF FREEDOM FOR ERROR	8	DEGREES OF FREEDOM DUE TO REGRESSION	4
TOTAL DEGREES OF FREEDOM	12	NUMBER OF DATA POINTS	13

VARIANCE-COVARIANCE MATRIX

	A	B	C	D	E
A	.11704D+40	-.17446D+21	-.26301D+20	.47403D+19	.97033D+18
B	-.17446D+21	.30265D+02	-.15025D+02	-.11396D+01	-.28338D+00
C	-.26301D+20	-.15025D+02	.301[illegible]0D+02	.72200D+00	.13677D+00
D	.47403D+19	-.11396D+01	.72200D+00	.16300D+00	-.21155D-01
E	.97033D+18	-.28338D+00	.13677D+00	-.21155D-01	.15515D-01

MILITARY COSTS - NO MEMORY OR FLOATING POINT - LOG-LINEAR FIT

LOG-LINEAR REGRESSION -- LN Y = LN A + B * LN X1 + C * LN X2 + D * LN X3 + E * LN X4

SUMMARY TABLE

NOTE -- STATISTICS ARE BASED ON LOGARITHMS

PARAMETER		VALUE	STANDARD ERROR	T-RATIO	SIGNIF LEVEL	BETA COEFF
A		.13262E+21				
LN A	(CONSTANT)	46.32951	21.36042	2.16894	.06192	
B	DELIV YR	-12.99062	5.53605	-2.34656	.04693	-.63388
C	WRD LNTH	4.32082	3.60542	1.19981	.26454	.27663
D	MIPS	.40144	.29455	1.36287	.21064	.55558
E	MAX MEMO	.52377	.09464	5.53360	.00770	.88423

CORRELATION MATRIX

VARIABLE		MEAN	STANDARD DEVIATION	LN ADJ. CPU	LN DELIV YR	LN WRD LNTH	LN MIPS	LN MAX MEMO
LN Y	ADJ. CPU	3.67925	.50716	1.00000	.05350	-.10105	.41106	.68531
LN X1	DELIV YR	4.34052	.02475	.05350	1.00000	.19651	.47457	.52472
LN X2	WRD LNTH	2.78165	.03267	-.10105	.19651	1.00000	-.31610	-.16148
LN X3	MIPS	-1.54506	.44673	.41106	.47457	-.31610	1.00000	.50279
LN X4	MAX MEMO	7.77504	1.38509	.68531	.52472	-.16148	.50279	1.00000

COEFFICIENT OF DETERMINATION (UNADJ), R SQ	.68996	MEAN OF ABSOLUTE RELATIVE DEVIATIONS (LN	.05591
STANDARD ERROR OF ESTIMATE	.34588	COEFF VARIATION (STD ERR EST / MEAN Y OBS)	.08915
SUM OF SQUARES OF RESIDUALS (LN	.95686	SUM OF SQUARES TOTAL (LN	3.08654
F VALUE	4.49125	DURBIN-WATSON STATISTIC	1.83787
DEGREES OF FREEDOM FOR ERROR	8	DEGREES OF FREEDOM DUE TO REGRESSION	4
TOTAL DEGREES OF FREEDOM	12	NUMBER OF DATA POINTS	13

VARIANCE-COVARIANCE MATRIX

	LN A	B	C	D	E
LN A	.45627E+03	-.70646E+02	-.25982E+02	.76399E-01	-.40493D-01
B	-.70646E+02	.30648E+02	-.89637E+01	-.68150E+00	-.21039D+00
C	-.25982E+02	-.89637E+01	.12999E+02	.43670E+00	.62368D-01
D	.76399E-01	-.68150E+00	.43670E+00	.86760E-01	-.60079D-02
E	-.40493E-01	-.21039E+00	.62368E-01	-.60079E-02	.83978D-02

SEMILOG REGRESSION -- LN Y = A + B * X1 + C * X2

SUMMARY TABLE

NOTE -- STATISTICS ARE BASED ON LOGARITHMS

PARAMETER		VALUE	STANDARD ERROR	T-RATIO	SIGNIF LEVEL	BETA COEFF
A	(CONSTANT)	13.49538	1.64518	8.20177	.00000	
B	DELIV YR	-.17816	.02135	-8.34472	.00000	-.62314
C	CYCLE	-.65534D-01	.12658	-.51774	.60566	-.03866

CORRELATION MATRIX

VARIABLE		MEAN	STANDARD DEVIATION	LN CNTS/BIT	DELIV YR	CYCLE
LN Y	CNTS/BIT	-.15723	.70199	1.00000	-.61859	.03476
X1	DELIV YR	76.32174	2.45503	-.61859	1.00000	-.11783
X2	CYCLE	.78620	.41414	.03476	-.11783	1.00000

COEFFICIENT OF DETERMINATION (UNADJ), R SQ	.38412	MEAN OF ABSOLUTE RELATIVE DEVIATIONS (LN	1.96724
STANDARD ERROR OF ESTIMATE	.55581	COEFF VARIATION (STD ERR EST / MEAN Y OBS)	-3.53493
SUM OF SQUARES OF RESIDUALS (LN	34.59898	SUM OF SQUARES TOTAL (LN	56.17826
F VALUE	34.92705	DURBIN-WATSON STATISTIC	1.27553
DEGREES OF FREEDOM FOR ERROR	112	DEGREES OF FREEDOM DUE TO REGRESSION	2
TOTAL DEGREES OF FREEDOM	114	NUMBER OF DATA POINTS	115

VARIANCE-COVARIANCE MATRIX

	A	B	C
A	.27066D+01	-.34314D-01	-.12421D-01
B	-.34314D-01	.45553D-03	.31846D-03
C	-.12421D-01	.31846D-03	.16022D-01

CURVES REGRESSION ANALYSIS COMPUTER PROGRAM
(JULY 1976)

COMMERCIAL REPORT VS. YEAR AND CYCLE TIME - SEMICONDUCTOR - LINEAR FIT   DATE: 06/24/80 TIME: 11.51.26. PAGE: 1

LINEAR REGRESSION -- Y = A + B * X1 + C * X2

SUMMARY TABLE

PARAMETER	VALUE	STANDARD ERROR	T-RATIO	SIGNIF LEVEL	BETA COEFF
A (CONSTANT)	25.62612	3.27482	7.82520	.00000	
B DELIV YR	-.31563	.04245	-7.42765	.00000	-.57752
C CYCLE	-.635866E-01	.25751	-.24690	.80543	-.01920

CORRELATION MATRIX

VARIABLE	MEAN	STANDARD DEVIATION	CNTS/BIT	DELIV YR	CYCLE
Y CNTS/BIT	1.47656	1.34692	1.00000	-.57537	.04549
X1 DELIV YR	76.35652	2.46445	-.57537	1.00000	-.11200
X2 CYCLE	.77681	.40669	.04549	-.11200	1.00000

COEFFICIENT OF DETERMINATION (UNADJ). R SQ	.33141	MEAN OF ABSOLUTE RELATIVE DEVIATIONS	.60794
STANDARD ERROR OF ESTIMATE	1.11113	COEFF VARIATION (STD ERR EST / MEAN Y OBS)	.75280
SUM OF SQUARES OF RESIDUALS	138.27616	SUM OF SQUARES TOTAL	206.81736
F VALUE	27.75026	DURBIN-WATSON STATISTIC	1.54295
DEGREES OF FREEDOM FOR ERROR	112	DEGREES OF FREEDOM DUE TO REGRESSION	2
TOTAL DEGREES OF FREEDOM	114	NUMBER OF DATA POINTS	115

VARIANCE-COVARIANCE MATRIX

	A	B	C
A	.10724E+02	-.136150E+00	-.506640E-01
B	-.136150E+00	.180058E-02	.122560E-02
C	-.506640E-01	.122560E-02	.663100E-01

COMMERCIAL MEMORY VS. YEAR AND CYCLE TIME - SEMICONDUCTOR - SEMI-LOG (LN Y) DATE: 06/24/80 TIME: 11.51.26. PAGE: 14

SEMILOG REGRESSION -- LN Y = A + B * X1 + C * X2

SUMMARY TABLE

NOTE -- STATISTICS ARE BASED ON LOGARITHMS

PARAMETER	VALUE	STANDARD ERROR	T-RATIO	SIGNIF LEVEL	BETA COEFF
A (CONSTANT)	16.64975	1.71467	9.71017	.00000	
B DELIV YR	-.21621	.02225	-9.71757	.00000	-.68028
C CYCLE	-.84951D-01	.13483	-.62991	.53004	-.04410

CORRELATION MATRIX

VARIABLE	MEAN	STANDARD DEVIATION	LN CNTS/BIT	DELIV YR	CYCLE
LN Y CNTS/BIT	.07441	.78323	1.00000	-.67534	.03210
X1 DELIV YR	76.35652	2.46445	-.67534	1.00000	-.11200
X2 CYCLE	.77661	.40629	.03210	-.11200	1.00000

COEFFICIENT OF DETERMINATION (UNADJ), R SQ	.45801	MEAN OF ABSOLUTE RELATIVE DEVIATIONS (LN	1.28388
STANDARD ERROR OF ESTIMATE	.58176	COEFF VARIATION (STD ERR EST / MEAN Y OBS)	7.81806
SUM OF SQUARES OF RESIDUALS (LN	37.90833	SUM OF SQUARES TOTAL (LN	69.94222
F VALUE	47.32199	DURBIN-WATSON STATISTIC	1.23201
DEGREES OF FREEDOM FOR ERROR	112	DEGREES OF FREEDOM DUE TO REGRESSION	2
TOTAL DEGREES OF FREEDOM	114	NUMBER OF DATA POINTS	115

VARIANCE-COVARIANCE MATRIX

	A	B	C
A	.29401E+01	-.37326E-01	-.13944D-01
B	-.37326E-01	.49565E-03	.33600D-03
C	-.13944E-01	.33600E-03	.18179D-01

CIVILIAN MEMORY VS. YEAR AND CYCLE TIME - CORE - EXPONENTIAL FIT DATE: 05/21/80 TIME: 17.54.21. PAGE: 30

EXPONENTIAL REGRESSION -- Y = EXP(A + B * X1 + C * X2)

SUMMARY TABLE

PARAMETER	VALUE	INITIAL GUESS	STANDARD ERROR	T-RATIO	SIGNIF LEVEL
A (CONSTANT)	28.04221	15.60409	2.03527	13.77811	.00000
B DELIV YR	-.35876	-.20329	.02977	-12.05092	.00000
C CYCLE	-.99644	.10589D-01	.11511	-8.65670	.00000

CORRELATION MATRIX

VARIABLE	MEAN	STANDARD DEVIATION	CNTS/BIT	DELIV YR	CYCLE
Y CNTS/BIT	4.35185	7.45593	1.00000	-.59325	.18309
X1 DELIV YR	72.90000	3.41197	-.59325	1.00000	-.53212
X2 CYCLE	1.12367	.74522	.18309	-.53212	1.00000

COEFFICIENT OF DETERMINATION (UNADJ), R SQ	.67306
STANDARD ERROR OF ESTIMATE	4.31182
SUM OF SQUARES OF RESIDUALS	1617.48409
F VALUE	89.55846
Y INTERCEPT	1508613806286.96875
DEGREES OF FREEDOM FOR ERROR	87
TOTAL DEGREES OF FREEDOM	89
MEAN OF ABSOLUTE RELATIVE DEVIATIONS	.90620
COEFF VARIATION (STD ERR EST / MEAN Y OBS)	.99079
SUM OF SQUARES TOTAL	4947.58478
DURBIN-WATSON STATISTIC	1.34697
DEGREES OF FREEDOM DUE TO REGRESSION	2
NUMBER OF DATA POINTS	90

VARIANCE-COVARIANCE MATRIX

	A	B	C
A	.41423D+01	-.60493D-01	-.90422D-01
B	-.60493D-01	.88627D-03	.11690D-02
C	-.90422D-01	.11690D-02	.13249D-01

CURVES REGRESSION ANALYSIS COMPUTER PROGRAM
(JULY 1976)

COMMERCIAL MEMORY VS. YEAR AND CYCLE TIME - CORE - LINEAR FIT

LINEAR REGRESSION -- Y = A + B * X1 + C * X2

SUMMARY TABLE

PARAMETER	VALUE	STANDARD ERROR	T-RATIO	SIGNIF LEVEL	BETA COEFF
A (CONSTANT)	165.79765	26.01595	7.14222	.00000	
B DELIV YR	-2.41567	.34321	-7.03255	.00000	-.70187
C CYCLE	-2.83216	1.57191	-1.80175	.07513	-.17982

CORRELATION MATRIX

VARIABLE	MEAN	STANDARD DEVIATION	CNTS/BIT	DELIV YR	CYCLE
Y CNTS/BIT	6.69176	11.63756	1.00000	-.60656	.19217
X1 DELIV YR	72.86636	3.44224	-.60656	1.00000	-.53000
X2 CYCLE	1.12564	.75159	.19217	-.53000	1.00000

COEFFICIENT OF DETERMINATION (UNADJ), R SQ	.39117
STANDARD ERROR OF ESTIMATE	9.34457
SUM OF SQUARES OF RESIDUALS	7422.27984
F VALUE	27.30636
DEGREES OF FREEDOM FOR ERROR	85
TOTAL DEGREES OF FREEDOM	87
MEAN OF ABSOLUTE RELATIVE DEVIATIONS	2.14501
COEFF VARIATION (STD ERR EST / MEAN Y OBS)	1.39644
SUM OF SQUARES TOTAL	12191.11604
DURBIN-WATSON STATISTIC	1.28124
DEGREES OF FREEDOM DUE TO REGRESSION	2
NUMBER OF DATA POINTS	88

VARIANCE-COVARIANCE MATRIX

	A	B	C
A	.67675E+03	-.61740E+01	-.19965E+01
B	-.61740E+01	.11720E+00	.28594E+00
C	-.19965E+01	.28594E+00	.24705E+01

COMMERCIAL MEMORY VS. YEAR AND CYCLE TIME - CORE - EXPONENTIAL FIT　　DATE: 06/23/80 TIME: 14.03.36. PAGE: 6

EXPONENTIAL REGRESSION -- Y = EXP(A + B * X1 + C * X2)

SUMMARY TABLE

PARAMETER	VALUE	INITIAL GUESS	STANDARD ERROR	T-RATIO	SIGNIF LEVEL
A (CONSTANT)	28.89661	17.52683	2.10678	13.71600	.00000
B DELIV YR	-.36561	-.22478	.03085	-11.83190	.00000
C CYCLE	-.98604	.136140-01	.11515	-8.56310	.00000

CORRELATION MATRIX

VARIABLE	MEAN	STANDARD DEVIATION	CNTS/BIT	DELIV YR	CYCLE
Y CNTS/BIT	6.69170	11.83755	1.00000	-.60656	.19217
X1 DELIV YR	72.98636	3.44224	-.60656	1.00000	-.53000
X2 CYCLE	1.12564	.75159	.19217	-.53000	1.00000

COEFFICIENT OF DETERMINATION (UNADJ), R SQ	.68108	MEAN OF ABSOLUTE RELATIVE DEVIATIONS	.92292
STANDARD ERROR OF ESTIMATE	6.76324	COEFF VARIATION (STD ERR EST / MEAN Y OBS)	1.01069
SUM OF SQUARES OF RESIDUALS	3888.02085	SUM OF SQUARES TOTAL	12191.11604
F VALUE	90.76125	DURBIN-WATSON STATISTIC	1.37591
Y INTERCEPT	3545188620736.87167		
DEGREES OF FREEDOM FOR ERROR	85	DEGREES OF FREEDOM DUE TO REGRESSION	2
TOTAL DEGREES OF FREEDOM	87	NUMBER OF DATA POINTS	88

VARIANCE-COVARIANCE MATRIX

	A	B	C
A	.443850+01	-.648940-01	-.955870-01
B	-.648940-01	.951710-03	.124500-02
C	-.955870-01	.124500-02	.132590-01

CURVES REGRESSION ANALYSIS COMPUTER PROGRAM
(JULY 1976)

MILITARY MEMORY VS. YEAR AND CYCLE TIME - CORE - LINEAR FIT

LINEAR REGRESSION -- Y = A + B * X1 + C * X2

SUMMARY TABLE

PARAMETER	VALUE	STANDARD ERROR	T-RATIO	SIGNIF LEVEL	BETA COEFF
A (CONSTANT)	29.59671	49.45330	.59846	.56428	
B DELIV YR	-.25527	.57841	-.43787	.67160	-.18948
C CYCLE	-4.96832	6.71464	-.73990	.47822	-.32018

CORRELATION MATRIX

VARIABLE	MEAN	STANDARD DEVIATION	CNTS/BIT	DELIV YR	CYCLE
Y CNTS/BIT	4.87917	2.60149	1.00000	.02313	-.19435
X1 DELIV YR	76.83333	1.94625	.02313	1.00000	-.66404
X2 CYCLE	1.05833	.16765	-.19435	-.66404	1.00000

COEFFICIENT OF DETERMINATION (UNADJ), R SQ	.05764	MEAN OF ABSOLUTE RELATIVE DEVIATIONS	.42476
STANDARD ERROR OF ESTIMATE	2.79163	COEFF VARIATION (STD ERR EST / MEAN Y OBS)	.57215
SUM OF SQUARES OF RESIDUALS	70.15884	SUM OF SQUARES TOTAL	74.44509
F VALUE	.27626	DURBIN-WATSON STATISTIC	1.26529
DEGREES OF FREEDOM FOR ERROR	9	DEGREES OF FREEDOM DUE TO REGRESSION	2
TOTAL DEGREES OF FREEDOM	11	NUMBER OF DATA POINTS	12

VARIANCE-COVARIANCE MATRIX

	A	B	C
A	.24456D+04	-.14371D+02	-.26678D+02
B	-.14371D+02	.33426D+00	.25791D+01
C	-.26678D+02	.25791D+01	.45029D+02

MILITARY MEMORY VS. YEAR AND CYCLE TIME - CORE - EXPONENTIAL FIT   DATE: 06/23/80 TIME: 13.44.42. PAGE: 4

EXPONENTIAL REGRESSION -- Y = EXP(A + B * X1 + C * X2)

SUMMARY TABLE

PARAMETER	VALUE	INITIAL GUESS	STANDARD ERROR	T-RATIO	SIGNIF LEVEL
A (CONSTANT)	10.16071	6.74431	10.55532	.96262	.36089
B DELIV YR	-.87915D-01	-.56978D-01	.12654	-.69476	.50473
C CYCLE	-1.74065	-.83618	1.47565	-1.18502	.26656

CORRELATION MATRIX

VARIABLE	MEAN	STANDARD DEVIATION	CNTS/BIT	DELIV YR	CYCLE
Y CNTS/BIT	4.87917	2.60149	1.00000	.02313	-.19435
X1 DELIV YR	76.83333	1.94625	.02313	1.00000	-.66404
X2 CYCLE	1.05333	.16765	-.19435	-.66404	1.00000

COEFFICIENT OF DETERMINATION (UNADJ). R SQ	.09436	MEAN OF ABSOLUTE RELATIVE DEVIATIONS	.41574
STANDARD ERROR OF ESTIMATE	2.73760	COEFF VARIATION (STD ERR EST / MEAN Y OBS)	.56096
SUM OF SQUARES OF RESIDUALS	67.42054	SUM OF SQUARES TOTAL	74.44509
F VALUE	.46687	DURBIN-WATSON STATISTIC	1.23337
Y INTERCEPT	25666.78044		
DEGREES OF FREEDOM FOR ERROR	9	DEGREES OF FREEDOM DUE TO REGRESSION	2
TOTAL DEGREES OF FREEDOM	11	NUMBER OF DATA POINTS	12

VARIANCE-COVARIANCE MATRIX

	A	B	C
A	.11141D+03	-.13255D+01	-.94285D+01
B	-.13255D+01	.16011D-01	.94034D-01
C	-.94285D+01	.94034D-01	.21781D+01

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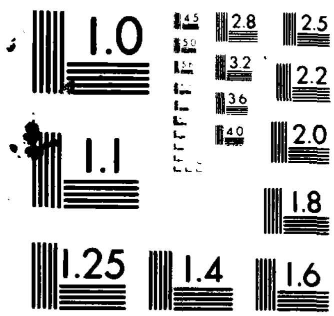

MICROCOPY RESOLUTION TEST CHART

NATIONAL BUREAU OF STANDARDS 1963 A

APPENDIX C

MANUFACTURERS' CODES

Commercial

1. AID Advanced Information Design, Inc.
2. AJI Anderson-Jacobson, Inc.
3. BUR Burroughs Corporation
4. CAD Cado Systems Corporation
5. CDI Cascade Data, Inc.
6. CDP California Data Processors
7. CCC Century Computer Corporation
8. CMC Cincinnati Milacron, Inc.
9. CAI Computer Automation, Inc.
10. CHI Computer Hardware, Inc.
11. CDC Control Data Corporation
12. CSP CSP, Inc.
13. DGC Data General Computer
14. DPC Datapoint Corporation
15. DCC Digital Computer Controls
16. DEC Digital Equipment Corporation
17. DGI Digital Group, Inc.
18. DSC Digital Scientific Corporation
19. DSY Digital Systems Corporation
20. FAI Functional Automation, Inc.
21. GAI General Automation, Inc.
22. GRI GRI Computer Corporation
23. HCP Harris Corporation
24. HPC Hewlett-Packard Company
25. HON Honeywell Information Systems, Inc.
26. IBM International Business Machines Corporation
27. LEC Lockheed Electronics Company
28. MDC Microdata Corporation
29. MOD Modular Computer Systems, Inc.

Commercial (Cont'd)

30. NDC Nanodata Corporation
31. NDI Nuclear Data, Inc.
32. PEC Perkin Elmer Computer Systems Division
33. PBS Philips Business Systems, Inc.
34. PPS Plessey Peripheral Systems, Inc.
35. PCI Prime Computer, Inc.
36. RDS Raytheon Data Systems Company
37. SUD Sperry Univac Division, Sperry Rand Corporation
38. SEL Systems Engineering Laboratories, Inc.
39. TAN Tandem Computers, Inc.
40. TEK Tektronix, Inc.
41. TII Texas Instruments, Inc.
42. WLI Wang Laboratories, Inc.
43. WEC Westinghouse Electric Corporation

Military

1. AUT Autonetics Division, Rockwell Corporation
2. HON Honeywell Information Systems, Inc.
3. PPS Plessey Peripheral Systems, Inc.
4. ROL Rolm Corporation
5. UTN United Technologies, Norden Division

APPENDIX D

DERIVATION OF MIPS FORMULAS

The basic formulas shown in equations (a) and (d) below are from Dr. Rein Turn's publications*:

(a) For CPUs with hardware or software multiply, and multiplication time datum available:

$$MIPS = \frac{1}{0.7(t_a) + 0.3(t_m) + 2.0(t_{mc})}$$

(b) For CPUs with software multiply, but multiplication time datum not available (assumes $t_m = 10(t_a)$:

$$MIPS = \frac{1}{3.7(t_a) + 2.0(t_{mc})}$$

(c) For CPUs with hardware multiply, but multiplication time datum not available (assumes $t_m = 6(t_a)$:

$$MIPS = \frac{1}{2.5(t_a) + 2.0(t_{mc})}$$

(d) For CPUs with hardware or software multiply, multiplication time datum available, and has "look ahead" pipeline feature:

$$MIPS = \frac{1}{0.7(t_a) + 0.3(t_m) + 2.0(k)\ (t_{mc})}$$

where:

t_a = instruction execution add time, microseconds

t_m = instruction execution multiply time, microseconds

t_{mc} = memory cycle time, microseconds

k = look ahead factor (1.0 = no look ahead)

* (1) Kennedy, J.R., et al, Advanced Data Processing Technology, CDRL A004, TRW Report 32 304-6921-008, 15 July 1978.

(2) Turn, Rein, Computers in the 1980's, Columbia University Press, 1974.

For some computer models, the multiplication execution times were not available, so equations (b) and (c) had to be developed. Equations (b) and (c) were derived from the general equation (a) by inserting separate average multiplication factors for software and hardware cases where the actual multiplication times were not known. The average factors were 6 times add time for hardware multiply CPUs, and 10 times for software multiply (i.e., performed by programmed subroutines). These factors were empirically - derived from the data shown in Tables D.1 and D.2.

It has been pointed out by some experts that the 30 percent multiply instructions assumed in all the equations may be conservative (i.e., too high of a percentage). Consequently, the calculated MIPS values may also be conservative (i.e., estimated MIPS may be low).

TABLE D.1

PROCESSORS WITH HARDWARE MULTIPLY/DIVIDE AS STANDARD

	FIXED POINT ADD	FIXED POINT MULTIPLY	FACTOR RELATIONSHIP
DEC PDP 11/55	0.97	3.89	4.0
DEC VAX 11/780	0.4	3.4	8.5
CAI LSI-2	4.1	14.8	3.6
CAI LSI-4/90	1.5	11.9	7.9
CAI SYFA	2.4	12.8	5.3
CDC 18-17A	1.8	17.4	9.7
CDC 18-20	1.76	6.6	12.0
DGC C/330	0.6	7.2	12.0
HPC HP2100	1.96	10.8	5.5
HP21Mx	1.94	13.0	6.7
HP1000M	1.9	12.5	6.6
HP3000-III	0.55	5.25	9.5
HON 6/06	2.0	8.8	4.4
HON 6/34	1.9	12.7	6.7
PEC 6/16	0.9	6.6	7.3
8/16	0.75	9.25	12.3
8/32C	0.4	2.7	6.8
3240	0.85	3.84	4.5
MDC 3200	0.41	5.2	12.7
7870	0.2	1.2	6.0
7830	0.2	1.3	6.5
Modcomp IV	0.64	3.5	5.5
PCI 550	0.56	4.2	7.5
PCI 750	0.24	1.38	5.8
SEL 32/35	1.8	6.2	3.4
SEL 32/75	1.2	5.5	4.6
TII 960B	3.6	8.6	2.4
TII 980B	1.75	2.65	1.5
SUD V77-400	1.32	5.94	4.5
SUD V77-600	0.74	4.79	6.5
SUD V77-200	2.31	5.11	2.2

Average of 32 factor relationships, $\frac{198.2}{32} = 6.19$ (use 6 rounded)

TABLE D.2

PROCESSORS WITH SOFTWARE MULTIPLY/DIVIDE

	FIXED POINT ADD	MULTIPLY	FACTOR RELATIONSHIP
DEC PDP 11/04	3.2	9.9	3.09
DEC PDP 11/34A	2.03	8.9	4.38
DEC PDP 11/45	.30	3.3	11.0
DEC PDP 11/35	1.07	9.16	8.56
DGC Nova 4/C	0.4	4.4	10.0
DGC Nova 4/X	0.2	4.4	20.0
PEC 50	3.25	19.4	5.97
PEC 74	1.5	34.0	22.7
IBM Series/1, Model 5	2.64	10.78	4.8

Average of 9 factor relationships, $\frac{89.78}{9} = 9.98$

Use 10 rounded

NOTE: These processors perform multiplies and divides by programmed subroutines.

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