3-D Interconnects Using Cu Wafer Bonding : Technology and Applications

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Abstract

3-D interconnects hold tremendous potential to reduce global interconnect latency and power dissipation. Moreover, it allows heterogeneous integration, i.e., monolithic integration of different technologies (e.g., logic, memory, and RF). This paper explores the opportunities and challenges of the 3-D integration approach by low temperature direct Cu-to-Cu wafer bonding. A thorough description of process integration will be given and key technological challenges will be highlighted. In particular, interfacial morphologies of low temperature Cu-to-Cu wafer bonding at 400 ^{o}C have been characterized structurally. Microstructure examination results show excellent bonding properties. In addition, CAD tools for 3-D IC design and layout are being developed. Potential 3-D applications to system-on-a-chip will be discussed.

Introduction

While dimensional scaling has consistently improved device gate switching delay, it has a reverse effect on global interconnects [1]. The global interconnects RC delay has increasingly become the circuit performance limiting factor especially in the deep sub-micron regime. Even though Cu/low-K material systems have been introduced to improve the interconnect's RC delay, they are not a long-term solution. This is because the diffusion barrier material used in Cu metallization is of a finite thickness and has higher resistivity than Cu resulting in a higher effective resistivity than bulk Cu. The surface electron scattering effect and high operating temperature make the situation worse [2]. When chip size continues to increase to accommodate more functionality, the total interconnect's length increases at the same time. This causes tremendous amount of power being dissipated unnecessarily in the interconnects.

To seek a long-term solution, the ITRS has outlined 3-D interconnects as one of the promising options that allows shorter global interconnects and hence improved RC delay [3]. Shorter global interconnects can also lower power dissipation. High density device packaging and heterogeneous systems integration are among other potential advantages offered by the 3-D integration approach. This paper will discuss the opportunity for 3-D integration using a novel Cu-Cu wafer bonding approach. In addition, we will discuss the progress of CAD tools development works intended for 3-D integration. We will also highlight potential 3-D applications, specifically system-on-a-chip application and benefits offered by 3-D integration in terms of noise and crosstalk reduction.

Overview of 3-D Research

There are research efforts on a few possible technology options to realize a 3-D structure, either using recrystallization [4,5] or wafer bonding [6-8]. Subramanian *et al.* [4] reported 100-nm TFT devices having on-off current ratio > 10^6 and subthreshold slope of 107 mV/dec hence attesting the suitability of Germanium-seeding for fabrication of high performance TFT, suitable for use in vertically integrated three-dimensional (3-D) circuits. Chan *et al.* [5] used recrystallization of amorphous silicon by metal-(Nickel)-induced-lateral-crystallization (MILC) to demonstrate a 3-D ring oscillator with lower propagation delay than that of a 2-D circuit.

While the recrystallization technique finds specifics applications in memory devices, it is not suitable for other applications. Thermal budget imposed by the first layer and imperfect crystallization of the second layer make this technique less attractive. Another approach that is under intense research is the wafer bonding approach. The wafer bonding option can be done by using a dielectric or a conductive layer at the bonding interface. Lu *et al.* [7] have demonstrated the potential of wafer bonding using dielectric glue (Flare) as a baseline process for 3-D interconnects. Using Low Temperature Oxide (LTO) bonding, Warner *et al*. [8] have fabricated operational 3-D ring oscillators and via chains.

Our 3-D approach is based on earlier work on Cu-Cu wafer bonding [6].

3-D Process Flow

Three-dimensional integrated circuit (3-D IC) is a vertical stack consisting of multiple device and interconnect layers that are connected together by interlayer vertical vias. In our 3-D integration scheme, two FEOL active device wafers are stacked in a back-to-face fashion and bonded together by means of low temperature Cu-to-Cu thermo compression. Interlayer vertical vias electrically interconnect the device layers together. Low temperature wafer bonding is necessary since the pre-bonding device layers already have Al metal interconnect lines. This is an attractive scheme because it allows lower aspect ratio interlayer vertical vias and thinner bonding layer. We will briefly discuss the process sequence in this proposed 3-D integration scheme as illustrated in Fig. 1(a)-(f) and technological challenges will be highlighted.

Handle wafer attachment

Figure 1(a)-(f) depicts the process sequence to fabricate a 3-D CMOS inverter. The bottom device layer is an nMOS device fabricated on bulk Si while the top device layer is a pMOS device fabricated on SOI wafer independently prior to the 3-D integration. To start with, the front side of the top layer is attached to a handle wafer as shown in Fig. 1(b). A handle wafer is needed to provide mechanical strength and for ease of wafer handling. Therefore, the bonding has to be strong enough to hold the SOI wafer during subsequent processes. Note that this bonding is a sacrificial one, as the handle wafer will be released from the final 3-D stack. This dictates the ease of handle wafer release at the end. There are a few bonding options currently under investigation, either using an adhesive [9] or metallic [10] bonding interface. This work is based on Cu-to-Cu bonding to form a SOI (Device Wafer)/Zr/Cu-Cu/Zr/Si (Handle Wafer) stack.

Zr plays a role during handle wafer release and this will be explained in a following subsection.

SOI Thin Back

In Fig. 1(c), the SOI substrate is ready to be thinned back after handle wafer attachment. A combination of mechanical grinding, plasma dry etch and chemical wet etch can be used for this thinning step. In order to achieve good etch stop behavior, it is typical to etch the final 50μm to 100 μm of Si using wet chemical etch. The buried oxide (BOX) serves as the etch stop layer as there is an excellent selectivity between Si and oxide in wet etchants like KOH or TMAH [11]. The handle wafer has to be protected against chemical attack by an SiN coating.

Backside vias and bonding pads formation

Backside interlayer vertical vias and Cu pads are created on the thinned SOI wafer. Note that in this 3-D integration scheme, the requirement for via aspect ratio is relaxed as vias are formed on both wafers and connected. There are two sets of Cu pads. The first set is the via pads to form electrical connection between both device layers and the second set is the dummy pads to increase the bonding area hence increase the bonding strength. This is schematically shown in Fig. 1(d).

Low temperature Cu wafer bonding

Figure 1(e) shows that the top device layer is aligned to the bottom device layer, presumably with Cu pads already created on it, and bonded at low temperature with a constant down force in an inert ambient. A final post-bonding annealing step allows inter-diffusion at the Cu-Cu interface and promotes grain growth. A more elaborate discussion on Cu wafer bonding will be given in the next section.

Handle wafer release

Finally, the handle wafer is released and the 3-D IC is ready as shown in Fig. 1(f). It is essential that this step is as fast as possible to minimize process damage to the 3-D stack. In our current work, higher etching rate of Zr in diluted HF as compared to Cu is used to create undercut and hence to release the handle wafer.

Note that we have used bulk Si as the substrate wafer for the purpose of demonstration. In the case that the top pMOS SOI device is partially depleted, SOI wafer might be a better choice for bottom nMOS device to account for possible electrical mismatch from the hysteretic floating body effect. The airgaps between Cu pads might potentially cause reliability concerns.

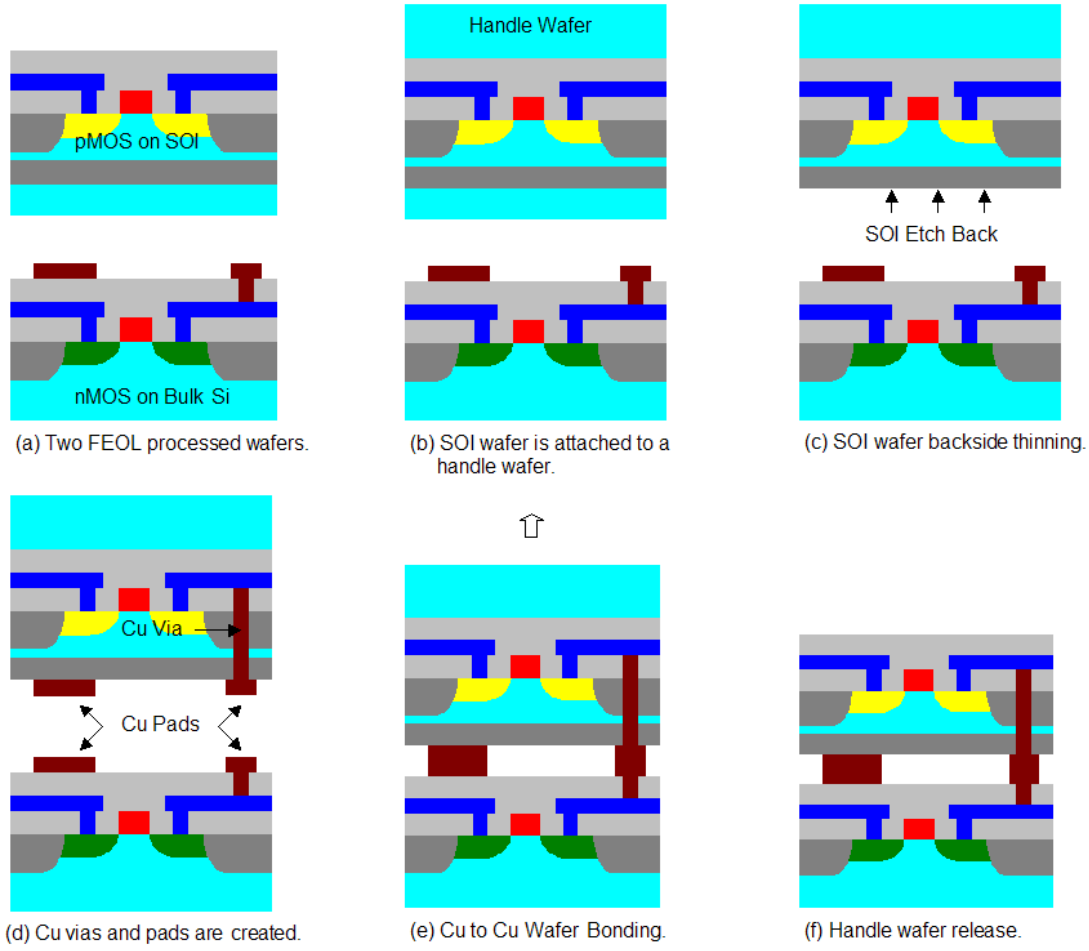

Figure 1: Process flow for 3-D integration scheme using Cu wafer bonding.

Using metal as bonding interface is an attractive choice because metal is a good heat conductor and this will help circumvent the heat dissipation problem encountered in 3-D IC. At the same time, a metal interface allows additional wiring and routing. Cu is a metal of choice because it is a mainstream CMOS material, and it has good electrical (ρ_{Cu} =1.7 mΩ.cm vs ρ_{Al} =2.65 mΩ.cm) and thermal (K_{Cu} = 400 W m^{-1} K^{-1} vs K_{Al} = 235 W m^{-1} K^{-1}) conductivities and longer electro-migration lifetime. Another advantage offered by metal bonding interface is better crosstalk immunity between device layers and this will be explained in the section on applications.

Note that we have used a back-to-face bonding fashion. In this back-to-face bonding fashion, the SOI wafer is thinned and bonded to the substrate wafer, hence eliminating the potential damage from the SOI thinning step to the whole 3-D stack.

Characterization of low temperature Cu-to-Cu wafer bonding

Since our 3-D integration is enabled by low temperature Cu-to-Cu wafer bonding, this section will be devoted to discussion on several aspects of it, including bonding mechanism and interfacial morphologies of bonded Cu-Cu layer.

We have demonstrated and characterized wafer bonding by Cu thermo compression on blank Si wafers. A pair of 100 mm Si wafers coated with 50 nm of Ta (diffusion barrier layer) and 300 nm of Cu films were successful bonded when wafer contact occurred at 400^{o}C with a down force of 4000 mbar for 30 min, followed by post-bonding anneal at 400^{o}C for 30 min in inert N_2 ambient. A post-bonding anneal is required for successful bonding. The morphology of the bonded Cu-Cu layer was examined using transmission electron microscope (TEM) and scanning electron microscope (SEM). In addition, the oxygen distribution of the copper bonded wafers was examined by energy dispersion spectrometer.

The TEM micrographs in Fig. 2(a)-(c) show the evolution of interface morphologies at different stages of wafer bonding and annealing. It is evident that there is strong grain growth during bonding and annealing. During bonding, the copper atoms at the surfaces of different layers may inter-diffuse. However, the grain growth is not fully completed and the bonded layer may still contain defects in the individual layers. Therefore after bonding, the two original Cu layers can still be distinguished as seen in Fig. 2(b). During post-bonding anneal, diffusion across the Cu-Cu interface and grain growth are further enhanced. Recrystallization is also initiated and the Cu-Cu interface in some regions starts to disappear. This is the onset of a homogeneous Cu-Cu bond. So the role of post-bonding annealing is to provide sufficient energy to complete the grain growth and thus to achieve a stable microstructure as in Fig. 2(c). As a result, the two Cu layers can no longer be distinguished. A more elaborate discussion on different interfacial morphologies of the Cu bonded layer and possible bonding mechanisms can be found in [12].

A transformation of preferred grain orientation from (111) of as deposited layer to (220) of the final bonded layer is also observed. Note that random grains that form a zigzag grain boundary near the middle of the bonded layer are clearly seen in the TEM micrograph in Fig. 2(c). This is very encouraging as it suggests that the bonded layer acts like a bulk layer of Cu.

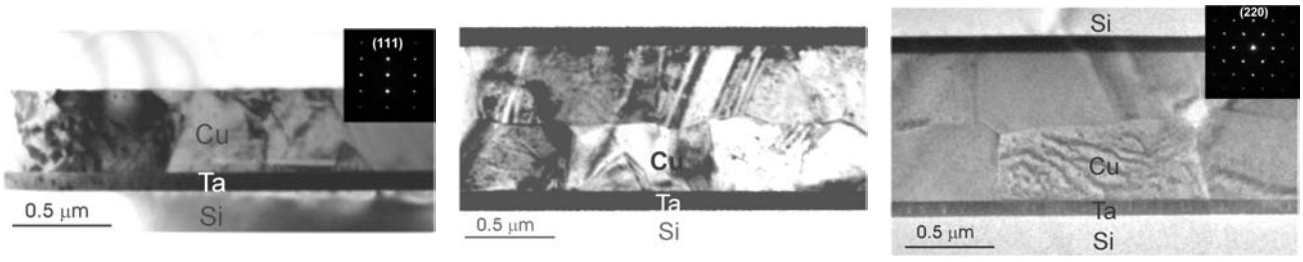

Figure 2 (a)-(c) : XTEM images of the Cu-Cu bonded layer and the major diffraction pattern of single grains for selective area: (a) before bonding (b) after 30 min bonding (c) after 30 min bonding and annealing. [13]

In previous research, the qualitative bonding strength of copper wafers was examined using the razor test [6]. A well bonded wafer pair can withstand the razor test. EDS result shows that the oxygen distribution in the bonded layer is uniformly distributed and sparse. The EDS result was published elsewhere [14].

3-D CAD Tools Development

Another aspect of our research concerns the digital design flow for 3-D integrated circuits. With a view towards full-system synthesis using 3-D technology, we are developing a set of design tools for 3-D integration. This effort comprises placement, routing, layout, and verification tools for 3-D digital integrated circuits. With the use of such tools, we will be able to verify and expand upon the predictions made by stochastic interconnect models for 3-D, in addition to being able to design and fabricate digital circuits for 3-D integration.

3-D Integration for System-on-a-chip Applications

3-D integration permits the realization of System-on-a-chip (SOC) and can result in substantial performance improvements. For example, 3-D integration using bonding allows monolithic integration of different technologies. A device layer that is optimized for analog circuits could be combined with another device layer that is optimized for logic. Furthermore, 3-D integration also mitigates parasitic substrate noise coupling. Near perfect isolation can be achieved by allowing the analog and digital systems to exist on separate substrates while communication through high density vias. In addition, crosstalk within a digital block as a result of capacitive coupling of switching signals can also be reduced in a 3-D design. The additional capacitance due to the presence of another device layer diverts field lines from the wire-wire interaction thus reducing the wire-wire coupling and this is shown in Fig. 3. In Fig. 3, V_p is the voltage induced in a wire as a result of switching voltage V_{in} in an adjacent wire.

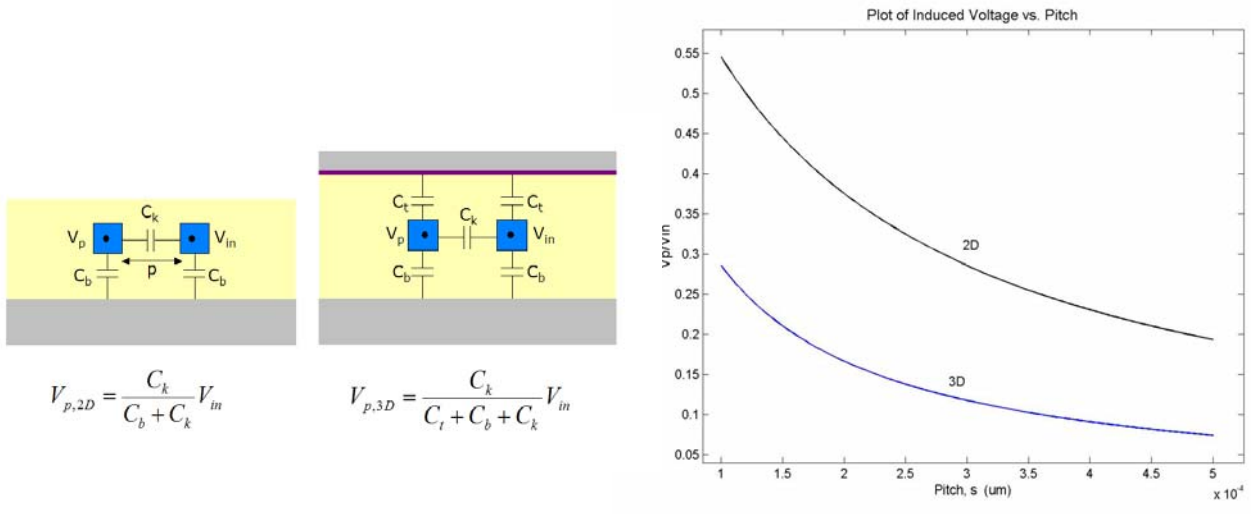

Figure 3 : Crosstalk comparison in 2-D and 3-D structure.

Conclusions

We discussed the process flow for 3-D interconnects based on low temperature Cu-to-Cu wafer bonding. The impressive bonding properties of wafer using Cu thermo compression hold tremendous promise for 3-D IC integration. In particular, 3-D integration is an attractive technology for mixed-signal system-on-a-chip applications.

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