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1978

Double-well fast CMOS SRAM (Hitachi)

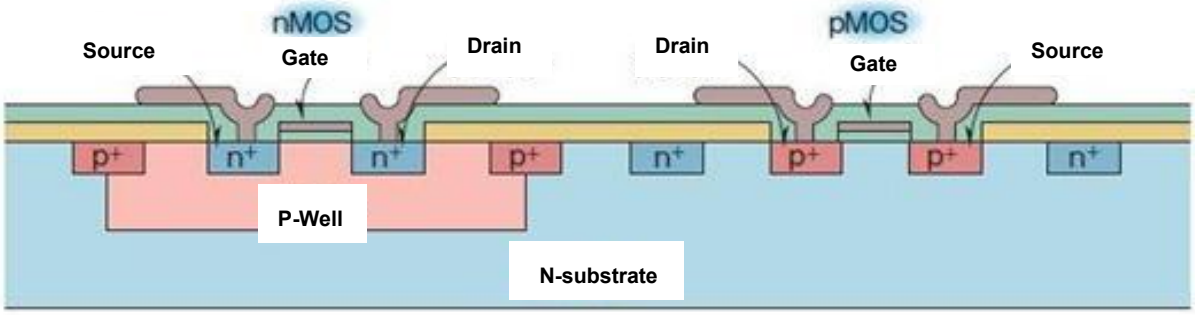
~ Integrated Circuit ~

CMOS devices were popular for watches and calculators since the beginning of 1970. Although CMOS had the feature of low power consumption, it was slow in operation speed, and NMOS was mainly used for computer applications for its high speed performance. For this reason, CMOS stayed as niche technology used only in fields where low power consumption is important, such as watches and calculators. In addition, since CMOS forms PMOS and NMOS on the same wafer, the manufacturing process was long and the cost was high.
In this situation, Hitachi announced the development of a 4 Kbit high speed SRAM at the ISSCC (International Solid-State Circuits Conference) in 1978. This product adopted the following technologies to ensure high speed.
(1) Using wafers with low impurity concentration, substrate concentration for forming PMOS and NMOS is independently set by implantation (twin-well structure).
(2) Instead of 6MOS type memory cells common in CMOS, high resistance polysilicon load type memory cells are adopted. Cell size is reduced and signal transmission delay in the word line and data line is reduced.
(3) A vertical bipolar transistor is adopted on the Vcc side of the final output stage to eliminate the lack of driving force of the PMOS.
(4) 3μm process was adopted which was the most advanced process at the time.

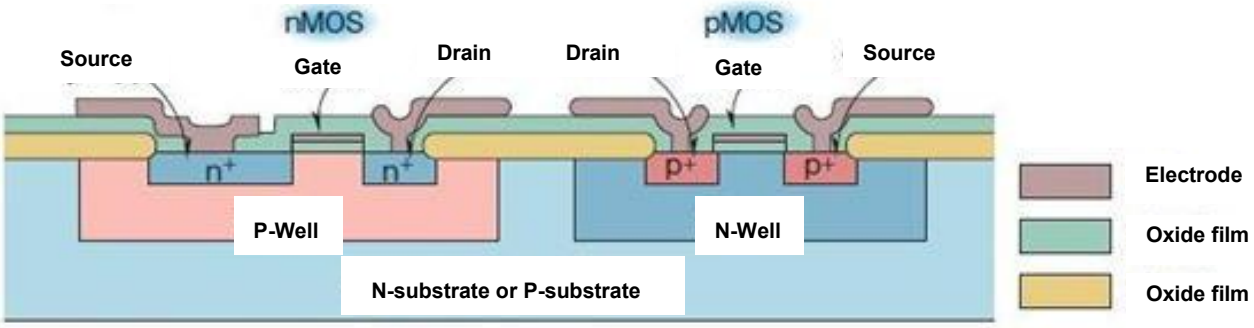
At that time, the fastest SRAM was Intel's 4 Kbit NMOS SRAM 2147, with the access time of 55/70 ns, and Hitachi's SRAM achieved the same 55/70 ns. The product launched by Hitachi was named HM6147, and its power consumption was as low as 15mA compared to the current consumption of 110mA in 2147.

With this SRAM, it came to be widely recognized that high-speed devices could be made in CMOS, and thereafter DRAM and microprocessors were also made in CMOS, and almost all LSI is now CMOS. It was a product that put CMOS to a mainstream position, which had been a niche technology characterized by low power consumption.

Conventional CMOS LSI



Twin-well CMOS LSI



Devised twin-well CMOS technology realizing high-speed performance

The twin-well CMOS structure in which both p-well and n-well are formed enables the optimization of impurity concentrations independently for n-MOS and p-MOS, thereby realizing high speed operation. Conventional CMOS has only p-well, and the impurity concentrations cannot be optimized for both n-MOS and p-MOS at the same time.

Fig. Comparison of conventional CMOS and twin-well CMOS

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