RISC Processors

COMP375 Computer Architecture and Organization

RISC Traits

- Pipelined
- Simple instructions
- Few instructions
- No microcode
- Few addressing modes
- Load/Store architecture
- Sliding register stack
- Delayed branches
- Fast

Current RISC Systems

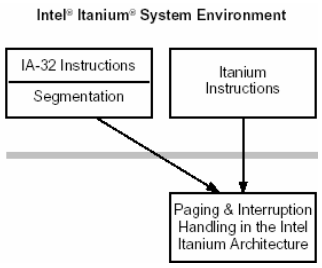
- **PowerPC** – The processor in the Apple Power Mac. Produced by IBM and Apple.
- **Sparc** – The processor in Sun workstations and servers. Produced by Sun Microsystems. First commercial RISC.
- **Itanium** – In new servers replacing the Intel Pentium. Produced by Intel.

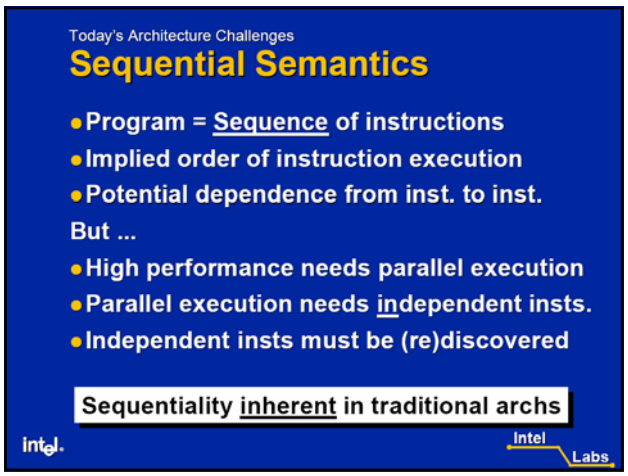
Intel Itanium®

- Intel's latest RISC system.
- The current processor is the Itanium 2.
- Intel seems to indicate that this is the replacement for the Pentium chip.

Support of Pentium Instructions

- The Itanium can execute both Itanium instructions and Pentium (IA-32) instructions
- There are jump to IA-32/Itanium instructions





Today's Architecture Challenges

Sequential Semantics ...

Dependent	Independent
add r1 = r2, r3	add r1 = r2, r3
sub r4 = r1, r2	sub r4 = r11, r2
shl r5 = r4, r8	shl r5 = r14, r8

- Compiler knows the available parallelism
  - but has no "vocabulary" to express it
- Hardware must (re)discover parallelism

Complex hardware needed to (re)extract ILP

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Today's Architecture Challenges

Resource Constraints

- Small Register Space
  - Limits compilers ability to "express" parallelism
  - Creates false dependencies (overcome by renaming)
- Shared Resources
  - Condition flags, Control registers, etc.
  - Forces dependencies on otherwise independent insts
- Floating-Point Resources
  - Limited performance even in ILP rich applications
  - Data parallel applications need flexible resources

Limited Resources: a fundamental constraint

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Itanium® Architecture Performance Features

- Explicitly Parallel Instruction Semantics
- Predication and Control/Data Speculation
- Massive, Massive Resources (regs, mem)
- Register Stack and its Engine (RSE)
- Memory hierarchy management support
- Software Pipelining Support
- ...

Challenges addressed from the ground up

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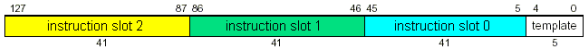
Instruction Bundles

- Explicitly Parallel /instruction Computing (EPIC)
- Three 41 bit instructions are grouped into a bundle with a 5 bit template.
- There must be no dependencies within the instructions of a bundle.



Compiler to Processor Hints

- Every memory load and store in the Itanium architecture has a 2-bit cache hint field
- The compiler can provide a hint to indicate if a branch is likely to be taken.
- Templates define which execution units will be used and if dependencies exist.

Predication

- Control flow to Data flow

Predication removes/reduces branches

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Predication ...

- Unpredictable branches removed
  - Misprediction penalties eliminated
- Basic block size increases
  - Compiler has a larger scope to find ILP
- ILP within the basic block increases
  - Both "then" and "else" executed in parallel
- Wider machines are better utilized

Predication enables and enhances ILP

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Register Stacks

- Many RISC processors have a large number of registers, not all of which are visible at any one time.
- The mapping of register X to a hardware register changes when a function is called.

Today's Architecture Challenges

Procedure Call Overhead

- Modular programming increasingly used
  - Programs tend to be call intensive
- Register space is shared by caller and callee
- Call/Returns require register save/restores
- Software convention has its limitations
  - Parameter passing limited
  - Extra saves/restores when not needed

Shared resources create more overhead

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Before a Function Call

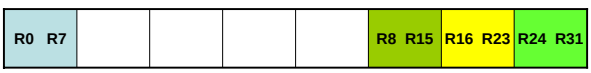
- Assume the assembly language programmer sees 32 registers.
- Before a function call, arguments and the return address are put in registers R24 to R31.

After a Function Call

- After a function call, the input arguments and the return address are available in registers R8 to R15.
- R16 to R23 are used for local variables.
- R24 to R31 contain arguments to next function

After another Function Call

- After another function call, the input arguments and the return address are again available in registers R8 to R15.
- Return values are also put in R8 to R15 upon function return.



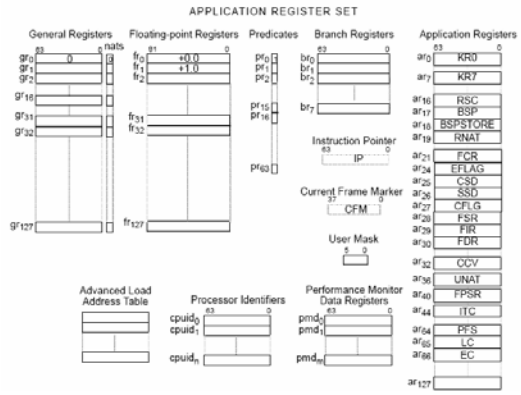
After Function Return

- After the function return, the return values are available in registers R24 to R31.

Itanium Register Stack

- The Itanium uses a sliding register system somewhat similar to the generic description
- General registers 0 through 31 are termed the **static general registers**.
- General registers 32 through 127 are termed the **stacked general registers**.
- A function can specify how many of the stacked general registers the system is to shift.
- GP0 is always zero.

Itanium Registers



Register Stack Engine (RSE)

- **Automatically saves/restores stack registers without software intervention**
  - Provides the illusion of infinite physical registers
    - by mapping to a stack of physical registers in memory
  - Overflow: Alloc needs more registers than available
  - Underflow: Return needs to restore frame saved in memory
- **RSE may be designed to utilize unused memory bandwidth to perform register spill and fill operations in the background**

RSE eliminates stack management overhead

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Itanium Floating Point

- The Itanium has 128 floating-point registers
- Each register holds an 82-bit floating point value.
- Values are rounded as they are stored as 32 bit floats or 64 bit doubles.

Floating-Point Architecture

- **Fused Multiply Add Operation**
  - An efficient core computation unit
- **Abundant Register resources**
  - 128 registers (32 static, 96 rotating)
- **High Precision Data computations**
  - 82-bit unified internal format for all data types
- **Software divide/square-root**
  - High throughput achieved via pipelining

FP: High performance and ___ high precision

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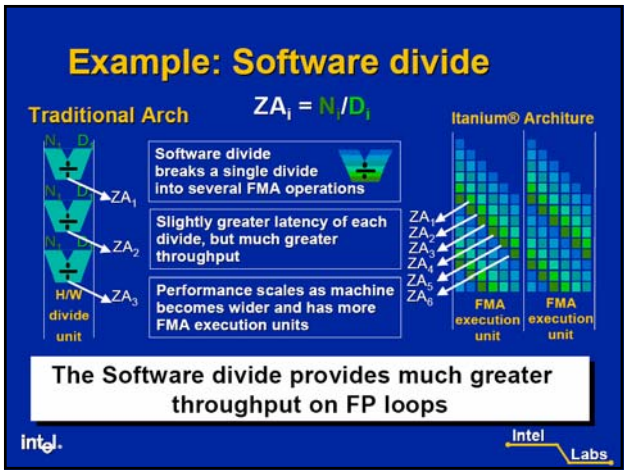


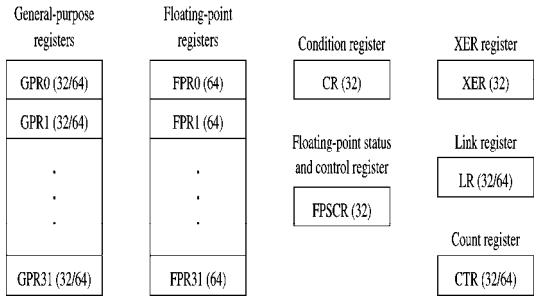
Endian

- The Itanium can execute in Big Endian or Little Endian mode.
- Instruction fetches are always Little Endian

Itanium OS Support

- Redhat Linux servers will run on the Itanium. The desktop does not.
- Microsoft Windows Servers will run on the Itanium. Windows XP Professional will not.
- Sun Solaris runs on 64 bit Sparc processors, but not on the Intel Itanium.

PowerPC Registers



PowerPC Branches

- Every jump instruction has two extra bits
- AA bit
  - 1 (use absolute address)
  - 0 (use relative address)
- LK bit
  - 0 (no link --- branch)
  - 1 (link --- turns branch into a procedure call)