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# CHAPTER 1

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# HOW SEMICONDUCTOR CHIPS ARE MADE

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## 1.1 INTRODUCTION

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Over the past decades, an information world that encompasses computers, the Internet, wireless communication, and global positioning systems has emerged. The center of this information world is enabled by many tiny *integrated circuit* (IC) chips embedded in the systems.

ICs are used in many walks of life—in sectors including consumer products, home appliances, automobiles, *information technology* (IT), telecom, medical, military and aerospace applications. Continuous research and development coupled with nanotechnology will make ICs smaller and more powerful. In the foreseeable future, the size of a computer will shrink to the size of a fingernail and reach the practical limit of an IC that is *smaller, faster, cheaper, and consumes low power*. The semiconductor industry can help drive nanotechnology; thus, they are mutually beneficial.\*

The evolution from chip to *Microelectromechanical Systems* (MEMS) combines IC manufacturing and micromachining techniques to install motors, sensors, pumps, valves, or radio receivers and antennas on a chip. MEMS applications encompass IT, entertainment, biological, medical, and automotive sectors.† Similar IC technologies and manufacturing processes can be applied in manufacturing flat panel display.

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## 1.2 WHAT IS A MICROCHIP?

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Microchips, or chips, are basically made of thousands to millions of transistors packed into a small piece of silicon. A transistor is an electronic switch that contains no moving parts but uses electricity to turn itself on and off. The transistors are wired together, using aluminum or copper, to perform

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\*Stephen Marx, "Using Microtechnology to Get to Nanotechnology," *Machine Design*, September 2004.

†Dave Thomas, "Key MEMS Building Blocks," *Solid State Technology*, April 2004.

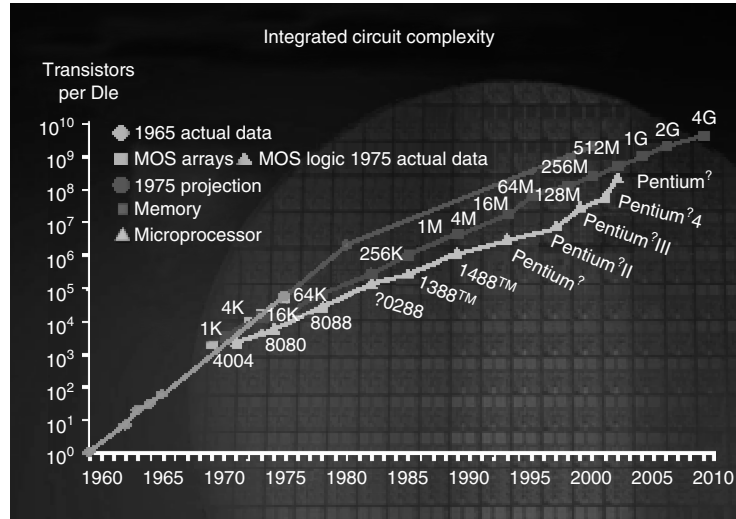


FIGURE 1.1 Moore's law.\* (Image Courtesy of Intel Corporation.)

different functions. A transistor is turned on when a low-voltage electrical charge is applied to the gate. This change in the electrical charge on the transistor allows electrons to move from the source to the drain. There are several types of switch technologies—CMOS (complementary metal oxide semiconductor), RF CMOS, silicon germanium (SiGe), BiCMOS, and CMOS on *silicon-on-insulator* (SOI) technologies.

### 1.3 MOORE'S LAW

Dr. Gordon Moore made his famous observation in 1965 and the press called it *Moore's law*. Moore observed and predicted the doubling of transistors in the same size of an IC every two years (Fig. 1.1).

Moore's law has tremendous implications—it motivates and challenges all of us. With a global consumer's need and an orchestrated and cooperative effort from all industry manufacturers, suppliers, government organizations, consortia, and collaborations between universities and semiconductor industries, we are marching and keeping pace with Moore's law.<sup>1</sup> Intel expects that it will continue at least through the end of this decade.

### 1.4 HOW CHIPS ARE DESIGNED

Once the customer and chip design house agree on the purpose of a chip, the design process commences. A typical design process includes architecture, logics, circuit, verification, layout, test, approval of design, and release to fabrication.

\*"No Exponential Is Forever ... but We Can Delay 'Forever'," Gordon Moore, *International Solid State Circuits Conference*, February 10, 2003.

## 1.5 WHERE CHIPS ARE MADE

Chips are made in the most sophisticated manufacturing plants in the world, called wafer fabrication facilities or *wafer fab*. Typically 300-mm fabs cost \$2 billion to build and equip. Today, there are over 1000 fabs around the world producing millions of chips everyday.

The chip manufacturing process occurs in a cleanroom of a fab. A class-one cleanroom provides the world's cleanest environment where air is continuously filtered to keep airborne contaminants to not more than one dust per cubic foot. Huge air filtration systems completely change the air in the cleanroom at the rate of about 10 times per minute. In addition to the cleanest air, stringent cleanliness requirements are also followed in the use of chip-making materials, chemicals, and processing equipment. Workers in fabs wear special clothing including gowns called "bunny suits," hoods, face-masks, glasses, gloves, and shoe covers to avoid contaminating the chips. The temperature, barometric pressure, and humidity are controlled. All these efforts to avoid contamination in fabs are needed to ensure an accepted yield of chips that meet specifications.

## 1.6 HOW CHIPS ARE MADE

Computer chips are built with pure silicon (99.999999 percent pure) and metals. A silicon seed crystal is dipped in purified molten silicon and is rotated and pulled out as it revolves to grow into a silicon cylinder or ingot\* (Fig. 1.2). Once the ingot reaches the desired size, it is prepared, inspected, and tested. The ingot is then sliced into many thin silicon wafers that are then polished. Hundreds of chips are made from each wafer.

Chips are made in a precise manufacturing process that involves hundreds of operations being executed layer by layer onto a silicon wafer with constant testing. Chip making involves repeating processes using ultraviolet light, polymers, solvents, and gases. The processes include insulating (silicon dioxide), placing (deposition), patterning (with stencils known as masks), removing (etching), implanting (doping) and diffusion, and depositing interconnection metals (aluminum, copper).

Each layer consists of thousands of microscopic components. In the process of building these layers, thousands to millions of transistors are created and interconnected. When completed, a single wafer will contain hundreds of identical dies (chips) that must pass rigorous testing and are then cut from the wafer. Each chip is then mounted onto a metal or plastic package. The mounted chip undergoes final testing and then is ready to be assembled into final products.

Intel's website illustrates how chips are made in detail.<sup>2</sup>

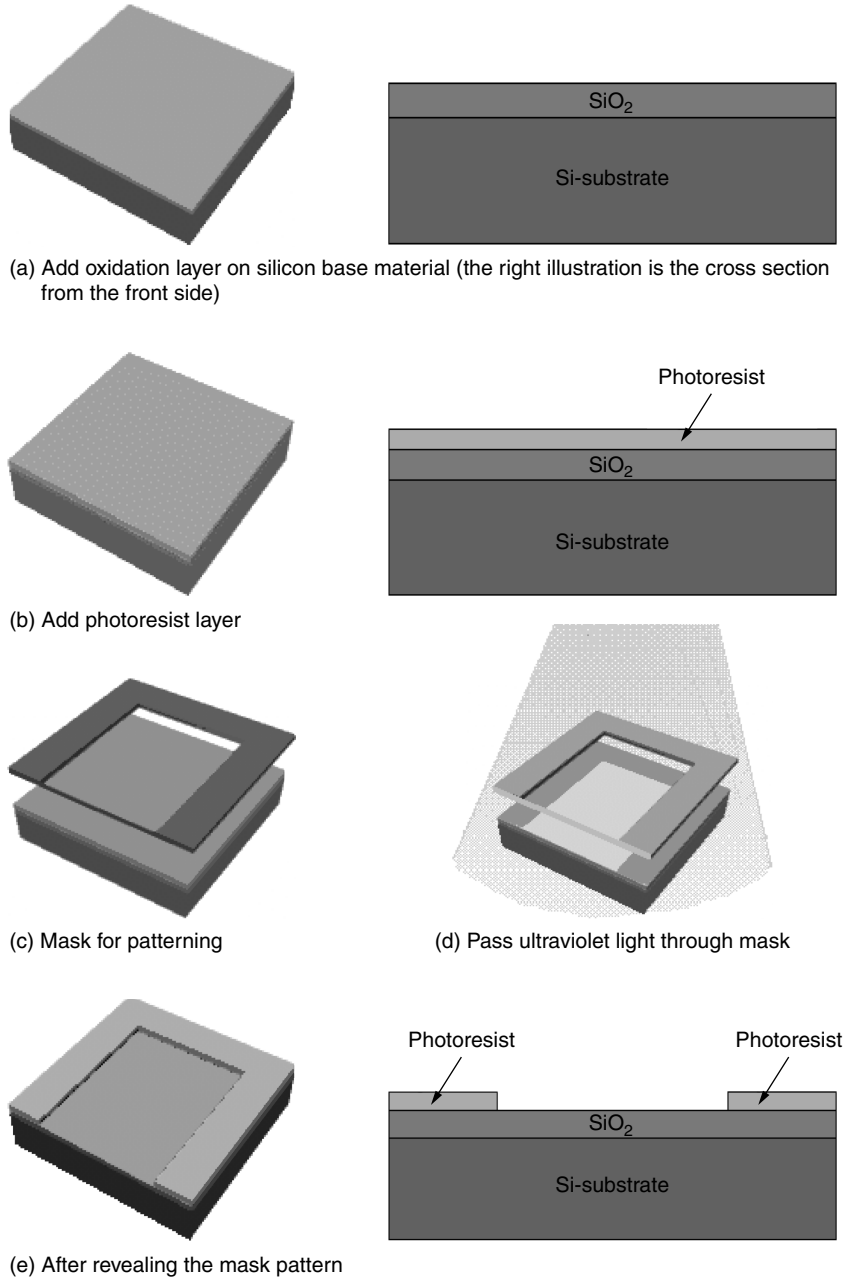


**FIGURE 1.2** Silicon ingot and silicon wafer. (Courtesy of Dooson Company.)

### 1.6.1 Oxidation Layering

On a silicon-based wafer, the first thin layer of silicon dioxide (Fig. 1.3(a)) is formed over the complete wafer by exposing the wafer to a high temperature in a furnace. The oxidation temperature is generally in the range of 900–1200°C. The silicon dioxide layer is used to provide insulation to protect the silicon beneath it and to form transistor gates.

<sup>2</sup>Dooson company, [www.dooson-inc.com](http://www.dooson-inc.com).



**FIGURE 1.3** Process steps for patterning silicon dioxide: (a) add oxidation layer on silicon base, (b) add photoresist layer, (c) mask for patterning, (d) pass ultraviolet light through mask, (e) after removing photoresist and revealing the mask pattern, (f) after etching of silicon dioxide, (g) after removing photoresist.

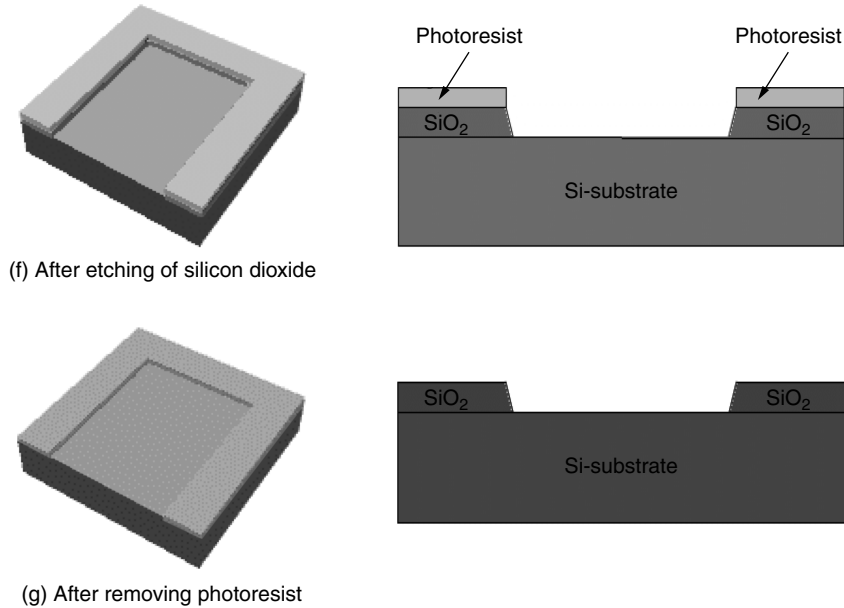


FIGURE 1.3 (Continued)

### 1.6.2 Photoresist Coating

The wafer is then uniformly coated with a substance called photoresist (Fig. 1.3(b)), a light-sensitive material that can be processed into a specific pattern after being exposed to ultraviolet light in the shape of the desired pattern. There are two main types of photoresists—negative and positive. When a negative resist is used, the unexposed portion of the photoresist becomes soluble, leaving a *negative* image. Alternatively when a positive resist is used, the exposed portion of the photoresist becomes soluble. Both positive and negative resists can sometimes be used on a single mask for two steps, making complementary regions available for processing, and therefore reducing the number of masks.<sup>3</sup>

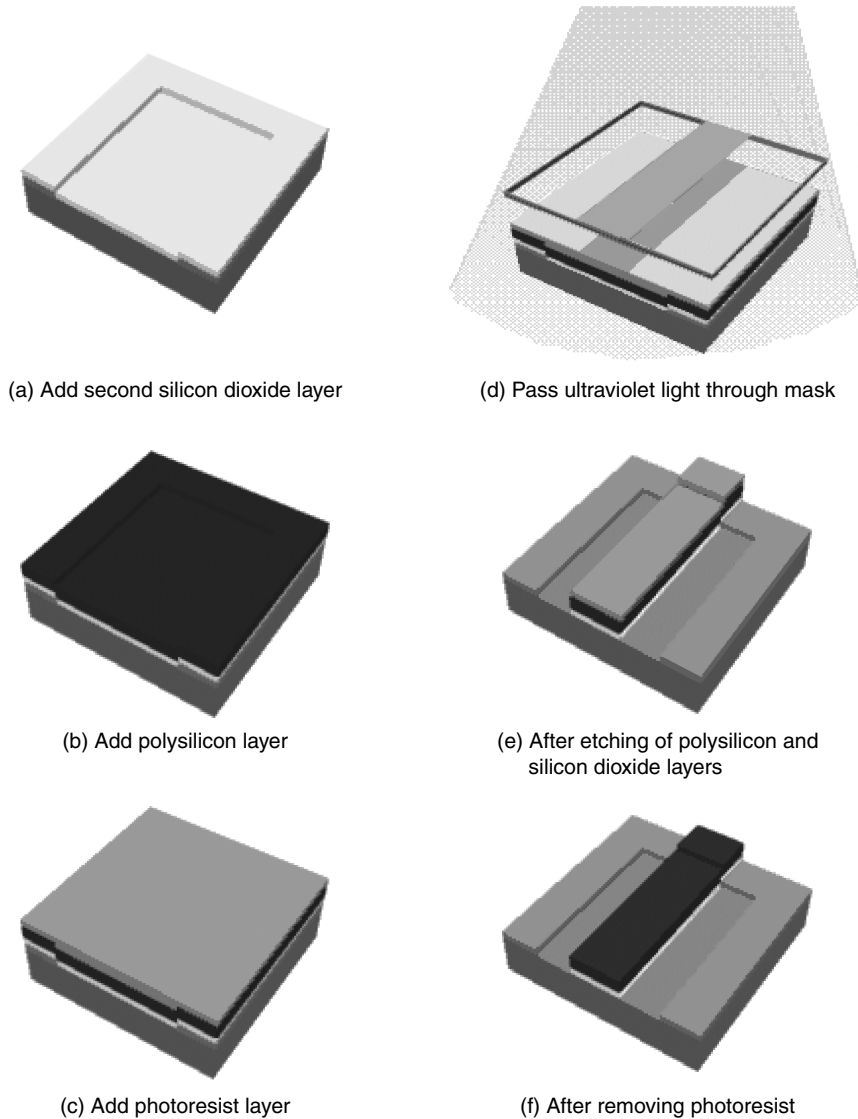
### 1.6.3 Patterning

Through the process called photolithography, ultraviolet light is then passed through a patterned glass mask, or stencil, onto the silicon wafer (Fig. 1.3(c)). The mask represents one color layer of the integrated circuit from mask blueprints and contains a specific pattern that is to be transferred to the silicon. Assuming a positive photoresist, the mask is transparent in the region that needs to be processed and opaque in the others. When the ultraviolet light exposes the photoresist through the combination of mask and wafer (Fig. 1.3(d)), the photoresist becomes soluble wherever the mask is transparent.

After pattern generation, the exposed photoresist is dissolved by spraying the wafer with the developing solvent (Fig. 1.3(e)). This reveals a pattern of the photoresist made by the mask on the silicon dioxide. Then the wafer is hardened at a low temperature so that the remaining photoresist, which can resist the strong acid, is used to etch the exposed oxide layer.

### 1.6.4 Etching

The revealed silicon dioxide is removed through a process called etching, which stops at the silicon surface (Fig. 1.3(f)). There are two main types of etching technologies—wet and dry etching.



**FIGURE 1.4** Process steps for patterning a polygon layer: (a) add second silicon dioxide layer, (b) add polysilicon layer, (c) add photoresist layer, (d) pass ultraviolet light through mask, (e) after etching of silicon dioxide, (f) after removing photoresist.

Wet etching removes the areas that are not covered by photoresist with liquids, including many different types of acids, bases, and caustic solutions, as a function of the material that is to be removed.<sup>3</sup> In dry etching, or plasma etching, the reactive ionized gas is used in place of a wet-etching solution. Dry etching provides a higher resolution than wet etching, and therefore has emerged to replace wet chemistry approaches in modern semiconductor manufacturing.<sup>4</sup>

After silicon dioxide etching, the rest of the photoresist is removed (Fig. 1.3(g)) in a photoresist stripper by using either a solvent or plasma oxidation. This process leaves ridges of silicon dioxide on the silicon wafer base with the same pattern as the image on the mask. Figure 1.3 illustrates the

process steps of how to transfer a pattern onto the silicon wafer. The sequence of the process steps patterns exactly one layer of the semiconductor material, and the same sequence patterns the layer of the complete surface of the wafer. Thus, hundreds of millions of patterns are transferred to semiconductor surface simultaneously.

### 1.6.5 Layering

To introduce a polygon layer, a second and thinner layer of silicon dioxide is grown from thermal oxidation as before over the ridges and etched areas of the wafer base (Fig. 1.4(a)). Then a layer of polysilicon (Fig. 1.4(b)) and another layer of the photoresist (Fig. 1.4(c)) are evenly spread on the wafer.

The photolithography process is applied to define the polygon region. Ultraviolet light exposes the photoresist through a second mask, leaving a new pattern for polysilicon on the photoresist (Fig. 1.4(d)). The photoresist is dissolved with a solvent to expose the polysilicon and silicon dioxide, which are then etched away with chemicals (Fig. 1.4(e)). After the remaining photoresist is removed (Fig. 1.4(f)), ridges of polysilicon and silicon dioxide are left on the polygon region. Figure 1.4 illustrates the process steps of how to transfer another polysilicon layer on the previous layer.

A similar process will be repeated over and over again with each mask to pattern different layers of deposited materials. During this manufacturing process, conductive regions are formed and insulated from each other. Later they are selectively connected to each other to produce an integrated circuit.

### 1.6.6 Doping: Diffusion and Ion Implantation

Many steps in the IC manufacturing process require a change in the dopant concentration of some areas to make them more conductive. Two approaches are used to introduce dopants—diffusion and ion implantation.

Diffusion implantation is performed by either exposing the wafer to a high-temperature environment of dopant vapor (gaseous diffusion) or predepositing dopant ions on the surface and then thermally driving them in by high-temperature processing (nongaseous diffusion). The final concentration is greatest at the surface and decreases deeper in the material.

Ion implantation is performed by bombarding the exposed areas of the silicon wafer with various chemical impurities called ions. With an implanter, ions are accelerated and implanted into the top layer of the silicon wafer just below the surface, altering conductivity in these areas. Figure 1.5 illustrates the exposed area before and after ion implantation. The acceleration of the ions determines how deep they will penetrate the material, while the exposure time determines the dosage. Therefore ion implantation provides a better controlled doping mechanism than diffusion. This is the reason doping technology has shifted from diffusion process to high-energy ion implantation in modern semiconductor manufacturing.<sup>4</sup>

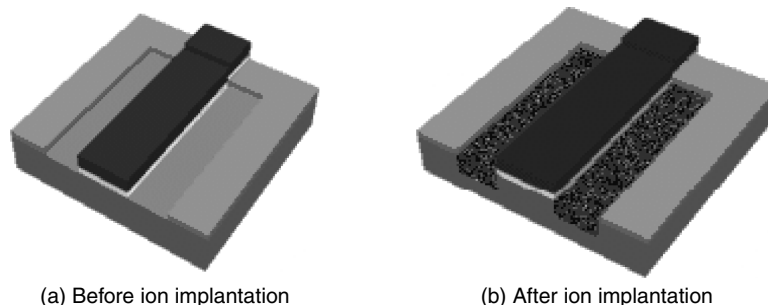
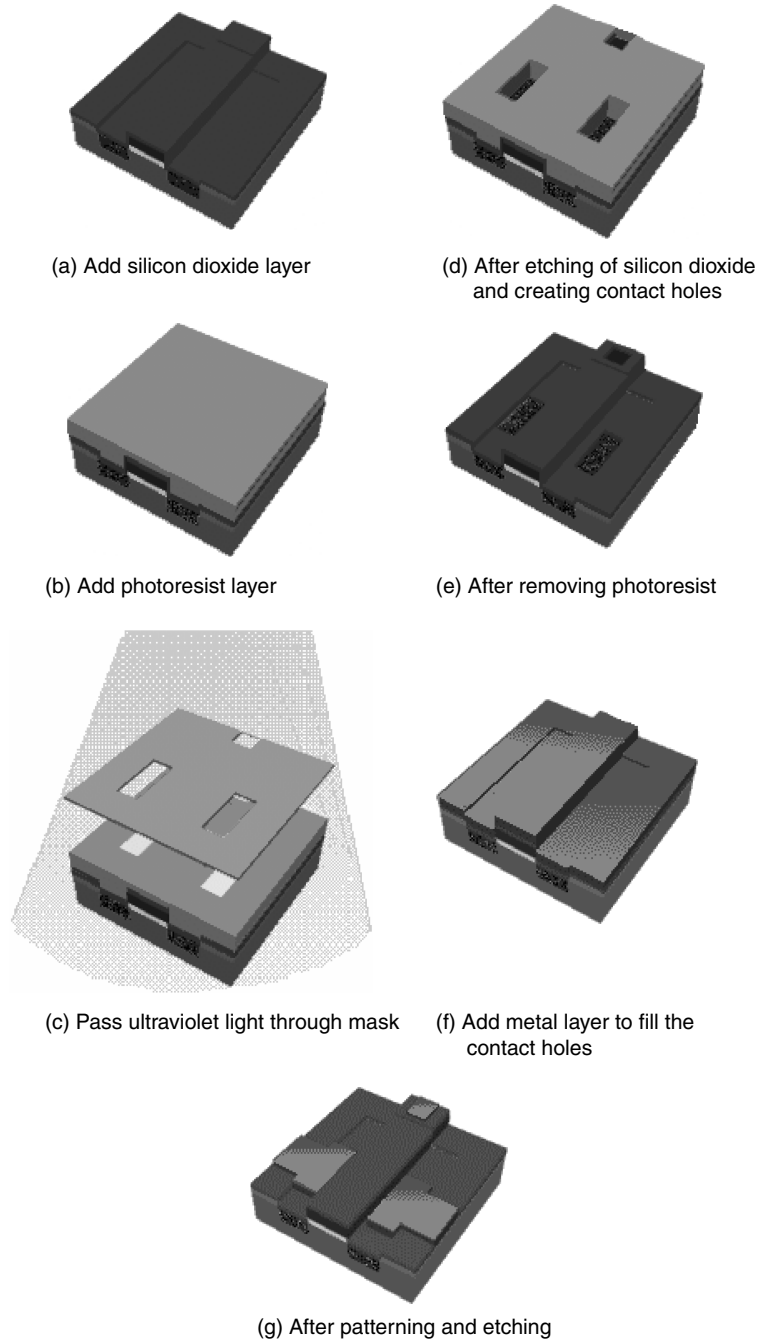


FIGURE 1.5 Ion implantation: (a) before ion implantation, (b) after ion implantation.



**FIGURE 1.6** Process steps of depositing interconnect metal: (a) add silicon dioxide layer, (b) add photoresist layer, (c) pass ultraviolet light through mask, (d) after etching of silicon dioxide and creating contact holes, (e) after removing photoresist, (f) add metal layer to fill the contact holes, (g) after patterning and etching.



### 1.6.7 Depositing Interconnection Metals

To connect different layers, similar layering and patterning processes are repeated (Fig. 1.6(a)–(c)). A mask is used to define contact holes allowing for the connections to be made between layers. After the etching of the silicon dioxide in the exposed area (Fig. 1.6(d)) and the removal of the remaining photoresist (Fig. 1.6(e)), the contact holes are created. A combination of tungsten and aluminum is then deposited onto the whole wafer to fill the contact holes under high-vacuum conditions (Fig. 1.6(f)). Another patterning and etching stage defines a contact pattern and leaves strips of the metal to make the electrical connections (Fig. 1.6(g)). In sophisticated circuits, the interconnect wiring is so complex that it is impossible to complete within a single layer.

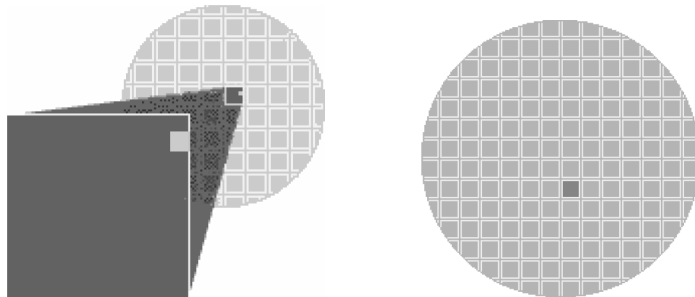
Approximately 20 layers are connected to form an IC in a three-dimensional structure. The exact number of layers on a wafer depends on the complexity of the design. After all the desired levels are in place, a final layer of insulation is deposited to protect the fragile aluminum wiring. In the last photolithograph step, small pads along the edge of the microchip are left exposed. These aluminum pads are the contact points between the microscopic wiring of the IC and the outside world.

### 1.6.8 Testing

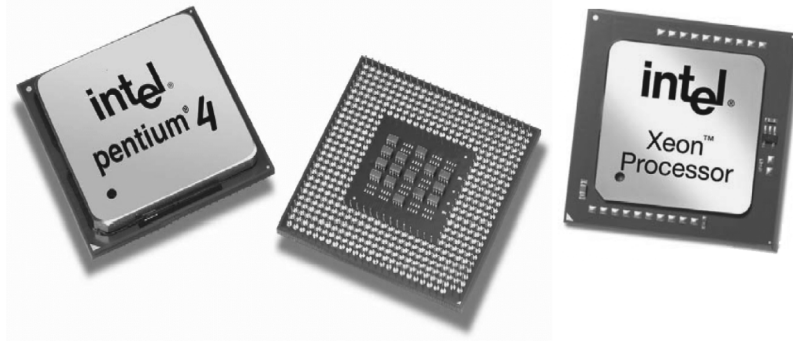
In the previous example a simplified process is completed to manufacture a tiny portion of a microchip. In reality, making a chip is much more complex. The complete run of the manufacturing process might involve hundreds of individual steps and take weeks to complete. Identical chips, or dies, are created in batches on a single wafer, and each finished wafer may contain hundreds of actual chips. A chip on a finished wafer is illustrated in Fig. 1.7. Despite the care taken in the fabrication process, not all the chips on the wafer work. Automated methods are used to test the microscopic circuitry of each device on the wafer before it is cut into individual chips with a diamond saw, separating the chips on the wafer.

### 1.6.9 Packaging

Each chip is then inserted into a protective package that provides mechanical support and an electrical connection interface with other external devices. The tiny chip is mounted on a metal frame, and thin gold wires connect the individual pin on the frame to the small aluminum pad on the chip. Thus, the pins on the metal frame are attached to the microscopic circuitry. To further protect the chip and its fragile wire bonds, the chip is encapsulated in hard plastic. Packaging also removes the heat generated by the circuit and protects the chip against environmental conditions such as humidity.<sup>3</sup> The type of package depends on the type of microprocessor and its usage (Fig. 1.8).



**FIGURE 1.7** Each square represents a chip on a finished wafer.



**FIGURE 1.8** Packaged microprocessors.

Each packaged chip is loaded on the testing board to test one more time, marking the last step in the chip-making process. The chips would be electrically stressed far beyond normal conditions, so weak chips are forced to fail before they are put into customers' products. The chips are now ready for shipping to companies that will use them to make everyday items.

## REFERENCES

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