IEEE P802.3bt™/D1.5

Draft Standard for Ethernet Amendment: Physical Layer and Management Parameters for DTE Power via MDI over 4-Pair

Prepared by the

LAN/MAN Standards Committee
of the
IEEE Computer Society

This draft is an amendment of IEEE Std 802.3-201x. This amendment increases the maximum PD power available by utilizing all four pairs in the structured wiring plant. Draft D1.5 is prepared for Task Force Review. This draft expires 6 months after the date of publication or when the next version is published, whichever comes first.

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IEEE Standards Department
445 Hoes Lane
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Abstract: This amendment to IEEE Std 802.3-201x increases the maximum PD power available by utilizing all four pairs in the structured wiring plant, which represents a substantial change to the capabilities of Ethernet. The power classification information exchanged during negotiation will be extended to allow meaningful power management capability.These enhancements solve the problem of higher power and more efficient power-over-Ethernet delivery systems.

Keywords: Ethernet; DTE power via MDI, power-over-Ethernet.

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Introduction

Editor's Note (to be removed prior to publication):

This front matter is provided for comment only. Front matter is not part of a published standard and is therefore, not part of the draft standard. You are invited to review and comment on it as it will be included in the published standard after approval.

One exception to IEEE style that is consciously used to simplify the balloting process is the numbering of the front matter. Instead of the front matter being lower case Roman numeral page numbers, with the draft restarting at 1 with arabic page numbers, balloted front matter and draft are numbered consecutively with arabic page numbers.

This introduction is not part of IEEE P802.3bt, IEEE Draft Standard for Ethernet. Amendment: Physical Layer and Management Parameters for DTE Power via MDI over 4-pair.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The Media Access Control (MAC) protocol specified in IEEE Std 802.3 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was included in the experimental Ethernet developed at Xerox Palo Alto Research Center. While the experimental Ethernet had a 2.94 Mb/s data rate, IEEE Std 802.3-1985 specified operation at 10 Mb/s. Since 1985 new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3x specified full duplex operation and a flow control protocol, IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-201x and are not maintained as separate documents.

At the date of IEEE Std 802.3bt-20XX publication, IEEE Std 802.3 is comprised of the following documents:

IEEE Std 802.3-201x

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

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Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 90 and Annex 83A through Annex 86A. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 89 and associated annexes includes general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

IEEE Std 802.3bk™-2013

Amendment 1—This amendment includes changes to EPON as defined in IEEE Std 802.3-201x and adds the physical layer specifications and management parameters for EPON operation on point-to-multipoint passive optical networks supporting extended power budget classes of PX30 (29 dB for 1G-EPON), PX40 (33 dB for 1G-EPON), PRX40 (33 dB for 10/1G-EPON), and PR40 (33 dB for 10/10G-EPON).

IEEE Std 802.3bt-201x

This amendment includes enhancements that will increase the maximum power available beyond current standards by utilizing all four pairs in the structured wiring plant.

A companion document IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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David J. Law, *IEEE 802.3 Working Group Chair*
Adam Healey, *IEEE 802.3 Working Group Vice-Chair*
Pete Anslow, *IEEE 802.3 Working Group Secretary*
Steven B. Carlson, *IEEE 802.3 Working Group Executive Secretary*
Valerie Maguire, *IEEE 802.3 Working Group Treasurer*

Chad Jones, *IEEE P802.3bt DTE Power via MDI over 4-Pair Task Force Chair*
Koussalya Balasubramanian,
IEEE P802.3bt DTE Power via MDI over 4-Pair Task Force Editor-in-Chief (1st phase)
Lennart Yseboodt, *IEEE P802.3bt DTE Power via MDI over 4-Pair Task Force Editor-in-Chief (2nd phase)*
David Abramson, *IEEE P802.3bt DTE Power via MDI over 4-Pair Task Force Comment Editor*

This standard is dedicated to the memory of our friend and colleague Martin Patoka

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*Member Emeritus

Also included are the following nonvoting IEEE-SA Standards Board liaisons:

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Michelle D. Turner
IEEE Standards Senior Program Manager, Document Development

Lisa Perry
IEEE Standards Program Manager, Technical Program Development

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Draft Standard for Ethernet Amendment: Physical Layer and Management Parameters for DTE Power via MDI over 4-Pair

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NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.

TO BE REMOVED PRIOR TO FINAL PUBLICATION: Reviewers and the publication editor should note that editing instructions have been written to minimize the probability of changes being lost at publication from other IEEE 802.3 amendment projects running in parallel (e.g., IEEE P802.3bj and IEEE P802.3bk) that modified the same text and tables.

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1. Introduction

Editor's Note: The following clause 1.3 is a place holder for new content. If no new references are added prior to entering sponsor ballot, this clause will be deleted from the ballot draft.

1.3 Normative references

Insert the following references in alphanumerical order:

1.4 Definitions

Replace 1.4.241, 1.4.415, 1.4.425, 1.4.426 as follows:

1.4.241 Link section: The portion of the link segment from the PSE to the PD.

1.4.415 Type 1 PD: A PD that provides a Class 0, 1, 2 or 3 signature during Physical Layer classification (see IEEE 802.3, Clause 33).

1.4.425 V_{PD}: The voltage at the PD PI measured between any positive conductor of a powered pair and any negative conductor of the corresponding powered pair (see IEEE 802.3, Clause 33)."

1.4.426 V_{PSE}: The voltage at the PSE PI measured between any positive conductor of a powered pair and any negative conductor of the corresponding powered pair (see IEEE 802.3, Clause 33).

Insert the following new definitions into the list, in alphanumerical order:

pairset: Either of the two valid 4-wire connections as listed in 33.2.3.

~~Single-signature PD: A PD that shares the same detection signature, classification signature, and maintain power signature between both pairsets (see IEEE 802.3, Clause 33).~~

~~Dual-signature PD: A PD that has independent detection signatures, classification signatures, and maintain power signatures on each pairset (see IEEE 802.3, Clause 33).~~

Type 3 PD: A PD that provides a Class 1 to Class 6 signature during Physical Layer classification, implements multiple-Event classification, and accepts power on both modes simultaneously (see IEEE 802.3, Clause 33).

Type 3 PSE: A PSE that supports PD Types 1-3 and supports Low MPS (see IEEE 802.3, Clause 33).

Type 4 PD: A PD that provides a Class 7 or 8 signature during Physical Layer classification, implements multiple-Event classification, is capable of Data Link Layer classification, and accepts power on both Modes simultaneously (see IEEE 802.3, Clause33).

Type 4 PSE: A PSE that supports PD Types 1-4 and supports 4-pair power and Low MPS (see IEEE 802.3, Clause 33).

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Editor's Note: The following clause 1.5 is a place holder for new content. If no new abbreviations are added prior to entering sponsor ballot, this clause will be deleted from the ballot draft.

1.5 Abbreviations

Insert the following new abbreviations into the list, in alphabetical order:

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25. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX

25.4 Specific requirements and exceptions

The 100BASE-TX PMD (including MDI) shall comply to the requirements of TP-PMD, 7, 8, 9, 10, and 11, and normative Annex A with the exceptions listed below. In TP-PMD, informative annexes B, C, E, G, I, and J, with exceptions listed below, provide additional information useful to PMD sublayer implementers. Where there is conflict between specifications in TP-PMD and those in this standard, those of this standard shall prevail.

25.4.1 Change to 7.2.3.1.1, "Line state patterns"

Descrambler synchronization on the Quiet Line State (QLS), Halt Line State (HLS), and Master Line State (MLS) Line State Patterns cited in TP-PMD 7.2.3.1.1 is optional.

25.4.2 Change to 7.2.3.3, "Loss of synchronization"

The synchronization error triggered by PH_Invalid as defined in TP-PMD 7.2.3.3a is not applicable.

25.4.3 Change to Table 8-1, "Contact assignments for twisted pair"

100BASE-TX for twisted pair adopts the contact assignments of 10BASE-T. Therefore, the contact assignments shown in TP-PMD Table 8-1 shall instead be as depicted in Table 25–1.

Table 25–1—Twisted-pair MDI contact assignments

Contact	PHY without internal crossover MDI SIGNAL	PHY with internal crossover MDI SIGNAL
1	Transmit +	Receive +
2	Transmit –	Receive –
3	Receive +	Transmit +
4		
5		
6	Receive –	Transmit –
7		
8		

25.4.4 Deletion of 8.3, "Station labelling"

Clause 8.3 of TP-PMD shall not be applied to 100BASE-TX.

25.4.5 Change to 9.1.7, "Worst case droop of transformer"

Change text in Section 25.4.5 as follows:

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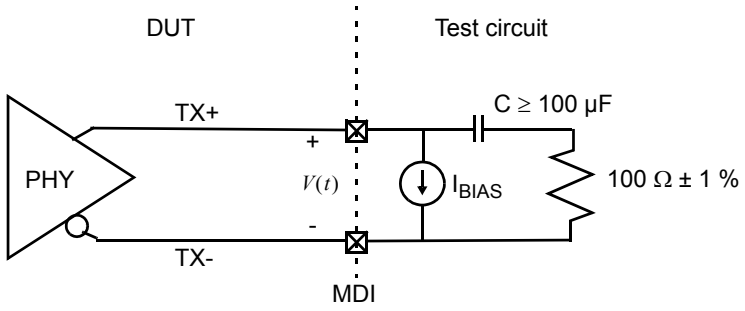
A 100BASE-TX receiver in a Type 2 or greater Endpoint PSE or Type 2 or greater PD (see Clause 33) shall meet the requirements of 25.4.7. A 100BASE-TX transmitter in a Type 2 or greater Endpoint PSE or Type 2 or greater PD delivering or accepting more than 13.0 W average power shall meet either the Open Circuit Inductance (OCL) requirement in 9.1.7 of TP-PMD, or meet the requirements of 25.4.5.1.

25.4.5.1 Equivalent system time constant

While transmitting the Data Dependent Jitter (DDJ) packet of TP-PMD A.2, using the test circuit shown in Figure 25–1, the equivalent system time constant, τ, shall be greater than 2.4 µs when calculated using measurement points A and C as shown in Figure 25–2.



DUT = Device under test

NOTE— I_{BIAS} is the current I_{unb} / 2 defined in Clause 33.

Figure 25–1—Type 2 System time constant test circuit

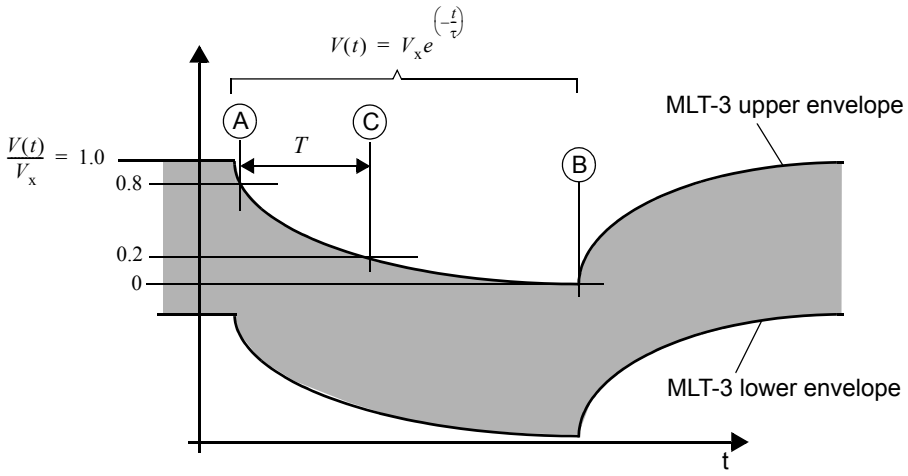


Figure 25–2—Type 2 System time constant measurement

Point B is the point of maximum baseline wander droop, and is the zero point for the vertical axis. Point A, with MDI voltage V_A, is earlier in time from B, with a magnitude that is 80 % of the MLT-3 upper envelope value. Point C, with MDI voltage V_C, is between A and B, with a magnitude that is 20 % of the MLT-3 upper envelope value. The time between A and C is *T*.

These measurements are to be made for the transmitter pair, observing the differential signal output at the MDI with intervening cable, meeting or exceeding the requirements of 25.4.7, less than 1 m long.

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The time constant of the transmitter MDI connected to the test circuit of Figure 25–1 is given by Equation (25–1).

$$\left\{ \tau = \frac{T}{\ln\left(\frac{V_A}{V_C}\right)} = \frac{2L}{R} \right\}_s \qquad (25–1)$$

where

τ	is the effective time constant of the transmitter
T	is the time in seconds from point A to point C as shown in Figure 25–2
V_A	is the MDI voltage at point A
V_C	is the MDI voltage at point C
L	is the open-circuit inductance of the Ethernet isolation transformer for all operating conditions
R	is the 100 Ω termination impedance

25.4.6 Replacement of 8.4.1, "UTP isolation requirements"

A PMD with a MDI that is a PI (see 33.1.3) shall meet the isolation requirements defined in 33.4.1.

A PMD with a MDI that is not a PI shall provide isolation between frame ground and all MDI leads including those not used by the 100BASE-TX PMD.

This electrical isolation shall withstand at least one of the following electrical strength tests.

a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in subclause 5.2.2 of IEC 60950-1:2001.
b) 2250 V dc for 60 s, applied as specified in subclause 5.2.2 of IEC 60950-1:2001.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 µs (1.2 µs virtual front time, 50 µs virtual time of half value), as defined in IEC 60950-1:2001 Annex N.

There shall be no insulation breakdown, as defined in subclause 5.2.2 of IEC 60950-1:2001, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 V dc.

NOTE—In the case of a PMD with a MDI that is not a PI, these requirements are equivalent to those found in TP-PMD.

25.4.7 Addition to 10.1, "Receiver"

Differential voltage signals generated by a remote transmitter that meets the specifications of Clause 25; passed through a link specified in 25.4.8; and received at the MDI of a 100BASE-TX PMD in a Type 2 or greater Endpoint PSE or a Type 2 or greater PD shall be translated into one of the PMD_UNITDATA.indicate messages with a bit error ratio less than 10^{-9} after link reset completion.

25.4.8 Change to 9.1.9, "Jitter"

The jitter measurement specified in 9.1.9 of TP-PMD may be performed using scrambled IDLEs.

In the LPI mode, jitter shall be measured using scrambled SLEEP code-groups transmitted during the TX_SLEEP state (see Figure 24–8). Total transmit jitter with respect to a continuous unjittered reference shall not exceed 1.4 ns peak-to-peak with the exception that the jitter contributions from the clock transitions

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occurring during the TX_QUIET state and the first 5 µs of the TX_SLEEP state or the first 5 µs of the IDLE state following a TX_QUIET state are ignored. The jitter measurement time period shall be not less than 100 ms and not greater than 1 s.

25.4.9 Cable plant

The twisted-pair cabling specification of TP-PMD 11.1 is replaced by that specified in this subclause. The term "link segment" used in this subclause refers to a duplex channel of two pairs. Specifications for a link segment apply equally to each of the two pairs of a duplex channel. All implementations of the balanced cabling link shall be compatible at the MDI.

25.4.9.1 Cabling system characteristics

The cabling system used to support a 100BASE-TX duplex channel requires two pairs of Category 5 balanced cabling with a nominal impedance of 100 Ω. The cabling system components (cables, cords, and connectors) used to provide the link segment shall consist of Category 5 components as specified in ANSI/TIA/EIA-568-A:1995 and ISO/IEC 11801:1995 (D).

NOTE—ISO/IEC 11801:2002 provides a specification (D) for media that exceeds the minimum requirements of this standard.

25.4.9.2 Link transmission parameters

The transmission parameters contained in this subclause are specified to ensure that a Category 5 link segment of up to 100 m, will provide a reliable medium. The transmission parameters of the link segment include insertion loss, characteristics impedance, return loss, NEXT loss, and external coupled noise.

25.4.9.2.1 Insertion loss

The insertion loss of the link segment shall be less than,

$$\text{Insertion_Loss}(f) < 2.1f^{0.529} + 0.4/f \qquad \text{(dB)}$$

at all frequencies from 1 MHz to 100 MHz. This includes the attenuation of the balanced cabling pairs, including work area and equipment cables plus connector losses within the link segment.

The insertion loss specification shall be met when the link segment is terminated in 100 Ω.

NOTE—The above equation approximates the insertion loss specification at 20°C for discrete frequencies of Category 5 100-meter links specified in ANSI/TIA/EIA-568-A Annex E and in TIA/EIA TSB-67.

25.4.9.2.2 Differential characteristic impedance

The nominal differential characteristic impedance of each link segment, which includes cable cords and connecting hardware, is 100 Ω for all frequencies between 1 MHz and 100 MHz.

25.4.9.2.3 Return loss

Each link segment shall meet or exceed the return loss specified in the following equation at all frequencies from 1 MHz to 100 MHz.

$$\text{Return_Loss}(f) \begin{cases} 15 & (1 - 20\ \text{MHz}) \\ 15 - 10\log_{10}(f/20) & (20 - 100\ \text{MHz}) \end{cases} \text{(dB)}$$

where f is the frequency in MHz. The reference impedance shall be 100 Ω.

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25.4.9.2.4 Differential near-end crosstalk (NEXT)

In order to limit the crosstalk at the near end of a duplex channel, the differential pair-to-pair near-end crosstalk (NEXT) loss between the two pairs of a duplex channel shall be at least,

$27.1 - 16.8\log_{10}\ (f/100)$ (dB)

where f is the frequency over the range of 1 MHz to 100 MHz.

NOTE—The above equation approximates the NEXT loss specification at discrete frequencies for Category 5 100-meter links specified in ANSI/TIA/EIA-568-A Annex E and in TIA/EIA TSB-67.

25.4.9.3 Noise environment

The 100BASE-TX noise environment consists of noise from external sources and could impact the objective BER. This noise may consist of sources outside the cabling that couple into the link segment via electric and magnetic fields. In addition noise from adjacent cables, referred to as alien crosstalk, may couple into the link segment. This alien crosstalk is generally present when cables are bound tightly together. To ensure robust operation a 100BASE-TX PHY should operate in the presence of an external noise as specified in 25.4.9.3.1.

25.4.9.3.1 External coupled noise

The differential noise coupled from external sources that is measured at the output of a filter connected to the output of the near end of a disturbed link segment should not exceed 40 mV peak-to-peak. The filter for this measurement is a fifth order Butterworth filter with a 3 dB cutoff at 100 MHz.

25.4.10 Replacement of 11.2, “Crossover function”

Subclause 11.2 of TP-PMD is replaced with the following:

A crossover function compliant with 14.5.2 shall be implemented except that a) the signal names are those used in TP-PMD, and b) the contact assignments for STP are those shown in Table 8-2 of TP-PMD. Note that compliance with 14.5.2 implies a recommendation that crossover (for both UTP and STP) be performed within repeater PHYs.

25.4.11 Change to A.2, “DDJ test pattern for baseline wander measurements”

The length of the test pattern specified in TP-PMD A.2 may be shortened to accommodate feasible 100BASE-X measurements, but shall not be shorter than 3000 code-groups.

NOTE—This pattern is to be applied to the MII. (When applied to the MAC, the nibbles within each byte are to be swapped, e.g., as delivered to the MAC, the test pattern would start, "60 c9 16 ...".)

25.4.12 Change to Annex G, “Stream cipher scrambling function”

An example of a stream cipher scrambling implementation is shown in TP-PMD Annex G. This may be modified to allow synchronization solely on the IDLE sequences between packets.

25.4.13 Change to Annex I, “Common mode cable termination”

The contact assignments shown in TP-PMD Figures I-1 and I-2 shall instead comply with those specified in Table 25–1.

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30. Management

30.9 Management for DTE Power via MDI

Editor's note: (to be removed before working group ballot): Clause 30 to be reviewed and updated when Clause 33 and 79 are stable.

30.9.1 PSE managed object class

This subclause formally defines the behaviours for the oPSE managed object class attributes and actions.

30.9.1.1 PSE attributes

30.9.1.1.1 aPSEID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aPSEID is assigned so as to uniquely identify a PSE among the subordinate managed objects of the containing object.;

30.9.1.1.2 aPSEAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

enabled	PSE functions enabled
disabled	PSE functions disabled

BEHAVIOUR DEFINED AS:
A read-only value that identifies the operational state of the PSE functions. An interface which can provide the PSE functions specified in Clause 33 will be enabled to do so when this attribute has the enumeration "enabled." When this attribute has the enumeration "disabled" the interface will act as it would if it had no PSE function. The operational state of the PSE function can be changed using the acPSEAdminControl action. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the PSE Enable bit specified in 33.5.1.1.5.;

30.9.1.1.3 aPSEPowerPairsControlAbility

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
Indicates the ability to control which PSE Pinout Alternative (see 33.2.3) is used for PD detection and power. When "true" the PSE Pinout Alternative used can be controlled through the aSectionSESs attribute. When "false" the PSE Pinout Alternative used cannot be controlled through the aSectionSESs attribute. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Pair Control Ability bit specified in 33.5.1.2.12;

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30.9.1.1.4 aPSEPowerPairs

Change text in section 30.9.1.1.4 as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

signal	PSE Pinout Alternative A
spare	PSE Pinout Alternative B
both	PSE Pinout Alternative A and Alternative B

BEHAVIOUR DEFINED AS:

A read-write value that identifies the supported PSE Pinout Alternative specified in 33.2.3. A GET operation returns the PSE Pinout Alternative in use. A SET operation changes the PSE Pinout Alternative used to the indicated value only if the attribute aSectionSESThreshold is "true." If the attribute aSectionSESThreshold is "false" a SET operation has no effect.

The enumeration "signal" indicates that PSE Pinout Alternative A is used for PD detection and power. The enumeration "spare" indicates that PSE Pinout Alternative B is used for PD detection and power. The enumeration "both" indicates that the PSE Pinout uses both Alternative A and Alternative B for detection and power. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Pair Control bits specified in 33.5.1.1.4.;

30.9.1.1.5 aPSEPowerDetectionStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

disabled	PSE disabled
searching	PSE searching
deliveringPower	PSE delivering power
test	PSE test mode
fault	PSE fault detected
otherFault	PSE implementation specific fault detected

BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the PD Detection function specified in 33.2.5.

The enumeration "disabled" indicates that the PSE State diagram (Figure 33–9) is in the state DISABLED. The enumeration "deliveringPower" indicates that the PSE State diagram is in the state POWER_ON. The enumeration "test" indicates that the PSE State diagram is in the state TEST_MODE. The enumeration "fault" indicates that the PSE State diagram is in the state TEST_ERROR. The enumeration "otherFault" indicates that the PSE State diagram is in the state IDLE due to the variable error_condition = true. The enumeration "searching" indicates the PSE State diagram is in a state other than those listed above. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the PSE Status bits specified in 33.5.1.2.11.

NOTE—A derivative attribute may wish to apply a delay to the use of the "deliveringPower" enumeration as the PSE state diagram will enter then quickly exit the POWER_ON state if a short-circuit or overcurrent condition is present when power is first applied.;

30.9.1.1.6 aPSEPowerClassification

Change text in section 30.9.1.1.6 as follows:

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ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

class0	Class 0 PD
class1	Class 1 PD
class2	Class 2 PD
class3	Class 3 PD
class4	Class 4 PD
class5	Class 5 PD
class6	Class 6 PD
class7	Class 7 PD
class8	Class 8 PD

BEHAVIOUR DEFINED AS:

A read-only value that indicates the PD Class of a detected PD as specified in 33.2.6.1.

This value is only valid while a PD is being powered, that is the attribute aLineSESThreshold reporting the enumeration "deliveringPower." If a Clause 22 MII or Clause 35 GMII is present, then this will map to the PD Class bits specified in 33.5.1.2.10.;

~~*Editor's note: dual-signature also needs to be addressed here.*~~

30.9.1.1.7 aPSEInvalidSignatureCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 33–9) enters the state SIGNATURE_INVALID. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Invalid Signature bit specified in 33.5.1.2.6.;

30.9.1.1.8 aPSEPowerDeniedCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 33–9) enters the state POWER_DENIED. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Power Denied bit specified in 33.5.1.2.4.;

30.9.1.1.9 aPSEOverLoadCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

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This counter is incremented when the PSE state diagram (Figure 33–9) enters the state ERROR_DELAY_OVER. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Overload bit specified in 33.5.1.2.8.;

30.9.1.1.10 aPSEShortCounter

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:
This counter is incremented when the PSE state diagram (Figure 33–9) enters the state ERROR_DELAY_SHORT. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Short Circuit bit specified in 33.5.1.2.7.;

30.9.1.1.11 aPSEMPSAbsentCounter

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:
This counter is incremented when the PSE state diagram (Figure 33–9) transitions directly from the state POWER_ON to the state IDLE due to tmpdo_timer_done being asserted. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the MPS Absent bit specified in 33.5.1.2.9.;

30.9.1.1.12 aPSEActualPower

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
An integer value indicating present (actual) power being supplied by the PSE as measured at the MDI in milliwatts. The behaviour is undefined if the state of aPSEPowerDetectionStatus is anything other than deliveringPower. The sampling frequency and averaging is vendor-defined.;

30.9.1.1.13 aPSEPowerAccuracy

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
An integer value indicating the accuracy associated with aPSEActualPower in +/- milliwatts.;

30.9.1.1.14 aPSECumulativeEnergy

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. The counter has a maximum increment rate of 100000 per

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second.

BEHAVIOUR DEFINED AS:

A count of the cumulative energy supplied by the PSE as measured at the MDI in millijoules.;

30.9.1.2 PSE actions

30.9.1.2.1 acPSEAdminControl

ACTION

APPROPRIATE SYNTAX:

Same as aSectionStatus

BEHAVIOUR DEFINED AS:

This action provides a means to alter aSectionStatus.;

30.9.2 PD managed object class

This subclause formally defines the behaviours for the oPD managed object class attributes.

30.9.2.1 PD attributes

30.9.2.1.1 aPDID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aPDID is assigned so as to uniquely identify a PD Power via MDI classification local system among the subordinate managed objects of the containing object.;

30.10 Layer management for Midspan

30.10.1 Midspan managed object class

This subclause formally defines the behaviours for the oMidSpan managed object class, attributes, and notifications.

30.10.1.1 Midspan attributes

30.10.1.1.1 aMidSpanID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aMidSpanID is assigned so as to uniquely identify a Midspan device among the subordinate managed objects of system (systemID and system are defined in ISO/IEC 10165-2:1992 [SMI]).;

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30.10.1.1.2 aMidSpanPSEGroupCapacity

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The aMidSpanPSEGroupCapacity is the number of PSE groups that can be contained within the Midspan device. Within each managed Midspan device, the PSE groups are uniquely numbered in the range from 1 to aMidSpanPSEGroupCapacity.

Some PSE groups may not be present in a given Midspan instance, in which case the actual number of PSE groups present is less than aMidSpanPSEGroupCapacity. The number of PSE groups present is never greater than aMidSpanPSEGroupCapacity.;

30.10.1.1.3 aMidSpanPSEGroupMap

ATTRIBUTE

APPROPRIATE SYNTAX:
BITSTRING

BEHAVIOUR DEFINED AS:
A string of bits which reflects the current configuration of PSE groups that are viewed by PSE group managed objects. The length of the bitstring is "aMidSpanPSEGroupCapacity" bits. The first bit relates to PSE group 1. A "1" in the bitstring indicates presence of the PSE group, "0" represents absence of the PSE group.;

30.10.1.2 Midspan notifications

30.10.1.2.1 nMidSpanPSEGroupMapChange

NOTIFICATION

APPROPRIATE SYNTAX:
BITSTRING

BEHAVIOUR DEFINED AS:
This notification is sent when a change occurs in the PSE group structure of a Midspan device. This occurs only when a PSE group is logically removed from or added to a Midspan device. The nMidSpanPSEGroupMapChange notification is not sent when powering up a Midspan device. The value of the notification is the updated value of the aMidSpanPSEGroupMap attribute.;

30.10.2 PSE Group managed object class

This subclause formally defines the behaviours for the oPSEGroup managed object class, attributes, actions, and notifications.

30.10.2.1 PSE Group attributes

30.10.2.1.1 aPSEGroupID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

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BEHAVIOUR DEFINED AS:

A value unique within the Midspan device. The value of aPSEGroupID is assigned so as to uniquely identify a PSE group among the subordinate managed objects of the containing object (oMidSpan). This value is never greater than aMidSpanPSEGroupCapacity.;

30.10.2.1.2 aPSECapacity

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The aPSECapacity is the number of PSEs contained within the PSE group. Valid range is 1–1024. Within each PSE group, the PSEs are uniquely numbered in the range from 1 to aPSECapacity. Some PSEs may not be present in a given PSE group instance, in which case the actual number of PSEs present is less than aPSECapacity. The number of PSEs present is never greater than aPSECapacity.;

30.10.2.1.3 aPSEMap

ATTRIBUTE

APPROPRIATE SYNTAX:

BitString

BEHAVIOUR DEFINED AS:

A string of bits that reflects the current configuration of PSE managed objects within this PSE group. The length of the bitstring is “aPSECapacity” bits. The first bit relates to PSE 1. A “1” in the bitstring indicates presence of the PSE, “0” represents absence of the PSE.;

30.10.2.2 PSE Group notifications

30.10.2.2.1 nPSEMapChange

NOTIFICATION

APPROPRIATE SYNTAX:

BitString

BEHAVIOUR DEFINED AS:

This notification is sent when a change occurs in the PSE structure of a PSE group. This occurs only when a PSE is logically removed from or added to a PSE group. The nPSEMapChange notification is not sent when powering up a Midspan device. The value of the notification is the updated value of the aPSEMap attribute.;

30.12 Layer Management for Link Layer Discovery Protocol (LLDP)

30.12.2 LLDP Local System Group managed object class

30.12.2.1 LLDP Local System Group attributes

30.12.2.1.5 aLldpXdot3LocPowerPortClass

ATTRIBUTE

APPROPRIATE SYNTAX:

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An ENUMERATED VALUE that has one of the following entries:

pClassPSE	PSE
pClassPD	PD

BEHAVIOUR DEFINED AS:

A read-only value that identifies the port ~~C~~class of the given port associated with the local system.;

30.12.2.1.6 aLldpXdot3LocPowerMDISupported

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean value used to indicate whether the MDI power is supported on the given port associated with the local system.;

30.12.2.1.7 aLldpXdot3LocPowerMDIEnabled

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean value used to identify whether MDI power is enabled on the given port associated with the local system.;

30.12.2.1.8 aLldpXdot3LocPowerPairControlable

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean value derived from the value of pethPsePortPowerPairsControlAbility object (defined in IETF RFC 3621) and used to indicate whether the pair selection can be controlled on the given port associated with the local system.;

30.12.2.1.9 aLldpXdot3LocPowerPairs

ATTRIBUTE

APPROPRIATE SYNTAX:

The same as used for aPSEPowerPairs

BEHAVIOUR DEFINED AS:

A read-only the value that contains the value of the pethPsePortPowerPairs object (defined in IETF RFC 3621) which is associated with the given port on the local system.;

30.12.2.1.10 aLldpXdot3LocPowerClass

ATTRIBUTE

APPROPRIATE SYNTAX:

The same as used for aPSEPowerClassification

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BEHAVIOUR DEFINED AS:

A read-only the value that contains the value of the pethPsePortPowerClassifications object (defined in IETF RFC 3621) which is associated with the given port on the local system.;

30.12.2.1.14 aLldpXdot3LocPowerType

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:

A GET attribute that returns a bit string indicating whether the local system is a PSE or a PD and whether it is Type 1 or Type 2. The first bit indicates Type 1 or Type 2. The second bit indicates PSE or PD. A PSE shall set this bit to indicate a PSE. A PD shall set this bit to indicate a PD.;

30.12.2.1.15 aLldpXdot3LocPowerSource

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:

A GET attribute that returns a bit string indicating the power sources of the local system. A PSE indicates whether it is being powered by a primary power source; a backup power source; or unknown. A PD indicates whether it is being powered by a PSE and locally; by a PSE only; or unknown.;

30.12.2.1.16 aLldpXdot3LocPowerPriority

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

low	low priority PD
high	high priority PD
critical	critical priority PD
unknown	priority unknown

BEHAVIOUR DEFINED AS:

A GET attribute that returns the priority of a PD system. For a PSE, this is the priority that the PSE assigns to the PD. For a PD, this is the priority that the PD requests from the PSE.
A SET operation changes the priority of the PD system to the indicated value.;

30.12.2.1.17 aLldpXdot3LocPDRequestedPowerValue

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the PD requested power value. For a PD, it is the power value that the PD has currently requested from the remote system. PD requested power value is the maximum input average power the PD ever draws under this power allocation if accepted. For a PSE, it is the power value that the PSE mirrors back to the remote system. This is the PD requested power value that was used by the PSE to compute the power it has currently allocated to the remote system. The

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PD requested power value is encoded according to Equation (79–1), where *X* is the decimal value of aLldpXdot3LocPDRequestedPowerValue.;

30.12.2.1.18 aLldpXdot3LocPSEAllocatedPowerValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PSE allocated power value. For a PSE, it is the power value that the PSE has currently allocated to the remote system. The PSE allocated power value is the maximum input average power that the PSE wants the PD to ever draw under this allocation if it is accepted. For a PD, it is the power value that the PD mirrors back to the remote system. This is the PSE allocated power value that was used by the PD to compute the power that it has currently requested from the remote system. The PSE allocated power value is encoded according to Equation (79–2), where *X* is the decimal value of aLldpXdot3LocPSEAllocatedPowerValue.;

Insert four new managed object classes as shown in 30.12.2.1.18a, 30.12.2.1.18b, 30.12.2.1.18c, 30.12.2.1.18d

30.12.2.1.18a aLldpXdot3LocPDMeasuredVoltageValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns PD measured voltage value. For a PD, it is the measured voltage value that the PD has currently measured and sent to the remote system. PD measured voltage value is the voltage measured at its PI. The PD measured voltage value is encoded according to Table 79–6c, where x is the decimal value of aLldpXdot3LocPDMeasuredVoltageValue.

30.12.2.1.18b aLldpXdot3LocPDMeasuredCurrentValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns PD measured current value. For a PD, it is the measured current value that the PD has currently measured and sent to the remote system. PD measured current value is the current measured at its PI. The PD measured current value is encoded according to Table 79–6c, where x is the decimal value of aLldpXdot3LocPDMeasuredCurrentValue.

30.12.2.1.18c aLldpXdot3LocPSEMeasuredVoltageValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns PSE measured voltage value. For a PSE, it is the measured voltage value that the PSE has currently measured and sent to the remote system. PSE measured voltage

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value is the voltage measured at its PI. The PSE measured voltage value is encoded according to Table 79–6d, where x is the decimal value of aLldpXdot3LocPSEMeasuredVoltageValue.

30.12.2.1.18d aLldpXdot3LocPSEMeasuredCurrentValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns PSE measured current value. For a PSE, it is the measured current value that the PSE has currently measured and sent to the remote system. PSE measured current value is the current measured at its PI. The PSE measured current value is encoded according to Table 79–6d, where x is the decimal value of aLldpXdot3LocPSEMeasuredCurrentValue.

30.12.2.1.21 aLldpXdot3LocReducedOperationPowerValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the reduced operation power value. For a PD, it is a power value that is lower than the currently requested power value. This reduced operation power value represents a power state in which the PD could continue to operate, but with less functionality than at the current PD requested power value. The PSE could optionally use this information in the event that the PSE subsequently requests a lower PD power value than the PD requested power value. For a PSE, it is a power value that the PSE could ask the PD to move to if the PSE wants the PD to move to a lower power state. The definition and encoding of PD requested power value is the same as described in aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17). The default value for this field is the hexadecimal value FFFF.;

30.12.3 LLDP Remote System Group managed object class

This subclause formally defines the behaviours for the oLldpXdot3RemSystemsGroup managed object class attributes.

30.12.3.1.5 aLldpXdot3RemPowerPortClass

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:
pClassPSE PSE
pClassPD PD

BEHAVIOUR DEFINED AS:
A read-only value that identifies the port ~~C~~class of the given port associated with the remote system.;

30.12.3.1.6 aLldpXdot3RemPowerMDISupported

ATTRIBUTE

APPROPRIATE SYNTAX:

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BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean value used to indicate whether the MDI power is supported on the given port associated with the remote system.;

30.12.3.1.7 aLldpXdot3RemPowerMDIEnabled

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean value used to identify whether MDI power is enabled on the given port associated with the remote system.;

30.12.3.1.8 aLldpXdot3RemPowerPairControlable

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean value is derived from the value of pethPsePortPowerPairsControlAbility object (defined in IETF RFC 3621) and is used to indicate whether the pair selection can be controlled on the given port associated with the remote system.;

30.12.3.1.9 aLldpXdot3RemPowerPairs

ATTRIBUTE

APPROPRIATE SYNTAX:

The same as used for aPSEPowerPairs

BEHAVIOUR DEFINED AS:

A read-only the value that contains the value of the pethPsePortPowerPairs object (defined in IETF RFC 3621) which is associated with the given port on the remote system.;

30.12.3.1.10 aLldpXdot3RemPowerClass

ATTRIBUTE

APPROPRIATE SYNTAX:

The same as used for aPSEPowerClassification

BEHAVIOUR DEFINED AS:

A read-only the value that contains the value of the pethPsePortPowerClassifications object (defined in IETF RFC 3621) which is associated with the given port on the remote system.;

30.12.3.1.14 aLldpXdot3RemPowerType

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:

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A GET attribute that returns a bit string indicating whether the remote system is a PSE or a PD and whether it is Type 1 or Type 2. The first bit indicates Type 1 or Type 2. The second bit indicates PSE or PD.;

30.12.3.1.15 aLldpXdot3RemPowerSource

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:
A GET attribute that returns a bit string indicating the power sources of the remote system. When the remote system is a PSE, it indicates whether it is being powered by a primary power source; a backup power source; or unknown. When the remote system is a PD, it indicates whether it is being powered by a PSE and locally; locally only; by a PSE only; or unknown.;

30.12.3.1.16 aLldpXdot3RemPowerPriority

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED value list that has the following entries:

low	low priority PD
high	high priority PD
critical	critical priority PD
unknown	priority unknown

BEHAVIOUR DEFINED AS:
A GET operation returns the priority of the PD system received from the remote system. For a PSE, this is the priority that the remote system requests from the PSE. For a PD, this is the priority that the remote system has assigned to the PD.;

30.12.3.1.17 aLldpXdot3RemPDRequestedPowerValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PD requested power value that was used by the remote system to compute the power value that is has currently allocated to the PD. For a PSE, it is the PD requested power value received from the remote system. The definition and encoding of PD requested power value is the same as described in aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17).;

30.12.3.1.18 aLldpXdot3RemPSEAllocatedPowerValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PSE allocated power value received from the remote system. For a PSE, it is the PSE allocated power value that was used by the remote system to compute the power value that it has currently requested from the PSE. For a PD, it is the PSE allocated power value received from the remote system. The definition and encoding of PSE allocated power value

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is the same as described in aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.18).;

Insert four new remote system group managed object classes as shown in 30.12.3.1.18a, 30.12.3.1.18b, 30.12.3.1.18c, 30.12.3.1.18d

30.12.3.1.18a aLldpXdot3RemPDMeasuredVoltageValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns PD measured voltage received from the remote system by a PSE. The definition and encoding of PD measured voltage value is the same as described in aLldpXdot3LocPDMeasuredVoltageValue 30.12.2.1.18a.

30.12.3.1.18b aLldpXdot3RemPDMeasuredCurrentValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns PD measured current received from the remote system by a PSE. The definition and encoding of PD measured current value is the same as described in aLldpXdot3LocPDMeasuredCurrentValue 30.12.2.1.18b.

30.12.3.1.18c aLldpXdot3RemPSEMeasuredVoltageValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns PSE measured voltage received from the remote system by a PD. The definition and encoding of PSE measured voltage value is the same as described in aLldpXdot3LocPSEMeasuredVoltageValue 30.12.2.1.18c.

30.12.3.1.18d aLldpXdot3RemPSEMeasuredCurrentValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns PSE measured current received from the remote system by a PD. The definition and encoding of PSE measured current value is the same as described in aLldpXdot3LocPSEMeasuredCurrentValue 30.12.2.1.18d.

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33. Data Terminal Equipment (DTE) Power via Media Dependent Interface (MDI)

33.1 Overview

Change text in Section 33.1 as follows:

This clause defines the functional and electrical characteristics of two optional power (non-data) entities, a Powered Device (PD) and Power Sourcing Equipment (PSE), for use with the MAU defined in Clause 14 and the PHYs defined in Clause 25, ~~and~~ Clause 40 and Clause 55. These entities allow devices to draw/ supply power using the same generic cabling as is used for data transmission.

This clause uses several terms defined in Clause 1.4.

DTE powering is intended to provide a 10BASE-T, 100BASE-TX, ~~or~~ 1000BASE-T, or 10GBASE-T device with a single interface to both the data it requires and the power to process this data. This clause specifies the following:

a) A power source to add power to the 100 Ω balanced cabling system
b) The characteristics of a powered device's load on the power source and the structured cabling
c) A protocol allowing the detection of a device that requests power from a PSE
d) Methods to classify devices based on their power needs
e) A method for powered devices and power sourcing equipment to dynamically negotiate and allocate power
f) A method for scaling supplied power back to the detect level when power is no longer requested or required

The importance of item c) above should not be overlooked. Given the large number of legacy devices (both IEEE 802.3 and other types of devices) that could be connected to a 100 Ω balanced cabling system, and the possible consequences of applying power to such devices, the protocol to distinguish compatible devices and non-compatible devices is important to prevent damage to non-compatible devices.

The detection and powering algorithms are likely to be compromised by cabling that is not point-to-point, resulting in unpredictable performance and possibly damaged equipment.

This clause differentiates between the two ends of the powered portion of the link, defining the PSE and the PD as separate but related devices.

Delete section 33.1.1 and renumber sections:

~~**33.1.1 Objectives**~~

~~The following are objectives of Power via MDI:~~

~~a) *Power* – A PD designed to the standard, and within its range of available power, can obtain both power and data for operation through the MDI and therefore needs no additional connections.~~

~~b) *Safety* – A PSE designed to the standard does not introduce non-SELV (Safety Extra Low Voltage) power into the wiring plant.~~

~~c) *Compatibility* – Clause 33 utilizes the MDIs of 10BASE-T, 100BASE-TX, and 1000BASE-T, without modification. Type 1 operation adds no significant requirements to the cabling. Type 2 operation requires ISO/IEC 11801:1995 Class D or better cabling., and a derating of the cabling~~

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~~maximum ambient operating temperature. The clause does not address the operation of 10GBASE-T. For 10GBASE-T operation, the channel model specified in Clause 55 needs to be met without regard to DTE Power via MDI presence or operation.~~

~~d) *Simplicity* – The powering system described here is no more burdensome on the end users than the requirements of 10BASE-T, 100BASE-TX, or 1000BASE-T.~~

33.1.2 Compatibility considerations

All implementations of PD and PSE systems shall be compatible at their respective Power Interfaces (PIs) when used in accordance with the restrictions of Clause 33 where appropriate. Designers are free to implement circuitry within the PD and PSE in an application-dependent manner provided that the respective PI specifications are satisfied.

Change text in section 33.1.3 as follows:

33.1.3 Relationship of DTE Power via MDI to the IEEE 802.3 Architecture

DTE Power via MDI comprises an optional non-data entity. As a non-data entity, it does not appear in a depiction of the OSI Reference Model. Figure 33–1 depicts the positioning of DTE Power via MDI in the case of the PD.

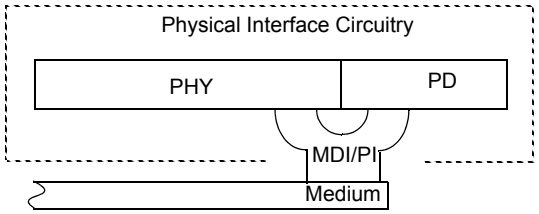

Figure 33–1—DTE Power via MDI powered device relationship to the physical interface circuitry and the IEEE 802.3 CSMA/CD LAN model

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Figure 33–2 and Figure 33–3 depict the positioning of DTE Power via MDI in the cases of the Endpoint PSE and the Midspan PSE, respectively.

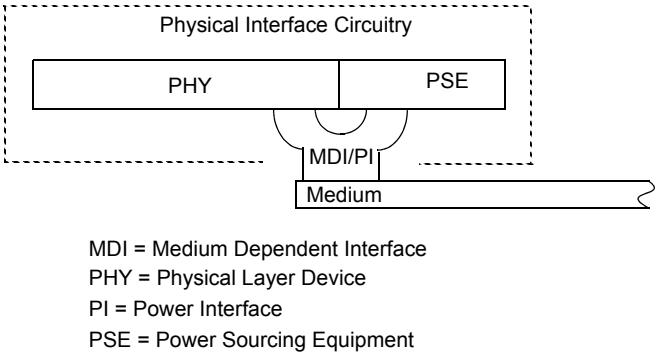

Figure 33–2—DTE Power via MDI Endpoint power sourcing equipment relationship to the physical interface circuitry and the IEEE 802.3 CSMA/CD LAN model

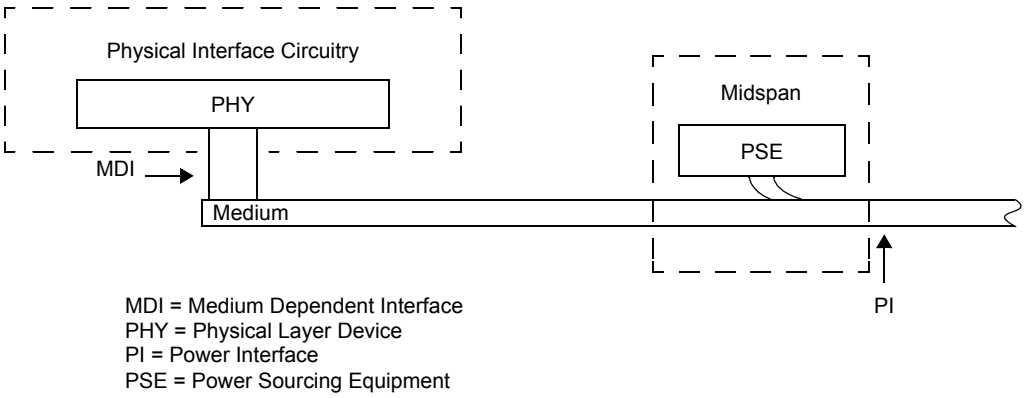

Figure 33–3—DTE Power via MDI Midspan power sourcing equipment relationship to the physical interface circuitry and the IEEE 802.3 CSMA/CD LAN model

The Power Interface (PI) is the ~~generic term that refers to the~~ mechanical and electrical interface between the PSE or PD and the transmission medium as defined in 1.4.324 (1.4.337 in P802.3bx/D3.1).

In an Endpoint PSE and in a PD, the PI is ~~encompassed within~~ the MDI as defined in 1.4.256 (1.4.269 in P802.3bx/D3.1).

PSE power interface specifications that are defined at the MDI apply to an Endpoint PSE. They may or may not apply to a Midspan PSE PI.

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Editor's Note: Editor to consult with staff on duplication of definitions. Waiting for response from staff - note will be removed once response is received.

Change title and text of 33.1.4 as follows:

33.1.4 Type 1 and Type 2 System parameters

A power system consists ~~consisting~~ of a single PSE, ~~link segment, and~~ a single PD, and the link section connecting them. ~~defined~~ PSEs and PDs are categorized by Type. The power system ~~as either Type 1, or Type 2 and~~ has certain basic parameters defined according to Table 33–1. These parameters define not only certain performance characteristics of the system, but are also used in calculating the various electrical characteristics of PSEs and PDs as described in 33.2 and 33.3.

Replace Table 33-1 as follows:

Table 33–1—System power parameters Vs maximum PSE Class

System Power Limit (Maximum PSE Class[1])	Nominal Highest Current per pair[2] (I_{Cable}, A)	Channel pairset maximum DC loop resistance (R_{Ch}, Ω)	Minimum Cabling Type[3]
Class 0 to 3	0.350	20.0	Twisted-pair cabling per 14.4 and 14.5 (Class D or Category 5 recommended)
Class 4	0.600	12.5	Class D (ISO/IEC 11801:1995) or Category 5 (ANSI/EIA/TIA-568-A:1995)
Class 5 and 6	0.600	12.5	Class D (ISO/IEC 11801:2002) or Category 5e (ANSI/EIA/TIA-568-B.2:2001)
Class 7 and 8[4]	0.960	12.5	Class D (ISO/IEC 11801:2002) or Category 5e (ANSI/EIA/TIA-568-B.2:2001)

[1]See Table 33–7, Table 33–7a, and Table 33–7b for a mapping of Class to PSE output power
[2]In Type 3 and Type 4 operation, the current per pairset will be impacted by pair-to-pair system resistance unbalance. See section 33.2.7.4.1.
[3]See sections 33.1.4.1 and 33.1.4.2.
[4]For additional information, see TIA TSB-184-A.

I_{Cable} is the current on one twisted pair in the multi-twisted pair cable. For Type 1 and Type 2 systems, two twisted pairs are required to source I_{Cable}—one carrying (+ I_{Cable}) and one carrying (– I_{Cable}), from the perspective of the PI. All four twisted pairs, connected from PSE PI to PD PI are required to source greater than Class 4 power at the PSE PI - two pairsets each having one twisted pair carrying (+ I_{Cable}) and one twisted pair carrying (– I_{Cable}), from the perspective of the PI.

It should be noted that the cable references use "DC loop resistance," which refers to a single conductor. This clause uses "DC pair loop resistance," which refers to a pair of conductors in parallel. Therefore, R_{Ch} is related to, but not equivalent to, the "DC loop resistance" called out in the cable references.

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Change title and text of 33.1.4.1 as follows:

33.1.4.1 ~~Type 2~~ Cabling requirements

Type 1 power levels may be transmitted over all specified premises cabling that meets the requirements specified in Table 33–1. Type 2 operation requires Class D, or better, cabling as specified in ISO/IEC 11801:1995, with the additional requirement that channel DC loop resistance shall be 25 Ω or less. These requirements are also met by Category 5e or better cable and components as specified in ANSI/TIA-568-C.2; or Category 5 cable and components as specified in ANSI/TIA/EIA-568-A. Type 3 and Type 4 operation requires Class D or better cabling as specified in ISO/IEC 11801:2002. These requirements are also met by Category 5e or better cable and components as specified in ANSI/TIA-568-C.2.

Under worst-case conditions, Type 2, Type 3, and Type 4 operation requires a 10 °C reduction in the maximum ambient operating temperature of the cable when all cable pairs are energized at I_{Cable} (see Table 33–1), or a 5 °C reduction in the maximum ambient operating temperature of the cable when half of the cable pairs are energized at I_{Cable}. Additional cable ambient operating temperature guidelines for Type 2, Type 3, and Type 4 operation are provided in ISO/IEC TR 29125 [B49][1] and TIA TSB-184 [B61].

Editor's Note: TIA TR42.7 is updating TSB-184 to TSB-184-A. Change references to TSB-184-A before publication.

Change title and text of Section 33.1.4.2 as follows:

33.1.4.2 ~~Type 1 and Type 2~~ Channel requirements

~~Type 1, and Type 2 Operation~~ Link sections for all Types shall comply with the resistance unbalance requirements for twisted pair cabling as specified in ISO/IEC 11801:2002 and ANSI/TIA-568-C.2. Refer to Annex 33A for more information including 4-pair operation channel requirements for pair-to-pair resistance unbalance. ~~Operation for all types requires that the resistance unbalance shall be 3 % or less. Resistance unbalance is a measure of the difference between the two conductors of a twisted pair in the 100 Ω balanced cabling system. Resistance unbalance is defined as in Equation (33–1):~~

$$\left\{\frac{(R_{max} - R_{min})}{(R_{max} + R_{min})} \times 100\right\}_{\%} \qquad \text{~~(33–1)~~}$$

~~where~~

~~R_{max} is the resistance of the channel conductor with the highest resistance~~

~~R_{min} is the resistance of the channel conductor with the lowest resistance~~

33.2 Power sourcing equipment (PSE)

The PSE is the portion of the end station or midspan equipment that provides the power to a single PD. The PSE's main functions are as follows:

— To search the link section for a PD
— To supply power to the detected PD through the link section
— To monitor the power on the link section
— To remove power when no longer requested or required, returning to the searching state

[1]The numbers in brackets correspond to those of the bibliography in Annex A.

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An unplugged link section is one instance when power is no longer required.

In addition, power classification mechanisms exist to provide the PSE with detailed information regarding the power needs of the PD.

A PSE is electrically specified at the point of the physical connection to the cabling.

Insert a new section 33.2.0a after section 33.2 as follows:

33.2.0a PSE Type Descriptions

PSEs can be categorized as either Type 1, Type 2, Type 3, or Type 4 PSEs. Table 33–1a summarizes the permissible PSE Types along with supported parameters.

Table 33–1a—Permissible PSE Types

PSE Type	Maximum Class Supported	Supports 4-pair power	Low MPS support[1]	Physical Layer Classification	Data Link Layer Classification	Optional Features
Type 1	Class 3	No	No	Optional Single-Event	Optional	
Type 2	Class 4	No	No	Single-Event or Multiple-Event	Optional[2]	
Type 3	Class 3	Optional	Yes	Single-Event[3]	Optional	Autoclass
Type 3	Class 4	Optional	Yes	Multiple-Event	Optional	Autoclass
Type 3	Class 6	Yes	Yes	Multiple-Event	Optional	Autoclass
Type 4	Class 8	Yes	Yes	Multiple-Event	Optional	Autoclass

[1] Refer to 33.3.8 for details.
[2] Mandatory if only Single-Event Physical Layer classification is implemented. Refer to Table 33–8 for valid classification permutations.
[3] Single-Event Classification differs between Types. Please refer to Table 33–10 items 11 and 12 for details.

33.2.1 PSE location

Change text of section 33.2.1 as follows:

PSEs may be placed in two locations with respect to the link segment, either coincident with the DTE/Repeater or midspan. A PSE that is coincident with the DTE/Repeater is an "Endpoint PSE." A PSE that is located within a link segment that is distinctly separate from and between the MDIs is a "Midspan PSE." The requirements of this document shall apply equally to Endpoint and Midspan PSEs unless the requirement contains an explicit statement that it applies to only one implementation. The location of Alternative A and Alternative B Endpoint PSEs and Midspan PSEs are illustrated in Figure 33–4, Figure 33–5, Figure 33–5a, Figure 33–5b, Figure 33–6, ~~and~~ Figure 33–7, Figure 33–7a, and Figure 33–7b.

PSEs can be compatible with 10BASE-T, 100BASE-TX, ~~and/or~~ 1000BASE-T and/or 10GBASE-T. ~~PSEs may support either Alternative A, Alternative B, or both.~~

Change the title and text of Section 33.2.2 as follows:

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33.2.2 Midspan PSE variants ~~Types~~

There are ~~two~~ several variants ~~types~~ of Midspan PSEs defined.

10BASE-T/100BASE-TX Midspan PSE:

A Midspan PSE that results in a link that can support only 10BASE-T and 100BASE-TX operation (see Figure 33–6). Note that this limitation is due to the presence of the Midspan PSE whether it is supplying power or not.

1000BASE-T Midspan PSE:

A Midspan PSE that results in a link that can support 10BASE-T, 100BASE-TX, and 1000BASE-T operation (see Figure 33–7).

10GBASE-T Midspan PSE:

A Midspan PSE that results in a link that can support 1000BASE-T and 10GBASE-T operation, and optionally support 10BASE-T and 100BASE-TX operation (see Figure 33–7).

NOTE—See 33.4.9.2 for Alternative A Midspan PSEs.

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Change title of Figure 33-4 as follows:

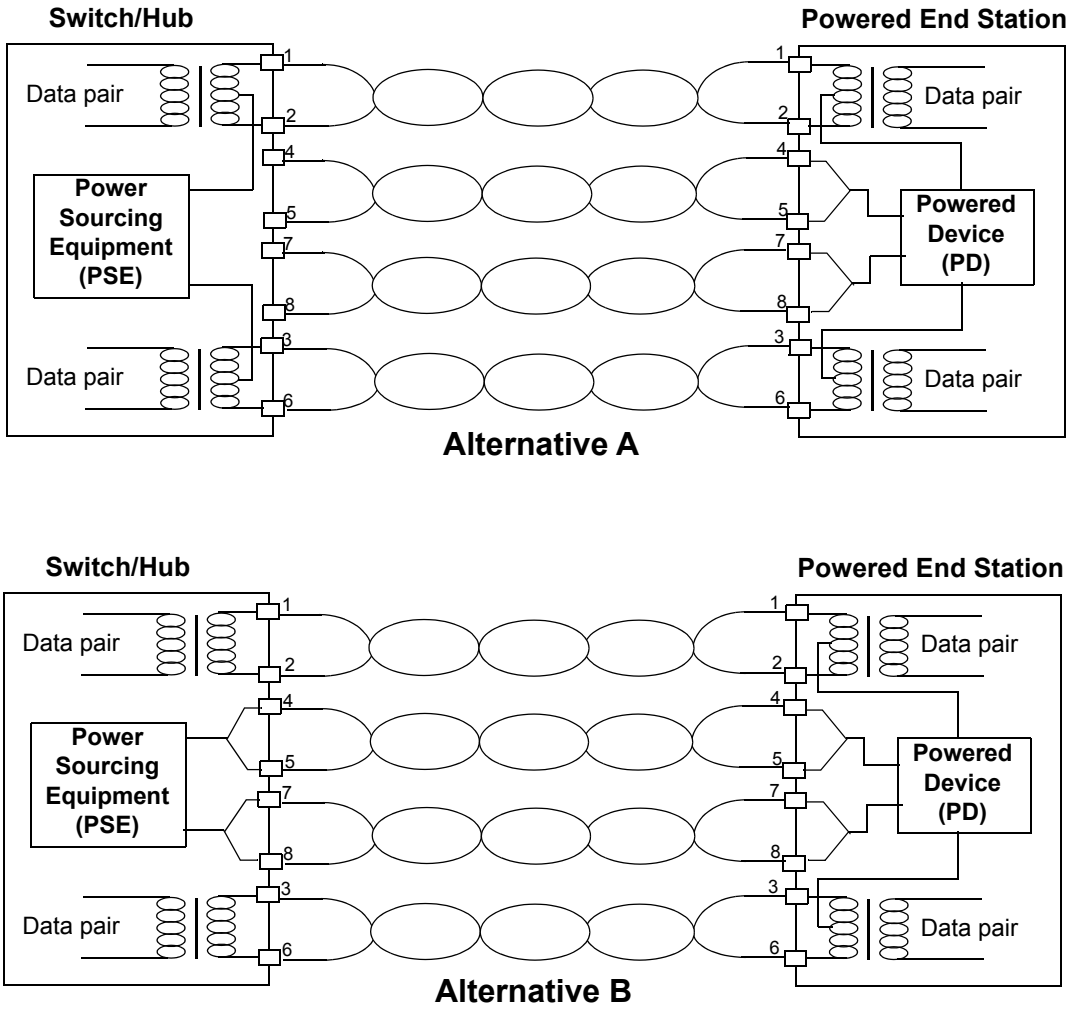

Figure 33–4—10BASE-T/100BASE-TX 2-Pair Endpoint PSE location overview

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Change the Title of Figure 33-5 as follows:

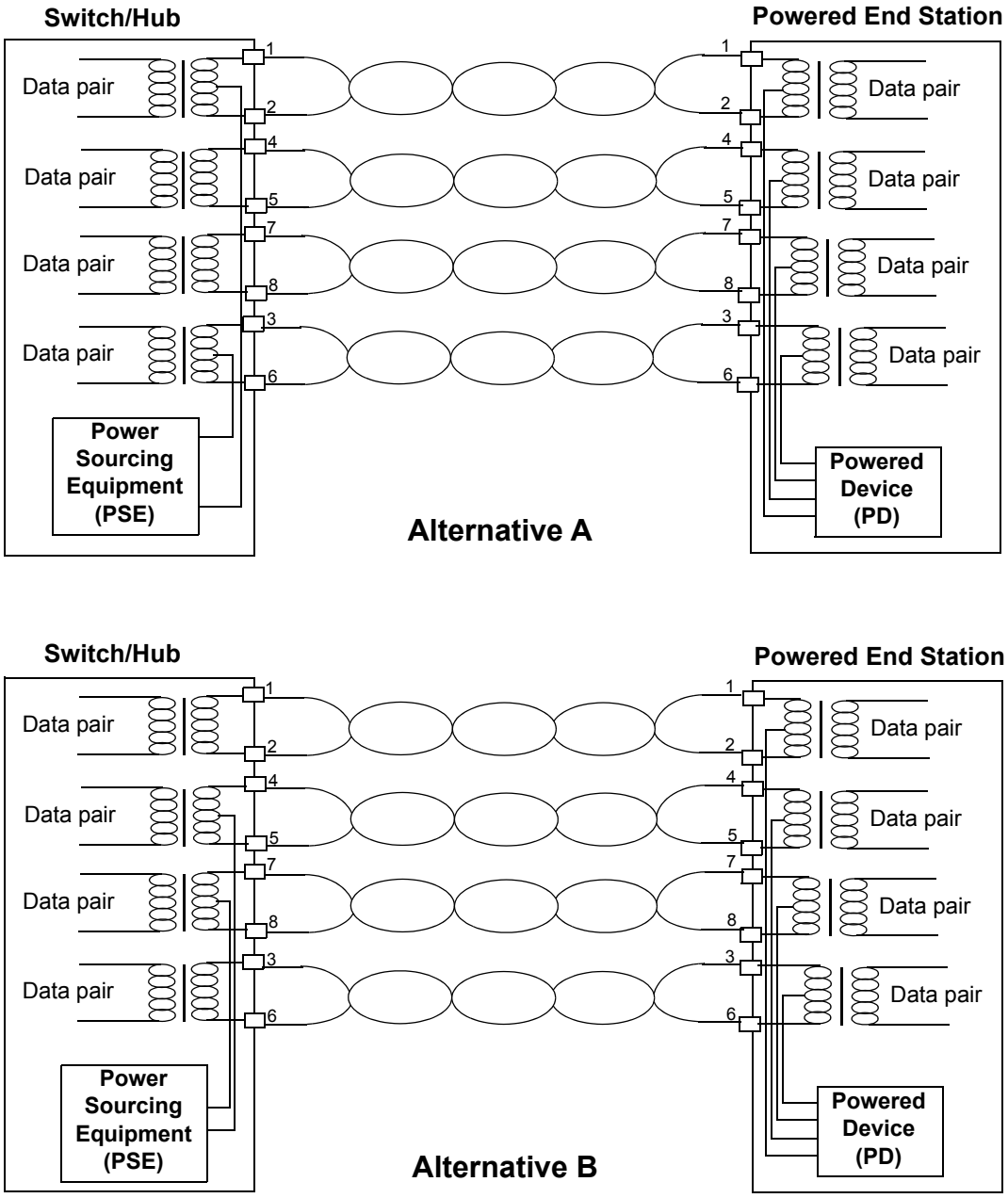

Figure 33–5—1000BASE-T/10GBASE-T 2-Pair Endpoint PSE location overview

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Insert two new figures - figure 33-5a and 33-5b as follows:

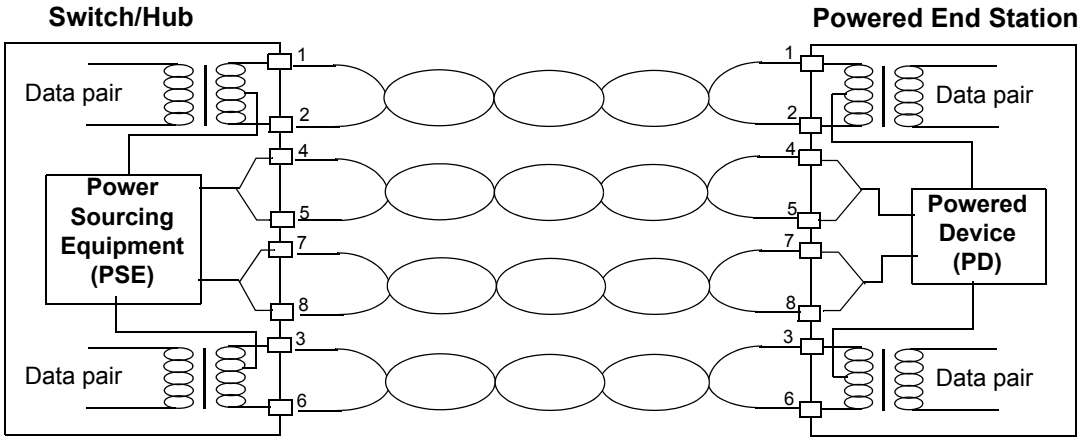

Figure 33–5a—10BASE-T/100BASE-TX 4-Pair Endpoint PSE location overview

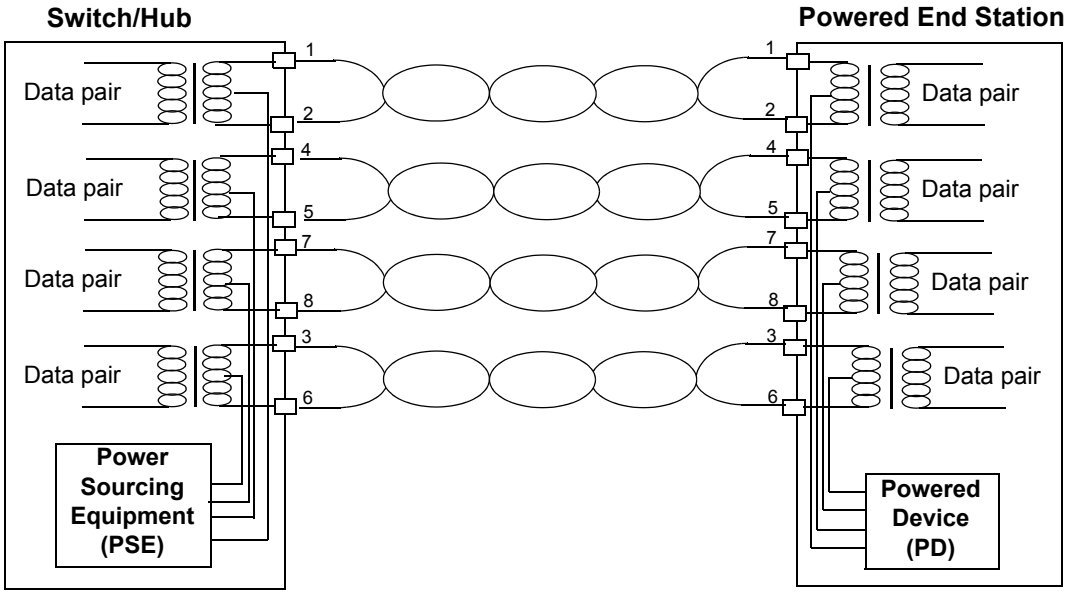

Figure 33–5b—1000BASE-T/10GBASE-T 4-Pair Endpoint PSE location overview

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Change title of Figure 33-6 as follows:

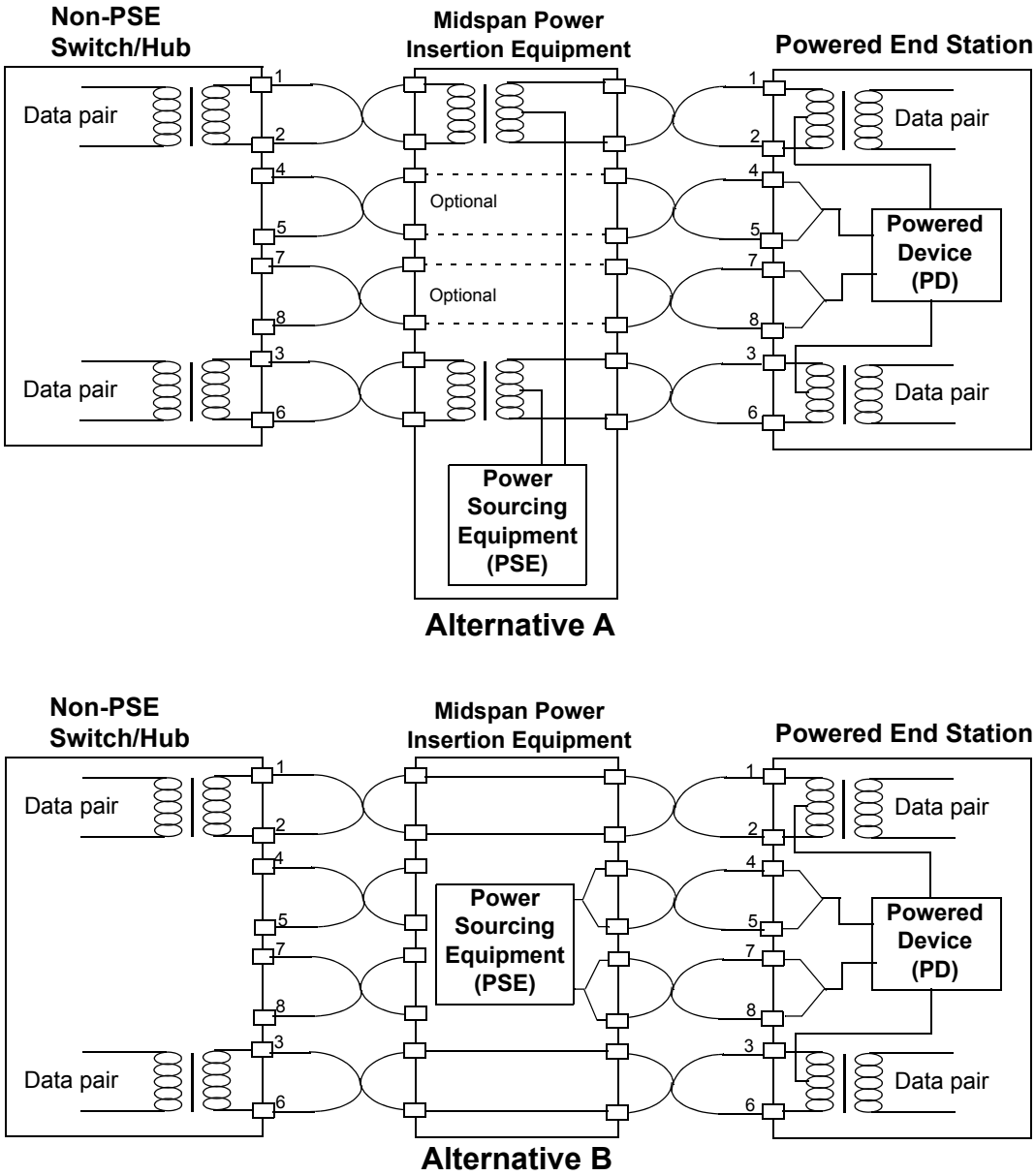

Figure 33–6—10BASE-T/100BASE-TX <u>2-Pair</u> Midspan PSE location overview

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Change the title of Figure 33-7 as follows:

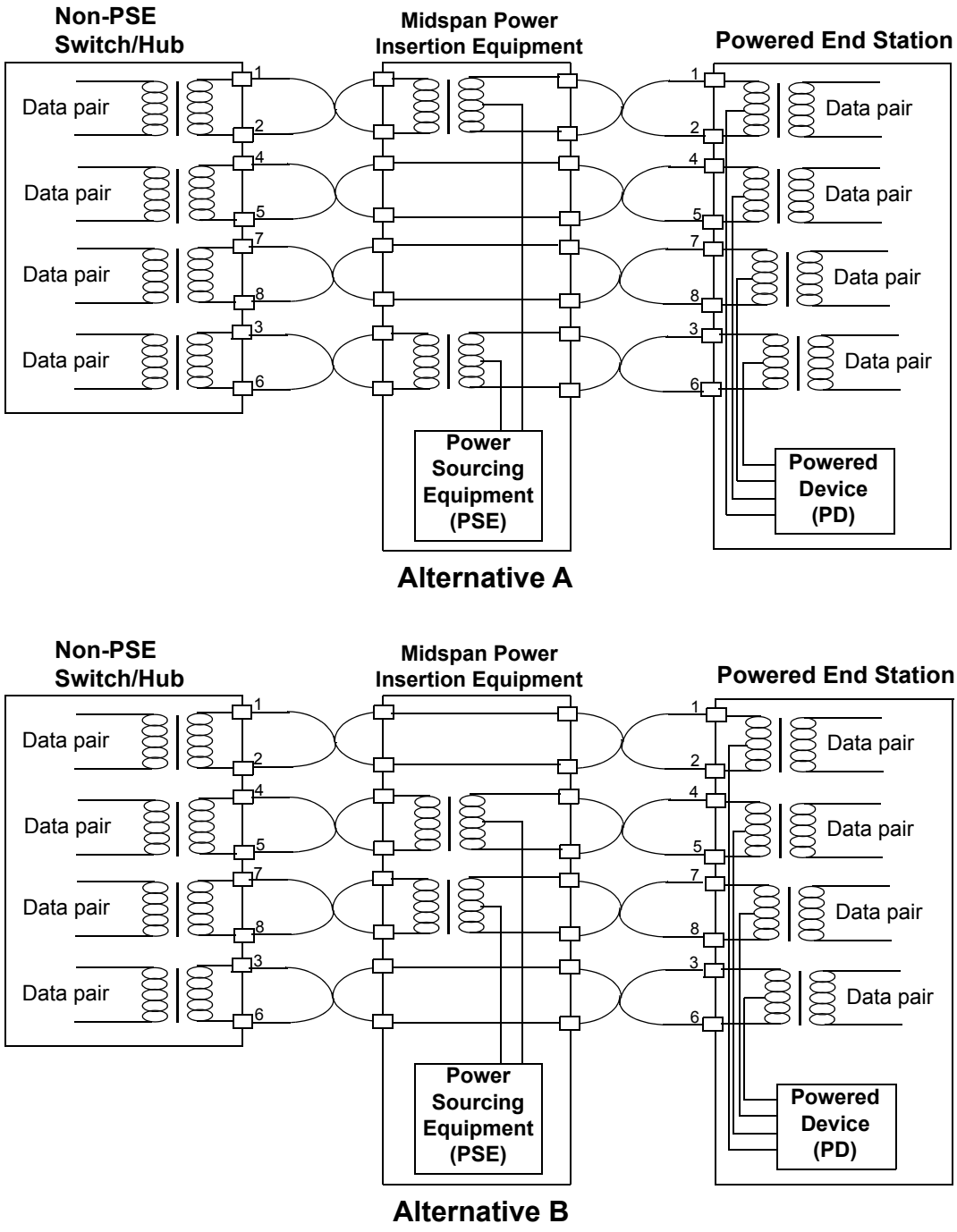

Figure 33–7—1000BASE-T/10GBASE-T 2-Pair Midspan PSE location overview

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Insert Figure 33-7a and Figure 33-7b after Figure 33-4 as follows:

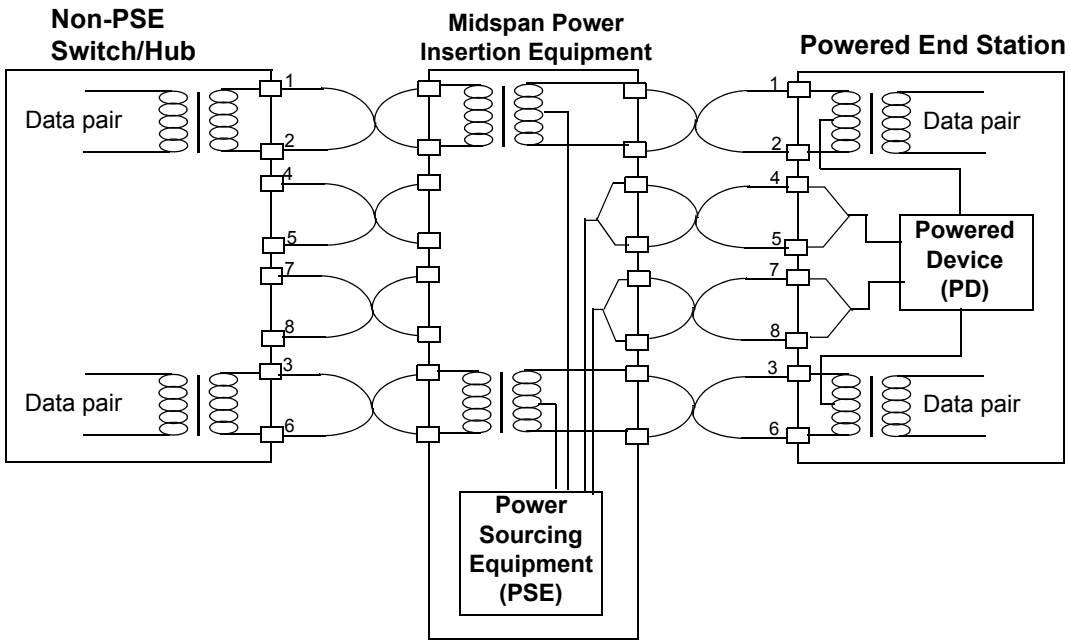

Figure 33–7a—10BASE-T/100BASE-TX 4-Pair Midspan PSE location overview

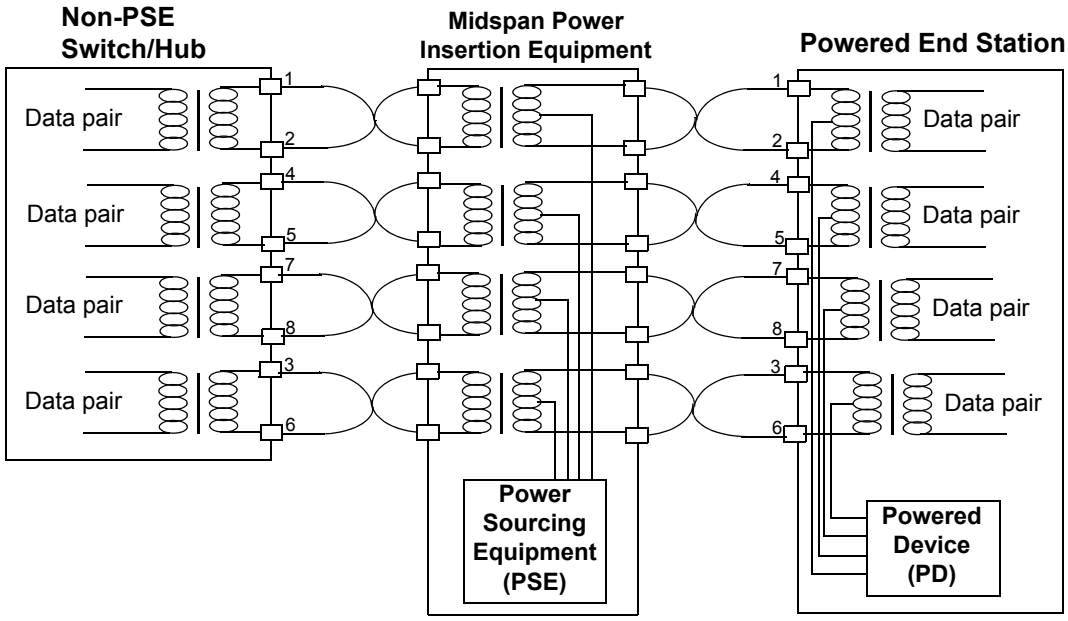

Figure 33–7b—1000BASE-T/10GBASE-T 4-Pair Midspan PSE location overview

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Change the text in section 33.2.3 as follows:

33.2.3 PI pin assignments

A PSE device may provide power via one or both of the two valid four-wire connections. In each four-wire connection, the two conductors associated with a pair each carry the same nominal current in both magnitude and polarity. Figure 33–8, in conjunction with Table 33–2, illustrates the valid alternatives.

Table 33–2—PSE Pinout alternatives

Conductor	Alternative A (MDI-X)	Alternative A (MDI)	Alternative B(S) ~~(All)~~	Alternative B(X)
1	Negative V_{PSE}	Positive V_{PSE}		
2	Negative V_{PSE}	Positive V_{PSE}		
3	Positive V_{PSE}	Negative V_{PSE}		
4			Positive V_{PSE}	Negative V_{PSE}
5			Positive V_{PSE}	Negative V_{PSE}
6	Positive V_{PSE}	Negative V_{PSE}		
7			Negative V_{PSE}	Positive V_{PSE}
8			Negative V_{PSE}	Positive V_{PSE}

Insert new table 33-2a after table 33-2 as follows:

Table 33–2a—Permitted Pinout alternatives per Type

PSE Type	Alternative A (MDI-X)	Alternative A (MDI)	Alternative B(S)	Alternative B(X)
Type 1 and Type 2	Yes	Yes	Yes	No
Type 3	Yes	Yes	Yes	Yes
Type 4	Yes	No	Yes	No

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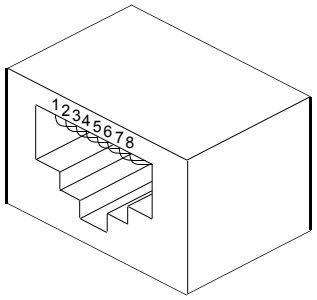

Figure 33–8—PD and PSE eight-pin modular jack

For the purposes of data transfer, the type of PSE data port is relevant to the far-end PD, and in some cases, to the cabling system between them. Therefore, Alternative A matches the positive voltage to the transmit pair of the PSE. ~~PSEs that use automatically configuring MDI/MDI-X ("Auto-MDI-X") ports may choose either polarity choice associated with Alternative A configurations~~. PSEs shall use only the permitted polarity configurations associated with Alternative A or Alternative B listed in Table 33–2a corresponding with their Type. For further information on the placement of MDI vs. MDI-X, see 14.5.2.

Type 1, Type 2 or Type 3 PSEs shall implement Alternative A, Alternative B, or both. Type 3 PSEs providing Class 5 or 6 power levels and Type 4 PSEs shall implement Alternative A and Alternative B. While a PSE may be capable of both Alternative A and Alternative B, Type 1 and Type 2 PSEs shall not operate both Alternative A and Alternative B ~~on the same link segment~~ simultaneously. Type 3 and Type 4 PSEs may operate simultaneously on both Alternatives, when the requirements of Section 33.2.5.6 are met.

Change text in Section 33.2.4 as follows:

33.2.4 PSE state diagrams

~~The~~ Type 1 and Type 2 PSEs shall provide the behavior of the state diagrams shown in Figure 33–9, Figure 33–9 continued, and Figure 33–10e. Type 3 and Type 4 PSEs shall provide the behavior of the state diagrams shown in Figure 33–10a to Figure 33–10d and Figure 33–10e.

33.2.4.1 Overview

Change the text in Section 33.2.4.1 as follows:

Connection Check timing requirements are specified in Table 33–3a. Detection timing requirements are specified in Table 33–4. Classification timing requirements are specified in Table 33–10. Autoclass timing requirements are specified in Table 33–10a. Power turn-on timing requirements are specified in Table 33–11.

~~Detection, classification, and power turn-on timing shall meet the specifications in Table 33–4, Table 33–10, and Table 33–11.~~

If power is to be applied, the PSE turns on power after a valid detection in less than T_{pon} as specified in Table 33–11. If the PSE cannot supply power within T_{pon}, it initiates and successfully completes a new detection cycle before applying power. See 33.2.7.13 for details.

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It is possible that two separate PSEs, one that implements Alternative A and one that implements Alternative B (see 33.2.1), may be attached to the same link segment. In such a configuration, and without the required backoff algorithm, the PSEs could prevent each other from ever detecting a PD by interfering with the detection process of the other.

A PSE performing detection using only Alternative B may fail to detect a valid PD detection signature. When this occurs, the PSE shall back off for at least T_{dbo} as specified in Table 33–11 before attempting another detection. During this backoff, the PSE shall not apply a voltage greater than V_{Off} to the PI. See 33.2.5.5 for more information on Alternative B detection backoff requirements.

~~If a PSE performs performing detection using Alternative B detects an open circuit (see 33.2.5.5 for more information on detection backoff requirements.) on the link section, then that PSE may optionally omit the detection backoff.~~

If a PSE performing detection using Alternative A detects an invalid signature, it should complete a second detection in less than T_{dbo} ~~min~~ after the beginning of the first detection attempt. This allows an Alternative A PSE to complete a successful detection cycle prior to an Alternative B PSE present on the same link section that may have caused the invalid signature.

In the Type 3 and Type 4 state diagram, Alternative A and Alternative B are depicted as serving distinct roles during 4-pair operation. In any implementation, the behaviors of the Alternatives may be reversed as long as the roles are established in IDLE and shall be maintained in every other state.

NOTE—A Type 1 PSE performing detection using Alternative A may need to have its DTE powering ability disabled when it is attached to the same link segment as a Type 2 Midspan PSE performing detection using Alternative B. This allows the Midspan PSE to successfully complete a detection cycle.

33.2.4.2 Conventions

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5.

Change the title and contents of 33.2.4.3, 33.2.4.4, 33.2.4.5, 33.2.4.6, and 33.2.4.7 as follows:

33.2.4.3 Type 1 and Type 2constants

The PSE state diagrams use the following constants:

PSE_TYPE
A constant indicating the Type of the PSE
Values:1: Type 1 PSE
2: Type 2 PSE

33.2.4.4 Type 1 and Type 2variables

The PSE state diagrams use the following variables:

class_num_events
A variable indicating the number of classification events performed by the PSE. A variable that is set in an implementation-dependent manner.
Values:0: PSE does not perform Physical Layer classification.
1: PSE performs 1-Event Physical Layer classification.
2: PSE performs 2-Event Physical Layer classification.

error_condition
A variable indicating the status of implementation-specific fault conditions or optionally other

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system faults that prevent the PSE from meeting the specifications in Table 33–11 and that require the PSE not to source power. These error conditions are different from those monitored by the state diagrams in Figure 33–10e.

Values:FALSE:No fault indication.
TRUE:A fault indication exists.

I_{Inrush}

Output current during POWER_UP (see Table 33–11 and Figure 33–13).

I_{Port}

Output current (see 33.2.7.6).

legacy_powerup

This variable is provided for PSEs that monitor the PI voltage output and use that information to indicate the completion of PD inrush current during POWER_UP operation. Using only the PI voltage information may be insufficient to determine the true end of PD inrush current; use of a fixed T_{Inrush} period is recommended. A variable that is set in an implementation-dependent manner.

Values:TRUE:The PSE supports legacy power up; this value is not recommended.
FALSE:The PSE does not support legacy power up. It is highly recommended that new equipment use this value.

mr_mps_valid

The PSE monitors either the DC or AC Maintain Power Signature (MPS, see 33.2.9.1). This variable indicates the presence or absence of a valid MPS.

Values:FALSE:If monitoring both components of the MPS, the DC component of MPS is absent or the AC component of MPS is absent. If monitoring only one component of MPS, that component of MPS is absent.
TRUE: If monitoring both components of the MPS, the DC component of MPS and the AC component of MPS are both present. If monitoring only one component of MPS, that component of MPS is present.

mr_pse_alternative

This variable indicates which Pinout Alternative the PSE uses to apply power to the link (see Table 33–2). This variable is provided by a management interface that may be mapped to the PSE Control register Pair Control bits (11.3:2) or other equivalent function.

Values:A: The PSE uses PSE pinout Alternative A.
B: The PSE uses PSE pinout Alternative B.

mr_pse_enable

A control variable that selects PSE operation and test functions. This variables is provided by a management interface that may be mapped to the PSE Control register PSE Enable bits (11.1:0), as described below, or other equivalent functions.

Values:disable: All PSE functions disabled (behavior is as if there was no PSE functionality). This value corresponds to MDIO register bits 11.1:0 = '00'.
enable: Normal PSE operation. This value corresponds to MDIO register bits 11.1:0 = '01'.
force_power: Test mode selected that causes the PSE to apply power to the PI when there are no detected error conditions. This value corresponds to MDIO register bits 11.1:0 = '10'.

option_detect_ted

This variable indicates if detection can be performed by the PSE during the ted_timer interval.

Values:FALSE:Do not perform detection during ted_timer interval.
TRUE:Perform detection during ted_timer interval.

option_vport_lim

This optional variable indicates if V_{PSE} is out of the operating range during normal operating state.

Values:FALSE:V_{PSE} is within the V_{Port_PSE} operating range as defined in Table 33–11.
TRUE:V_{PSE} is outside of the V_{Port_PSE} operating range as defined in Table 33–11.

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ovld_detected

A variable indicating if the PSE output current has been in an overload condition (see 33.2.7.6) for at least T_{CUT} of a one second sliding time.

Values:FALSE:The PSE has not detected an overload condition.
TRUE:The PSE has detected an overload condition.

pd_dll_power_type

A control variable output by the PSE power control state diagram (Figure 33–27) that indicates the Type of PD as advertised through Data Link Layer classification.

Values:1: PD is a Type 1 PD (default)
2: PD is a Type 2 PD

pi_powered

A variable that controls the circuitry that the PSE uses to power the PD.

Values:FALSE:The PSE is not to apply power to the link (default).
TRUE:The PSE has detected a PD, classified it if applicable, and determined the PD is to be powered; or power is being forced on in TEST_MODE.

power_applied

A variable indicating that the PSE has begun steady state operation by having asserted pi_powered, completed the ramp up of voltage, is not in a current limiting mode, and is operating beyond the POWER_UP requirements of 33.2.7.5.

Values:FALSE:The PSE is either not applying power or has begun applying power but is still in POWER_UP.
TRUE:The PSE has begun steady state operation.

power_not_available

Variable that is asserted in an implementation-dependent manner when the PSE is no longer capable of sourcing sufficient power to support the attached PD. Sufficient power is defined by classification; see 33.2.6.

Values:FALSE:PSE is capable to continue to source power to a PD.
TRUE:PSE is no longer capable of sourcing power to a PD.

pse_available_power

This variable indicates the highest power PD Class that could be supported. The value is determined in an implementation-specific manner.

Values:0: Class 1
1: Class 2
2: Class 0 and Class 3
3: Class 4

pse_dll_capable

This variable indicates whether the PSE is capable of performing optional Data Link Layer classification. See 33.6. This variable is provided by a management interface that may be mapped to the PSE Control register Data Link Layer Classification Capability bit (11.5), as described below, or other equivalent functions. A variable that is set in an implementation-dependent manner.

Values:FALSE:The PSE's Data Link Layer classification capability is not enabled.
TRUE:The PSE's Data Link Layer classification capability is enabled.

pse_dll_enabled

A variable indicating whether the Data Link Layer classification mechanism is enabled. See 33.6.

Values:FALSE:Data Link Layer classification is not enabled.
TRUE:Data Link Layer classification is enabled.

pse_ready

Variable that is asserted in an implementation-dependent manner to probe the link segment.

Values:FALSE:PSE is not ready to probe the link segment.
TRUE:PSE is ready to probe the link segment.

NOTE—Care should be taken when negating this variable in a PSE performing detection using Alternative A after an invalid signature is detected due to the delay it introduces between detection attempts (see 33.2.4.1).

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pse_reset

Controls the resetting of the PSE state diagram. Condition that is TRUE until such time as the power supply for the device that contains the PSE overall state diagrams has reached the operating region. It is also TRUE when implementation-specific reasons require reset of PSE functionality.
Values:FALSE:Do not reset the PSE state diagram.
TRUE:Reset the PSE state diagram.

pse_skips_event2

The PSE can choose to bypass a portion of the classification state flow. A variable that is set in an implementation-dependent manner.
Values:FALSE:The PSE does not bypass MARK_EV1.
TRUE:The PSE does bypass MARK_EV1.

short_detected

A variable indicating if the PSE output current has been in a short circuit condition for T_{LIM} within a sliding window (see 33.2.7.7).
Values:FALSE:The PSE has not detected a short circuit condition.
TRUE:The PSE has detected qualified short circuit condition.

temp_var

A temporary variable used to store the value of the state variable mr_pd_class_detected.

PSEs shall meet at least one of the allowable variable definition permutations described in Table 33–3.

Change the title of Table 33-3 as follows:

Table 33–3—Allowed Type 1 and Type 2 PSE variable definition permutations

PSE Type	Variables	
	class_num_events	**pse_dll_capable**
Type 2	2	FALSE
		TRUE
	1	TRUE
Type 1	1	FALSE
		TRUE
	0	FALSE
		TRUE

33.2.4.5 Type 1 and Type 2 timers

All timers operate in the manner described in 14.2.3.2 with the following addition: a timer is reset and stops counting upon entering a state where “stop x_timer” is asserted.

tcle1_timer

A timer used to limit the first classification event time in 2-Event classification; see T_{CLE1} in Table 33–10.

tcle2_timer

A timer used to limit the second classification event time in 2-Event classification; see T_{CLE2} in Table 33–10.

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tdbo_timer
: A timer used to regulate backoff upon detection of an invalid signature; see T_{dbo} in Table 33–11.

tdet_timer
: A timer used to limit an attempt to detect a PD; see T_{det} in Table 33–11.

ted_timer
: A timer used to regulate a subsequent attempt to power a PD after an error condition causes power removal; see T_{ed} in Table 33–11. The default state of this timer is ted_timer_done.

tinrush_timer
: A timer used to monitor the duration of the inrush event; see T_{Inrush} in Table 33–11.

tme1_timer
: A timer used to limit the first mark event time in 2-Event classification; see T_{ME1} in Table 33–10.

tme2_timer
: A timer used to limit the second mark event time in 2-Event classification; see T_{ME2} in Table 33–10.

tmpdo_timer
: A timer used to monitor the dropout of the MPS; see T_{MPDO} in Table 33–11.

tpdc_timer
: A timer used to limit the classification time; see T_{pdc} in Table 33–10.

tpon_timer
A timer used to limit the time for power turn-on; see T_{pon} in Table 33–11.

33.2.4.6 Type 1 and Type 2 functions

do_classification
: This function returns the following variables:

  pd_requested_power: This variable indicates the power class requested by the PD. A Type 1 PSE that measures a Class 4 signature assigns that PD to Class 0. See 33.2.6.

  Values:
  - 0: Class 1
  - 1: Class 2
  - 2: Class 0 or Class 3
  - 3: Class 4

  mr_pd_class_detected: The class of the PD associated with the PD classification signature; see Table 33–7 and 33.2.6.

  Values:
  - 0: Class 0
  - 1: Class 1
  - 2: Class 2
  - 3: Class 3
  - 4: Class 4

do_detection
: This function returns the following variables:

  signature:
  This variable indicates the presence or absence of a PD.

  Values:
  - open_circuit:The PSE has detected an open circuit. This value is optionally returned by a PSE performing detection using Alternative B.
  - valid: The PSE has detected a PD requesting power.
  - invalid: Neither open_circuit, nor valid PD detection signature has been found.

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mr_valid_signature:
This variable indicates that the PSE has detected a valid signature.
Values: FALSE: No valid signature detected.
TRUE: Valid signature detected.

do_mark
This function produces the classification mark event voltage. This function does not return any variables.

set_parameter_type
This function is used by a Type 2 PSE to evaluate the Type of PD connected to the link based on Physical Layer classification or Data Link Layer classification results. The PSE's PI electrical requirements defined in Table 33–11 are set to values corresponding to either a Type 1 or Type 2 PSE. This function returns the following variable:

parameter_type: A variable used by a Type 2 PSE to pick between Type 1 and Type 2 PI electrical requirement parameter values defined in Table 33–11.
Values: 1: Type 1 PSE parameter values (default)
2: Type 2 PSE parameter values

When a Type 2 PSE powers a Type 2 PD, the PSE may choose to assign a value of '1' to parameter_type if mutual identification is not complete (see 33.2.6) and shall assign a value of '2' to parameter_type if mutual identification is complete.

When a Type 2 PSE powers a Type 1 PD, the PSE shall meet the PI electrical requirements of a Type 1 PSE, but may choose to meet the electrical requirements of a Type 2 PSE for I_{Con}, I_{LIM}, T_{LIM}, and P_{Type} (see Table 33–11).

Change the title of Figure 33–9 as follows:

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33.2.4.7 Type 1 and Type 2 state diagrams

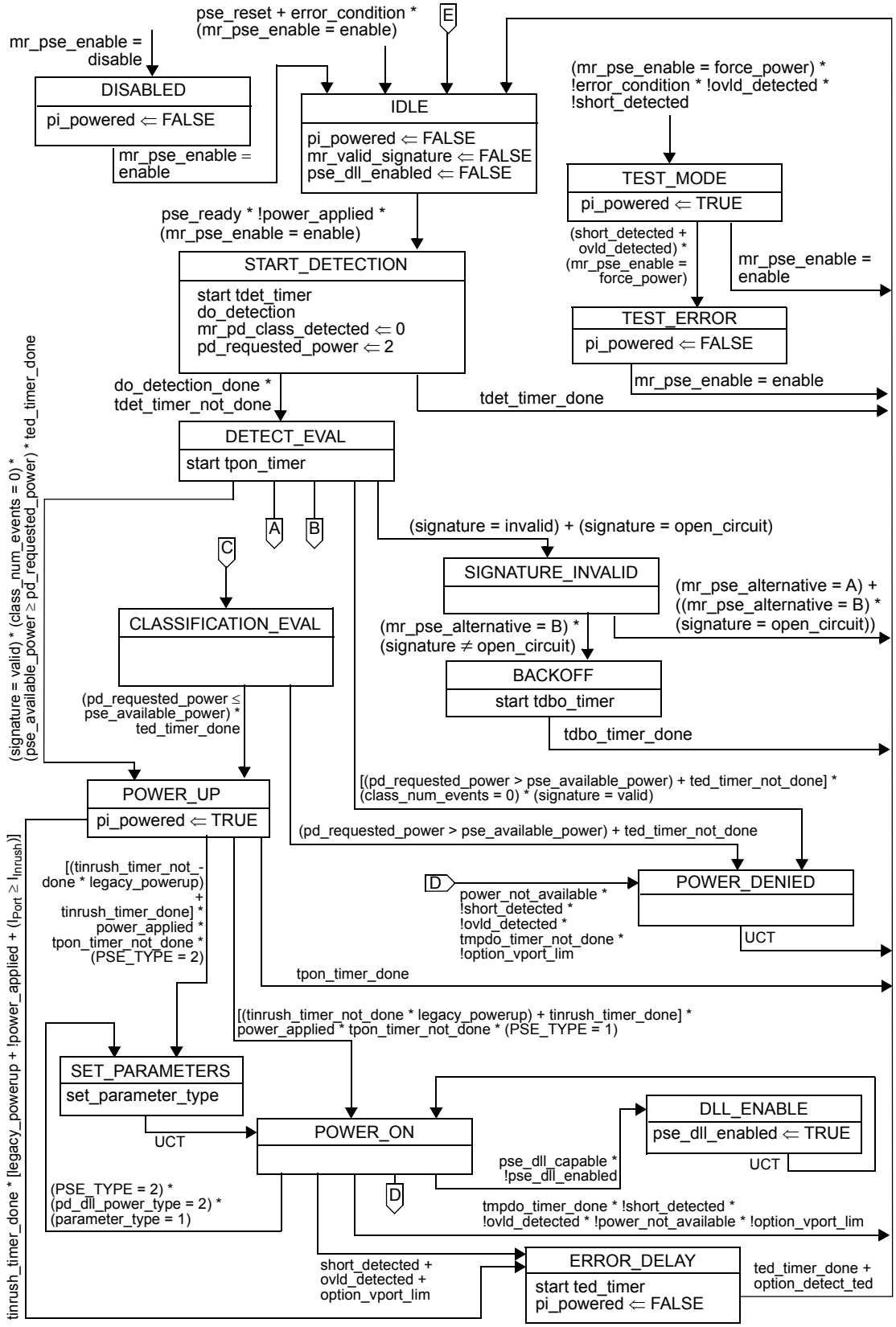

Figure 33–9—Type 1 and Type 2 PSE state diagram

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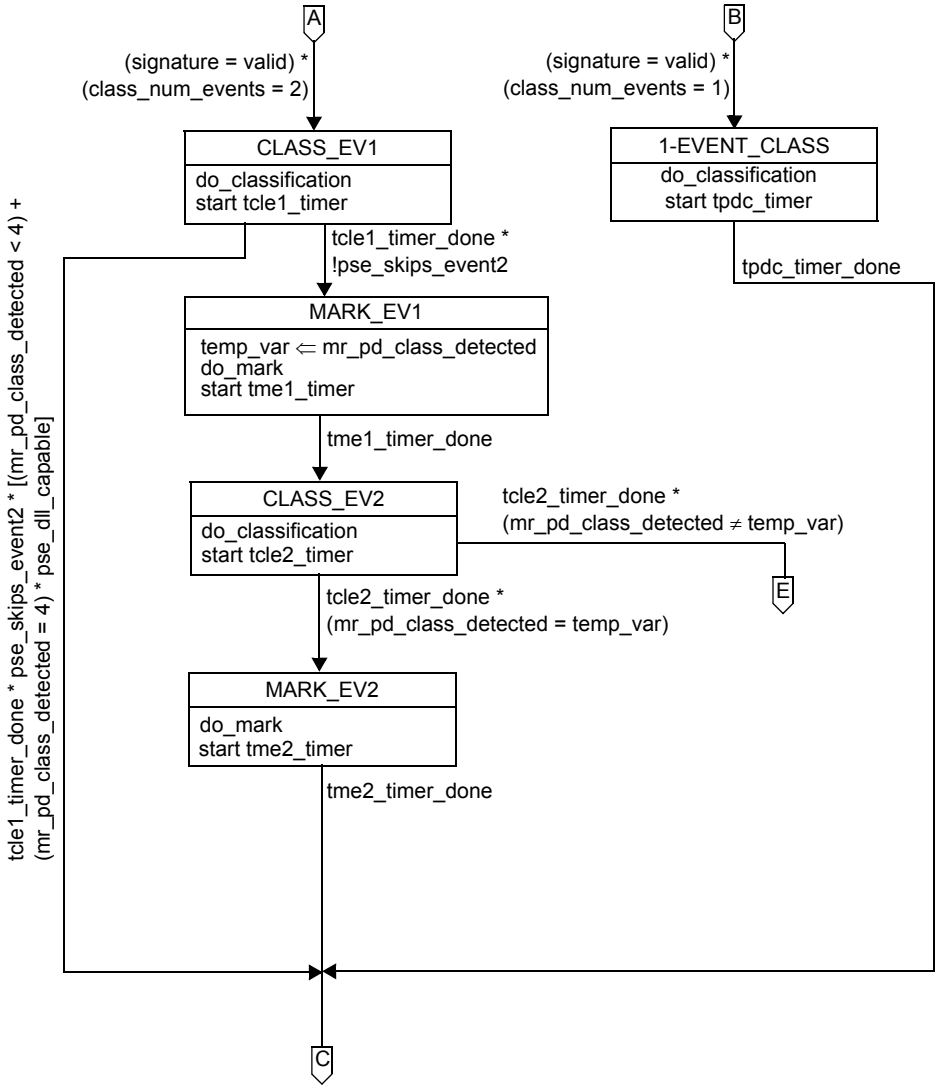

Figure 33–9—Type 1 and Type 2 PSE state diagram *(continued)*

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Change title of Figure 33-10 as follows:

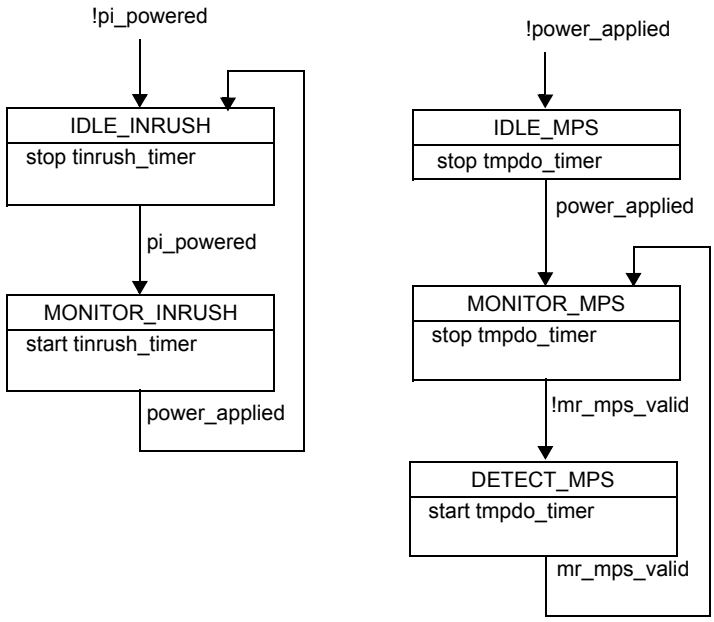

Figure 33–10—PSE monitor inrush and monitor MPS state diagrams

Insert new sections 33.2.4.8, 33.2.4.9, 33.2.4.10, 33.2.4.11, and 33.2.4.12 as follows:

33.2.4.8 Type 3 and Type 4 constants

The PSE state diagrams use the following constants:

CC_DET_SEQ
: A constant indicating the sequence in which the PSE performs connection check and detection.
Values:
: 0: Connection Check is followed by staggered detection ~~for a single-signature PD and parallel detection for a dual-signature PD.~~
: ~~1: Detection on a pairset is followed by~~ connection check and then detection on the other pairset ~~for a single-signature PD and both pairsets for a dual-signature PD~~.
: 2: Connection check and detection on both pairsets are performed within a single T_{det} window.
: 3: Connection check is followed by staggered detection.

33.2.4.9 Type 3 and Type 4 variables

~~alt_done_pri~~
: ~~A variable used to coordinate the main single-signature state diagram with the pseudo-independent dual-signature state diagram for the Primary Alternative.~~
: ~~Values:~~
: ~~FALSE: The pseudo-independent state diagram is not ready to return to global IDLE within the single-signature state diagram.~~
: ~~TRUE: The pseudo-independent state diagram is ready to return to global IDLE within the single-signature state diagram.~~

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~~alt_done_sec~~

~~A variable used to coordinate the main single-signature state diagram with the pseudo-independent dual-signature state diagram for the Secondary Alternative.~~

~~Values:~~

~~FALSE: The pseudo-independent state diagram is not ready to return to global IDLE within the single-signature state diagram.~~

~~TRUE: The pseudo-independent state diagram is ready to return to global IDLE within the single-signature state diagram.~~

alt_pri

A variable used to select which Alternative assumes the role of Primary in the state diagram.

Values:

a: Alternative A is assigned Primary, and Alternative B is assigned Secondary.

b: Alternative B is assigned Primary, and Alternative A is assigned Secondary.

alt_pri_pwrd

A variable that controls the circuitry that the PSE uses to power the PD over the Alternative that has been assigned as Primary.

Values:

FALSE: The PSE is not to apply power to the Primary Alternative.

TRUE: The PSE has detected, classified, and will power a PD on the Primary Alternative; or power is being forced on the Primary Alternative in TEST_MODE.

alt_sec_pwrd

A variable that controls the circuitry that the PSE uses to power the PD over the Alternative that has been assigned as Secondary.

Values:

FALSE: The PSE is not to apply power to the Secondary Alternative.

TRUE: The PSE has detected, classified, and will power a PD on the Secondary Alternative; or power is being forced on the Secondary Alternative in TEST_MODE.

class_num_events

A variable indicating the maximum number of classification events performed by the PSE. A variable that is set in an implementation-dependent manner.

Values:

0: PSE does not perform Physical Layer classification.

1: PSE performs Single-Event Physical Layer classification or Multiple-Event Physical Layer classification with a maximum of 1 class event.

2: PSE performs Multiple-Event Physical Layer classification with a maximum of 2 class events.

4: PSE performs Multiple-Event Physical Layer classification with a maximum of 4 class events.

5: PSE performs Multiple-Event Physical Layer classification with a maximum of 5 class events.

det_start_pri

A variable that indicates to the Secondary Alternative that the Primary Alternative is between START_DETECT and POWER_UP.

Values:

FALSE: The Primary Alternative is not between START_DETECT and POWER_UP.

TRUE: The Primary Alternative is between START_DETECT and POWER_UP.

det_start_sec

A variable that indicates to the Primary Alternative that the Secondary Alternative is between START_DETECT and POWER_UP.

Values:

FALSE: The Secondary Alternative is not between START_DETECT and POWER_UP.

TRUE: The Secondary Alternative is between START_DETECT and POWER_UP.

det_temp

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A temporary variable that indicates whether a 4-pair PSE has completed detection on only one alternative.

Values:

0: The PSE has not completed a detection on only one Alternative.

1: The PSE has completed a detection on only one Alternative.

dll_4PID

A variable that indicates whether the PSE and PD have negotiated 2-pair or 4-pair power.

Values:

0: 2-pair power negotiated.

1: 4-pair power negotiated.

error_condition

A variable indicating the status of implementation-specific fault conditions or optionally other system faults that prevent the PSE from meeting the specifications in Table 33–11 and that require the PSE not to source power. These error conditions are different from those monitored by the state diagrams in Figure 33–10e.

Values:

FALSE: No fault indication.

TRUE: A fault indication exists.

$I_{Inrush-2P}$

Output current per pairset during POWER_UP (see Table 33–11 and Figure 33–13).

$I_{Port-2P-pri}$

Total output current sourced by Primary Alternative (see 33.2.7.6).

$I_{Port-2P-sec}$

Total output current sourced by Secondary Alternative (see 33.2.7.6).

Editor's note (remove D1.6): Variables I_{Port}, $I_{Port-2P}$, and $I_{Port-2P-other}$ are not present in the current variable list. Section 33.2.7 depends on these. To be resolved.

mr_force_pwr_pri

This variable indicates if the Primary Alternative is to apply power to the link while in TEST_MODE (see Table 33–2). This variable is provided by a management interface that may be mapped to the PSE Control register Pair Control bit (11.6) or other equivalent function.

Values:

FALSE: The Primary Alternative is not powered.

TRUE: The Primary Alternative is powered.

mr_force_pwr_sec

This variable indicates if the Secondary Alternative is to apply power to the link while in TEST_MODE (see Table 33–2). This variable is provided by a management interface that may be mapped to the PSE Control register Pair Control bit (11.7) or other equivalent function.

Values:

FALSE: The Secondary Alternative is not powered.

TRUE: The Secondary Alternative is powered.

mr_mps_valid

The PSE monitors the Maintain Power Signature (MPS, see 33.2.9.1). This variable indicates the presence or absence of a valid MPS.

Values:

FALSE: MPS is absent.

TRUE: MPS is present.

mr_mps_valid_pri

The PSE monitors the Maintain Power Signature (MPS, see 33.2.9.1) on the Primary Alternative. This variable indicates the presence or absence of a valid MPS.

Values:

FALSE: MPS is absent.

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TRUE: MPS is present.

mr_mps_valid_sec

The PSE monitors the Maintain Power Signature (MPS, see 33.2.9.1) on the Secondary Alternative. This variable indicates the presence or absence of a valid MPS.

Values:

FALSE: MPS is absent.

TRUE: MPS is present.

mr_pse_alternative

This variable indicates which Pinout Alternative the PSE uses to apply power to the link (see Table 33–2). This variable is provided by a management interface that may be mapped to the PSE Control register Pair Control bits (11.3:2) or other equivalent function.

Values:

a: The PSE uses PSE pinout Alternative A.

b: The PSE uses PSE pinout Alternative B.

both: The PSE uses both Alternative A and Alternative B.

mr_pse_enable

A control variable that selects PSE operation and test functions. This variables is provided by a management interface that may be mapped to the PSE Control register PSE Enable bits (11.1:0), as described below, or other equivalent functions.

Values:

disable: All PSE functions disabled (behavior is as if there was no PSE functionality). This value corresponds to MDIO register bits 11.1:0 = ‘00’.

enable: Normal PSE operation. This value corresponds to MDIO register bits 11.1:0 = ‘01’.

force_power: Test mode selected that causes the PSE to apply power to the PI when there are no detected error conditions. This value corresponds to MDIO register bits 11.1:0 = ‘10’.

mr_pse_ss_mode

A variable that controls whether the PSE 2-pair or 4-pair powers a Class 0-4 ~~single-signature~~ PD.

0: ~~Single-signature~~ PD is 2-pair powered

1: ~~Single-signature~~ PD is 4-pair powered

option_detect_ ted

This variable indicates if detection can be performed by the PSE during the ted_timer interval.

Values:

FALSE: Do not perform detection during ted_timer interval.

TRUE: Perform detection during ted_timer interval.

option_vport_lim

This optional variable indicates if V_{PSE} is out of the operating range during normal operating state.

Values:

FALSE: V PSE is within the $V_{Port_PSE\text{-}2P}$ operating range as defined in Table 33–11.

TRUE: V PSE is outside of the $V_{Port_PSE\text{-}2P}$ operating range on at least one pairset as defined in Table 33–11.

pd_4pair_cand

This variable is used by the PSE to indicate that a connected PD is a candidate to receive power on both Modes. This variable is a function of the results of Detection, Connection Check, and 4PID.

Values:

FALSE: The PD is not a candidate to receive power on both Modes.

TRUE: The PD is a candidate to receive power on both Modes.

pd_dll_power_type

A control variable output by the PSE power control state diagram (Figure 33–27) that indicates the Type of PD as advertised through Data Link Layer classification.

Values:

1: PD is a Type 1 PD (default)

2: PD is a Type 2 PD

3: PD is a Type 3 PD

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4: PD is a Type 4 PD

Editor's Note: Mutual identification will require a variable pd_power_type similar to pd_dll_power_ type.

~~pism~~

~~A variable used by the single-signature state machine to kick off the pseudo-independent dual-signature state machines.~~

~~Values:~~

~~FALSE: Single-signature state machine has control of the Alternatives.~~

~~TRUE: Single-signature state machine has passed control of the Alternatives to the pseudo-independent dual-signature state machines.~~

power_not_available

Variable that is asserted in an implementation -de pendent manner when the PSE is no longer capable of sourcing sufficient power to support the attached PD. Sufficient power is defined by classification; see 33.2.6.

Values:

FALSE: PSE is capable to continue to source power to a PD.

TRUE: PSE is no longer capable of sourcing power to a PD.

power_not_available_pri

Variable that is asserted in an implementation-dependent manner when the PSE is no longer capable of sourcing sufficient power on the Primary Alternative to support the attached PD. Sufficient power is defined by classification; see 33.2.6.

Values:

FALSE: PSE is capable to continue to source power to a PD.

TRUE: PSE is no longer capable of sourcing power to a PD.

power_not_available_sec

Variable that is asserted in an implementation-dependent manner when the PSE is no longer capable of sourcing sufficient power on the Secondary Alternative to support the attached PD. Sufficient power is defined by classification; see 33.2.6.

Values:

FALSE: PSE is capable to continue to source power to a PD.

TRUE: PSE is no longer capable of sourcing power to a PD.

pse_avail_pwr

This variable indicates the highest power PD Class that could be supported. The value is determined in an implementation-specific manner.

Values:

1: Class 1
2: Class 2
3: Class 0 or 3
4: Class 4
5: Class 5
6: Class 6
7: Class 7
8: Class 8

pse_avail_pwr_pri

This variable indicates the highest power PD Class that could be supported on the Primary Alternative. The value is determined in an implementation-specific manner.

Values:

1: Class 1
2: Class 2
3: Class 0 or Class 3
4: Class 4
5: Class 5

pse_avail_pwr_sec

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This variable indicates the highest power PD Class that could be supported on the Secondary Alternative. The value is determined in an implementation-specific manner.

Values:

1: Class 1
2: Class 2
3: Class 0 or Class 3
4: Class 4
5: Class 5

pse_dll_capable

This variable indicates whether the PSE is capable of performing optional Data Link Layer classification. See 33.6 for a description of Data Link Layer functionality. This variable is provided by a management interface that may be mapped to the PSE Control register Data Link Layer Classification Capability bit (11.5), as described below, or other equivalent functions. A variable that is set in an implementation-dependent manner.

Values:

FALSE: The PSE's Data Link Layer classification capability is not enabled.
TRUE: The PSE's Data Link Layer classification capability is enabled.

pse_dll_enabled

A variable indicating whether the Data Link Layer classification mechanism is enabled. See 33.6.

Values:

FALSE: Data Link Layer classification is not enabled.
TRUE: Data Link Layer classification is enabled.

pse_ready

Variable that is asserted in an implementation-dependent manner to probe the link segment.

Values:

FALSE: PSE is not ready to probe the link segment.
TRUE: PSE is ready to probe the link segment.

NOTE—Care should be taken when negating this variable in a PSE performing detection using Alternative A after an invalid signature is detected due to the delay it introduces between detection attempts (see 33.2.4.1).

pse_reset

Controls the resetting of the PSE state diagram. Condition that is TRUE until such time as the power supply for the device that contains the PSE overall state diagrams has reached the operating region. It is also TRUE when implementation-specific reasons require reset of PSE functionality.

Values:

FALSE: Do not reset the PSE state diagram.
TRUE: Reset the PSE state diagram.

pwr_app_pri

A variable indicating that the PSE has begun steady state operation on the Primary Alternative by having asserted alt_pri_pwrd, completed the ramp up of voltage, is not in a current limiting mode, and is operating beyond the POWER_UP requirements of 33.2.7.5.

Values:

FALSE: The PSE is either not applying power or has begun applying power but is still in POWER_UP on the Primary Alternative.
TRUE: The PSE has begun steady state operation on the Primary Alternative.

pwr_app_sec

A variable indicating that the PSE has begun steady state operation on the Secondary Alternative by having asserted alt_sec_pwrd, completed the ramp up of voltage, is not in a current limiting mode, and is operating beyond the POWER_UP requirements of 33.2.7.5.

Values:

FALSE: The PSE is either not applying power or has begun applying power but is still in POWER_UP on the Secondary Alternative.
TRUE: The PSE has begun steady state operation on the Secondary Alternative.

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short_det_pri
: A variable indicating if the PSE output current has been in a short circuit condition on the Primary Alternative.
Values:
FALSE: The PSE has not detected a short circuit condition on the Primary Alternative.
TRUE: The PSE has detected a short circuit condition on the Primary Alternative.

short_det_sec
: A variable indicating if the PSE output current has been in a short circuit condition on the Secondary Alternative.
Values:
FALSE: The PSE has not detected a short circuit condition on the Secondary Alternative.
TRUE: The PSE has detected a short circuit condition on the Secondary Alternative.

temp_var
: A temporary variable used to store the value of the state variable mr_pd_class_detected.

PSEs shall meet at least one of the allowable variable definition permutations described in Table 33–3a.

Table 33–3a—Allowed PSE variable definition permutations

PSE Type	class_num_events
Type 4	1, 2, 4, 5
Type 3	1, 2, 4
Type 2	1, 2
Type 1	0, 1

PSEs shall issue no more Class events than the Class they are capable of supporting. For example, this would apply to a PSE that is oversubscribed and in power management mode or a PSE that has a hardware limitation.

~~*Editor's Note (remove prior to D2.0): Table 33-3a must be updated to take dual-signature into account. Reason: when connected to a DS PD, PSEs need to produce 3 events in order to verify Type.*~~

33.2.4.10 Type 3 and Type 4 timers

All timers operate in the manner described in 14.2.3.2 with the following addition: a timer is reset and stops counting upon entering a state where "stop x_timer" is asserted.

Editor's Note: Timers for Autoclass need to be added.

tcc_timer
: A timer used to monitor the duration of Connection Check.

tcc2det_timer
: A timer used to limit the time between Connection Check and Detection when CC_DET_SEQ = 0. See Table 33–3a.

tcle2_timer
: A timer used to limit the second classification event time in Multiple-Event classification; see T_{CLE2} in Table 33–10.

tcle3_timer

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A timer used to limit the third through fifth classification event time in Multiple-Event classification; see T_{CLE3} in Table 33–10.

tdbo_timer
A timer used to regulate backoff upon detection of an invalid signature; see T_{dbo} in Table 33–11.

tdet_timer
A timer used to limit an attempt to detect a PD; see T_{det} in Table 33–11.

tdet_timer_pri
A timer used to limit an attempt to detect a PD on the Primary Alternative; see T_{det} in Table 33–11.

tdet_timer_sec
A timer used to limit an attempt to detect a PD on the Secondary Alternative; see T_{det} in Table 33–11.

tdet2det_timer
A timer used to limit the time between the completion of a detection on one pairset and the beginning of a detection on the other. See Table 33–3a.

ted_timer
A timer used to regulate a subsequent attempt to power a PD after an error condition causes power removal; see T_{ed} in Table 33–11. The default state of this timer is ted_timer_done.

ted_timer_pri
A timer used to regulate a subsequent attempt to power a PD after an error condition causes power removal from the Primary Alternative; see T_{ed} in Table 33–11. The default state of this timer is ted_timer_pri_done.

ted_timer_sec
A timer used to regulate a subsequent attempt to power a PD after an error condition causes power removal from the Secondary Alternative; see T_{ed} in Table 33–11. The default state of this timer is ted_timer_sec_done.

tinrush_pri_timer
A timer used to monitor the duration of the inrush event on the Primary Alternative; see $T_{Inrush-2P}$ in Table 33–11.

tinrush_sec_time r
A timer used to monitor the duration of the inrush event on the Secondary Alternative; see $T_{Inrush-2P}$ in Table 33–11.

tlcf_timer
A timer used to limit the first classification event time in Multiple-Event classification; see T_{LCF} in Table 33–10.

tme1_timer
A timer used to limit mark event times for all but the last the first mark event time in during Multiple-Event classification; see T_{ME1} in Table 33–10.

tme2_timer
A timer used to limit the second final mark event time in Multiple-Event classification; see T_{ME2} in Table 33–10.

tmpdo_timer
A timer used to monitor the dropout of the MPS; see T_{MPDO} in Table 33–11.

tmpdo_timer_pri
A timer used to monitor the dropout of the MPS on the Primary Alternative; see T_{MPDO} in Table 33–11.

tmpdo_timer_sec
A timer used to monitor the dropout of the MPS on the Secondary Alternative; see T_{MPDO} in Table 33–11.

tpdc_timer
A timer used to limit the classification time; see T_{pdc} in Table 33–10.

tpon_timer

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A timer used to limit the time for power turn-on; see T_{pon} in Table 33–11.

tpon_timer_pri
A timer used to limit the time on the Primary Alternative for power turn-on; see T_{pon} in Table 33–11.

tpon_timer_sec
A timer used to limit the time on the Secondary Alternative for power turn-on; see T_{pon} in Table 33–11.

33.2.4.11 Type 3 and Type 4 functions

do_cxn_chk
This function initiates the Connection Check in as specified in 33.2.5.0a. This function returns the following variable:

sig_type: This variable indicates the Type of PD signature connected to the PI, with respect to 4-pair operation.
Values:
open_circ: The PSE has detected an open circuit on ~~both~~ pairsets.
single: The PSE has determined there is a ~~single-signature~~ PD ~~configuration~~ connected to ~~the~~ PI.
~~dual: The PSE has determined there is a dual-signature PD configuration connected to the PI.~~

do_classification
This function returns the following variables:

pd_cls_4PID: This variable indicates that 4PID has been established.
Values:
FALSE: PD is not a candidate for 4-pair power.
TRUE: PD is a candidate for 4-pair power.

pd_req_pwr: This variable indicates the power class requested by the PD. When a PD requests a higher class than a PSE can support, the PSE shall assign the PD Class 3, 4, or 6, whichever is the highest that it can support. See 33.2.6.
Values:
1: Class 1
2: Class 2
3: Class 0 or Class 3
4: Class 4
5: Class 5 (mr_pd_class_detected will have a value of 4 for the first two class events and a value of 0 for any subsequent class events.)
6: Class 6 (mr_pd_class_detected will have a value of 4 for the first two class events and a value of 1 for any subsequent class events.)
7: Class 7 (mr_pd_class_detected will have a value of 4 for the first two class events and a value of 2 for any subsequent class events.)
8: Class 8 (mr_pd_class_detected will have a value of 4 for the first two class events and a value of 3 for any subsequent class events.)

~~*Editor's Note: Dual-signature classification still needs to be taken into account here.*~~

mr_pd_class_detected: The PD classification signature seen during a classification event; see Table 33–7 and 33.2.6.
Values:
0: Class 0

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1: Class 1
2: Class 2
3: Class 3
4: Class 4
5: Class 5
6: Class 6
7: Class 7
8: Class 8

Editor's Note (remove D1.6): Valid classification signatures are 0 through 4, 5 and up don't exist.

do_classification_ pri

This function returns the following variables for the Primary Alternative:

pd_cls_4PID_pri: This variable indicates that 4PID has been established.
Values:
FALSE: PD is not a candidate for 4-pair power.
TRUE: PD is a candidate for 4-pair power.

pd_req_pwr_pri: This variable indicates the power class requested by the PD. When a PD requests a higher class than a PSE can support, the PSE shall assign the PD Class 3, 4, or 6, whichever is the highest that it can support. See 33.2.6.
Values:
1: Class 1
2: Class 2
3: Class 0 or Class 3
4: Class 4
5: Class 5 (mr_pd_class_detected_pri will have a value of 4 for the first two class events and a value of 0 for any subsequent class events.)

~~*Editor's Note: Dual-signature classification still needs to be taken into account here.*~~

mr_pd_class_detected_ pri: The PD classification signature seen during a classification event; see Table 33–7 and 33.2.6.
Values:
0: Class 0
1: Class 1
2: Class 2
3: Class 3
4: Class 4

do_classification_sec

This function returns the following variables for the Secondary Alternative:

pd_cls_4PID_sec: This variable indicates that 4PID has been established.
Values:
FALSE: PD is not a candidate for 4-pair power.
TRUE: PD is a candidate for 4-pair power.

pd_req_pwr_sec: This variable indicates the power class requested by the PD. When a PD requests a higher class than a PSE can support, the PSE shall assign the PD Class 3, 4, or 6, whichever is the highest that it can support. See 33.2.6.
Values:
0: Class 1

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1: Class 2
2: Class 0 or Class 3
3: Class 4
4: Class 5 (mr_pd_class_dete cte d_sec will have a value of 4 for the first two class events and a value of 0 for any subsequent class events.)

~~*Editor's Note: DS PD classification must be taken into account here.*~~

mr_pd_class_detected_sec: The PD classification signature seen during a classification event; see Table 33–7 and 33.2.6.

Values:
0: Class 0
1: Class 1
2: Class 2
3: Class 3
4: Class 4

do_detect_pri

This function returns the following variables (see 33.2.5):

sig_pri: This variable indicates the presence or absence of a valid PD detection signature on the Primary Alternative.

Values:
open_circuit: The PSE has detected an open circuit.
valid: The PSE has detected a PD requesting power.
invalid: Neither open circuit nor valid PD detection signature has been found.

mr_valid_sig_pri: This variable indicates that the PSE has detected a valid signature.

Values:
FALSE: No valid signature detected.
TRUE: Valid signature detected.

do_detect_sec

This function returns the following variables (see 33.2.5):

sig_sec: This variable indicates the presence or absence of a valid PD detection signature on the Secondary Alternative.

Values:
open_circuit: The PSE has detected an open circuit.
valid: The PSE has detected a PD requesting power.
invalid: Neither open circuit nor valid PD detection signature has been found.

mr_valid_sig_sec: This variable indicates that the PSE has detected a valid signature.

Values:
FALSE: No valid signature detected.
TRUE: Valid signature detected.

do_mark

This function produces the classification mark event voltage. This function does not return any variables.

set_parameter_type

This function is used by a PSE to evaluate the Type of PD connected to the link based on Physical Layer classification or Data Link Layer classification results. The PSE's PI electrical requirements

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defined in Table 33–11 are set to values corresponding to either a Type 1, or Type 2, Type 3, or Type 4 PSE. This function returns the following variable:

parameter_type: A variable used by a PSE to pick between Type 1, and Type 2, Type 3 and Type 4 PI electrical requirement parameter values defined in Table 33–11.
Values:
1: Type 1 PSE parameter values (default)
2: Type 2 PSE parameter values
3: Type 3 PSE parameter values
4: Type 4 PSE parameter values

When a Type 2 PSE powers a Type 2, Type 3 or Type 4 PD, the PSE may choose to assign a value of '1' to parameter_type if mutual identification is not complete (see 33.2.6) and shall assign a value of '2' to parameter_type if mutual identification is complete.

Editor's Note: This paragraph requires further study. => This paragraph is a Type 2 requirement and does not belong here.

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33.2.4.12 Type 3 and Type 4 state diagrams

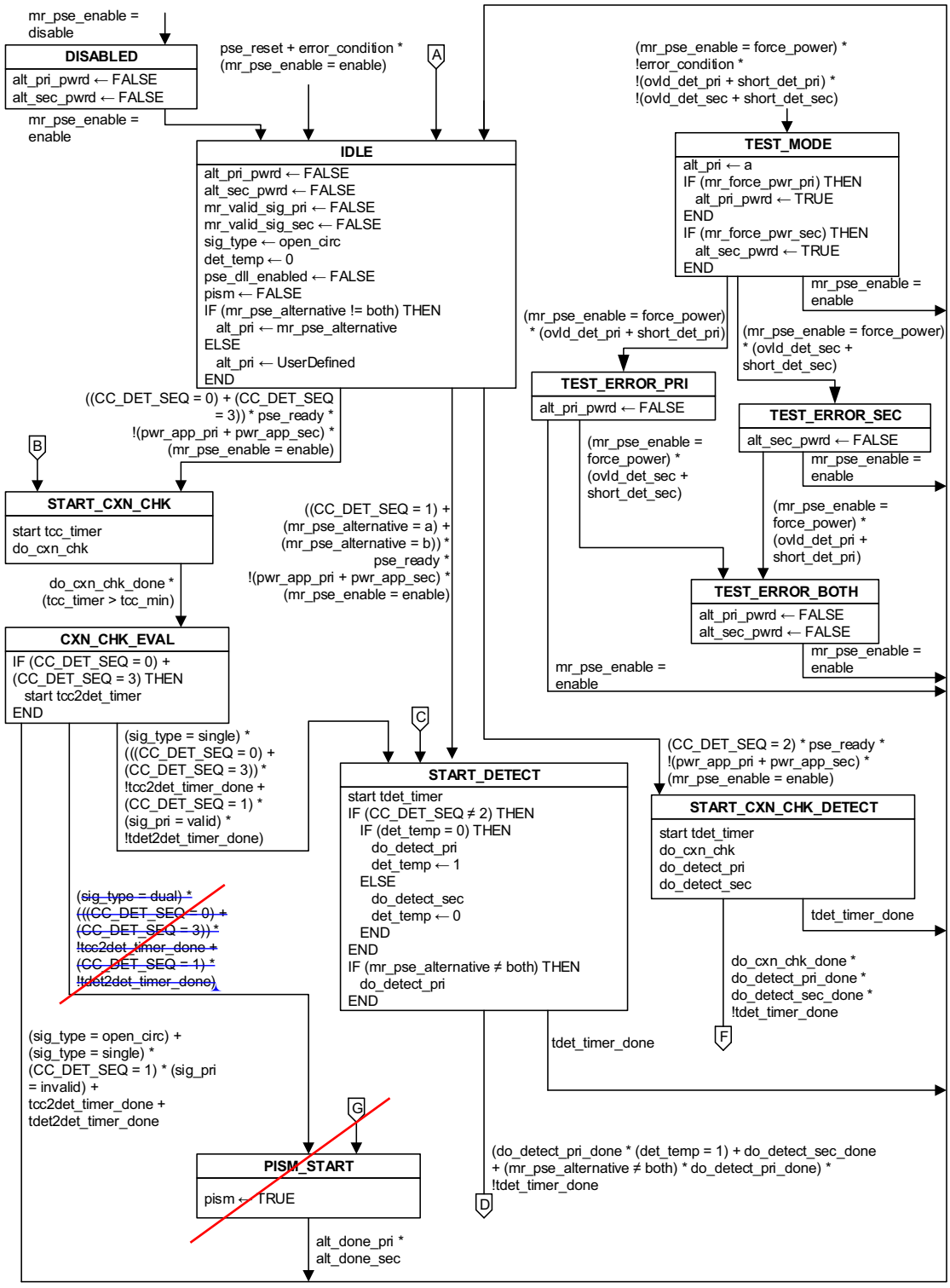

Figure 33–10a—Type 3 and Type 4 top level PSE state diagram

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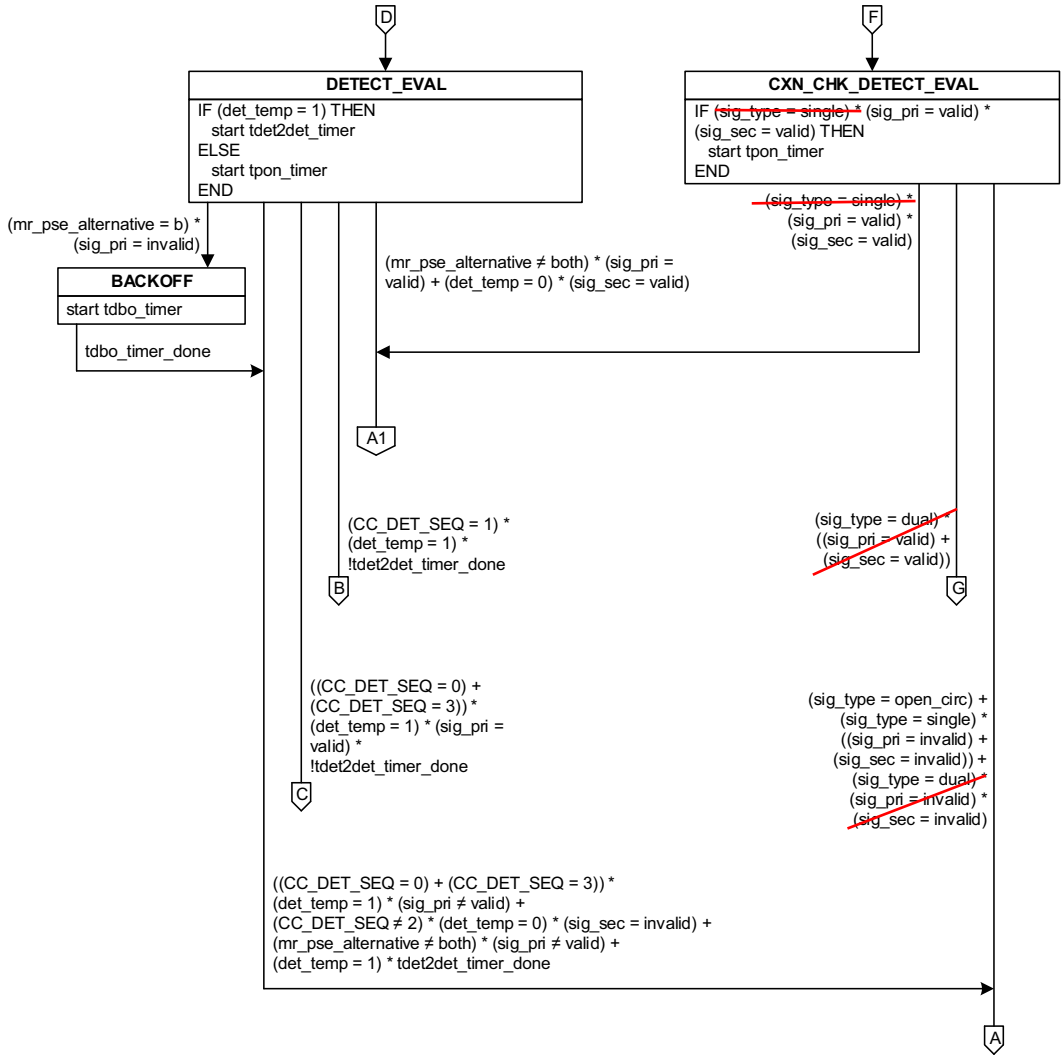

Figure 33–10a—Type 3 and Type 4 top level PSE state diagram (continued)

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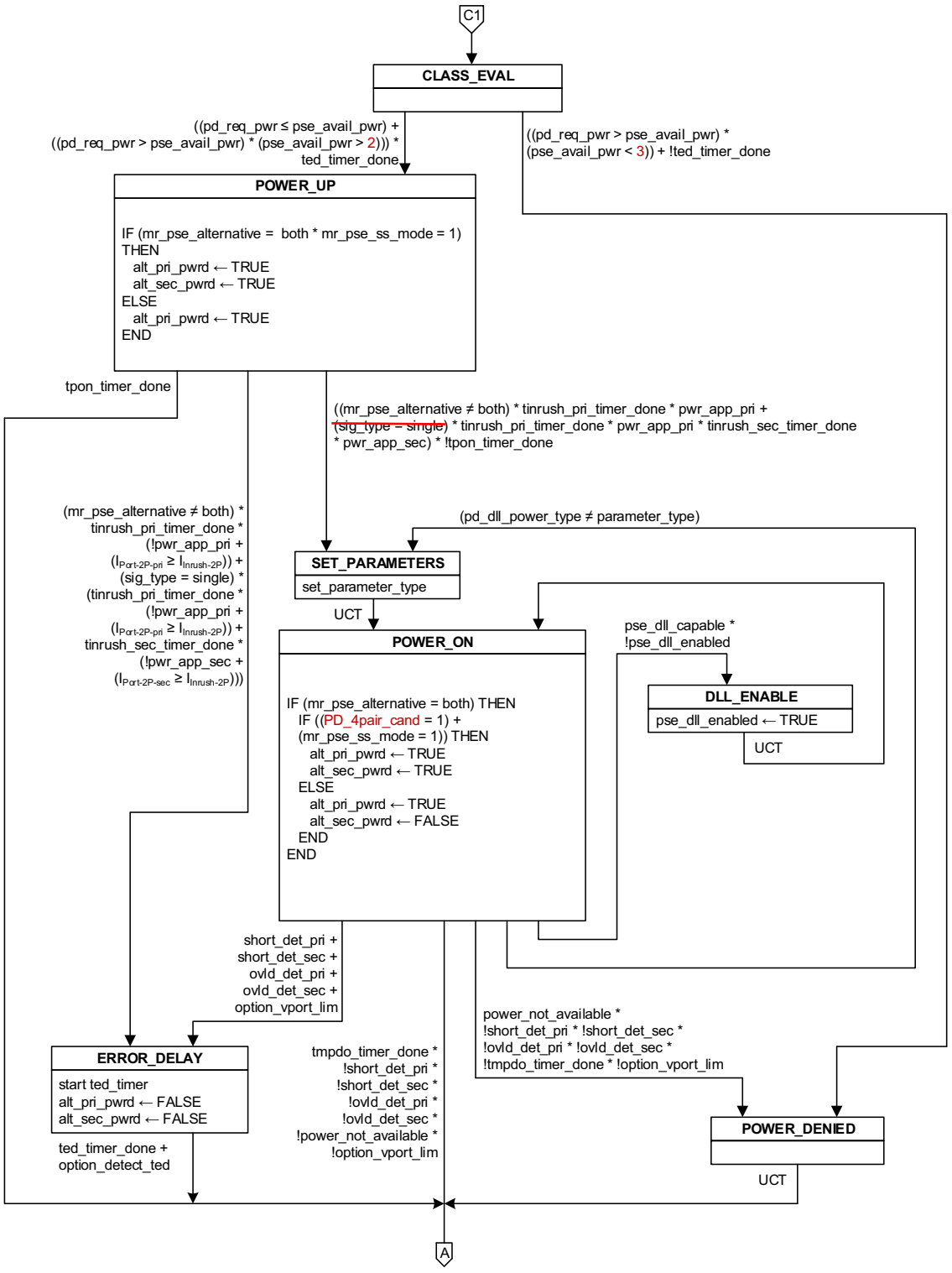

Figure 33–10a—Type 3 and Type 4 top level PSE state diagram (continued)

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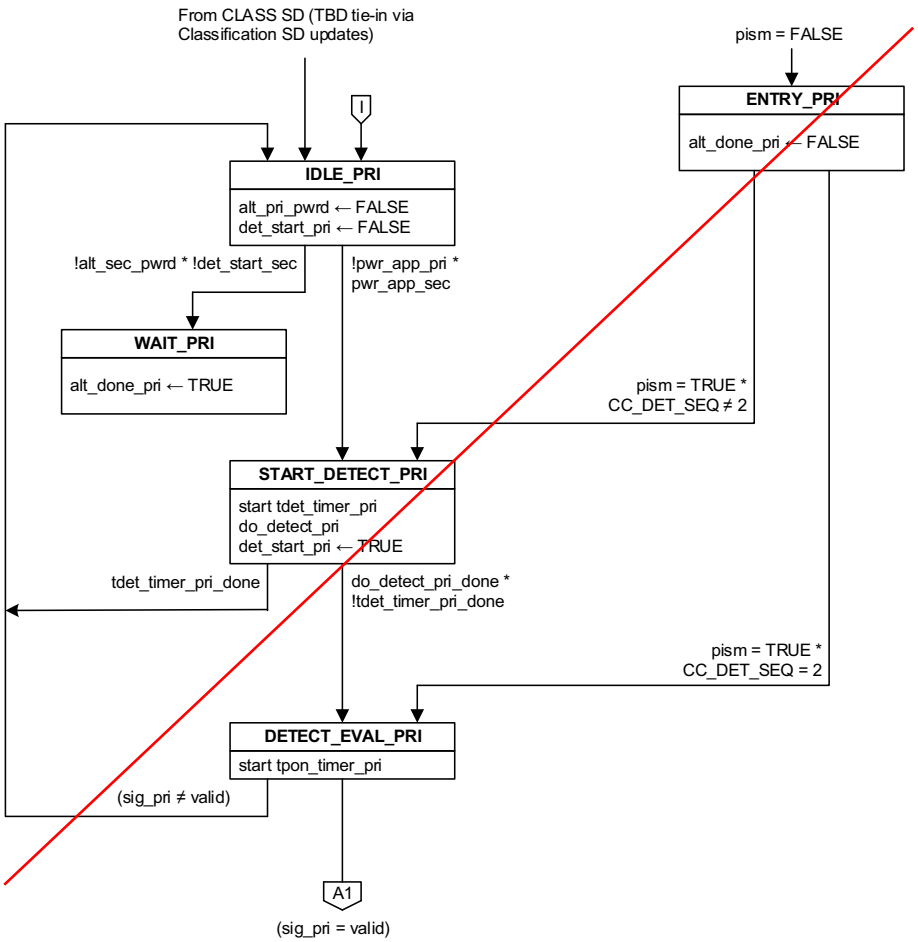

Figure 33–10b—Type 3 and Type 4 Alternative B dual-signature pseudo-independent PSE state diagram

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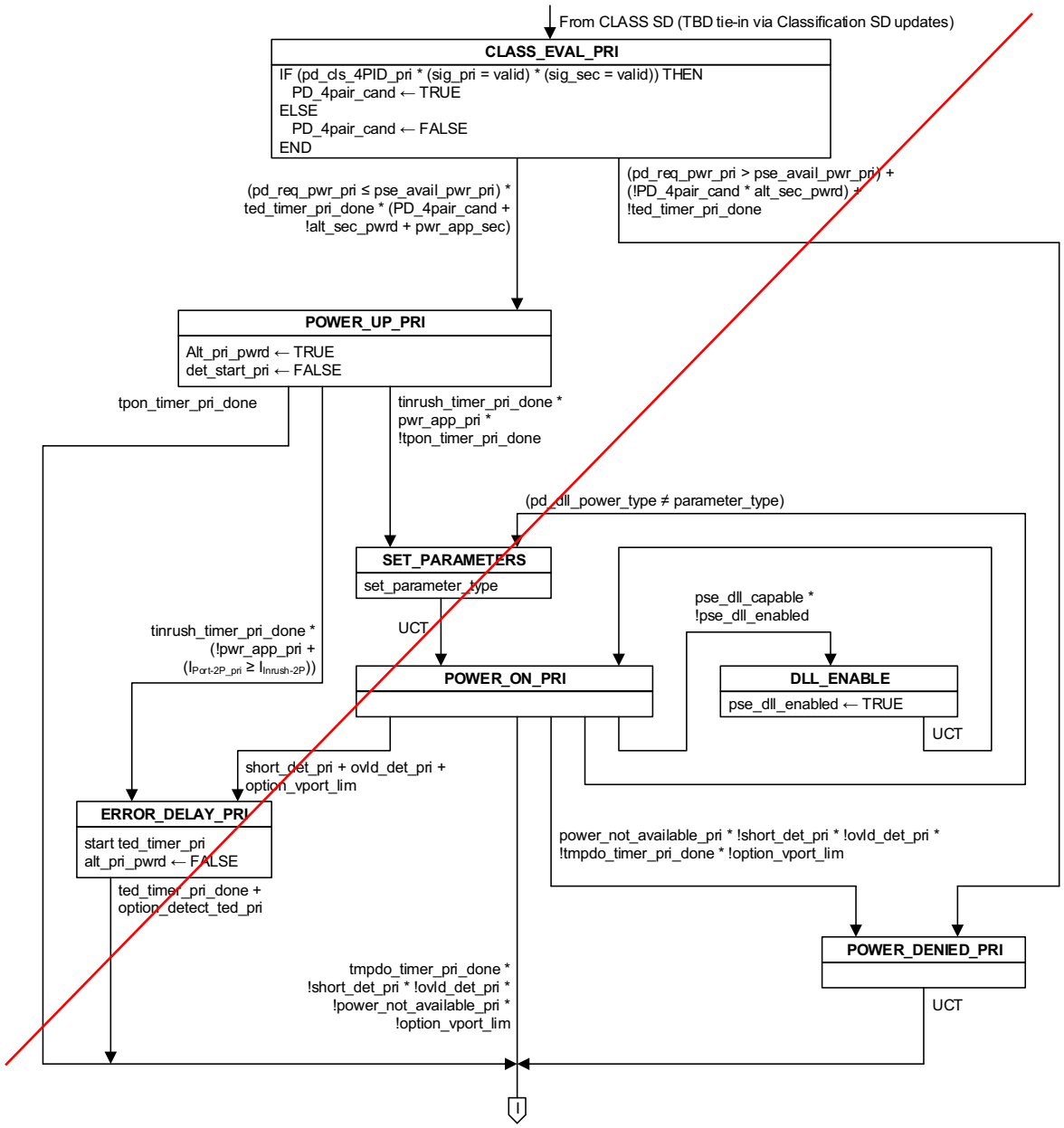

Figure 33–10b—Type 3 and Type 4 Alternative A dual-signature pseudo-independent PSE state diagram (continued)

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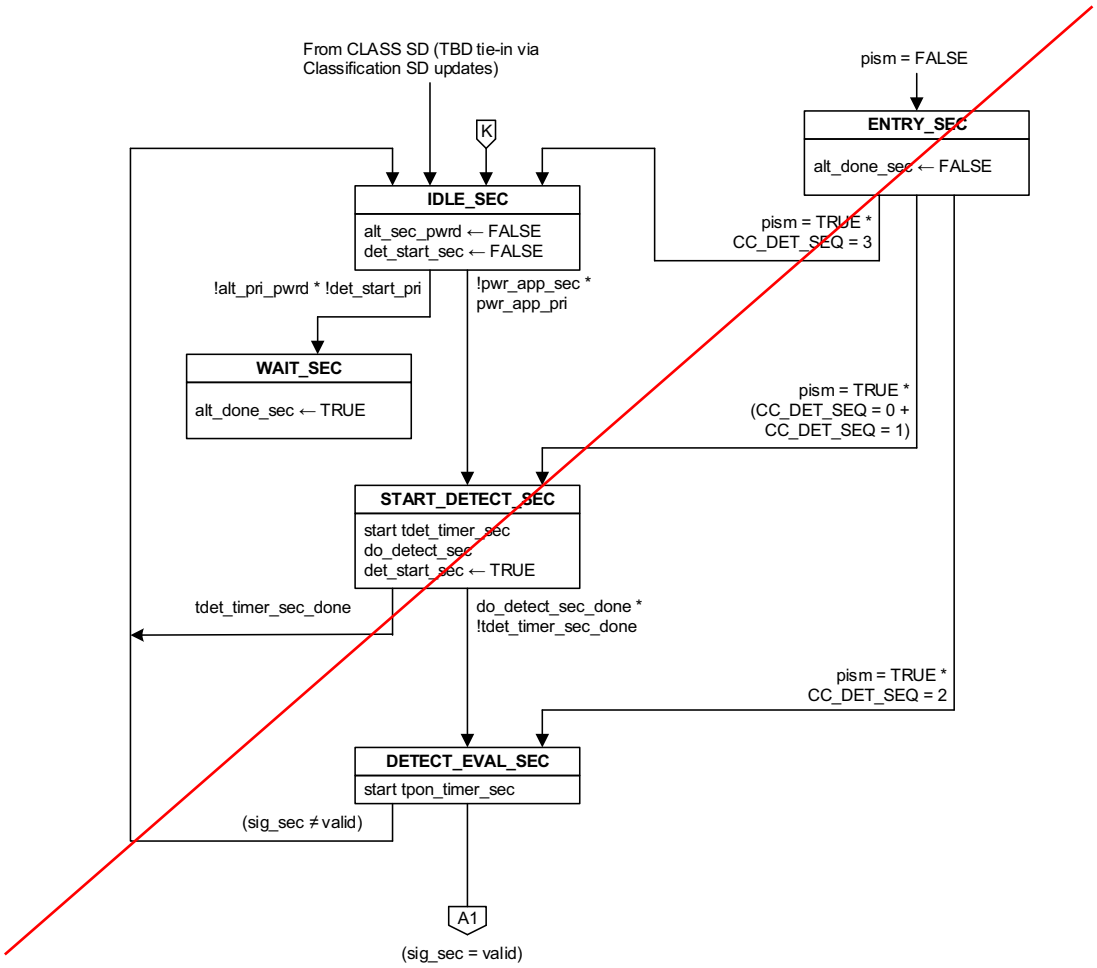

Figure 33–10c—Type 3 and Type 4 Alternative B dual-signature pseudo-independent PSE state diagram

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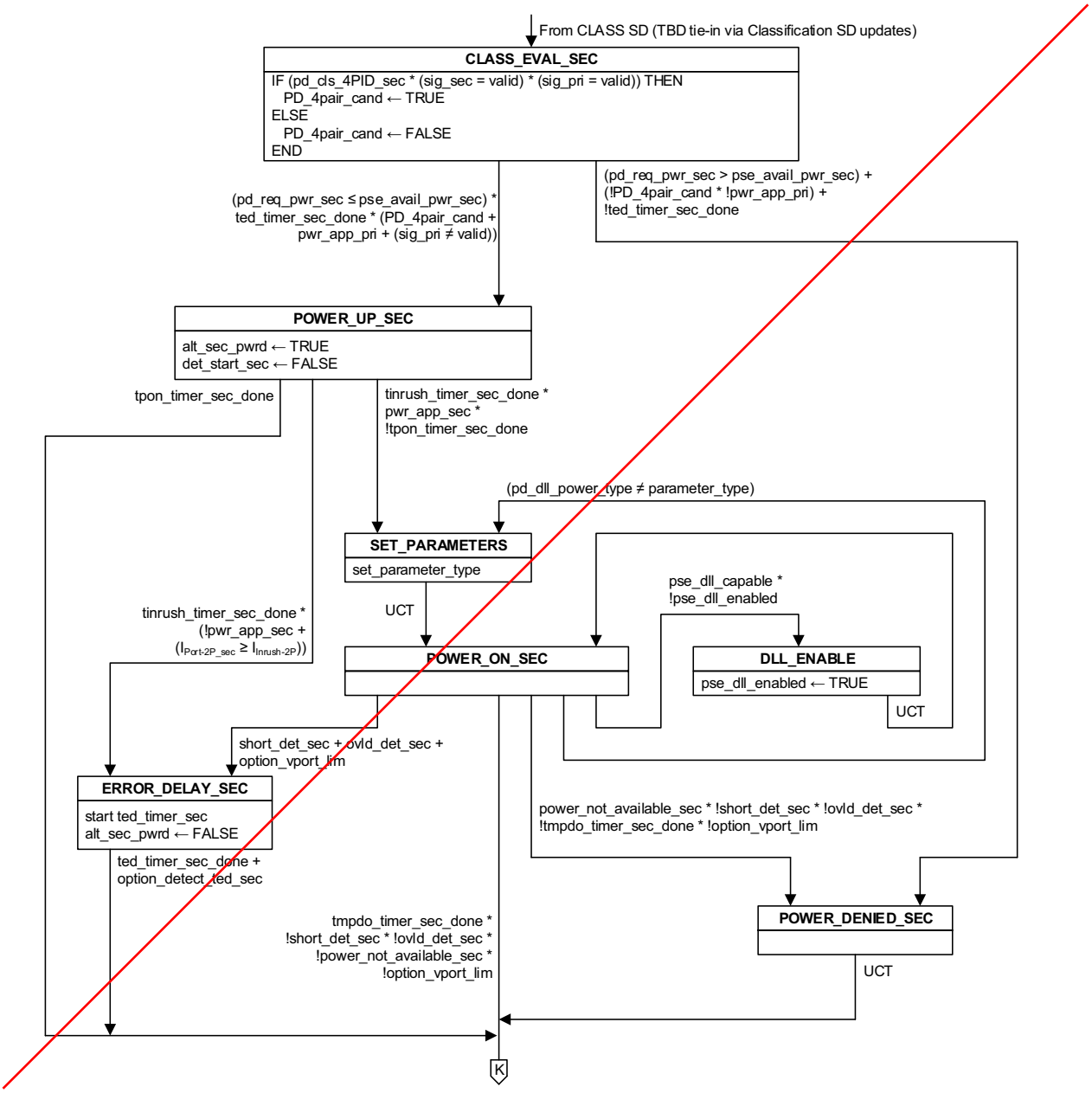

Figure 33–10c—Type 3 and Type 4 Alternative B dual-signature pseudo-independent PSE state diagram (continued)

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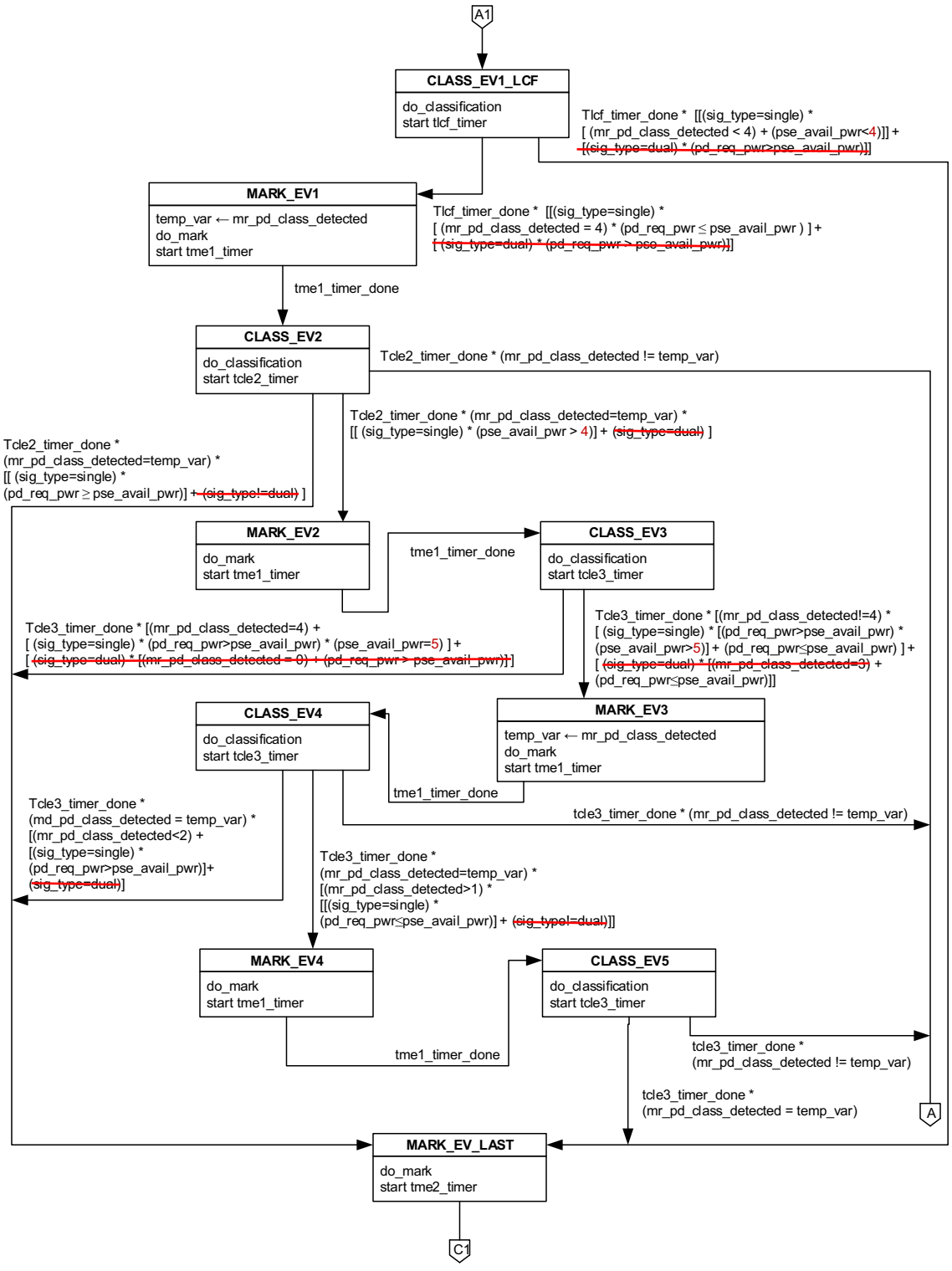

Figure 33–10d—Type 3 and Type 4 PSE classification state diagram

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Editor's Note: Classification section of state diagram to be updated with determination of variable PD_4pair_cand.

Editor's Note: The state diagram for Type 3 and Type 4 PSEs needs further study and participants are encouraged to provide presentations to address this need. Autoclass needs to be added to state machine. Diagram needs to be updated to reflect new exits from CLASS_EV3.

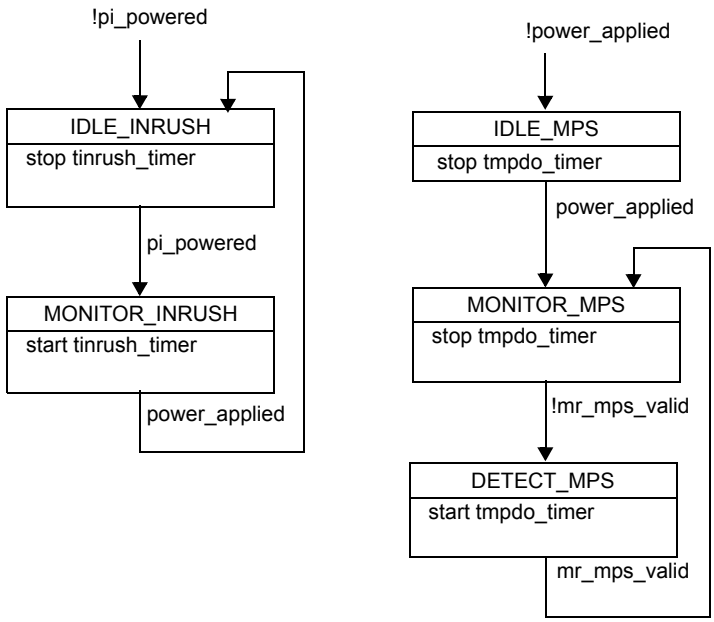

Figure 33–10e—Type 3 and Type 4 PSE monitor inrush and monitor MPS state diagrams

~~*Editor's Note: The State diagram shown in figure 33-9(TBD) needs to incorporate the 4PID requirements that are also covered in section 33.2.5.6. The state diagram for Type 3 and Type 4 does not address dual signature. Preferably this goes into a separate diagram to keep complexity manageable.*~~

Editor's Note: Faults on only one pairset need to be considered for the State Diagram.

Editor's Note: RED in the state diagram means changes made due to comments that make it deviate from

33.2.5 PSE detection of PDs

Change the text in section 33.2.5 as follows:

In any operational state, the PSE shall not apply operating power to ~~the PI~~ a pairset until the PSE has successfully detected a valid signature over that pairset, except as specified in 33.2.7.1. ~~PD requesting power~~

The PSE probes the link section in order to detect a valid PD detection signature. The PSE PI is connected to a PD through a link section ~~segment~~. In the following subclauses, the link is not called out to preserve clarity.

The PSE is not required to continuously probe to detect a PD signature. The period of time when a PSE is not attempting to detect a PD signature is implementation dependent. Also, a PSE may successfully detect a PD but then opt not to power the detected PD.

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~~The PSE shall turn on power only on the same pairs as those used for detection.~~

Insert new section 33.2.5.0a after section 33.2.5 as follows:

33.2.5.0a Connection check requirements

Type 3 and Type 4 PSEs that will deliver power on both pairsets shall complete a connection check prior to the classification of a PD as specified in 33.2.6. During connection check, the PSE shall determine if both pairsets are connected to a ~~single-signature~~ PD ~~or if the pairsets are connected to a dual-signature PD~~.

The exact method of the connection check is not specified. During connection check the PSE shall meet the specifications for open circuit voltage and short circuit current in Table 33–4. In addition, only tests that result in a voltage at the PSE PI that is below V_{valid}(max) as specified in Table 33–4 shall be used to determine whether a ~~single-signature~~ PD ~~or dual-signature PD~~ is attached to ~~the two~~ pairsets.

The specification of T_{cc2det}, defined in Table 33–3a, applies to the time between the end of connection check and the beginning of detection on at least one pairset. If the connection check takes place after the beginning of detection, this specification does not apply.

The specification of $T_{det2det}$, defined in Table 33–3a, applies to the time between the end of detection on the first pairset to the beginning of detection on the other pairset when connected to a ~~single-signature~~ PD.

Table 33–3b—Connection check timing requirements

Item	Parameter	Symbol	Unit	Min	Max	Additional Information
1	Connection check to detection time	T_{cc2det}	s		0.400	Applies only when connection check is performed before the start of detection.
2	Detection to detection time	$T_{det2det}$	s		0.400	~~Applies only when connected to a single-signature PD (TBD).~~
3	Connection check timing	T_{cc}	s	0.2		

The connection check is rerun before applying power if power up fails to meet the timing requirements in both Table 33–3a and 33.2.7.13 or power is absent on both pairsets simultaneously or if the state machine reaches the IDLE state.

If the voltage on either pairset rises above V_{valid} max, (defined in Table 33–4) during connection check, the PSE shall reset the PD by bringing the voltage at the PI below V_{off} max, defined in Table 33–11 before performing classification.

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Editor's Note: An informative annex should be considered. Test setup/compliance testing needs to be defined.

33.2.5.1 PSE detection validation circuit

The PSE shall detect the PD by probing via the PSE PI. The PSE shall present a non-valid PD detection signature as defined in Table 33–15 when probed in either polarity by another PSE. An illustrative embodiment of a detection circuit is shown in Figure 33–11.

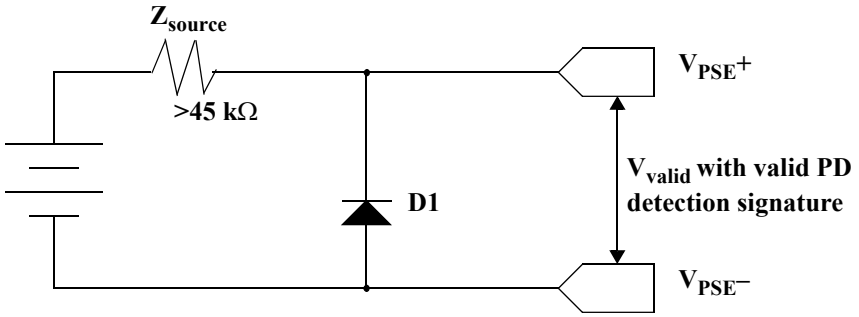

Figure 33–11—PSE detection source

A functional equivalent of the detection circuit that has no source impedance limitation but restricts the PSE detection circuit to the first quadrant is shown in Figure 33–12.

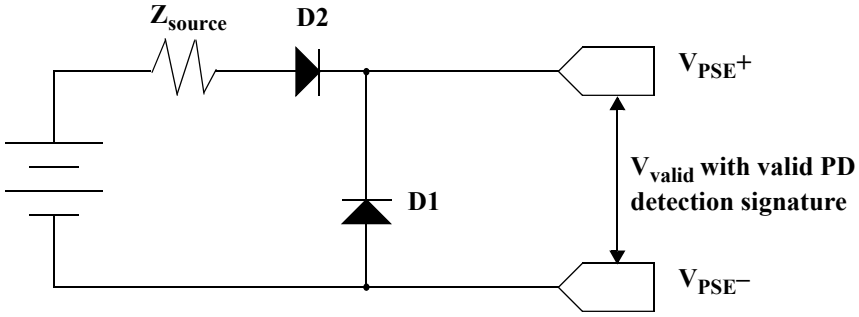

Figure 33–12—Alternative PSE detection source

In Figure 33–11 and Figure 33–12, the diode D1 presents a non-valid PD detection signature for a reversed voltage PSE to PSE connection.

The open circuit voltage and short circuit current shall meet the specifications in Table 33–4. The PSE shall not be damaged by up to 5 mA backdriven current over the range of V_{oc} as specified in Table 33–4. Output capacitance shall be as specified in Table 33–11.

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Change Table 33-4 as follows:

Table 33–4—PSE PI per pairset detection state electrical requirements

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Open circuit voltage	V_{oc}	V		30.0	In detection state ~~only~~ or connection check state
2	Short circuit current	I_{sc}	A		0.005	In detection state ~~only~~ or connection check state
3	Valid test voltage	V_{valid}	V	2.80	10.0	—
4	Voltage difference between test points	ΔV_{test}	V	1.00		—
5	Slew rate	V_{slew}	V/µs		0.100	—

33.2.5.2 Detection probe requirements

The detection voltage at the PSE PI shall be within the V_{valid} voltage range (as specified in Table 33–4) with a valid PD detection signature connected (as specified in Table 33–14).

In evaluating the presence of a valid PD, the PSE shall make at least two measurements with V_{PSE} values that create at least a ΔV_{test} difference as specified in Table 33–4. ~~An effective resistance is calculated from two voltage/current measurements made during the detection process~~An effective resistance is calculated from two or more measurements made during the detection process.

The resistance is calculated with Equation (33–2):

$$R = \left\{ \frac{(V_2 - V_1)}{(I_2 - I_1)} \right\}_{\Omega} \quad (33–2)$$

where

V_1 and V_2 are the first and second voltage measurements made at the PSE PI, respectively

I_1 and I_2 are the first and second current measurements made at the PSE PI, respectively

R is the effective resistance

Attached PI capacitance may be determined using these measurements and the port RC time-constant charging characteristics.

NOTE—Settling time before voltage or current measurement: the voltage or current measurement should be taken after V_{PSE} has settled to within 1 % of its steady state condition with a valid PD detection signature connected (as specified in Table 33–14).

The PSE shall control the slew rate of the probing detection voltage when switching between detection voltages to be less than V_{slew} as specified in Table 33–4.

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33.2.5.3 Detection criteria

Change text in section 33.2.5.3 as follows:

A pairset with all of the characteristics specified in Table 33–5 shall be accepted as a valid PD detection signature by a PSE. ~~PSE shall accept as a valid signature a link section with both of the following characteristics: between the powering pairs with an offset voltage up to V_{os} max and an offset current up to I_{os} max, as specified in Table 33–5:~~

~~a) Signature resistance R_{good}, and~~
~~b) Parallel signature capacitance C_{good}.~~

Change Table 33-5 as follows:

Table 33–5—Valid PD detection signature electrical characteristics

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Accept signature resistance	R_{good}	kΩ	19.0	26.5	—
2	Accept signature capacitance	C_{good}	µF		0.150	—
3	Signature offset voltage ~~tolerance~~	V_{os}	V	0	2.00	—
4	Signature offset current ~~tolerance~~	I_{os}	µA	0	12.0	—

CAUTION

In a multiport system, the implementer should maintain DC isolation through the termination circuitry to eliminate cross-port leakage currents.

33.2.5.4 Rejection criteria

Change first paragraph of 33.2.5.4 as follows:

The PSE shall reject a pairset within a link section~~s~~ as having an invalid signature, when the pairset ~~those link sections~~ exhibit~~s~~ any of the following characteristics ~~between the powering pairs,~~ as specified in Table 33–6:

a) Resistance less than or equal to R_{bad} min, or
b) Resistance greater than or equal to R_{bad} max, or
c) Capacitance greater than or equal to C_{bad} min.

A PSE may accept or reject a signature resistance in the band between R_{good} min and R_{bad} min, and in the band between R_{good} max and R_{bad} max. A PSE may accept or reject a parallel signature capacitance in the band between C_{good} max and C_{bad} min.

In instances where the resistance and capacitance meet the detection criteria, but one or both of the offset~~s~~ ~~tolerances~~ are exceeded, the detection behavior of the PSE is undefined.

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Table 33–6—Invalid PD detection signature electrical characteristics

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Reject signature resistance	R_{bad}	kΩ	15.0	33.0	—
2	Reject signature capacitance	C_{bad}	µF	10.0		—
3	Open circuit resistance	R_{open}	MΩ	0.500		—

33.2.5.5 Open circuit criteria

If a PSE that is performing detection using Alternative B (see 33.2.3) determines that the impedance at the PI is greater than R_{open} as defined in Table 33–6, it may optionally consider the link to be open circuit and omit the tdbo_timer interval.

Insert new section 33.2.5.6 after section 33.2.5.5 as follows:

33.2.5.6 4PID requirements

Type 3 and Type 4 PSEs shall determine whether an attached PD with Classes 0 to 4 is a candidate to receive power on both pairsets prior to applying power to the second pairset. This determination is referred to as 4PID. 4PID shall be initially (TBD) determined as a logical function of the detection state of both pairsets, the result of connection check as described in 33.2.5.0aa, mutual identification, and the results of other system information. It shall be stored in the variable PD_4pair_cand, defined in 33.2.4.4.

33.2.6 PSE classification of PDs and mutual identification

Change text of Section 33.2.6 as follows:

The ability for the PSE to query the PD in order to determine the power requirements of that PD is called classification. The interrogation and power classification function is intended to establish mutual identification and is intended for use with advanced features such as power management.

Mutual identification is the mechanism that allows a Type 2, Type 3, or Type 4 PD to differentiate between Type 1, ~~PSEs from~~ Type 2, Type 3, and Type 4 PSEs. Additionally, mutual identification allows Type 2, Type 3 or Type 4 PSEs to differentiate between Type 1, ~~and~~ Type 2, Type 3, and Type 4 PDs. PDs or PSEs that do not implement classification will not be able to complete mutual identification and can only perform as Type 1 devices.

There are two forms of classification: Physical Layer classification and Data Link Layer (DLL) classification ~~(DLL)~~.

~~Physical Layer classification occurs before a PSE supplies power to a PD when the PSE asserts a voltage onto the PI and the PD responds with a current representing a limited number of power classifications.~~ Physical Layer classification occurs before a PSE supplies power to a PD when the PSE asserts a voltage onto one or both pairsets and the PD responds to each class event with a current representing one of a limited number of classification signatures. Based on the response of the PD, the minimum power level at the output of the PSE is P_{Class} as shown in Equation (33–3). P_{Class} applies to the total PD power. Physical Layer classification encompasses two methods, known as ~~1-Event~~ Single-Event Physical Layer classification (see 33.2.6.1) and ~~2~~ Multiple-Event Physical Layer classification (see 33.2.6.2).

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The PSE shall provide V_{Class} with a current limitation of I_{Class_LIM}, as defined in Table 33–10 only for a pairset with a valid detection signature. Polarity shall be the same as defined for V_{Port_PSE-2P} in 33.2.3 and timing specifications shall be as defined in Table 33–10.

The minimum power output by the PSE for a particular PD ~~class~~ Class is defined by Equation (33–3). ~~This equation applies to 2-pair operation, and 4-pair operation when connected to a single-signature PD, or connected to a dual-signature PD that advertised the same class signature on both pairsets.~~ Alternatively, PSE implementations may use $V_{PSE} = V_{Port_PSE-2P}$ min and $R_{Chan} = R_{Ch}$ ~~max~~ when powering using a single pairset, or $R_{Chan} = R_{Ch}/2$ when powering using two pairsets ~~and~~ to arrive at over-margined values as shown in Table 33–7.

$$P_{Class} = \left\{ V_{PSE} \times \left(\frac{V_{PSE} - \sqrt{V_{PSE}^2 - 4 \times R_{Chan} \times \cancel{n \times} P_{Class_PD}}}{2 \times R_{Chan}} \right) \right\}_W \quad (33\text{–}3)$$

where

V_{PSE} is the voltage at the PSE PI as defined in 1.4.423
R_{Chan} is the channel DC ~~pair~~ loop resistance
P_{Class_PD} is the PD's power classification (see ~~Table 33-18~~ Table 33–16a)
~~n~~ ~~n=2 for Type 3 or Type 4 PSEs when connected to a dual-signature PD. n=1 for all other cases.~~

Add the following at the end of 33.2.6:

The minimum output power on a pairset for Type 3 and Type 4 PSEs that apply 4-pair power to a dual-signature PD which requests a different class signature on each pairset is defined by Equation 33-3a.

$$P_{Class\text{-}2P} = \left\{ V_{PSE} \times \left(\frac{V_{PSE} - \sqrt{V_{PSE}^2 - 4 \times R_{Chan} \times P_{Class_PD}}}{2 \times R_{Chan}} \right) \right\}_W \quad (33\text{–}3a)$$

where

V_{PSE} is the voltage at the PSE PI as defined in 1.4.423
R_{Chan} is the channel DC loop resistance
P_{Class_PD} is the PD's power classification (see Table 33–16a)

If the PD connected to the PSE performs Autoclass (see 33.2.6.3, 33.3.5.3, and Annex 33C), the PSE may set its minimum power output based on $P_{Autoclass}$, the power drawn during Autoclass measurement window, increased by at least the margin P_{ac_margin} calculated from the measured power by Equation (33–3b), in order to account for potential increase in channel resistance due to temperature increase, with a maximum value defined in Table 33–7 of the corresponding PD Class and a minimum of 4.0 Watts. PSEs that have additional information about the actual channel DC resistance or temperature conditions may choose to use a lower Autoclass margin than that defined by Equation (33–3b).

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Editor's Note: Section 33.2.6 needs references to Tables 33-7 through 33-7b. Readers are encouraged to suggest text.

Replace Table 33-7 as follows:

Table 33–7—Physical Layer power classifications ~~for single-signature PDs~~ (P_{Class})

PD Requested Class	Number of PSE Classification Events	Assigned Class	Minimum supported power levels at output of PSE (P_{Class})[1]
0	1	0	15.4 W
4	1	0	15.4 W[2]
1	1	1	4.00 W
2	1	2	7.00 W
3-8	1	3	15.4 W
4-8	2 or 3	4	30.0 W
5	4	5	45.0 W
6-8	4	6	60.0 W
7	5	7	75.0 W
8	5	8	90.0 W
NOTE—Data Link Layer classification takes precedence over Physical Layer classification.			

[1]This is the minimum required power at the PSE PI calculated using minimum $V_{Port_PSE\text{-}2P}$ and maximum R_{chan}. Use Equation (33–3) for other values of $V_{Port_PSE\text{-}2P}$ and R_{chan}. For maximum power available to PDs, see Table 33–18.
[2]Only applies to Type 1 and Type 2 PSEs.

Insert Table 33-7a and Table 33-7b after Table 33-7 as follows:

Table 33–7a—Physical Layer power classification for dual-signature PDs (P_{Class})

PD Requested Class Alt A	PD Requested Class Alt B	Number of PSE Classification Events on Alt A	Number of PSE Classification Events on Alt B	Assigned Class	Minimum supported power levels at output of PSE (P_{Class})
1	1	3	3	2	7.00 W
2	2	3	3	3	15.4 W
3	3	3	3	4	30.0 W
4	4	3	3	6	60.0 W
5	5	3	3	6	60.0 W
5	5	4	4	8	90.0 W

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Table 33–7b—Physical Layer power classification for dual-signature PDs ($P_{Class-2P}$)

PD Requested Class	Number of PSE Classification Events	Minimum supported power levels at output of PSE ($P_{Class-2P}$)
1	3	4.00 W
2	3	7.00 W
3	3	15.4 W
4-5	3	30.0 W
5	4	45.0 W

Editor's note (remove for D1.6): I added "PD" and "PSE" as in Tables 33-7 and 33-7a even though there was no comment.

Change the text in 33.2.6 as follows:

With Data Link Layer classification, the PSE and PD communicate using the Data Link Layer Protocol (see 33.6) after the data link is established. The Data Link Layer classification has finer power resolution and the ability for the PSE and PD to participate in dynamic power allocation wherein allocated power to the PD may change one or more times during PD operation. Data Link Layer classification takes precedence over Physical Layer classification. The Physical Layer classification of the PD is the maximum power that the PD draws across all output voltages and operational modes.

A PSE shall meet one of the allowable classification configurations ~~permutations~~ listed in Table 33–8.

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Replace Table 33-8 with the table shown below:

Table 33–8—PSE classification configurations

Type 1 PSE		
Physical Layer	**No DLL**	**DLL**
Multiple-Event	Invalid	Invalid
Single-Event	Valid	Valid
None	Valid	Valid
Type 2 PSE		
Physical Layer	**No DLL**	**DLL**
Multiple-Event	Valid	Valid
Single-Event	Invalid	Valid
None	Invalid	Invalid
Type 3, Type 4 PSE		
Physical Layer	**No DLL**	**DLL**
Multiple-Event	Valid	Valid
Single-Event	Invalid	Invalid
None	Invalid	Invalid

Subsequent to successful detection, a Type 1 PSE may optionally classify a PD using ~~1 Event~~Single-Event Physical Layer classification. Valid classification results are Classes ~~from~~ 0 up to ~~, 1, 2, 3,~~ and including 4, as listed in Table 33–7. If a Type 1 PSE does not implement classification, then the Type 1 PSE shall assign all PDs to Class 0. A Type 1 PSE may optionally implement Data Link Layer classification.

Subsequent to successful detection, all Type 2 PSEs perform classification using at least one of the following: ~~2~~Multiple-Event Physical Layer classification; ~~2~~Multiple-Event Physical Layer classification and Data Link Layer classification; or ~~1 Event~~Single-Event Physical Layer classification and Data Link Layer classification.

Subsequent to successful detection, all Type 3 and Type 4 PSEs perform classification using at least one of the following: Multiple-Event Physical Layer classification; or Multiple-Event Physical Layer classification and Data Link Layer classification. ~~Both pairsets attached to a dual-signature PD shall be classified by Type 3 and Type 4 PSEs that will deliver 4-pair power.~~

If a PSE successfully completes detection of a PD, but the PSE fails to complete classification of a PD, then a Type 1 PSE shall either return to the IDLE state or assign the PD to Class 0; a Type 2, Type 3 or Type 4 PSE shall return to the IDLE state.

~~When connected to a dual-signature PD, the PSE shall treat the requested power over each pairset independently.~~

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Change title and text of Section 33.2.6.1 as follows:

33.2.6.1 PSE ~~1-Event~~Single-Event Physical Layer classification

When ~~1-Event~~Single-Event Physical Layer classification is implemented, classification consists of the application of V_{Class} and the measurement of I_{Class} in a single classification event SINGLE-EVENT_CLASS—as defined in the state diagram in Figure 33–9.

~~The PSE shall provide to the PI V_{Class} with a current limitation of I_{Class_LIM}, as defined in Table 33–10. Polarity shall be the same as defined for $V_{Port_PSE_2P}$ in 33.2.3 and timing specifications shall be as defined by T_{pde} in Table 33–10.~~

The PSE shall measure the resultant I_{Class} and classify the PD based on the observed current according to Table 33–9. All measurements of I_{Class} shall be taken after the minimum relevant class event timing in Table 33–10. This measurement is referenced from the application of V_{Class} min to ignore initial transients.

If the result of the class event is Class 4, a Type 1 PSE shall assign the PD to Class 0; a Type 2 PSE treats the PD as a Type 2 PD but may provide Class 0 power until mutual identification is complete.

If the measured I_{Class} is within the range of I_{Class_LIM}, a Type 1 PSE shall either return to the IDLE state or classify the PD as Class 0; a Type 2, Type 3 or Type 4 PSE shall return to the IDLE state.

Change title and text of Section 33.2.6.2 as follows:

33.2.6.2 PSE ~~2~~Multiple-Event Physical Layer classification

When ~~2~~Multiple-Event Physical Layer classification is implemented, classification consists of the application of V_{Class} and the measurement of I_{Class} in a series of classification and mark events—CLASS_EV1 or CLASS_EV1_LCF, MARK_EV1, CLASS_EV2, ~~and~~ MARK_EV2, CLASS_EV3, MARK_EV3, CLASS_EV4, MARK_EV4, CLASS_EV5, and MARK_EV_LAST—as defined in the state diagram in Figure 33–9.

Editor's note: Update Figure reference above when state diagrams are completed.

Type 2 PSEs shall provide a maximum of 2 class and 2 mark events. Type 3 PSEs shall provide a maximum of 4 class and 4 mark events. Type 4 PSEs shall provide a maximum of 5 class and 5 mark events.

~~The~~ A PSE in the state CLASS_EV1 shall provide to the PI V_{Class} as defined in Table 33–10. The timing specification shall be as defined by T_{CLE1} in Table 33–10. ~~The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–9.~~

A PSE in the state CLASS_EV1_LCF shall provide to the PI V_{Class} as defined in Table 33–10. The timing specification shall be as defined by T_{LCF} in Table 33–10. The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–9 between 6 ms and 75 ms after transitioning into the state CLASS_EV1_LCF. The PSE may continue to monitor the current past 75 ms. If the PSE did not measure I_{Class} in the range of Class 0 before T_{ACS} min and the PSE measures I_{Class} in the range of Class 0 after T_{ACS} max this indicates the PD will perform Autoclass. (see 33.3.5.3).

When the PSE is in the state MARK_EV1, MARK_EV2, MARK_EV3, or MARK_EV4 the PSE shall provide to the PI V_{Mark} as defined in Table 33–10. The timing specification shall be as defined by T_{ME1} in Table 33–10.

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When the PSE is in the state CLASS_EV2, the PSE shall provide to the PI V_{Class}, subject to the T_{CLE2} timing specification, as defined in Table 33–10. ~~The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–9.~~

~~When the PSE is in the state MARK_EV2, the PSE shall provide to the PI V_{Mark} as defined in Table 33–10. The timing specification shall be as defined by T_{ME1} in Table 33–10.~~

When the PSE is in the state CLASS_EV3, CLASS_EV4, or CLASS_EV5 the PSE shall provide to the PI V_{Class}, subject to the T_{CLE3} timing specification, as defined in Table 33–10.

In states CLASS_EV1, CLASS_EV2, and CLASS_EV3, the PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–9.

When the PSE is in the state MARK_EV_LAST, the PSE shall provide to the PI V_{Mark} as defined in Table 33–10. The timing specification shall be as defined by T_{ME2} in Table 33–10.

The mark event states, MARK_EV1, ~~and~~ MARK_EV2, MARK_EV3, MARK_EV4 and MARK_EV_LAST commence when the PI voltage falls below V_{Class} min and end when the PI voltage exceeds V_{Class} min. The V_{Mark} requirement is to be met with load currents in the range of I_{Mark} as defined in Table 33–17.

NOTE—In a properly operating system, the port may or may not discharge to the V_{Mark} range due to the combination of channel and PD capacitance and PD current loading. This is normal and acceptable system operation. For compliance testing, it is necessary to discharge the port in order to observe the V_{Mark} voltage. Discharge can be accomplished with a 2 mA load for 3 ms, after which V_{Mark} can be observed with minimum and maximum load current.

If any measured I_{Class} is equal to or greater than I_{Class_LIM} min as defined in Table 33–10, a Type 2, Type 3 or Type 4 PSE shall return to the IDLE state. ~~The class events shall meet the I_{Class_LIM} current limitation. The mark events shall meet the I_{Mark_LIM} current limitation.~~ The PSE shall limit class event currents to I_{Class_LIM} and shall limit mark event currents to I_{Mark_LIM}.

Editor's note: Cleanup of previous paragraph due to bad readability (strikeouts/underlines). Remove note for D1.5.

All measurements of I_{Class} shall be taken after the minimum relevant class event timing of Table 33–10. This measurement is referenced from the application of V_{Class} min to ignore initial transients.

All class event voltages and mark event voltages shall have the same polarity as defined for V_{Port_PSE-2P} in 33.2.3. The PSE shall complete ~~2~~Multiple-Event Physical Layer classification and transition to the POWER_ON state without allowing the voltage at the PI to go below V_{Mark} min. If the PSE returns to the IDLE state, it shall maintain the PI voltage at V_{Reset} for a period of at least T_{Reset} min before starting a new detection cycle.

Type 3 and Type 4 PSEs, ~~when connected to single-signature PDs,~~ shall transition directly from CLASS_EV1_LCF to MARK_EV_LAST if they implement only one class event.

If the result of the first class event is Class 4, ~~the~~ a Type 2 PSE may omit the subsequent mark and class events only if the PSE implements Data Link Layer classification. In this case, a Type 2 PSE treats the PD as a Type 2 PD but may provide Class 0 power until mutual identification is complete.

If the result of the first class event is any of Classes 0, 1, 2, or 3, ~~the~~ a Type 2 PSE treats the PD as a Type 1 PD and may omit the subsequent mark and class events and classify the PD according to the result of the first class event. If the result of the first class event is any of Classes 0, 1, 2, or 3, a Type 3 or Type 4 PSE treats a ~~single-signature~~ PD as a Type 1 PD and shall omit the subsequent class events, transition directly to

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MARK_EV_LAST, and classify the PD according to the result of the first class event. ~~If the class signature detected during CLASS_EV1_LCF is 0, a Type 3 or Type 4 PSE treats a dual-signature PD as a Type 1 PD and shall omit the subsequent mark and class events and classify the PD as Class 0.~~

~~*Editor's Note (Remove prior to D2.0): We need to address behavior for matched and unmatched classes for mixed Type PDs.*~~

When a PD requests a higher Class than a Type 3 or Type 4 PSE can support, the PSE assigns the PD Class 3, 4, or 6, whichever is the highest that it can support.

A Type 3 or Type 4 PSE ~~connected to a single-signature PD~~ shall skip all subsequent class events and transition directly to Mark_EV_LAST if the class signature detected during CLASS_EV3 is 4. A Type 4 PSE shall skip MARK_EV_4 and CLASS_EV5 and transition directly to Mark_EV_LAST if the class signature detected during CLASS_EV4 is 0 or 1. Classification events may appear on one or both pairsets.

~~A Type 3 or Type 4 PSE connected to a dual-signature PD shall skip all subsequent class events and transition directly to MARK_EV_LAST if the class signature detected during CLASS_EV3 is 0, 1, 2 or 4. See Annex 33D for an overview of Multiple-Event physical layer classification.~~

Table 33–9—PD classification

Measured I_{Class}	Class signature
0 mA to 5.00 mA	Class signature 0
> 5.00 mA and < 8.00 mA	Either class signature 0 or 1
8.00 mA to 13.0 mA	Class signature 1
> 13.0 mA and < 16.0 mA	Either class signature 1 or 2
16.0 mA to 21.0 mA	Class signature 2
> 21.0 mA and < 25.0 mA	Either class signature 2 or 3
25.0 mA to 31.0 mA	Class signature 3
> 31.0 mA and < 35.0 mA	Either class signature 3 or 4
35.0 mA to 45.0 mA	Class signature 4
> 45.0 mA and < 51.0 mA	Either class signature 4 or invalid class signature

NOTE—A Type 1 PSE may ignore I_{Class} and report Class 0.

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Change Table 33-10 as follows:

Table 33–10—PSE Physical Layer classification electrical requirements

Item	Parameter	Symbol	Units	Min	Max	Single- or Multiple-Event	Additional information
1	Class event voltage	V_{Class}	V	15.5	20.5	~~1~~Single, ~~2~~Multiple	
2	Class event current limitation	I_{Class_LIM}	A	0.051	0.100	~~1~~Single, ~~2~~Multiple	
3	Mark event voltage	V_{Mark}	V	7.00	10.0	~~2~~Multiple	
4	Mark event current limitation	I_{Mark_LIM}	A	0.005	0.100	~~2~~Multiple	
5	1st class event timing	T_{CLE1}	ms	6.00	30.0	~~2~~Multiple	Applies only to Type 1 or Type 2 PSEs
6	~~1st m~~Mark event timing (except last mark event)	T_{ME1}	ms	6.00	12.0	~~2~~Multiple	
7	2nd class event timing	T_{CLE2}	ms	6.00	30.0	~~2~~Multiple	
8	~~2nd~~ Last mark event timing	T_{ME2}	ms	6.00		~~2~~Multiple	~~Time from end of detection until power on~~ The maximum value of T_{ME2} is limited by T_{pon}, as defined in 33.2.7.13.
9	Classification reset voltage	V_{Reset}	V	0	2.80	~~2~~Multiple	See section 33.2.6.2
10	Classification reset timing	T_{Reset}	ms	15.0		~~2~~Multiple	See section 33.2.6.2
11	~~1~~Single-Event Physical Layer classification timing	T_{pdc}	ms	6.00	75.0	~~1~~Single	
12	Long first class event timing	T_{LCF}	ms	88	105	Multiple	Only applies to Type 3 and Type 4 PSEs. See 33.2.6.2.
13	Third through fifth class event timing	T_{CLE3}	ms	6	20	Multiple	Only applies to Type 3 and Type 4 PSEs. See 33.2.6.2.

Editor's note: Need to perform thermal analysis on new classification timings/events on both existing and new

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PDs.

Insert Section 33.2.6.3 before Section 33.2.7 as follows:

33.2.6.3 Autoclass

Type 3 and Type 4 PSEs may implement an extension of Physical Layer classification known as Autoclass. The purpose of Autoclass is to allow the PSE to determine the actual maximum power draw of the connected PD. See Annex 33C for more information on Autoclass.

If the PSE implements Autoclass and the connected PD performs Autoclass, the PSE shall measure $P_{Autoclass}$. $P_{Autoclass}$ is the power consumption of a connected PD measured throughout the period bounded by T_{AUTO_PSE1} and T_{AUTO_PSE2}, defined in Table 33–10a. T_{AUTO_PSE1} and T_{AUTO_PSE2} timing is referenced from the transition of the POWER_UP or SET_PARAMETERS state to the POWER_ON state. The power consumption shall be defined as the highest average power measured throughout the period bounded by T_{AUTO_PSE1} and T_{AUTO_PSE2}. Average power is calculated using any sliding window with a width in the range of T_{AUTO_Window} as defined in Table 33–10a.

Table 33–10a—Autoclass electrical requirements

Item	Parameter	Symbol	Units	Min	Max	Additional Information
1	Autoclass power measurement start	T_{AUTO_PSE1}	s	1.4	1.6	Measured from transition to state POWER_ON
2	Autoclass power measurement end	T_{AUTO_PSE2}	s	3.1	3.5	Measured from transition to state POWER_ON
3	Autoclass average power sliding window	T_{AUTO_Window}	s	0.15	0.3	

$$P_{ac_margin} = \left\{ \begin{array}{l} 0.0014 \times P_{Autoclass}^2 - 0.004 \times P_{Autoclass} + 0.04 \text{ for Type 3 over 2-pair} \\ 0.0014 \times P_{Autoclass}^2 - 0.007 \times P_{Autoclass} + 0.05 \text{ for Type 3 over 4-pair} \\ 0.0008 \times P_{Autoclass}^2 - 0.004 \times P_{Autoclass} + 0.04 \text{ for Type 4 over 2-pair} \\ 0.0014 \times P_{Autoclass}^2 - 0.004 \times P_{Autoclass} + 0.04 \text{ for Type 4 over 4-pair} \end{array} \right\}_{W} \quad (33\text{–}3b)$$

where

P_{ac_margin} is minimum margin the PSE adds to the measured power $P_{Autoclass}$ in Watts

$P_{Autoclass}$ is the measured power during the Autoclass window between T_{AUTO_PSE2} and T_{AUTO_PSE2}

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33.2.7 Power supply output

Change text in section 33.2.7 as follows:

~~PSE behavior conforms to the state diagrams in Figure 33–9, Figure 33–9 continued, and Figure 33–10e.~~ When the PSE provides power to the PI, it shall conform with Table 33–11. ~~Table 33–11 limits show values that support worst-case operating limits.~~ Table 33–11 limit values support operation under worst-case operating conditions. These ranges may be narrowed when additional information is known and applied in accordance with this specification. Power may be removed from both pairsets any time power is removed from one pairset.

Change Table 33-11 as follows:

Table 33–11—PSE output PI electrical requirements for all PD Classes, unless otherwise specified

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
1	Output voltage per pairset in the POWER_ON state	V_{Port_PSE-2P}	V	44.0	57.0	1	See 33.2.7.1.
				50.0		2, 3	
				52.0		4	
1a	Output Voltage pair-to-pair difference of pairs with the same polarity in the POWER_ON state	$V_{Port_PSE_diff}$	mV		10	3, 4	Open Load Voltage. Test Setup TBD.
2	Voltage transient below V_{Port_PSE-2P} min	K_{Tran_lo}	%		7.6	2, 3, 4	See 33.2.7.2.
3	Power feeding ripple and noise:						
	f < 500 Hz		V_{pp}		0.500	~~1, 2~~ All	See 33.2.7.3.
	500 Hz to 150 kHz				0.200		
	150 kHz to 500 kHz				0.150		
	500 kHz to 1 MHz				0.100		
4	Continuous total output current capability in POWER_ON state	I_{Con}	A	P_{Class} / V_{Port_PSE-2P}		~~1, 2,~~ All	See 33.2.7.4.
4a	Pairset current including unbalance effect						
	Class 0-4	$I_{Con-2P-unb}$	A	I_{Con}		3, 4	See 33.2.7.4 and 33.2.7.4.1.
	Class 5			0.550		3, 4	
	Class 6			0.682		3, 4	
	Class 7			0.777		4	
	Class 8			0.925		4	
~~5~~	~~Output current in POWER_UP state~~	~~I_{Inrush}~~	~~A~~	~~0.400~~	~~See info~~	~~All~~	~~See 33.2.7.5. Max value defined by Figure 33–13.~~

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Table 33–11—PSE output PI electrical requirements for all PD Classes, unless otherwise specified *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
5	Output current in POWER_UP state	I_{Inrush}	A	0.400	0.450	All	For Class 0-4 ~~single signature~~ PDs. ~~For dual signature PDs with different class over each pairset, this requirement applies over each pairset.~~ See 33.2.7.5. See max value definition in Figure 33–13.
5a	Output current in POWER_UP state	I_{Inrush}	A	0.400	0.900	3, 4	For ≥ Class 5 ~~single signatures~~ PD. ~~For dual signature PD with the same class per pairset.~~ Total current for both pairsets. See 33.2.7.5. See max value definition in Figure 33–13.
5b	Output current per pairset in POWER_UP state	$I_{Inrush-2P}$	A	0.150	0.600	3, 4	For ≥ Class 5 ~~single signatures~~ PD. ~~For dual signature PD with the same class per pairset.~~ See 33.2.7.5. See max value definition in Figure 33–13.
5c	Output current in POWER_UP state	I_{Inrush}	A	0.800	0.900	4	For class 7 and 8 PDs. ~~For dual signature PD with the same class per pairset.~~ Total current for both pairsets. See 33.2.7.5. See max value definition in Figure 33–13.
5d	Output current per pairset in POWER_UP state	$I_{Inrush-2P}$	A	0.400	0.600	4	For class 7 and 8 ~~For dual signature PD with the same class per pairset.~~ See 33.2.7.5. See max value definition in Figure 33–13.
6	Inrush time per pairset	$T_{Inrush-2P}$	s	0.050	0.075	~~1, 2~~ All	See 33.2.7.5.
7	Overload current per pairset, detection range	I_{CUT-2P}	A	P_{Class} / V_{PSE}	I_{LIM-2P}	1, 2	Optional limit; see 33.2.7.6, Table 33–7.
				I_{Con-2P}		3, 4	
8	Overload time limit per pairset	T_{CUT-2P}	s	0.050	0.075	~~1, 2~~ All	See 33.2.7.7.

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Table 33–11—PSE output PI electrical requirements for all PD Classes, unless otherwise specified *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
9	Output current per pairset – at short circuit condition						
		I_{LIM-2P}	A	0.400	See info	1	See 33.2.7.7. Max value defined by Figure 33–14.
				0.684		2	
	Class 0-4			0.684		3, 4	
	Class 5			0.562		3, 4	
	Class 6			0.702		3, 4	
	Class 7			0.829		4	
	Class 8			0.990		4	
10	Short circuit time limit per pairset	T_{LIM-2P}	s	0.050	See info	1	See 33.2.7.1 and 33.2.7.7.
				0.010		2, 3	
				0.006		4	
11	Continuous output power capability in POWER_ON state	P_{Con}	W	P_{Class}		~~1, 2~~ All	See 33.2.7.10, Table 33–7.
12	PSE Type power ~~minimum~~	P_{Type}	W	15.4		1, 3	See 33.1.4, 33.2.7.12a
				30.0		2	
				75.0	99.9	4	
13	Power turn on time	T_{pon}	s		0.400	~~1, 2,~~ All	See 33.2.7.13.
14	Turn on rise time per pairset	T_{Rise}	µs	15.0		~~1, 2~~ All	From 10 % to 90 % of the voltage difference at the PI in POWER_ON state from the beginning of POWER_UP.
15	Turn off time per pairset	T_{Off}	s		0.500	~~1, 2~~ All	See 33.2.7.8.
16	Turn off voltage per pairset	V_{Off}	V		2.80	~~1, 2~~ All	See 33.2.7.9.
17	DC MPS current to be met on at least one pairset[1]						
		I_{Hold}	A	0.005	0.010	1, 2	See 33.2.9.1.2.
	~~Single-signature PD,~~ Class 0-4			0.002	0.005	3, 4	
	~~Single-signature PD,~~ Class 5-8			0.002	0.007	3, 4	
	DC MPS current to be met on both pairsets						
	~~Dual-signature PD~~	I_{Hold}	A	0.002	0.007	3, 4	

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Table 33–11—PSE output PI electrical requirements for all PD Classes, unless otherwise specified *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
17a	DC MPS total current to be met when the sum of both pairs with the same polarity is measured[2]						
	~~Single-signature PD,~~ Class 0-4	I_{Hold}	A	0.004	0.009	3, 4	See 33.2.9.1.2.
	~~Single-signature PD,~~ Class 5-8			0.004	0.014	3, 4	
18	PD Maintain Power Signature dropout time limit	T_{MPDO}	s	0.300	0.400	1, 2	See 33.2.9.
				0.320		3, 4	
19	PD Maintain Power Signature time for validity	T_{MPS}	s	0.060		1, 2	See 33.2.9.
				0.006		3, 4	
20	Intra-pair ~~C~~current unbalance	I_{unb}	A		3 % × I_{Cable}	1	See 33.2.7.11, 33.4.8. NOTE—For practical implementations, it is recommended that Type 1 PSEs support Type 2, 3, 4 I_{unb} requirements.
					3 % × I_{Peak}	2, 3, 4	
21	Alternative B detection backoff time	T_{dbo}	s	2.00		~~1, 2,~~ All	
22	Output capacitance during detection state over a pairset	C_{out}	µF		0.520	~~1, 2,~~ All	
23	Detection timing	T_{det}	s		0.500	~~1, 2,~~ All	Time to complete detection on a pairset. ~~of a PD.~~
24	Error delay timing	T_{ed}	s	0.750		~~1, 2,~~ All	Delay before PSE may attempt subsequent powering of a pairset after power removal from that pairset because of an error condition.

[1]Item 17 applies to PSEs that measure currents per pairset to check the MPS.
[2]Item 17a applies to PSEs that measure the sum of the pair currents of the same polarity to check the MPS.

Editor's Note (for Table 33-11):
1. I_{cut-2P} min values are subject to final E2EP2P_Iunb/Runb results after conducting statistical analysis (if required) which will result with lower values. The current values are derived from worst case analysis model.
2. The following case needs to be addressed: If PSE is using active or passive pair-to-pair current balancing circuitry, K_I_{cut} may be lower (down to 0.5) per equation TBD.
3. E2EP2P_Iunb is the highest (~30%) on the pairs were we don't sense the current and lower on the pair we sense current (~15%). While specifying the PSE port current capacity per the highest P2P_Iunb is the correct approach (which we already did), it is worth to consider if I_{lim} and I_{cut} need to be calculated per the pairs with highest unbalance or per the pairs with lower unbalance. The reason for this question is: I_{cut} and I_{lim} values are set to much higher values than the actual current measure due to much higher P2P_UNB. As a result the actual I_{lim} protection will be activated ~11.1% above Type 4 maximum power. The solution is: I_{cut}, I_{peak}, I_{lim}

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will be allowed to be decreased if PSE Rmax and Rmin are increased by a small constant resistance per equation TBD which is actually what happened in the negative pairs. To be discussed in the group.
4. Item 4a still under investigation with respect to PD Vdiff.

33.2.7.1 Output voltage in the POWER_ON state

Change text of Section 33.2.7.1 as follows:

The specification for $V_{Port_PSE\text{-}2P}$ in Table 33–11 shall be met with a (I_{Hold} max × $V_{Port_PSE\text{-}2P}$ min) to P_{Type} min load step at a rate of change of at least 15 mA/µs. The voltage transients as a result of load changes up to 35 mA/µs shall be limited to 3.5 V/µs max.

A PSE in the POWER_ON state may remove power from ~~the PI~~ a pairset when the ~~PI~~ pairset voltage no longer meets the $V_{Port_PSE\text{-}2P}$ specification.

A Type 3 or Type 4 PSE that has assigned Class 1-4 to a ~~single-signature~~ PD and is in the POWER_ON state may transition between 2-pair and 4-pair power at any time, including after the expiration of T_{pon}.

33.2.7.2 Voltage transients

Change text of Section 33.2.7.2 as follows:

A Type 2, Type 3, and Type 4 PSE shall maintain an output voltage no less than K_{Tran_lo} below $V_{Port_PSE\text{-}2P}$ min for transient conditions lasting more than 30 µs and less than 250 µs, and meet the requirements of 33.2.7.7.

Transients less than 30 µs in duration may cause the voltage at the PI to fall more than K_{Tran_lo}. The minimum PD input capacitance allows a Type 1 or Type 2 ~~the~~ PD to operate for any input voltage transient lasting less than 30 µs. Transients lasting more than 250 µs shall meet the $V_{Port_PSE\text{-}2P}$ specification.

33.2.7.3 Power feeding ripple and noise

Change text of Section 33.2.7.3 as follows:

The specification for power feeding ripple and noise in Table 33–11 shall be met for common-mode and/or pair-to-pair noise values for power outputs from (I_{Hold} max × $V_{Port_PSE\text{-}2P}$ min) to P_{Type} min for PSEs at static operating $V_{Port_PSE\text{-}2P}$. The limits are meant to preserve data integrity. To meet EMI standards, lower values may be needed. For higher frequencies, see 33.4.4, ~~and~~ 33.4.5, and 33.4.6.

33.2.7.4 Continuous output current capability in the POWER_ON state

Replace section 33.2.7.4 as follows:

PSEs that operate in 2-pair mode shall be able to source $I_{Con\text{-}2P}$ as specified in Equation (33–3c). $I_{Con\text{-}2P}$ is the current the PSE supports on the powered pairset.

$$I_{Con\text{-}2P} = \left\{ \frac{P_{Class}}{V_{PSE}} \right\}_A \qquad (33\text{–}3c)$$

where

P_{Class} is P_{Class} as defined in Table 33–7

V_{PSE} is the voltage at the PSE PI as defined in 1.4.423

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Type 3 and Type 4 PSEs operating in 4-pair mode, ~~connected to a single-signature PD, or connected to a dual-signature PD that advertised the same class signature on each pairset~~ shall be able to source I_{Con}, I_{Con-2P}, and I_{Con-2P_unb} as specified in Table 33–11 and Equation (33–3d). I_{Con-2P} is the current the PSE supports on each pairset and is defined by Equation Equation (33–3d). A PSE is not required to support I_{Con-2P} values greater than I_{Con-2P_unb}. I_{Con} is the total current of both pairs with the same polarity that a PSE supports. I_{Con-2P_unb} is the maximum current the PSE supports over one of the pairs of same polarity under maximum unbalance condition (see 33.2.7.4.1) in the POWER_ON state.

$$I_{Con\text{-}2P} = \{\min(I_{Con} - I_{Port\text{-}2P\text{-}other},\ I_{Con\text{-}2P_unb})\}_A \qquad (33\text{–}3d)$$

where

I_{Con} is the total current a PSE is able to source as defined in Table 33–11

$I_{Port\text{-}2P\text{-}other}$ is the output current on the other pairset (see 33.2.4.4).

$I_{Con\text{-}2P_unb}$ is the current a PSE is able to source on a pairset due to unbalance as defined in Table 33–11

Type 3 and Type 4 PSEs operating in 4-pair mode, connected to a dual-signature PD that advertised a different class signature on each pairset, shall be able to source I_{Con-2P} on each pairset as specified in Equation (33–3e). Note that for these PDs I_{Con-2P} is calculated using Equation (33–3e) for each pairset independently.

$$I_{Con\text{-}2P} = \left\{\frac{P_{Class\text{-}2P}}{V_{PSE}}\right\}_A \qquad (33\text{–}3e)$$

where

P_{Class_2P} is $P_{Class-2P}$ as defined in Table 33–11

V_{PSE} is the voltage at the PSE PI as defined in 1.4.423

In addition to I_{Con}, I_{Con-2P} and $I_{Con-2P-unb}$ as specified in Table 33–11, the PSE shall support the following AC current waveform parameters, while within the operating voltage range of V_{Port_PSE-2P}:

$I_{Peak-2P}$ minimum for T_{CUT-2P} minimum and 5 % duty cycle minimum, where

$$I_{Peak} = \left\{\frac{V_{PSE} - \sqrt{V_{PSE}^2 - 4 \times R_{Chan} \times P_{Peak_PD}}}{2 \times R_{Chan}}\right\}_A \qquad (33\text{–}4)$$

where

V_{PSE} is the voltage at the PSE PI as defined in 1.4.423

R_{Chan} is the channel loop resistance; this parameter has a worst-case value of R_{Ch}. R_{Ch} is defined in Table 33–1.

P_{Peak_PD} is the total peak power a PD may draw for its Class; see Table 33–18

I_{Peak} is the total current of both pairs with the same polarity that a PSE supports.

$$I_{Peak\text{-}2P_unb} = \left\{(1 + K_{IPeak}) \times \frac{I_{Peak}}{2}\right\}_A \qquad (33\text{–}4a)$$

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where

K_{IPeak} The value of K_{IPeak}, defined in Equation (33–4b), is based on a curve fit and is dimensionless

I_{Peak} is the total peak current a PSE supports per Equation (33–4)

$$K_{IPeak} = \begin{cases} \min(0.214 \times R_{chan}^{-0.363}, 0.330) & \text{for Class 5} \\ \min(0.199 \times R_{chan}^{-0.350}, 0.300) & \text{for Class 6} \\ \min(0.180 \times R_{chan}^{-0.326}, 0.270) & \text{for Class 7} \\ \min(0.176 \times R_{chan}^{-0.325}, 0.260) & \text{for Class 8} \end{cases} \quad (33\text{–}4b)$$

where

R_{Chan} is the channel DC loop resistance

PSEs that operate in 2-pair mode shall be able to source $I_{Peak\text{-}2P}$ as specified in Equation (33–4c). $I_{Peak\text{-}2P}$ is the current the PSE supports on the powered pairset.

$$I_{Peak\text{-}2P} = \{I_{Peak}\}_A \quad (33\text{–}4c)$$

where

I_{Peak} is the total peak current a PSE supports per Equation (33–4)

Type 3 and Type 4 PSEs operating in 4-pair mode, ~~connected to a single-signature PD,~~ shall be able to source I_{Peak} , $I_{Peak\text{-}2P}$, and $I_{Peak\text{-}2P_unb}$ as specified in Table 33–11 and Equation (33–4d). $I_{Con\text{-}2P}$ is the current the PSE supports on each pairset and is defined by Equation (33–4d). A PSE is not required to support $I_{Peak\text{-}2P}$ values greater than $I_{Peak\text{-}2P_unb}$. I_{Peak} is the total current of both pairs with the same polarity that a PSE supports. $I_{Peak\text{-}2P_unb}$ is the maximum current the PSE supports over one of the pairs of same polarity under maximum unbalance condition (see 33.2.7.4.1) in the POWER_ON state.

$$I_{Peak\text{-}2P} = \{\min(I_{Peak} - I_{Port\text{-}2P\text{-}other}, I_{Peak\text{-}2P_unb})\}_A \quad (33\text{–}4d)$$

where

I_{Peak} is the total peak current a PSE supports per Equation (33–4)

$I_{Port\text{-}2P\text{-}other}$ is the output current on the other pairset (see 33.2.4.4 (XREF))

$I_{Peak\text{-}2P_unb}$ is the minimum current due to unbalance effects a PSE must support on a pairset as defined in Table 33–11.

Type 3 and Type 4 PSEs operating in 4-pair mode, connected to a dual-signature PD, shall be able to source $I_{Peak\text{-}2P}$ on each pairset as specified in Equation (33–4e). Note that for these PDs $I_{Peak\text{-}2P}$ is calculated using Equation (33–4e) for each pairset independently.

$$I_{Peak\text{-}2P} = \left\{ \frac{V_{PSE} - \sqrt{V_{PSE}^2 - 4 \times R_{Chan} \times P_{Peak_PD\text{-}2P}}}{2 \times R_{Chan}} \right\}_A \quad (33\text{–}4e)$$

where

V_{PSE} is the voltage at the PSE PI as defined in 1.4.126

R_{Chan} is the channel loop resistance; this parameter has a worst-case value of R_{Ch}. R_{Ch} is defined in Table 33–1.

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$P_{Peak_PD\text{-}2P}$ is the total ~~peak power a PD~~ may draw for its Class on a pairset; see Table 33–18

Insert Section 33.2.7.4.1 and Section 33.2.7.4.2 after section 33.2.7.4 as follows:

33.2.7.4.1 PSE PI pair-to-pair resistance and current unbalance

Type 3 and Type 4 PSEs operating over 4-pair are subject to unbalance requirements in this section. The contribution of PSE PI pair-to-pair effective resistance unbalance (PSE_P2PRunb) to the whole effective system end to end resistance unbalance (E2EP2PRunb), is specified by PSE maximum (R_{PSE_max}) and minimum (R_{PSE_min}) common mode effective resistance in the powered pairs of same polarity.

The PSE_P2PRunb determined by R_{PSE_max} and R_{PSE_min} ensures that along with any other parts of the system, i.e. channel (cables and connectors) and the PD, the maximum pair current including unbalance does not exceed $I_{con\text{-}2P\text{-}unb}$ as defined in Table 33–11 during normal operating conditions. $I_{con\text{-}2P\text{-}unb}$ is the pairset current in the case of maximum unbalance and will be higher than $I_{con}/2$. $I_{con\text{-}2P\text{-}unb}$ is specified for total channel common mode pair resistance from 0.1 Ω to R_{ch}. For channels with common mode pair resistance lower than 0.1 Ω, see Annex 33B.

R_{PSE_max} and R_{PSE_min} are specified and measured under maximum P_{Class} sourcing conditions. Conformance with Equation (33–4f) shall be met for R_{PSE_max} and R_{PSE_min}.

$$R_{PSE_max} = \left\{ \begin{array}{ll} 2.200 \times R_{PSE_min} - 0.040 & \text{for Class 5} \\ 2.015 \times R_{PSE_min} - 0.040 & \text{for Class 6} \\ 1.800 \times R_{PSE_min} - 0.030 & \text{for Class 7} \\ 1.750 \times R_{PSE_min} - 0.030 & \text{for Class 8} \end{array} \right\}_{\Omega} \quad (33\text{–}4f)$$

where

R_{PSE_max} is the maximum PSE common mode effective resistance in the powered pairs of same polarity.

R_{PSE_min} is the minimum PSE common mode effective resistance in the powered pairs of same polarity.

The values of R_{PSE_max} and R_{PSE_min} are implementation specific and need to satisfy Equation (33–4f). See Annex 33B for the test setup and test conditions for R_{PSE_max} and R_{PSE_min}.

~~*Editor's Note: Numbers to be updated for DS PDs.*~~

33.2.7.5 Output current in POWER_UP mode

Editor's Note:

- Timing requirements for 4-pair power to be added to this section.

- ~~To verify that in dual signature PD with same class i.e. same load, the PD startup is guaranteed if one of the pairsets has Inrush-2P_min and the 2nd has the rest of the current. If both pairsets are turned on as the same time, there is no issue at all.~~

- To update the definition of dual signature PD with the ~~same class signature that it is a single load PD as opposed to dual signature PD with different class that has isolated different loads and hence end to end~~

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pair to pair resistance unbalance is zero. This will simplify the spec and make it clearer.
- Table 33-11 item 5a -5d: to verify that PSE is allowed to do inrush limit with 2P mode.

Change the text of 33.2.7.5 as follows:

~~POWER_UP mode occurs between the PSE's transition to the POWER_UP state and either the expiration of T_{Inrush} or the conclusion of PD inrush currents (see 33.3.7.3).~~ POWER_UP mode occurs on each pairset between the PSE's transition to the POWER_UP state on that pairset and either the expiration of $T_{Inrush\text{-}2P}$ or, for Type 1 and Type 2 PSEs that make use of legacy powerup, the conclusion of PD inrush currents on that pairset (see 33.3.7.3). Type 3 and Type 4 PSEs that apply power to both pairsets ~~when connected to a single-signature PD~~ shall reach the POWER_ON state on both pairsets within $T_{Inrush\text{-}2P}$ max, starting with the first pairset transitioning into the POWER_UP state. ~~However, for practical implementations, it is recommended that the POWER_UP mode persist for the complete duration of T_{Inrush}, as the PSE may not be able to correctly ascertain the conclusion of a PD's inrush behavior.~~ See legacy_powerup variable in section 33.2.4.4 for more information on the POWER_UP to POWER_ON transition.

The PSE shall limit the maximum current sourced ~~at the PI~~ per pairset ($I_{Inrush\text{-}2P}$) and the total inrush current (I_{Inrush}) during POWER_UP per the requirements of Table 33–11 item 5 or items 5a and item 5b or items 5c and item 5d. The maximum inrush current sourced by the PSE per pairset shall not exceed the per pairset ~~PSE~~ inrush template in Figure 33–13 and Equation (33–5) when operating Class 0-4 PDs and Figure 33–13 and Equation (33–5a) when operating a ~~single-signature~~ PD with Class 5 and above ~~or when operating a dual-signature PD with the same class over each pairset~~.

The minimum value of $I_{Inrush\text{-}2P}$ includes the effect of end to end pair to pair resistance unbalance.

Type 4 PSEs supporting Class 7 and 8 when implementing $I_{Inrush\text{-}2P}$ and Inrush requirements per Table 33–11 items 5a and 5b and when connected to a ~~single-signature~~ PD through a channel resistance of 0.1 Ω to 12.5 Ω per pairset, shall successfully power up within 50 ms without startup oscillations a PD with C_{port} per pairset as defined in 33.3.7.3 in parallel to a Class 2 load during POWER_UP period in addition to the other requirements of 33.3.7.

a) During POWER_UP, for ~~PI~~ pairset voltages between 0 V and 10 V, the minimum $I_{Inrush\text{-}2P}$ requirement is 5 mA.
b) During POWER_UP, for ~~PI~~ pairset voltages between 10 V and 30 V, the minimum $I_{Inrush\text{-}2P}$ requirement is 60 mA.
c) During POWER_UP for Class 4 or lower, for ~~PI~~ pairset voltages above 30 V, the minimum $I_{Inrush\text{-}2P}$ requirement is as specified in Table 33–11 item 5. For Class 5 and higher the minimum $I_{Inrush\text{-}2P}$ and I_{Inrush} requirement are as specified in Table 33–11 item 5a and item 5b or as specified in Table 33–11 items 5c and 5d.
d) For Type 1 PSE, measurement of minimum $I_{Inrush\text{-}2P}$ requirement to be taken after 1 ms to allow startup transients. A Type 2 PSE that uses ~~1-Event~~Single-Event Physical Layer classification, and requires the 1 ms settling time, shall power up a ~~e~~Class 4 PD as if it used ~~2~~Multiple-Event Physical Layer classification.

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Replace Figure 33-13 with the following:

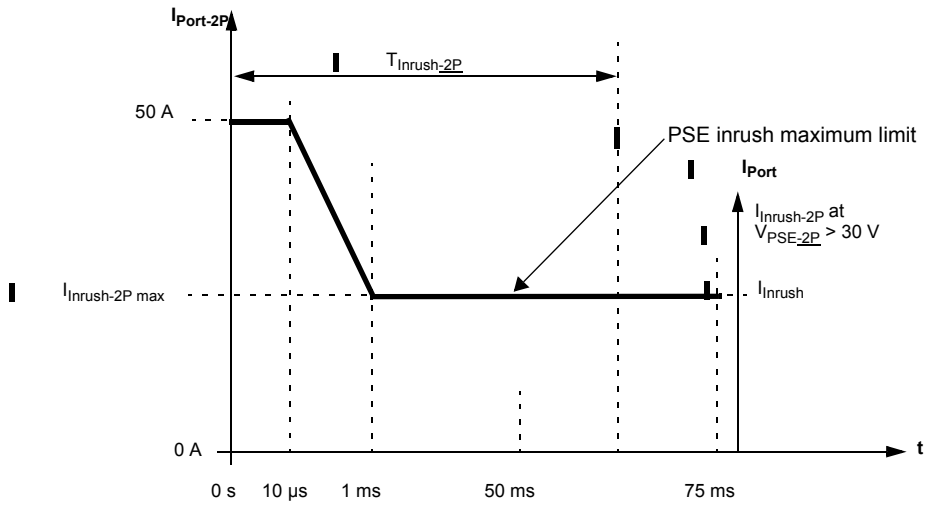

Figure 33–13—$I_{Inrush\text{-}2P}$ current and timing limits, per pairset in POWER_UP

Replace Equation 33-5 as follows:

The PSE inrush maximum limit, $I_{PSEIT\text{-}2P}$, is defined by the following segments:

$$I_{PSEIT\text{-}2P}(t) = \left\{ \begin{array}{ll} 50.0 & \text{for } 0 < t < 10.0\times10^{-6} \\ \text{TBD=function of (t, Iinrush-2P max)} & \text{for } 10.0\times10^{-6} \le t < 0.001 \\ I_{Inrush\text{-}2P} \text{ max} & 0.001 \le t < 0.075 \end{array} \right\}_{A} \quad (33\text{–}5)$$

where

t is the time in seconds

Editor's Note: To update the TBD in equation 33-5. Add Equation 33-5a after equation 33-5 to describe the template of Figure 33-13 for Iinrush.

Insert new Equation 33-5a as follows:

Coming soon: Equation 33-5a (33–5a)

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33.2.7.6 Overload current

Change the text of 33.2.7.6 as follows:

If $I_{Port\text{-}2P}$, the current supplied per pairset by the PSE to the PI, exceeds $I_{CUT\text{-}2P}$ min for longer than $T_{CUT\text{-}2P}$ min, the PSE may remove power from ~~the PI~~that pairset. The cumulative duration of $T_{CUT\text{-}2P}$ is measured with a sliding window of at least 1 second width.

~~The $I_{CUT\text{-}2P}$ threshold may equal the $I_{Peak\text{-}2P}$ value determined by Equation (33–4).~~

33.2.7.7 Output current—at short circuit condition

Change the text of Section 33.2.7.7 as follows:

Equation (33–6), Equation (33–7), and Figure 33–14 apply to Type 1 and Type 2 PSEs. Equation (33–6a), Equation (33–7a), and Figure 33–14a apply to Type 3 and Type 4 PSEs that operate in 2-pair mode, ~~as well as to Type 3 and Type 4 PSEs operating in 4-pair mode, connected to a dual-signature PD that advertised a different class signature on each pairset.~~ Equation (33–6b), Equation (33–7b), and Figure 33–14b apply to Type 3 PSEs operating in 4-pair mode, ~~connected to single-signature PDs, or connected to a dual-signature PD that advertised the same class signature on each pairset.~~ Equation (33–6c), Equation (33–7c), and Figure 33–14c apply to Type 4 PSEs operating in 4-pair mode, ~~connected to a single-signature PD, or connected to a dual-signature PD that advertised the same class signature on each pairset.~~

A PSE may remove power from the PI if the PI current meets or exceeds the "PSE lowerbound template" in Figure 33–14, Figure 33–14a, and Figure 33–14b. Power shall be removed from ~~the~~ a pairset ~~PI~~ of a PSE before the pairset ~~PI~~ current exceeds the "PSE upperbound template" in Figure 33–14, Figure 33–14a, and Figure 33–14b. ~~When connected to a single-signature PD,~~ a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset.

Replace Figure 33-14 with the following:.

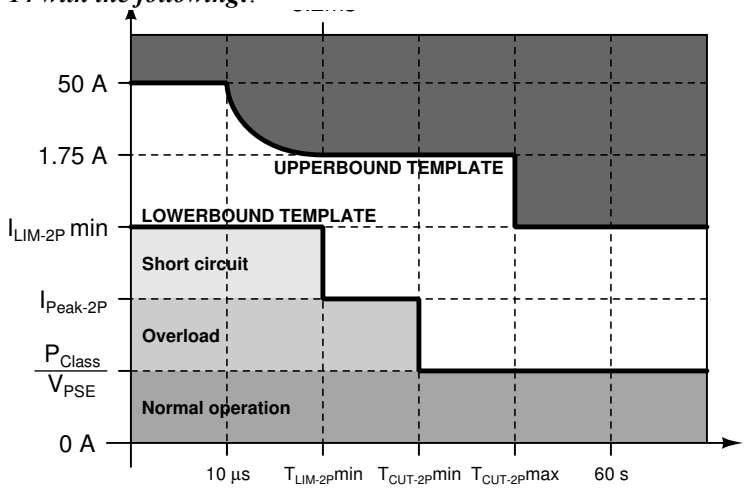

Figure 33–14—POWER_ON state, per pairset operating current template for Type 1 and Type 2 PSEs.

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Insert three new figures 33-14a, 33-14b, and 33-14c after figure 33-14 as follows:

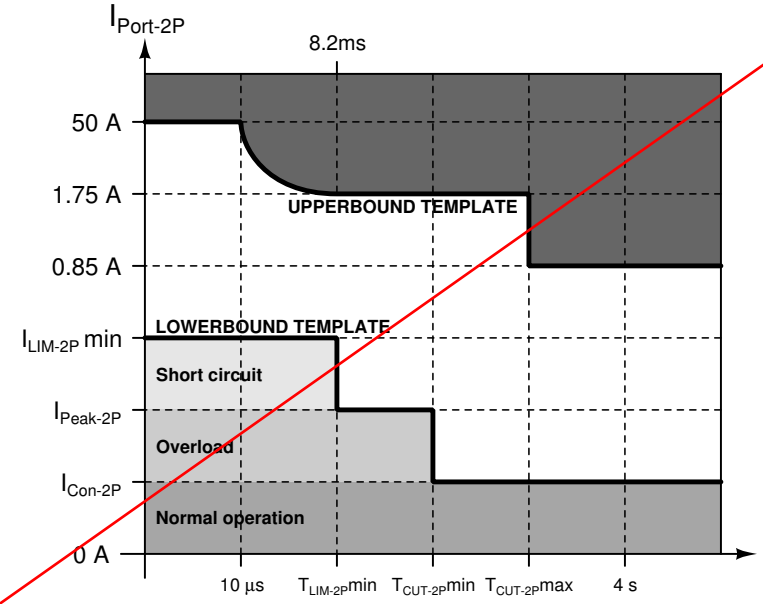

Figure 33–14a—POWER_ON state, per pairset operating current template for Type 3 and Type 4 PSEs connected to dual-signature PDs that advertise a different class code on each pairset.

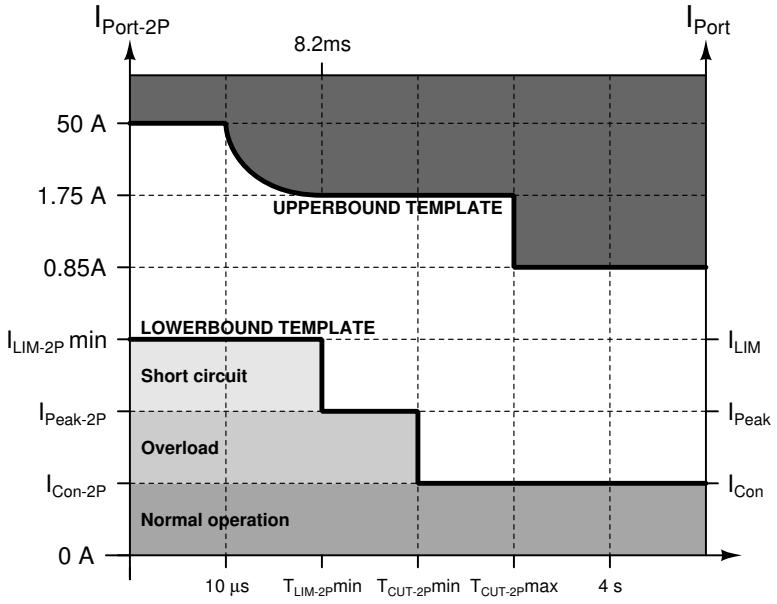

Figure 33–14b—POWER_ON state, per pairset operating current template for Type 3 PSEs ~~connected to single-signature PDs, or connected to dual-signature PDs that advertised the same class signature on each pairset.~~

The maximum value of $I_{LIM\text{-}2P}$ is the PSE upperbound template described by Equation (33–6), Equation (33–6a), Equation (33–6b), Equation (33–6c), ~~and~~ Figure 33–14, Figure 33–14a, Figure 33–14b, and Figure 33–14c. $I_{LIM\text{-}2P}$ minimum value in Table 33–11 item 9 for Class 5 and above includes E2EP2PRunb effect.

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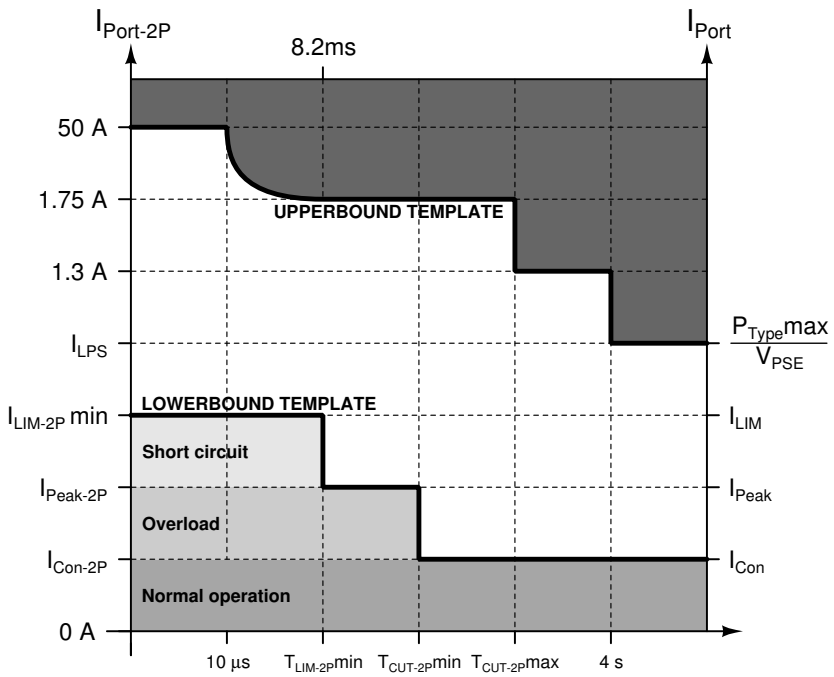

Figure 33–14c—POWER_ON state, per pairset operating current template for Type 3 PSEs ~~connected to single-signature PDs, or connected to dual-signature PDs that advertised the same class signature on each pairset.~~

The PSE upperbound template, $I_{\underline{PSEUT\text{-}2P}}$, is defined by the following segments:

$$I_{\underline{PSEUT\text{-}2P}}(t) = \begin{cases} 50.0 & \text{for } (0 \le t < 10.0\times10^{-6}) \\ \sqrt{\frac{K}{t}} & \text{for } (10.0\times10^{-6} \le t < 8.20\times10^{-3}) \\ 1.75 & \text{for } (8.20\times10^{-3} \le t < T_{\text{CUT-2P}}\text{max}) \\ I_{\text{LIM-2P}}\text{min} & \text{for } (T_{\text{CUT-2P}}\text{max} \le t) \end{cases}_{\text{A}} \quad (33\text{–}6)$$

Insert two new equations (33-6a) and (33-6b) after equation (33-6) as follows:

$$I_{\underline{PSEUT\text{-}2P}}(t) = \begin{cases} 50.0 \text{ for } (0 \le t < 10.0\times10^{-6}) \\ \sqrt{\frac{K}{t}} \text{ for } (10.0\times10^{-6} \le t < 8.20\times10^{-3}) \\ 1.75 \text{ for } (8.20\times10^{-3} \le t < T_{\text{CUT-2P}}\text{max}) \\ 0.85 \text{ for } (T_{\text{CUT-2P}}\text{max} \le t) \end{cases}_{\text{A}} \quad (33\text{–}6a)$$

$$I_{\underline{PSEUT\text{-}2P}}(t) = \begin{cases} 50.0 \text{ for } (0 \le t < 10.0\times10^{-6}) \\ \sqrt{\frac{K}{t}} \text{ for } (10.0\times10^{-6} \le t < 8.20\times10^{-3}) \\ 1.75 \text{ for } (8.20\times10^{-3} \le t < T_{\text{CUT-2P}}\text{max}) \\ 0.85 \text{ for } (T_{\text{CUT-2P}}\text{max} \le t) \end{cases}_{\text{A}} \quad (33\text{–}6b)$$

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$$I_{\underline{\text{PSEUT-2P}}}(t) = \left\{ \begin{array}{ll} 50.0 & \text{for } (0 \le t < 10.0\times10^{-6}) \\ \sqrt{\frac{K}{t}} & \text{for } (10.0\times10^{-6} \le t < 8.20\times10^{-3}) \\ 1.75 & \text{for } (8.20\times10^{-3} \le t < T_{\text{CUT-2P}}\text{max}) \\ 1.3 & \text{for } (T_{\text{CUT-2P}}\text{max} \le t < 4.00) \\ I_{\text{TBDNAME}} & \text{for } (4.00 \le t) \end{array} \right\}_{\text{A}} \quad \text{(33–6c)}$$

where

t	is the duration in seconds that the PSE sources $I_{\text{Port-2P}}$
K	is 0.025 A^2s, an energy limitation constant for the ~~port~~ pairset current when it is not in steady state normal operation
$T_{\text{CUT-2P}}$ max	is T_{CUT} _max per pairset, as defined in Table 33–11
$I_{\text{LIM-2P}}$ min	is I_{LIM} _min per pairset, as defined in Table 33–11
P_{Type} max	is the maximum power for a given PSE Type
V_{PSE}	is the voltage at the PSE PI as defined in 1.4.423
$I_{\text{Port-2P-other}}$	is the output current on the other pairset (see 33.2.4.4)

The PSE shall limit ~~the~~ a pairset current to $I_{\text{LIM-2P}}$ for a duration of up to $T_{\text{LIM-2P}}$ in order to account for PSE dV/dt transients at the ~~PI~~ pairset. The cumulative duration of $T_{\text{LIM-2P}}$ may be measured with a sliding window.

The PSE lowerbound template, $I_{\text{PSELT-2P}}$, is defined by the following segments:

$$I_{\underline{\text{PSELT-2P}}}(t) = \left\{ \begin{array}{ll} I_{\text{LIM-2P}}\text{min} & \text{for } (0 \le t < T_{\text{LIM-2P}}\text{min}) \\ I_{\underline{\text{Peak-2P}}} & \text{for } (T_{\text{LIM-2P}}\text{min} \le t < T_{\text{CUT-2P}}\text{min}) \\ \frac{P_{\text{Class}}}{V_{\text{PSE}}} & \text{for } (T_{\text{CUT-2P}}\text{min} \le t) \end{array} \right\}_{\text{A}} \quad \text{(33–7)}$$

Insert three new equations (33-7a), (33-7b) and (33-7c) after equation (33-7) as follows:

$$I_{\underline{\text{PSELT-2P}}}(t) = \left\{ \begin{array}{ll} I_{\text{LIM-2P}}\text{min} & \text{for } (0 \le t < T_{\text{LIM-2P}}\text{min}) \\ I_{\text{Peak-2P}} & \text{for } (T_{\text{LIM-2P}}\text{min} \le t < T_{\text{CUT-2P}}\text{min}) \\ I_{\text{Con-2P}}\text{min} & \text{for } (T_{\text{CUT-2P}}\text{min} \le t) \end{array} \right\}_{\text{A}} \quad \text{(33–7a)}$$

$$I_{\underline{\text{PSELT-2P}}}(t) = \left\{ \begin{array}{ll} I_{\text{LIM-2P}}\text{min} & \text{for } (0 \le t < T_{\text{LIM-2P}}\text{min}) \\ I_{\text{Peak-2P}} & \text{for } (T_{\text{LIM-2P}}\text{min} \le t < T_{\text{CUT-2P}}\text{min}) \\ I_{\text{Con-2P}}\text{min} & \text{for } (T_{\text{CUT-2P}}\text{min} \le t) \end{array} \right\}_{\text{A}} \quad \text{(33–7b)}$$

$$I_{\underline{\text{PSELT-2P}}}(t) = \left\{ \begin{array}{ll} I_{\text{LIM-2P}}\text{min} & \text{for } (0 \le t < T_{\text{LIM-2P}}\text{min}) \\ I_{\text{Peak-2P}} & \text{for } (T_{\text{LIM-2P}}\text{min} \le t < T_{\text{CUT-2P}}\text{min}) \\ I_{\text{Con-2P}}\text{min} & \text{for } (T_{\text{CUT-2P}}\text{min} \le t) \end{array} \right\}_{\text{A}} \quad \text{(33–7c)}$$

where

t	is the duration that the PI sources $I_{\text{Port-2P}}$
$I_{\text{LIM-2P}}$ min	is the $I_{\text{LIM-2P}}$ min value per pairset for the PSE (see Table 33–11)

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$T_{LIM\text{-}2P}$ min	is $T_{LIM\text{-}2P}$ min per pairset as defined in Table 33–11
$T_{CUT\text{-}2P}$ min	is $T_{CUT\text{-}2P}$ min per pairset, as defined in Table 33–11
$I_{Peak\text{-}2P}$	is $I_{Peak\text{-}2P}$ per pairset, as defined in Equation (33–4)
P_{Class}	is P_{Class}, as defined in Table 33–7
V_{PSE}	is the voltage at the PSE PI
$I_{Con\text{-}2P}$	is the minimum supported continuous current on a pairset as defined in 33.2.7.4

If a short circuit condition is detected on a pairset, power removal from ~~the PI~~ that pairset shall begin within $T_{LIM\text{-}2P}$ as specified in Table 33–11. If $I_{Port\text{-}2P}$ exceeds the PSE lowerbound template, the PSE output voltage may drop below $V_{Port_PSE\text{-}2P}$ min.

A PSE in the POWER_ON state may remove power from a pairset without regard to T_{LIM} when the pairset voltage no longer meets the $V_{Port_PSE\text{-}2P}$ specification.

33.2.7.8 Turn off time

Change text in section 33.2.7.8 as follows:

The specification for T_{Off} in Table 33–11 shall apply to the discharge time from $V_{Port_PSE\text{-}2P}$ to V_{Off} of a pairset with a test resistor of 320 kΩ attached to that pairset~~the PI~~. In addition, it is recommended that the pairset ~~PI~~ be discharged when turned off. T_{Off} starts when V_{PSE} drops 1 V below the steady-state value after the pi_powered variable is cleared (see Figure 33–9). T_{Off} ends when $V_{PSE} \leq V_{Off}$ max. The PSE remains in the IDLE state as long as the average voltage across the pairset ~~PI~~ is below V_{Off} max. The IDLE state is the state when the PSE is not in detection, classification, or normal powering states.

33.2.7.9 Turn off voltage

The specification for V_{Off} in Table 33–11 shall apply to the PI voltage in the IDLE State.

33.2.7.10 Continuous output power capability in POWER_ON state

Change text of Section 33.2.7.10 as follows:

P_{Class} is the ~~class~~ Class power defined in 33.2.6 and Equation (33–3), or PSE allocated power (as defined in 79.3.2.6) added to the channel power loss for both pairsets combined.

$P_{Class\text{-}2P}$ is the class power defined in 33.2.6 and Equation (33–3b), or PSE allocated power (as defined in 79.3.2.6) added to the channel power loss for a pairset. ~~This parameter only applies to Type 3 and Type 4 PSEs operating both pairsets and connected to a dual-signature PD that advertised a different class signature on each pairset.~~

P_{Con} is valid over the range of $V_{Port_PSE\text{-}2P}$ defined in Table 33–11. Measurement of P_{Con} should be averaged using any sliding window with a width of 1 s.

A PSE may remove power from a PD that causes the PSE to source more than P_{Class}.

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~~*Editor's Note: Effects of single and dual-signature PDs to be considered.*~~

Change title and text of Section 33.2.7.11 as follows:

33.2.7.11 Intra-pair ~~C~~current unbalance

The specification for I_{unb} in Table 33–11 shall apply to the current unbalance between the two conductors of a power pair over the current load range.

A 100BASE-TX transmitter in a Type 2, Type 3 and Type 4 Endpoint PSEs shall meet the requirements of 25.4.5 in the presence of (I_{unb} / 2).

Insert new section 33.2.7.11a after section 33.2.7.11 as follows:

33.2.7.12 Type power

P_{Type} min is the minimum power a PSE is capable of sourcing.

Type 4 PSEs shall not source more power than P_{Type} max as specified in Table 33–11 calculated with any sliding window with a width up to 4 seconds. This equates to a maximum $I_{Port\text{-}2P}$ current I_{LPS} defined in Equation (33–7).

$$I_{LPS} = \left\{ \min \left(\frac{P_{Type}\max}{V_{PSE}} - I_{Port\text{-}2P\text{-}other}, 1.3 \right) \right\}_A \qquad (33\text{–}7d)$$

where

P_{Type} max	is the maximum power allowed for a given Type as defined in Table 33–11
V_{PSE}	is the voltage at the PSE PI as defined in 1.4.423
$I_{Port\text{-}2P\text{-}other}$	is the output current on the other pairset (see 33.2.4.4)

Editor's note: Lennart to check IEC62368, part 3.

33.2.7.13 Power turn on time

Change text in section 33.2.7.12 as follows:

The specification for T_{pon} in Table 33–11 applies to the PSE power up time for a PD after completion of detection. ~~If power is not applied as specified, a new detection cycle is initiated (see 33.2.4.1).~~

For Type 3 and Type 4 PSEs, ~~when connected to a single-signature PD,~~ both pairsets shall reach the POWER_ON state within T_{pon} after detection on last pairset. ~~When connected to a dual-signature PD, T_{pon} is applied from the completion of detection to the POWER_ON state for each pairset independently.~~

33.2.7.14 PSE stability

When connected together as a system, the PSE and PD might exhibit instability at the PSE side or the PD side or both due to the presence of negative impedance at the PD input. See Annex 33A for PSE design guidelines for stable operation.

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33.2.8 Power supply allocation

Change text in Section 33.2.8 as follows:

A PSE shall not initiate power provision to a link if a PD would not be able to ascertain the available amount of power based on the number of classification events produced by the PSE.

Editor's Note: The above paragraph needs more study.

The PSE may manage the allocation of power based on additional information beyond the classification of the attached PD. Allocating power based on additional information about the attached PD, and the mechanism for obtaining that additional information, is beyond the scope of this standard with the exception that the allocation of power shall not be based solely on the historical data of the power consumption of the attached PD.

See 33.6 for a description of Data Link Layer classification.

See Annex 33C for more information on how Autoclass can be used to manage the allocation of power.

If the system implements a power allocation algorithm, no additional behavioral requirement is placed on the system as it approaches or reaches its maximum power subscription. Specifically, the interaction between one PSE PI and another PSE PI in the same system is beyond the scope of this standard.

33.2.9 PSE power removal

Figure 33–10e shows the PSE monitor state diagrams. These state diagrams monitor for inrush current and the absence of the Maintain Power Signature (MPS).

If any of these conditions exist for longer than its related time limit, the power is removed from the PI.

33.2.9.1 PSE Maintain Power Signature (MPS) requirements

Change text in section 33.2.9.1 as follows:

The MPS consists of two components, an AC MPS component and a DC MPS component.

A Type 1 or Type 2 ~~The~~ PSE shall monitor either the DC MPS component, the AC MPS component, or both. A Type 3 or Type 4 PSE shall monitor only the DC MPS component.

33.2.9.1.1 PSE AC MPS component requirements

A PSE that monitors the AC MPS component shall meet the "AC Signal parameters" and "PSE PI voltage during AC disconnect detection" parameters in Table 33–12.

A PSE shall consider the AC MPS component to be present when it detects an AC impedance at the PI equal to or lower than $|Z_{ac1}|$ as defined in Table 33–12.

A PSE shall consider the AC MPS component to be absent when it detects an AC impedance at the PI equal to or greater than $|Z_{ac2}|$ as defined in Table 33–12. Power shall be removed from the PI when AC MPS has been absent for a time duration greater than T_{MPDO}.

A PSE may consider the AC MPS component to be either present or absent when it detects a AC impedance between the values $|Z_{ac1}|$ max and $|Z_{ac2}|$ min.

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Table 33–12—PSE PI parameters for AC disconnect-detection function

Item	Parameter	Symbol	Unit	Min	Max	Additional information
	AC signal parameters					
1a	PI probing AC voltage	V_open	V_{pp}	1.90	10% of the average value of V_{Port_PSE} within the limits of Table 33–11	Includes noise, ripple, etc. V_open is the AC voltage across the PI when the PD is not connected to the PI and before the detection of this condition by the PSE.
		V_open1	V_p		30.0 V, $V_{PSE} \leq$ 44.0 V	V_open1 is the AC voltage across the PI when the PD is not connected to the PI and after the detection of this condition by the PSE and the removal of power from the PI.
1b	AC probing signal frequency	F_p	kHz		0.500	
1c	AC probing signal slew rate	SR	V/µs		0.100	Positive or negative.
	AC source output impedance					
2a	Source output current during the operation of the AC disconnect detection function	I_sac	mA		5.00	During operation of the AC disconnect detection function.
2b	PSE PI impedance during PD detection when measured at the PSE PI	R_rev	kΩ	45.0		Specified in 33.2.5.1 and Figure 33–11. Shown here to clarify the difference in PI impedance during the signature detection function.
	PSE PI voltage during AC disconnect detection					
3a	PI AC voltage when PD is connected	V_{CLOSE}	V_{pp}			See Table 33–11, item 3.
3b	PI voltage when PD is disconnected	V_{PSE}	V_p		60.0	
	AC Maintain Power Signature					
4a	Valid impedance	$\lvert Z_{ac1} \rvert$	kΩ		27.0	F_p = 5 Hz, Testing voltage >2.5 V. See Figure 33–15.
4b	Invalid impedance	$\lvert Z_{ac2} \rvert$	kΩ	1980		See Figure 33–15.

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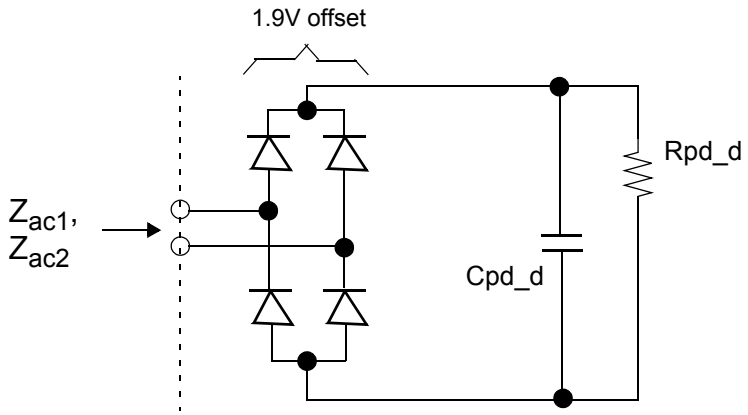

NOTE—Rpd_d and Cpd_d are specified in Table 33–19. Cpd_d may be located either in parallel with Z_{ac1} or as shown above.

Figure 33–15—Z_{ac1} and Z_{ac2} definition as indicated in Table 33–12

33.2.9.1.2 PSE DC MPS component requirements

Change text in section 33.2.9.1.2 as follows:

A PSE shall consider the DC MPS component to be present if $I_{Port\text{-}2P}$ or the sum of $I_{port\text{-}2P}$ of both pairs of the same polarity is greater than or equal to I_{Hold} max for a minimum of T_{MPS}. A PSE shall consider the DC MPS component to be absent if $I_{Port\text{-}2P}$ or the sum of $I_{port\text{-}2P}$ of both pairs of the same polarity is less than or equal to I_{Hold} min. A PSE may consider the DC MPS component to be either present or absent if $I_{Port\text{-}2P}$ or the sum of $I_{port\text{-}2P}$ of both pairs of the same polarity is in the range of I_{Hold}.

The values of $I_{Port\text{-}2P}$ or the sum of $I_{port\text{-}2P}$ of both pairs of the same polarity and the corresponding values of I_{Hold} shall meet the conditions specified in Table 33–11.

A Type 3 or Type 4 PSE, ~~when connected to a single-signature PD,~~ shall monitor either the sum of $I_{port\text{-}2P}$ of both pairs of the same polarity or the pairset with the highest $I_{Port\text{-}2P}$ current value and use the appropriate I_{Hold} level shown in Table 33–11. Power shall be removed from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.

~~A Type 3 or Type 4 PSE, when connected to a dual-signature PD shall monitor each pairset and use the appropriate I_{Hold} level shown in Table 33–11. The PSE shall remove power from any pairset on which the DC MPS has been absent for a duration greater than T_{MPDO}.~~

The specification for T_{MPS} in Table 33–11 applies only to the DC MPS component. The PSE shall not remove power from the port when $I_{Port\text{-}2P}$ or the sum of $I_{port\text{-}2P}$ of both pairs of the same polarity is greater than or equal to I_{Hold} max continuously for at least T_{MPS} every $T_{MPS} + T_{MPDO}$, as defined in Table 33–11. This allows a PD to minimize its power consumption.

33.3 Powered devices (PDs)

A PD is the portion of a device that is either drawing power or requesting power by participating in the PD detection algorithm. A device that is capable of becoming a powered device may or may not have the ability to draw power from an alternate power source and, if doing so, may or may not require power from the PI. PD capable devices that are neither drawing nor requesting power are also covered in this subclause.

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A PD is specified at the point of the physical connection to the cabling. Characteristics such as the losses due to voltage correction circuits, power supply inefficiencies, separation of internal circuits from external ground or other characteristics induced by circuits after the PI connector are not specified. Limits defined for the PD are specified at the PI, not at any point internal to the PD, unless specifically stated.

33.3.1 PD PI

Change first paragraph of section 33.3.1 as follows:

~~The~~ Type 1 and Type 2 PDs shall be capable of accepting power on either of two pairsets ~~of PI conductors~~ and may accept power on both pairsets. Type 3 and Type 4 PDs shall be capable of accepting power on either pairset and shall be capable of accepting power on both pairsets. The two ~~conductor sets~~pairsets are named Mode A and Mode B. In each four-wire connection, the two wires associated with a pair are at the same nominal average voltage. Figure 33–8 in conjunction with Table 33–13 illustrates the two power modes.

Table 33–13—PD pinout

Conductor	Mode A	Mode B
1	Positive V_{PD}, Negative V_{PD}	
2	Positive V_{PD}, Negative V_{PD}	
3	Negative V_{PD}, Positive V_{PD}	
4		Positive V_{PD}, Negative V_{PD}
5		Positive V_{PD}, Negative V_{PD}
6	Negative V_{PD}, Positive V_{PD}	
7		Negative V_{PD}, Positive V_{PD}
8		Negative V_{PD}, Positive V_{PD}

The PD shall be implemented to be insensitive to the polarity of the power supply and shall be able to operate per the PD Mode A column and the PD Mode B column in Table 33–13.

Change the note as follows:

NOTE—PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that are not implemented to be insensitive to polarity, are specifically not allowed by this standard.~~PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this standard.~~

The PD shall not source power on its PI.

The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage.

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Replace section 33.3.2 as follows:

33.3.2 PD Type descriptions

PDs can be categorized as either Type 1, Type 2, Type 3, or Type 4. ~~PDs can be constructed as single-signature or dual-signature as defined in 1.4 and 33.2.5.0a.~~ Table 33–13a shows the permissible PD Types along with supported parameters.

Table 33–13a—Permissible PD Types

PD Type	Single- or dual-signature	PD Class	4-pair Capable	Low MPS support[1]	Physical Layer Classification	Data Link Layer Classification	Other Optional Capbilities
Type 1		0-3	Optional	No	Single-Event	Optional	
Type 2		4	Optional	No	Multiple Event	Mandatory	
Type 3	Single	1-6	Mandatory	Yes[2]	Multiple Event	Mandatory[3]	Autoclass
	~~Dual~~	~~1-4~~	~~Mandatory~~	~~Yes[2]~~	~~Multiple Event~~	~~Mandatory~~	~~Autoclass~~
Type 4	Single	7-8	Mandatory	Yes[2]	Multiple Event	Mandatory	Autoclass
	Dual	~~5~~	~~Mandatory~~	~~Yes[2]~~	~~Multiple Event~~	~~Mandatory~~	~~Autoclass~~

[1] - See 33.3.8 for details. “Low” means lower standby MPS power, “high” means higher standby MPS power.
[2] - Need to support High MPS when connected to Type 1 or Type 2 PSEs for backward compatibility.
[3] - Type 3/SS Class 1-3 PDs are not required to implement DLL classification.

Editor’s Note: Classification section to be updated to move all Type 3 and Type 4 PSEs to multiple-event (Mark is considered an event).

Type 1 PDs implement a minimum of Single-Event Physical Layer classification and advertise a Single-Event class signature of 0, 1, 2, or 3. Class 0 is only permitted for Type 1 PDs.

Type 2 PDs implement both Multiple-Event Physical Layer classification (see 33.3.5.2) and Data Link Layer classification (see 33.6) and advertise a Multiple-Event class signature of 4 during all class events.

Type 3 ~~single-signature~~ PDs operating up to a maximum power draw corresponding to Class 3 or less implement a minimum of Multiple-Event Physical Layer Classification and advertise a Single-Event class signature of 1, 2, or 3.

~~Single-signature~~ Type 3 and Type 4 PDs operating with a maximum power draw corresponding to Class 4 or greater implement both Multiple-Event Physical Layer classification (see 33.3.5.2) and Data Link Layer classification (see 33.6). Such Type 3 PDs advertise a class signature of 4, 5, or 6, while Type 4 PDs advertise a class signature of 7 or 8.

~~Dual-signature Type 3 and Type 4 PDs implement a minimum of Multiple-Event Physical Layer classification and Data Link Layer Classification (see 33.6). Type 3 dual-signature PDs advertise a class signature of 1, 2, 3, or 4 on each pairset, while Type 4 dual-signature PDs advertise a class signature of 5 on at least one pairset.~~

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Type 4 ~~single-signature~~ PDs only advertise Class 7 and 8. ~~Type 4 dual-signature PDs advertise Class 5 on at least one pairset.~~

A Type 2, Type 3 or Type 4 PD that does not successfully observe a Multiple-Event Physical Layer classification or Data Link Layer classification shall conform to Type 1 PD power restrictions and shall provide the user with an active indication if underpowered. The method of active indication is left to the implementer.

Type 2, Type 3 and Type 4 PDs implementing 100BASE-TX (Clause 25) PHYs shall meet the requirements of 25.4.5 in the presence of (I_{unb} / 2).

Note - For PDs implementing both Clause 25 and Clause 33, this adds the unbalance current to the requirements in Clause 25.

Editor's Note: Need to move two normative requirements from section 33.3.2.

33.3.3 PD state diagram

The PD state diagram specifies the externally observable behavior of a PD. The PD shall provide the behavior of the state diagram shown in Figure 33–16.

~~*Editor's Note: To review state machine that clearly specify behavior of single signature and dual signature PDs regarding the detection , classification, powerup and power on requirements for each pairset/mode.*~~

33.3.3.1 Conventions

The notation used in the state diagram follows the conventions of state diagrams as described in 21.5.

33.3.3.2 Constants

The PD state diagram uses the following constants:

V_{Reset_th}
: Reset voltage threshold (see Table 33–17)

V_{Mark_th}
: Mark event voltage threshold (see Table 33–17)

class_sig
: PD classification, one of either 0, 1, 2, 3, or 4 (see Table 33–16)

33.3.3.3 Variables

The PD state diagram uses the following variables:

mdi_power_required
: A control variable indicating the PD is enabled and should request power from the PSE by applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. A variable that is set in an implementation-dependent manner.
Values:FALSE:PD functionality is disabled.
TRUE:PD functionality is enabled.

Change variable pd_2-event as follows:

pd_multi~~2~~-event
: A control variable indicating whether the PD presents a ~~2~~Multiple-Event class signature.

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Values:FALSE:PD does not present a ~~2~~Multiple-Event class signature.
TRUE:PD does present a ~~2~~Multiple-Event class signature.

pd_dll_capable

This variable indicates whether the PD implements Data Link Layer classification.

Values:FALSE:The PD does not implement Data Link Layer classification.
TRUE:The PD does implement Data Link Layer classification.

pd_dll_enabled

A variable indicating whether the Data Link Layer classification mechanism is enabled.

Values:FALSE:Data Link Layer classification is not enabled.
TRUE:Data Link Layer classification is enabled.

Change variable pd_max_power as follows:

pd_max_power

A control variable indicating the max power that the PD may draw from the PSE. See power classifications in Table 33–18.

Values:0: PD may draw Class 0 power
1: PD may draw Class 1 power
2: PD may draw Class 2 power
3: PD may draw Class 3 power
4: PD may draw Class 4 power
5: PD may draw Class 5 power
6: PD may draw Class 6 power
7: PD may draw Class 7 power
8: PD may draw Class 8 power

pd_reset

An implementation-specific control variable that unconditionally resets the PD state diagram to the OFFLINE state.

Values:FALSE:The device has not been reset (default).
TRUE:The device has been reset.

power_received

An indication from the circuitry that power is present on the PD's PI.

Values:FALSE:The input voltage does not meet the requirements of V_{Port_PD} in Table 33–18.
TRUE:The input voltage meets the requirements of V_{Port_PD}.

Change variable present_class_sig as follows:

present_class_sig_A

Controls presenting the classification signature that is used during first two class events (see 33.3.5) by the PD.

Values:FALSE:The PD classification signature is not to be applied to the link.
TRUE:The PD classification signature is to be applied to the link.

Insert the new parameter present_class_sig_B after present_class_sig_A as follows:

present_class_sig_B

Controls presenting the classification signature that is used during the third class event and all subsequent class events (see 33.3.5) by the PD.

Values:FALSE:The PD classification signature is not to be applied to the link.
TRUE:The PD classification signature is to be applied to the link.

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Change the parameter present_det_sig as follows:

present_det_sig
Controls presenting the detection signature (see 33.3.4) by the PD.
Values:FALSE:A non-valid PD detection signature is to be applied to the link.
TRUE:A valid PD detection signature is to be applied to the link over each pairset.
present_mark_sig
Controls presenting the mark event current and impedance (see 33.3.5.2.1) by the PD.
Values:FALSE:The PD does not present mark event behavior.
TRUE:The PD does present mark event behavior.
present_mps
Controls applying MPS (see) to the PD's PI.
Values:FALSE:The Maintain Power Signature (MPS) is not to be applied to the PD's PI.
TRUE:The MPS is to be applied to the PD's PI.

Change variable pse_dll_power_type as follows:

pse_dll_power_level~~type~~
A control variable output by the PD power control state diagram (Figure 33–28) that indicates the ~~type~~ power level of the PSE by which the PD is being powered.
Values:1: The PSE ~~is~~ has allocated Class 3 power or less ~~a Type 1 PSE~~ (default).
2: The PSE ~~is~~ has allocated Class 4 power.~~a Type 2 PSE.~~
3: The PSE has allocated Class 5 or Class 6 power.
4: The PSE has allocated Class 7 or Class 8 power.

Change variable pse_power_type as follows:

pse_power_level~~type~~
A control variable that indicates to the PD the level of power the PSE is supplying.~~the type of PSE by which it is being powered.~~
Values:1: The PSE ~~is~~ has allocated the PD's requested power or Class 3 power, whichever is less ~~a Type 1 PSE~~.
2: The PSE ~~is~~ has allocated the PD's requested power or Class 4 power, whichever is less ~~a Type 2 PSE~~.
3: The PSE has allocated the PD's requested power or Class 6 power, whichever is less.
4: The PSE has allocated the PD's requested power or Class 8 power, whichever is less.

V_{PD}
Voltage at the PD PI as defined in 1.4.422.

33.3.3.4 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where "stop x_timer" is asserted.

Change the timer tpowerdly_timer as follows:

tpowerdly_timer
A timer used to prevent the Type 2, 3, or 4 PD from drawing more than inrush current during the PSE's inrush period; see $T_{delay\text{-}2P}$ in Table 33–18.

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Insert 33.3.3.4a after 33.3.3.4 as follows:

33.3.3.4a Functions

do_class_timing

This function is used by a Type 3 or Type 4 PD to evaluate the Type of PSE connected to the link by measuring the length of the classification event. The classification event timing requirements are defined in Table 33–17. This function returns the following variable:

short_mps: A control variable that indicates to the PD the Type of PSE to which it is connected. This variable is used to indicate which MPS timing requirements (see 33.3.8) the PD should use.
Values: TRUE: The PSE uses Type 3, 4 MPS requirements.
FALSE: The PSE uses Type 1, 2 MPS requirements.

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Change State diagram in section 33.3.3.5 as follows:

33.3.3.5 State diagrams

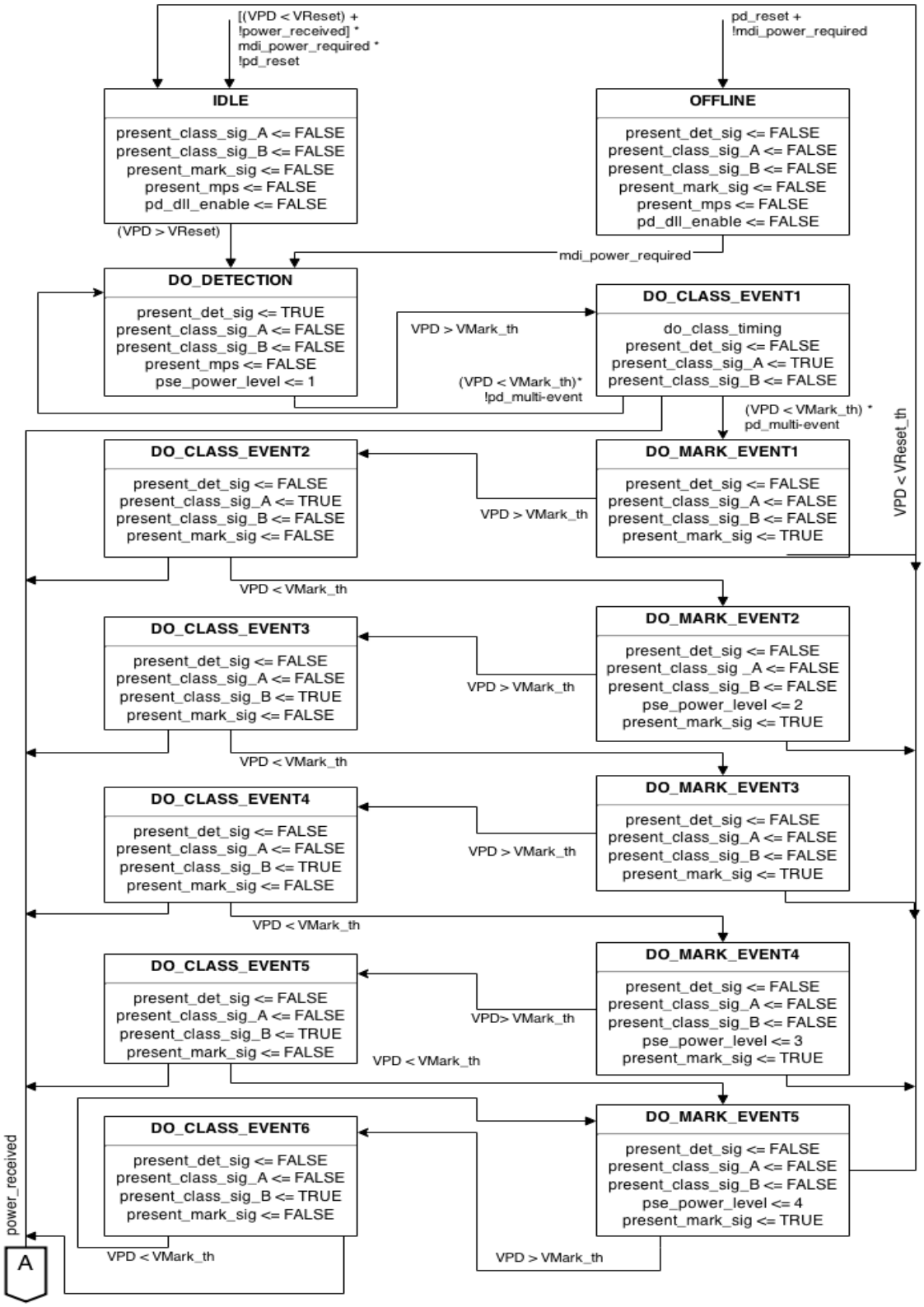

Figure 33–16—PD state diagram

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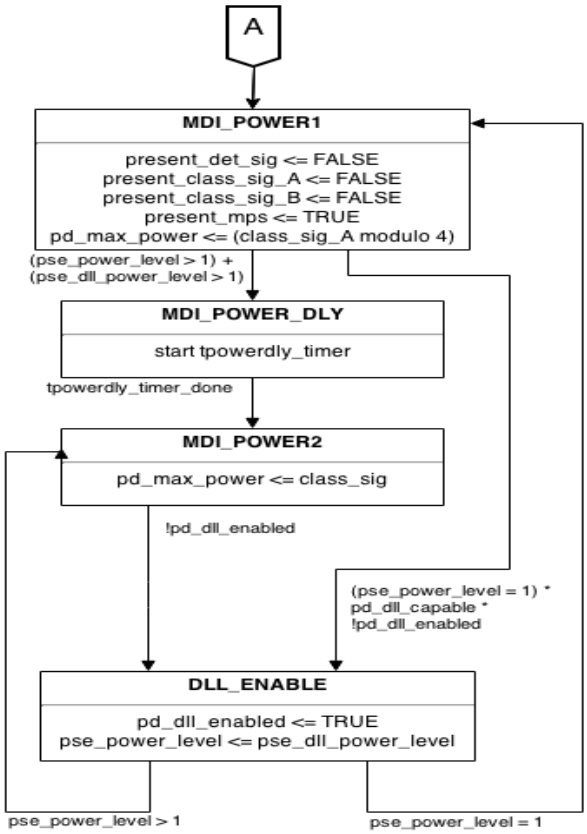

Figure 33–16—PD state diagram (*continued*)

Editor's Note: PD state diagram needs to be updated for Autoclass and detecting long first class events.

Change Note 1 as follows:

NOTE 1—DO_CLASS_EVENT6 ~~3~~ creates a defined behavior for a Type 2, Type 3 and Type 4 PD that is brought into the classification range repeatedly.

NOTE 2—In general, there is no requirement for a PD to respond with a valid classification signature for any DO_CLASS_EVENT duration less than T_{class}.

33.3.4 PD valid and non-valid detection signatures

Change text in section 33.3.4 as follows:

A PD presents a valid detection signature while it is in a state where it accepts power via the PI, but is not powered via the PI per Figure 33–16.

A PD presents a non-valid detection signature at the PI while it is in a state where it does not accept power via the PI per Figure 33–16.

A Type 2 PD presents a non-valid detection signature when in a mark event state per Figure 33–16.

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When a PD presents a valid or non-valid detection signature, it shall present the detection signature at the PI between Positive V_{PD} and Negative V_{PD} of PD Mode A and PD Mode B as defined in 33.3.1. ~~When a~~ A Type 1, Type 2, ~~or single-signature~~ Type 3 or Type 4 PD that is powered over only one pairset ~~becomes powered via the PI, it~~ shall present a non-valid detection signature on the ~~set of pairs from which it is not drawing power~~ unpowered pairset. ~~A Type 3 or Type 4 dual-signature PD that is powered over only one pairset shall present a valid detection signature on the unpowered pairset.~~

Any PD may indicate the ability to accept power on both pairsets using TLV variable PD 4P-ID in Table 79–6b or other (TBD) means.

Editor's Note: The above sentence requires further study based on the outcome of the 4PID work.

A PD may or may not present a valid detection signature when in the IDLE state.

The detection signature is a resistance calculated from two voltage/current measurements made during the detection process as defined in Equation (33–8).

$$R_{\text{detect}} = \left\{ \frac{(V_2 - V_1)}{(I_2 - I_1)} \right\}_{\Omega} \qquad (33\text{–}8)$$

where

V_1 and V_2 are the first and second voltage measurements made at the PD PI, respectively

I_1 and I_2 are the first and second current measurements made at the PD PI, respectively

R_{detect} is the effective resistance

A valid PD detection signature shall have the characteristics of Table 33–14.

A non-valid detection signature shall have one or both of the characteristics in Table 33–15.

Change Table 33-14 and 33-15 as follows:

A PD that presents a signature outside of Table 33–14 is non-compliant, while a PD that present the signature of Table 33–15 is assured to fail detection.

Table 33–14—Valid PD detection signature characteristics, measured at PD ~~input connector~~PI

Parameter	Conditions	Minimum	Maximum	Unit
R_{detect} (at any 1 V or greater chord within the voltage range conditions)	2.70 V to 10.1 V	23.7	26.3	kΩ
V_{offset}	See Figure 33–17	0	1.90	V
Voltage at the PI	I_{Port} = 124 µA	2.70		V
Input capacitance	2.70 V to 10.1 V	0.050	0.120	µF
Series input inductance	2.70 V to 10.1 V		0.100	mH

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Table 33–15—Non-valid PD detection signature characteristics, measured at PD ~~input connector~~PI

Parameter	Conditions	Range of values	Unit
R_{detect}	V_{PD} < 10.1 V	Either greater than 45.0 or less than 12.0	kΩ
Input capacitance	V_{PD} < 10.1 V	Greater than 10.0	µF

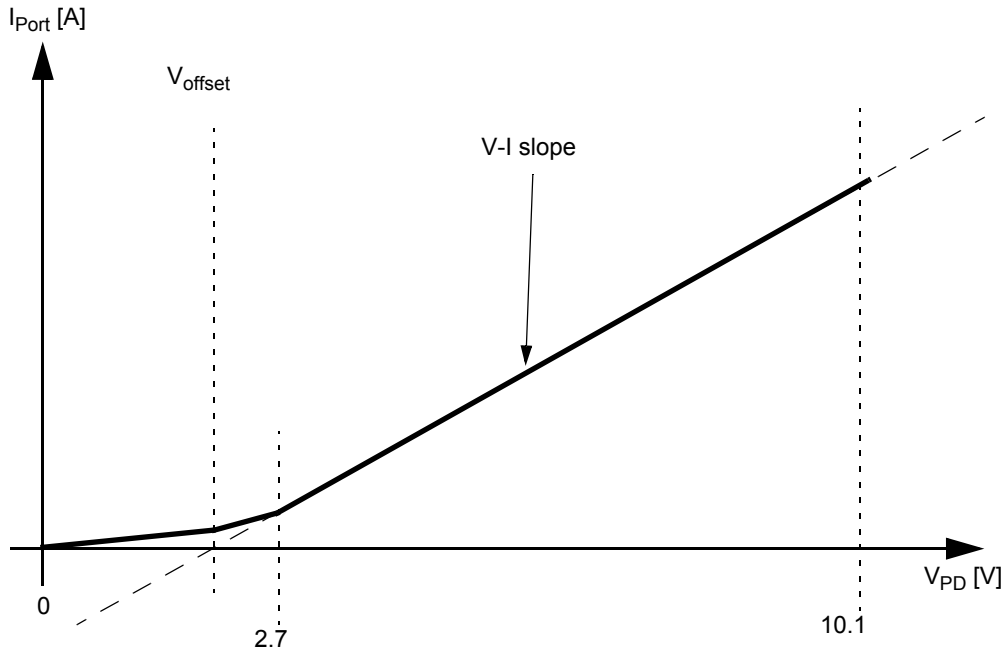

Figure 33–17—Valid PD detection signature offset

33.3.5 PD classifications

Change text in section 33.3.5 as follows:

See 33.2.6 for a general description of classification mechanisms.

The Physical Layer classification of the PD is the maximum power that a Type 1 or Type 2 PD draws across all input voltages and operational modes. The advertised Class during Physical Layer classification of the PD is the maximum power that a Type 3 or Type 4 PD shall draw across all input voltages and operational modes.

A PD may be classified by the PSE based on the Physical Layer classification information, Data Link Layer (DLL) classification, or a combination of both provided by the PD. The intent of PD classification is to provide information about the maximum power required by the PD during operation. Additionally, classification is used to establish mutual identification between Type 2, Type 3 and Type 4 PSEs and Type 2, Type 3 and Type 4 PDs.

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The method of classification depends on the Type of the PD and the Type of the attached PSE.

~~A PD shall meet at least one of the allowable classification permutations listed in Table 33–8~~.
A PD shall meet at least one of the allowed classification configurations listed in Table 33–15a.

A Type 1 PD may implement any of the class signatures in 33.3.5 and 33.6.

Insert new table 33-15a as follows:

Table 33–15a—PD Classification configurations

Type 1 PD		
Physical Layer	**No DLL**	**DLL**
Multiple-Event	Valid	Valid
Single-Event	Valid	Valid
None	Invalid	Invalid
Type 2 PD		
Physical Layer	**No DLL**	**DLL**
Multiple-Event	Invalid	Valid
Single-Event	Invalid	Invalid
None	Invalid	Invalid
Type 3, Type 4 PD		
Physical Layer	**No DLL**	**DLL**
Multiple-Event	Invalid[1]	Valid
Single-Event	Invalid	Invalid
None	Invalid	Invalid

[1]~~Single-signature~~ PDs not capable of drawing more than Class 3 power levels may omit Data Link Layer classification (see 33.6).

Type 2, Type 3, and Type 4 PDs at Class 4 or greater power levels shall implement both ~~2~~Multiple-Event class signature (see 33.3.5.2) and Data Link Layer classification (see 33.6).

PD classification behavior conforms to the state diagram in Figure 33–16.

Change title of and text in Section 33.3.5.1 and Table 33-16 as follows:

33.3.5.1 PD ~~1 Event~~Single-Event class signature

Class 0 is the default for Type 1 PDs. However, to improve power management at the PSE, a Type 1 PD may opt to provide a signature for Class 1 to 3.

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~~The PD is classified based on power. The Physical Layer classification of the PD is the maximum power that the PD draws across all input voltages and operational modes.~~

PDs implementing a ~~2~~Multiple-Event class signature shall return ~~Class 4~~ class_sig_A in accordance with the maximum power draw, P_{Class_PD}, as specified in ~~Table 33–18~~ Table 33–16a and the responses specified in Table 33–16a. Type 3 PDs operating with a maximum power draw corresponding to Class 1-3 respond to Single-Event classification by returning a Class signature 1, 2, or 3 in accordance with the maximum power draw, P_{Class_PD}. Since ~~1-Event~~Single-Event classification is a subset of ~~2~~Multiple-Event classification, Type 2, Type 3, and Type 4 PDs operating with a maximum power draw corresponding to Class 4 or higher, respond to ~~1-Event~~Single-Event classification with a Class 4 signature. Type 1 PDs may choose to implement a ~~2~~Multiple-Event class signature and return Class 0, 1, 2, or 3 in accordance with the maximum power draw, P_{Class_PD}. The Type 2, Type 3 and Type 4 PD's classification behavior shall conform to the electrical specifications defined by Table 33–17.

In addition to a valid detection signature, PDs shall provide the characteristics of a classification signature as specified in Table 33–16. ~~A~~ Type 1 and Type 2 PDs shall present one, and only one, classification signature during classification.

Change Table 33-16 as follows:

Table 33–16—Classification signature, measured at the PD ~~input connector~~PI

Parameter	Conditions	Minimum	Maximum	Unit
Current for class signature 0	14.5 V to 20.5 V	0	4.00	mA
Current for class signature 0 (Type 3)	14.5 V to 20.5 V	1.00	4.00	
Current for class signature 1	14.5 V to 20.5 V	9.00	12.0	
Current for class signature 2	14.5 V to 20.5 V	17.0	20.0	
Current for class signature 3	14.5 V to 20.5 V	26.0	30.0	
Current for class signature 4	14.5 V to 20.5 V	36.0	44.0	

Change title and text of Section 33.3.5.2 as follows:

33.3.5.2 PD ~~2~~Multiple-Event class signature

PDs implementing ~~a 2~~Multiple-Event Physical Layer classification shall present class_sig_A during DO_CLASS_EVENT1 and DO_CLASS_EVENT2 and class_sig_B during DO_CLASS_EVENT3, DO_CLASS_EVENT4, DO_CLASS_EVENT5 and DO_CLASS_EVENT6, as defined in Table 33–16a. ~~class signature shall return a Class 4 classification signature in accordance with the maximum power draw, P_{Class_PD}, as specified by Table 33–18.~~

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Insert table 33-16a as follows:

Table 33–16a—Physical Layer Classifications and Multiple Event Responses

PD Type	PD Signature	Class	class_sig_A	class_sig_B	P_{Class_PD} (W)
1		0	0	0	13.0
		1	1	1	3.84
		2	2	2	6.49
		3	3	3	13.0
2		4	4	4	25.5
3	Single-signature	1	1	1	3.84
		2	2	2	6.49
		3	3	3	13.0
		4	4	4	25.5
		5	4	0	40.0
		6	4	1	51.0
	~~Dual-signature~~	~~1~~	~~1~~	~~0~~	~~3.84~~
		~~2~~	~~2~~	~~0~~	~~6.49~~
		~~3~~	~~3~~	~~0~~	~~13.0~~
		~~4~~	~~4~~	~~0~~	~~25.5~~
4	Single-signature	7	4	2	62.0
		8	4	3	71.0
	~~Dual-signature~~	~~5~~	~~4~~	~~3~~	~~35.5~~

The PD's classification behavior shall conform to the electrical specifications defined by Table 33–17.

Until successful ~~2~~Multiple-Event Physical Layer classification or Data Link Layer classification has completed, a Type 2, Type 3 and Type 4 PD's pse_power_level~~type~~ state variable is set to '1'. ~~A~~ Type 2, Type 3 and Type 4 PDs shall conform to the electrical requirements as defined by Table 33–18 for the level ~~type~~ defined in the pse_power_level~~type~~ state variable.

~~Dual-signature PDs shall advertise a class signature of 1, 2, 3, 4, or 5 on each pairset. The Class advertised on each pairset is the power requested by the PD on that pairset. Dual-signature PDs may advertise a different class signature on each pairset. It is not recommended to use different class signatures if the dual-signature PD powers a single electrical load.~~

Type 3 and Type 4 PDs may determine if the PSE they are connected to supports low MPS by measuring the length of the first class event. The default value for short_mps is FALSE. If it chooses to implement low MPS, a PD may set short_mps to TRUE if the first class finger is longer than T_{LCF_PD} min and shall set short_mps to TRUE if the first class finger is longer than T_{LCF_PD} max.

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NOTE : See Table 33–16 for definition of class signatures 1-4.

Table 33–17—~~2~~Multiple-Event Physical Layer classification electrical requirements

Item	Parameter	Symbol	Units	Min	Max	Additional information
1	Class event voltage	V_{Class}	V	14.5	20.5	
2	Mark event voltage	V_{Mark}	V	6.90	10.1	
3	Mark event current	I_{Mark}	mA	0.250	4.00	See 33.3.5.2.1
4	Mark event threshold	V_{Mark_th}	V	10.1	14.5	See 33.3.5.2.1
5	Classification reset threshold	V_{Reset_th}	V	2.81	6.90	See 33.3.5.2.1
6	Classification reset voltage	V_{Reset}	V	0	2.81	See 33.3.5.2.1
7	Long first class event timing	T_{LCF_PD}	ms	75.5	87.5	See 33.3.8

33.3.5.2.1 Mark Event behavior

Change text in section 33.3.5.2.1 as follows:

When the PD is presenting a mark event signature as shown in the state diagram of Figure 33–16, the PD shall draw I_{Mark} as defined in Table 33–17 and present a non-valid detection signature as defined in Table 33–15.

The PD shall not exceed the I_{Mark} current limits when voltage at the PI enters the V_{Mark} specification as defined in Table 33–17.

V_{Mark_th} is the PI voltage threshold at which the PD implementing ~~2~~Multiple-Event class signature transitions into and out of the DO_CLASS_EVENT1, ~~or~~ DO_CLASS_EVENT2, DO_CLASS_EVENT3, DO_CLASS_EVENT4, DO_CLASS_EVENT5 or DO_CLASS_EVENT6 states as shown in Figure 33–16.

The PD shall draw I_{Mark} until the PD transitions from a DO_MARK_EVENT state to the IDLE state.

V_{Reset_th} is the PI voltage threshold at which the PD implementing ~~2~~Multiple-Event class signature transitions from a DO_MARK_EVENT state to the IDLE state as shown in Figure 33–16.

Insert the new section 33.3.5.3 after Section 33.3.5.2.1 as follows:

33.3.5.3 Autoclass

Type 3 and Type 4 PDs may choose to implement an extension of Physical Layer classification known as Autoclass. The purpose of Autoclass is to allow the PSE to determine the actual maximum power draw of the connected PD. See Annex 33C for more information on Autoclass.

A PD implementing Autoclass shall respond to Physical Layer classification as specified in 33.3.5.1 and 33.3.5.2 with the exception that the PD shall change its current during the first class event to class signature '0' no earlier than T_{ACS} min and no later than T_{ACS} max (as defined in Table 33–17a).

After power up, a PD implementing Autoclass shall draw its highest required power, subject to the requirements on P_{Class_PD} in 33.3.7.2, throughout the period bounded by T_{AUTO_PD1} and T_{AUTO_PD2}, measured

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from when V_{Port_PD} rises above V_{Port_PD} min. The PD shall not draw more power than the power consumed during the time from T_{AUTO_PD1} to T_{AUTO_PD2} (as defined in Table 33–17a) at any point until V_{Port_PD} falls below $V_{Reset_th,}$ unless the PD successfully negotiates a higher power level, up to the advertised Physical Layer classification, through Data Link Layer classification as defined in section 33.6.

Table 33–17a—Autoclass PD timing requirements

Item	Parameter	Symbol	Units	Min	Max	Additional Information
1	Autoclass signature timing	T_{ACS}	ms	75.5	87.5	Measured from transition to state DO_CLASS_EVENT_1
2	Autoclass power draw start time	T_{AUTO_PD1}	s		1.35	Measured from when V_{Port_PD} rises above V_{Port_PD} min
3	Autoclass power draw end time	T_{AUTO_PD2}	s	3.65		Measured from when V_{Port_PD} rises above V_{Port_PD} min

33.3.6 PSE Type identification

Change the text of section 33.3.6 as follows:

~~A Type 2 PD shall identify the PSE Type as either Type 1 or Type 2 (see Figure 33–16).~~

A PD shall identify a PSE Type as a Type lower or equal to its own Type.

A PD connected to a higher PSE Type than its own may identify that PSE as its own Type.

The default value of pse_power_level~~type~~ is 1. After a successful ~~2~~Multiple-Event Physical Layer classification has completed the pse_power_level is set to either 1, 2, 3, or 4.~~or~~ After a successful Data Link Layer classification has completed, the pse_power_level~~type~~ is set to either 1, 2, 3 or 4.

The PD resets the pse_power_level~~type~~ to '1' when the PD enters the DO_DETECTION state.

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33.3.7 PD power

The power supply of the PD shall operate within the characteristics in Table 33–18.

The PD may be capable of drawing power from a local power source. When a local power source is provided, the PD may draw some, none, or all of its power from the PI.

~~*Editor's Note (to be removed prior to D2.0): All PD power text should be reviewed with regards to DS PDs.*~~

Change Table 33-18 as follows:

Table 33–18—PD power supply limits

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
1	Input voltage per pairset						
	Class 1	V_{Port_PD-2P}	V	42.1 ~~37.0~~	57.0	1, 3	See 33.3.7.1, Table 33–1
	Class 2			40.8 ~~42.5~~		1, 3	
	Class 0, 3			37.0		1, 3	
	Class 4			42.5		2, 3	
	Class 5, ~~single-signature PD~~			44.3		3	
	~~Class 5, dual-signature PD~~			~~41.2~~		~~4~~	
	Class 6			42.5		3	
	Class 7			42.9		4	
	Class 8			41.2		4	
2	Transient operating input voltage per pairset	V_{Tran_lo-2P}	V	36.0		2, 3, 4	For time duration defined in 33.2.7.2
3	Input voltage range per pairset during overload	$V_{Overload-2P}$	V	36.0	57.0	1	See 33.3.7.4, Table 33–1
				41.4	57.0	2, 3	
				39.5	57.0	4	
4	Input average power, ~~Class 0 and Class 3~~	P_{Port_PD} ~~P_{Class_PD}~~	W		P_{Class_PD}[1] ~~13.0~~	1, 2, 3, 4	See 33.3.7.2, Table 33–1, Table 33–16a
	~~Input average power, Class 1~~				~~3.84~~	~~1~~	
	~~Input average power, Class 2~~				~~6.49~~	~~1~~	
	~~Input average power, Class 4~~				~~25.5~~	~~2~~	
5	~~Input inrush current~~	~~I_{Inrush_PD}~~	~~A~~		~~0.400~~	~~1, 2~~	~~Peak value See 33.3.7.3~~

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Table 33–18—PD power supply limits *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
5	Input inrush current	I_{Inrush_PD}	A		0.400	All	Peak value—See 33.3.7.3. For ~~single-signature~~ PD Class 0-4.
	Input inrush current per pair-set	I_{Inrush_PD-2P}			0.400		~~For dual-signature PDs with different class over each pair-set, this requirement applies over each pairset.~~
5a	Total inrush current	I_{Inrush_PD}	A		0.400	3, 4	Peak value—See 33.3.7.3. ~~Single-signature~~ PDs Class 5-6. ~~Dual-signature PDs with the same Class.~~
5b	Total inrush current	I_{Inrush_PD-2P}	A		0.300/TBD	3, 4	Peak value—See 33.3.7.3. ~~Single-signature~~ PDs Class 5-6. ~~Dual-signature PDs with the same class.~~
5c	Total inrush current	I_{Inrush_PD}	A		0.800	4	Peak value—See 33.3.7.3. ~~Single-signature~~ PDs Class 7-8. ~~Dual Signature PDs with the same class.~~
5d	Input inrush current per pair-set	I_{Inrush_PD-2P}	A		0.600	4	Peak value see 33.3.7.3. ~~Single-signature~~ PDs Class 7-8. ~~Dual-signature PDs with the same class~~.
6	Inrush to operating state delay	T_{delay}	s	0.080		2, 3, 4	See 33.3.7.3 ~~Single-signature PDs only~~
~~6a~~	~~Inrush to operating state~~ delay per pairset	~~T_{delay_2P}~~	s	0.080		3, 4	Dual-signature PDs only

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Table 33–18—PD power supply limits *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
7	Peak operating power						
	Class 0 and Class 3	P_{Peak_PD}	W		14.4	1, 3	See 33.3.7.4
	Class 1				5.00	1, 3	
	Class 2				8.36	1, 3	
	Class 4				1.11 × P_{Class_PD}	2, 3	
	Class 5 to 8				1.05 × P_{Class_PD}	3, 4	
8	Input current transient (absolute value)		mA/µs		4.70	~~1, 2,~~ All	See 33.3.7.5
9	PI capacitance during MDI_POWER states	C_{Port}	µF	5.00		~~1, 2,~~ All	See 33.3.7.6, 33.3.7.3
10	Ripple and noise						
	< 500 Hz		V_{pp} ~~pp~~		0.500	~~1, 2,~~ All	See 33.3.7.7. Balanced source impedance: R_{Ch}
	500 Hz to 150 kHz				0.200		
	150 kHz to 500 kHz				0.150		
	500 kHz to 1 MHz				0.100		
11	~~a)~~ PD Power supply turn on voltage	V_{On_PD}	V		42.0	~~1, 2,~~ All	See 33.3.7.1
	~~b)~~ PD power supply turn off voltage	V_{Off_PD}	V	30.0		~~1, 2,~~ All	
12	PD classification stability time	T_{class}	s		0.005	~~1, 2,~~ All	See 33.3.7.8
13	Backfeed voltage	V_{bfd}	V		2.80	~~1, 2,~~ All	See 33.3.7.9

[1]Class 6 and Class 8 PDs may exceed P_{Class_PD} under certain conditions (see 33.3.7.2)

33.3.7.1 Input voltage

Change text of Section 33.3.7.1 as follows:

The specification for $V_{Port_PD\text{-}2P}$ in Table 33–18 is for the input voltage range after startup (see 33.3.7.3), and accounts for loss in the cabling plant. Note, $V_{PD\text{-}2P} = V_{PSE\text{-}2P} - (R_{Chan} \times I_{Port\text{-}2P})$.

The PD shall turn on at a voltage less than or equal to V_{On_PD}. After the PD turns on, the PD shall stay on over the entire $V_{Port_PD\text{-}2P}$ range. The PD shall turn off at a voltage less than $V_{Port_PD\text{-}2P}$ minimum and greater than or equal to V_{Off_PD}.

The PD shall turn on or off without startup oscillation and within the first trial at any load value when fed by $V_{Port_PSE\text{-}2P}$ min to $V_{Port_PSE\text{-}2P}$ max (as defined in Table 33–11) with a series resistance within the range of R_{Ch} ~~valid Channel Resistance~~.

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33.3.7.2 Input average power

Change text of section 33.3.7.2 as follows:

P_{Class_PD} in Table 33–18 is determined by the Class assigned by the PSE. P_{Class_PD} values for each Class are shown in Table 33–16a. The assigned PSE Class is determined by the number of classification events and the advertised Class by the PD, as shown in Table 33–7, Table 33–7a, and Table 33–7b. The maximum average power, P_{Class_PD} in Table 33–16a and Table 33–18 or PDMaxPowerValue in 33.6.3.3, is calculated over a 1 second interval. PDs may dynamically adjust their maximum required operating power below P_{Class_PD} as described in 33.6. PDs may also adjust their maximum required operating power below P_{Class_PD} by using Autoclass (see 33.3.5.3).

NOTE—Average power is calculated using any sliding window with a width of 1 s.

For Class 6 or Class 8 PDs, P_{Class_PD} is the maximum power the PD shall consume when no additional information is available to the PD regarding actual channel DC resistance. If such a PD has additional information and does not cause the PSE to source more than P_{Class} it may exceed P_{Class_PD}.

33.3.7.2.1 System stability test conditions during startup and steady state operation

When the PD is fed by V_{Port_PSE} min to V_{Port_PSE} max with R_{Ch} (as defined in Table 33–1) in series, P_{Port_PD} shall be defined as shown in Equation (33–9):

$$P_{Port_PD} = \{V_{Port_PD} \times I_{Port}\}_W \quad (33–9)$$

where

P_{Port_PD}	is the average input power at the PD PI
V_{Port_PD}	is the static input voltage at the PD PI
I_{Port}	is the input current, either DC or RMS

NOTE—When connected together as a system, the PSE and PD might exhibit instability at the PSE side, the PD side, or both due to the presence of negative impedance at the PD input. See Annex 33A for PD design guidelines for stable operation.

33.3.7.3 Input inrush current

Replace first paragraph of Section 33.3.7.3 with the following:

Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with V_{port_PD-2P} requirements as defined in Table 33–16a, and ending when C_{Port} has reached a steady state and is charged to 99% of its final value. This period shall be less than $T_{Inrush-2P}$ min per Table 33–11. All PDs shall consume a maximum of Class 3 power for at least $T_{delay-2P}$ min. This allows the PSE to properly complete inrush.

Editor's Note: This paragraph has changed as a result of MR1277. Do not change this paragraph without consulting the request of MR1277.

Change second, third and fourth paragraph of Section 33.3.7.3 as follows:

~~Type 2 PDs with pse_power_type state variable set to 2 prior to power-on shall behave like a Type 1 PD for at least T_{delay} min.~~ $T_{delay-2P}$ for each pairset starts when V_{PD-2P} crosses the PD power supply turn on voltage, V_{On_PD}. This delay is required so that the Type 2, Type 3 and Type 4 PD does not enter a high power state before the PSE has had time to switch current limits on each pairset from $I_{Inrush-2P}$ to I_{LIM-2P}.

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For PDs operating at Class 0 to 6:
Input inrush current at startup is limited by the PSE if C_{Port} per pairset < 180 µF, as specified in Table 33–11. If C_{Port} per pairset ≥ 180 µF, input inrush current shall be limited by the PD so that I_{Inrush_PD} and I_{Inrush_PD-2P} per pairset max is satisfied.

Insert the following paragraphs:

~~For Type 3 and Type 4 PDs operating class 1–5 dual signature PDs:~~
~~Input inrush current at startup is limited by the PSE if C_{Port} per pairset < 180 µF, as specified in Table 33–11. If C_{Port} per pairset ≥180 µF, input inrush current shall be limited by the PD so that I_{Inrush_PD} max and $I_{Inrush-PD-2P}$ max is satisfied.~~

For Type 4 PDs operating class 7 and 8 ~~single signature~~ PDs:
Input inrush current at startup is limited by the PSE if C_{Port} per pairset < 360 µF, as specified in Table 33–11. If C_{Port} per pairset ≥360 µF, input inrush current shall be limited by the PD so that I_{Inrush_PD} max and $I_{Inrush-PD-2P}$ max is satisfied.

Insert the following note at the end of section 33.3.7.3 as follows:

NOTE— PDs may be subjected to PSE POWER_ON current limits during inrush when the PD input voltages reaches 99% of steady state or after $T_{inrush-2P}$ min. See 33.2.7.4 for details.

C_{Port} in Table 33–18 is the total PD input capacitance during POWER_UP and POWER_ON states that a PSE encounters when operating one or both pairsets~~, when connected to a single-signature PD. When a PSE is connected to a dual-signature PD, C_{Port} value requirements are specified in 33.3.7.6.~~ See Figure 33–17a for a simplified PSE-PD C_{Port} interpretation model.

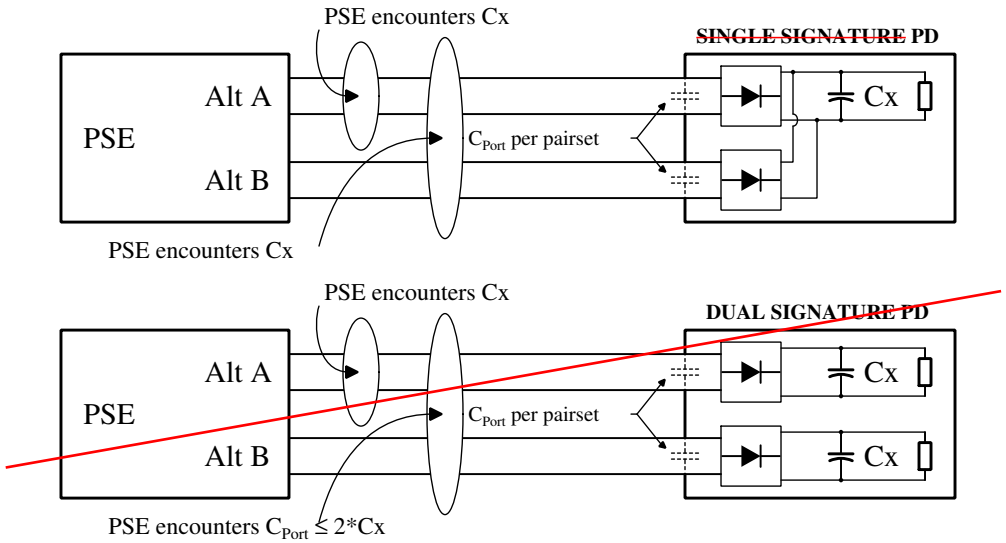

Figure 33–17a—C_{Port} interpretation model

33.3.7.4 Peak operating power

Change text in section 33.3.7.4 as follows:

$V_{Overload-2P}$ is the PD PI voltage when the PD is drawing the permissible P_{Peak_PD}.

At any static voltage at the PI, and any PD operating condition, with the exception of Class 6 or Class 8 PDs when additional channel DC resistance information is available to the PD, the peak power shall not exceed

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P_{Class_PD} max for more than $T_{CUT\text{-}2P}$ min, as defined in Table 33–11 and 5% duty cycle. Peak operating power shall not exceed P_{Peak} max.

For Class 6 and Class 8 PDs, when additional information is available to the PD regarding actual channel DC resistance, in any operating condition with any static voltage at the PI, the peak power shall not exceed P_{Class} at the PSE PI for more than T_{CUT} min, as defined in Table 33–11 and with 5% duty cycle.

Ripple current content (I_{Port_ac}) superimposed on the DC current level (I_{Port_dc}) is allowed if the total input power is less than or equal to P_{Class_PD} max, or P_{Class} at the PSE PI for Class 6 and Class 8 PDs.

The RMS, DC and ripple current shall be bounded by Equation (33–10):

$$I_{Port} = \{\sqrt{(I_{Port_dc})^2 + (I_{Port_ac})^2}\}_A \quad (33\text{–}10)$$

where

I_{Port} is the RMS input current
I_{Port_dc} is the DC component of the input current
I_{Port_ac} is the RMS value of the AC component of the input current

The maximum I_{Port} value for all PDs except those in Class 6 or Class 8, over the operating $V_{Port_PD\text{-}2P}$ range shall be defined by Equation (33–11) ~~the following equation~~:

Replace Equation 33-11 with the following:

$$I_{portmax} = \left\{\frac{P_{Class_PD}}{V_{Port_PD\text{-}2P}}\right\}_A \quad (33\text{–}11)$$

where

$I_{portmax}$ is the maximum DC and RMS input current
$V_{Port_PD\text{-}2P}$ is the ~~static input voltage~~ minimum specified input voltage at ~~the~~ a PD pairset~~PI~~
P_{Class_PD} is the maximum power, P_{Class_PD} max, as defined in Table 33–18

The maximum I_{Port} value for all PDs in Class 6 or Class 8, over the operating $V_{Port_PD\text{-}2P}$ range shall be defined by Equation (33–11a):

Insert new Equation 33-11a as follows:

$$I_{portmax} = \left\{\frac{P_{Class}}{V_{PSE}}\right\}_A \quad (33\text{–}11a)$$

where

$I_{portmax}$ is the maximum RMS input current
P_{Class} is the allocated ~~c~~Class power as defined in 33.2.6 and Equation (33–3)
V_{PSE} is the voltage at the PSE PI as defined in 1.4.426

Peak power, P_{Peak_PD}, for Class 4 is based on Equation (33–12). Peak power, P_{Peak_PD}, for Class 5 through 8 is based on Equation (33–12a). Equation (33–12) and Equation (33–12a) are used to ~~which~~ approximate~~s~~ the ratiometric peak powers of Class 0 through Class 8~~3~~. This equation may be used to calculate peak operating power for P_{Peak_PD} values obtained via Data Link Layer classification or Autoclass.

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$$P_{Peak_PD} = \{1.11 \times P_{Class_PD}\}_W \quad (33–12)$$

$$P_{Peak_PD} = \{1.05 \times P_{Class_PD}\}_W \quad (33–12a)$$

where

P_{Peak_PD} is the peak operating power

P_{Class_PD} is the input average power

NOTE—The duty cycle of the peak current is calculated using any sliding window with a width of 1 s.

33.3.7.5 Peak transient current

Change text in section 33.3.7.5 as follows:

When the input voltage at the PI is static and in the range of V_{Port_PD} defined by Table 33–18, the transient current drawn by ~~the~~ ~~a single-signature~~ PD shall not exceed 4.70 mA/µs in either polarity. ~~A dual-signature PD shall not exceed 4.70 mA/µs in either polarity per pairset under the same conditions.~~ This limitation applies after inrush has completed (33.3.7.3) and before the PD has disconnected.

Under normal operating conditions when there are no transients applied at the PD PI, Class 6 or Class 8 PDs, shall operate below the PD extended template defined in Figure 33–18. PDs of all other Classes ~~the PD~~ shall operate below the PD upperbound template defined in Figure 33–18. See 33.3.7.2 for details on Class 6 and Class 8 PD allowances.

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Replace Figure 33-18 with the following figure:

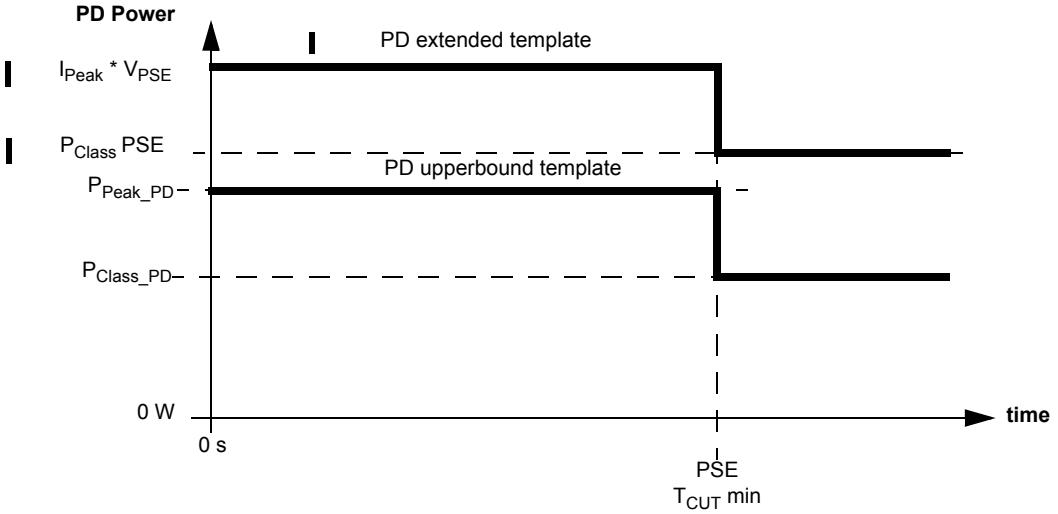

Figure 33–18—PD static operating mask

The PD upperbound template in Figure 33–18, P_{PDUT}, is described by Equation (33–13):

$$P_{\mathrm{PDUT}}(t) = \left\{ \begin{array}{ll} P_{\mathrm{Peak_PD}} & \text{for } (0 \le t < T_{\mathrm{cutmin}}) \\ P_{\mathrm{Class_PD}} & \text{for } (T_{\mathrm{cutmin}} \le t) \end{array} \right\}_{\mathrm{W}} \qquad (33\text{–}13)$$

where

t	is the duration in seconds that the PD sinks I_{Port}
$P_{\mathrm{Peak_PD}}$	is the peak operating power, $P_{\mathrm{Peak_PD}}$ max, as defined in Table 33–18
$P_{\mathrm{Class_PD}}$	is the maximum power, $P_{\mathrm{Class_PD}}$ max, as defined in Table 33–18
T_{cutmin}	is $T_{\mathrm{CUT\text{-}2P}}$ min, as defined in Table 33–11

Insert Equation 33-13a and text after equation 33-13 as follows:

The PD extended template in Figure 33–18, $\mathrm{P_{PDET}}$, is described by Equation (33–13):

$$P_{\mathrm{PDET}}(t) = \left\{ \begin{array}{ll} I_{\mathrm{Peak}} \times V_{PSE} & \text{for } (0 \le t < T_{\mathrm{cutmin}}) \\ P_{\mathrm{Class}} & \text{for } (T_{\mathrm{cutmin}} \le t) \end{array} \right\}_{\mathrm{W}} \qquad (33\text{–}13a)$$

where

t	is the duration in seconds that the PD sinks I_{Port}
I_{Peak}	is the peak operating current, I_{Peak} max, as defined in Equation (33–4)
V_{PSE}	is the voltage at the PSE.
P_{Class}	is the minimum power output by the PSE, as defined in Table 33–7, Table 33–7a and 33.2.6.
T_{cutmin}	is $T_{\mathrm{CUT\text{-}2P}}$ min, as defined in Table 33–11

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During PSE transient conditions in which the voltage at the PI is undergoing dynamic change, the PSE is responsible for limiting the transient current drawn by the PD for at least $T_{LIM\text{-}2P}$ min as defined in Table 33–11.

33.3.7.6 PD behavior during transients at the PSE PI

Change text in section 33.3.7.6 as follows:

Editor's Note: 1. Type 3 and Type 4 to be added (to parts other than the newly added first paragraph).

A PD shall continue to operate without interruption in the presence of transients at the PSE PI as defined in 33.2.7.2. A ~~single-signature PD~~ shall include C_{port} as defined in Table 33–18. ~~A dual-signature PD shall meet this requirement for each pairset.~~

PDs with power draw greater than Class 4 may require extra capacitance to maintain operation during PSE transients. Class 5 and 6 ~~single-signature~~ PDs will meet the requirement with $C_{port} \geq 10\mu F$. ~~Class 5 dual-signature PDs should include these C_{port} values at each pairset.~~ Class 7 and 8 ~~single-signature~~ PDs will meet this requirement with $C_{port} \geq 20\mu F$.

A Type 1 PD with input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. A Type 2 ~~or~~ Type 3 PD with peak power draw that does not exceed P_{Class_PD} max and has an input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. A Type 4 PD with peak power draw that does not exceed P_{Class_PD} max and has an input capacitance of 360µF or less requires no special considerations with regards to transients at the PD PI. PDs that do not meet these requirements shall comply with the following:

a) A Type 1 PD input current shall not exceed the PD upperbound template (see Figure 33–18) after T_{LIM} min (see Table 33–11 for a Type 1 PSE) when the following input voltage is applied. A current limited voltage source is applied to the PI through a R_{Ch} resistance (see Table 33–1). The current limit meets Equation (33–14) and the voltage ramps from V_{Port_PSE} min to V_{Port_PSE} max at 2250 V/s.

A Type 2 or Type 3 PD that demands less than Class 5 power levels shall meet both of the following:

a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33–18) within 4 ms. During this test, the PD PI voltage is driven from ~~50 V~~ $V_{Port_PSE\ min}$ to ~~5~~ $V_{Port_PSE\ min}$ ±2.5 V at greater than 3.5 V/µs, a source impedance ~~of~~within 2.5% of 1.5 Ω, and a source that supports a current greater than 2.5 A.
b) The PD shall not exceed the PD upperbound template beyond T_{LIM} min under worst-case current draw under the following conditions. The input voltage source drives V_{PD} from V_{Port_PSE} min to 56 V at 2250 V/s, the source impedance within 2.5% of~~is~~ R_{Ch} (see Table 33–1), and the voltage source limits the current to MDI $I_{LIM\text{-}2P}$ per Equation (33–14).

Change equation 33-14 as follows:

The current limit per pairset at the MDI (MDI $I_{LIM\text{-}2P}$) is defined by Equation (33–14):

$$\{pse_{\text{ILIM-2P min}}\}_{\text{mA}} < \{mdi_{\text{ILIM-2P}}\}_{\text{mA}} \leq \{pse_{\text{ILIM-2P min}}\}_{\text{mA}} + 5.00_{\text{mA}} \qquad (33\text{–}14)$$

where

$pse_{ILIM\text{-}2Pmin}$ is the PSE $I_{LIM\text{-}2P}$ min as defined in Table 33–11
$mdi_{ILIM\text{-}2P}$ is the per pairset current limit at the MDI (MDI I_{LIM})

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Append the following text to section 33.3.7.6

A Type 3 PD that demands Class 5 power levels shall meet both of the following:

a) The PD mode input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template value (see Figure 33–18) within 4ms. During the test, the voltage of both PD modes is driven from $V_{Port_PSE\ min}$ to $V_{Port_PSE\ min}$ + 2.5 V at greater than 3.5 V/µs, a source impedance within 2.5% of 1.5 Ω, and a source that supports a current greater than 5.0 A.
b) The PD shall not exceed the PD upperbound template beyond T_{LIM} min under worst-case current draw under the following conditions. The input voltage source drives both PD Modes from $V_{Port_PSE\ min}$ to 56 V at 2250 V/µs, the source impedance within 2.5% of R_{Ch} as defined in Table 33–1, and the voltage source limits the current to MDI I_{LIM-2P} per Equation (33–14).

A Type 3 or Type 4 PD that demands more than Class 5 power levels shall meet both of the following:

a) The PD mode input current spike shall not exceed 3.0 A and shall settle below the PD extended template value (see Figure 33–18) within 4 ms. During the test, the voltage of both PD modes is driven from V_{Port_PSE} min to V_{Port_PSE} min + 2.5 V at greater than 3.5 V/µs, a source impedance within 2.5% of 1.5 Ω, and a source that supports a current greater than 5.0 A.
b) The PD shall not exceed the PD upperbound template beyond T_{LIM} min under worst-case current draw under the following conditions. The input voltage source drives both PD Modes from V_{Port_PSE} min to 56 V at 2250 V/µs, the source impedance within 2.5% of R_{Ch} as defined in Table 33–1, and the voltage source limits the current to MDI I_{LIM-2P} per Equation (33–14).

~~*Editor's Note: Type 4 DS PDs need to be considered for following text (as do lower class DS PDs).*~~

33.3.7.7 Ripple and noise

Change first paragraph of Section 33.3.7.7 as follows:

The specification for ripple and noise in Table 33–18 shall be for the common-mode and/or differential pair-to-pair noise at the PD PI generated by the PD circuitry. The ripple and noise specification shall be for all operating voltages in the range of $V_{Port_PD_2P}$, and over the range of input power of the device.

The PD shall operate correctly in the presence of ripple and noise generated by the PSE that appears at the PD PI. These levels are specified in Table 33–11, item 3.

Limits are provided to preserve data integrity. To meet EMI standards, lower values may be needed.

The system designer is advised to assume the worst-case condition in which both PSE and PD generate the maximum noise allowed by Table 33–11 and Table 33–18, which may cause a higher noise level to appear at the PI than the standalone case as specified by this clause.

33.3.7.8 PD classification stability time

Following a valid detection and a rising voltage transition from V_{valid} to V_{Class}, the PD Physical Layer classification signature shall be valid within T_{class} as specified in Table 33–18 and remain valid for the duration of the classification period.

33.3.7.9 Backfeed voltage

When V_{Port_PD} max is applied across the PI at either polarity specified on the conductors for Mode A according to Table 33–13, the voltage measured across the PI for Mode B with a 100 kΩ load resistor connected shall not exceed V_{bfd} max as specified in Table 33–18. When V_{Port_PD} max is applied across the PI

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at either polarity specified on the conductors for Mode B according to Table 33–13, the voltage measured across the PI for Mode A with a 100 kΩ load resistor connected shall not exceed V_{bfd} max.

Insert new section 33.3.7.10 after section 33.3.7.9 as follows:

33.3.7.10 PD PI pair-to-pair resistance and current unbalance

All Class 5 and higher PDs shall not exceed $I_{con\text{-}2P\text{-}unb}$ for longer than $T_{CUT\text{-}2P}$ min as defined in Table 33–11 on any pair. PDs shall meet this requirement when connected to a common source voltage through a resistance of R_{source_min}=0.16 Ω ± 1% and R_{source_max}=0.19 Ω ± 1% to PD PI pairs of the same polarity for all PD operating conditions as shown in Figure 33–18a. R_{source_min} and R_{source_max} represent the V_{in} source impedance that consists of the PSE PI components (R_{PSE_min} and R_{PSE_max} as specified in 33.2.7.4.1) and the channel resistance. I_A and I_B are the pair currents of pairs with the same polarity. See Annex 33A.5 for design guide lines for meeting the above requirements.

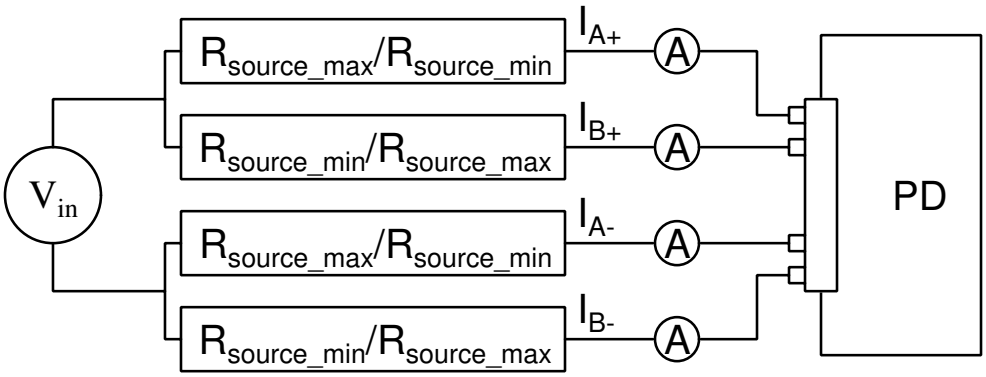

Figure 33–18a—PD PI pair-to-pair test circuit

Editor's Note: Longer channel resistances need to be added.

R_{PSE_max} and R_{PSE_min} represents PSE and channel effective source impedance that includes the effect of $V_{Port_PSE_diff}$ as specified in Table 33–11.

Change 33.3.8 as follows:

33.3.8 PD Maintain Power Signature

~~In order to maintain power, the PD shall provide a valid~~ A PD that requires power from the PI shall provide a valid Maintain Power Signature (MPS) at the PI. A PD that does not maintain the MPS components mentioned above may have its power removed within the limits of T_{MPDO} as specified in Table 33–11.

The MPS shall consist of current draw equal to or above I_{port_MPS} for a minimum duration of T_{MPS_PD} measured at the PD PI followed by an optional MPS dropout for no longer than T_{MPDO_PD}. The values of I_{port_MPS}, T_{MPS_PD}, and T_{MPDO_PD} are shown in Table 33–19a. A Type 1 or Type 2 PD, or a PD which does not detect a long first class event, shall in addition show the input impedance with resistive and capacitive components defined in Table 33–19.

Type 3 and Type 4 PDs that detect a long first class event in the range of T_{LCF_PD} may reduce T_{MPS_PD} in order to draw a lower standby MPS power. In absence of a long first class event the minimum T_{MPS_PD} is higher, and the standby MPS power is also higher.

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A Type 3 or Type 4 PD shall have T_{MPS_PD} measured with a series resistance representing the worst case cable resistance between the measurement point and the PD PI.

PDs using Autoclass shall use the I_{port_MPS} associated with the PD Class assigned by the PSE during Physical Layer classification.

See Annex 33F for PD design guidelines for MPS behavior.

Editor's Note: Informative annex on MPS behavior and design guidelines to be added.

~~A PD that does not maintain the MPS components in a) and b) mentioned above may have its power removed within the limits of T_{MPDO} as specified in Table 33–11.~~

Powered PDs that no longer require power, and identify the PSE as Type 1 or Type 2, shall remove both the current draw and impedance components ~~a) and b)~~ of the MPS. To cause Type 1 and Type 2 PSE power removal, the impedance of the PI should rise above Z_{ac2} as specified in Table 33–12.

Powered PDs that no longer require power, and identify the PSE as Type 3 or Type 4, shall remove the current draw component and may remove the impedance components of the MPS.

Table 33–19—PD Maintain Power Signature

Item	Parameter	Symbol	Unit	Min	Max	Additional information
~~1~~	~~Input current~~	~~I_{Port_MPS}~~	~~A~~	~~0.010~~		~~See~~
1	Input resistance	R_{pd_d}	kΩ		26.3	
2	Input capacitance	C_{pd_d}	µF	0.050		See Table 33–12

~~NOTE—A PD with C_{port} > 180 µF may not be able to meet the I_{Port_MPS} specification in Table 33-19 during the maximum allowed port voltage droop (V_{Port_PSE} max to V_{Port_PSE} min with series resistance R_{Ch}). Such a PD should increase its I_{Port} min or make other such provisions to meet the Maintain Power Signature.~~

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Insert Table 33-19a as follows:

Table 33–19a—PD DC Maintain Power Signature

Item	Parameter	Symbol	Units	Min	Max	PD Type	Conditions
1	Input Current	I_{Port_MPS}	A	0.01		1-4	- All Type 1 and Type 2 PDs and Type 3 ~~single-signature~~ PDs with P_{class_PD} ≤ PD Class 4 power limit. - Total PD current is sum of both pairsets.
				0.016		3, 4	- ~~Single-signature~~ PDs with P_{class_PD} > PD Class 4 power limit. - Total PD current is sum of both pairsets.
				0.008		3, 4	- Dual-signature PDs - ~~Applies to each powered~~ pairset.
2	PD Maintain Power Signature Time	T_{MPS_PD}	ms	75		1, 2	
						3, 4	short_mps = FALSE
				7		3, 4	short_mps = TRUE
3	PD Drop Out Period	T_{MPDO_PD}	ms		250	1, 2	
						3, 4	short_mps = FALSE
					310	3, 4	short_mps = TRUE

NOTE—PDs may not be able to meet the I_{Port_MPS} specification in Table 33–19a during the maximum allowed port voltage droop (V_{Port_PSE} max to V_{Port_PSE} min with series resistance R_{Ch}). Such a PD should increase its I_{Port} min or make other such provisions to meet the Maintain Power Signature.

33.4 Additional electrical specifications

Change text in section 33.4 as follows:

This clause defines additional electrical specifications for both the PSE and PD. The specifications apply for all PSE and PD operating conditions at the cabling side of the mated connection of the PI. The requirements apply during data transmission only when specified as an operating condition.

The requirements of 33.4 are consistent with the requirements of the 10BASE-T MAU and the 100BASE-TX, and 1000BASE-T, and 10GBASE-T PHYs.

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33.4.1 Isolation

Change text in section 33.4.1 as follows:

PDs and PSEs shall provide isolation between all accessible external conductors, including frame ground (if any), and all MDI leads including those not used by the PD or PSE. Any equipment that can be connected to a PSE or PD through a non-MDI connector that is not isolated from the MDI leads needs to provide isolation between all accessible external conductors, including frame ground (if any), and the non-MDI connector. Accessible external conductors are specified in subclause 6.2.1 b) of IEC 60950-1 and IEC 62368-1:~~2001~~.

This electrical isolation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in subclause 5.2.2 of IEC 60950-1 and IEC 62368-1:~~2001~~.
b) 2250 V dc for 60 s, applied as specified in subclause 5.2.2 of IEC 60950-1 and IEC 62368-1:~~2001~~.
c) An impulse test consisting of a 1500 V, 10/700 µs waveform, applied 10 times, with a 60 s interval between pulses. The shape of the impulses shall be 10/700 µs (10 µs virtual front time, 700 µs virtual time of half value), as defined in IEC 60950-1 and IEC 62368-1:~~2001~~ Annex N.

There shall be no insulation breakdown, as defined in subclause 5.2.2 of IEC 60950-1 and IEC 62368-1:~~2001~~, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 V dc.

Conductive link segments that have differing isolation and grounding requirements shall have those requirements provided by the port-to-port isolation of network interface devices (NID).

33.4.1.1 Electrical isolation environments

There are two electrical power distribution environments to be considered that require different electrical isolation properties. They are as follows:

— **Environment A:** When a LAN or LAN segment, with all its associated interconnected equipment, is entirely contained within a single low-voltage power distribution system and within a single building.
— **Environment B:** When a LAN crosses the boundary between separate power distribution systems or the boundaries of a single building.

33.4.1.1.1 Environment A requirements

Attachment of network segments via NIDs that have multiple instances of a twisted pair MDI requires electrical isolation between each segment and the protective ground of the NID.

For NIDs, the requirement for isolation is encompassed within the isolation requirements of the MAU or PHY (see 14.3.1.1, 25.4.6, and 40.6.1.1.). Equipment with multiple instances of PSE, PD, or both shall meet or exceed the isolation requirement of the MAU/PHY with which they are associated.

A multiport NID complying with Environment A requirements does not require electrical power isolation between link segments.

An Environment A PSE shall switch the more negative conductor. It is allowable to switch both conductors.

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33.4.1.1.2 Environment B requirements

Change text in section 33.4.1.1.2 as follows:

The attachment of network segments that cross Environment A boundaries requires electrical isolation between each segment and all other attached segments as well as to the protective ground of the NID.

For NIDs, the requirement for isolation is encompassed within the isolation requirements of the MAU or PHY (see 14.3.1.1, 25.4.6, and 40.6.1.1.). Equipment with multiple instances of PSE, PD, or both shall meet or exceed the isolation requirement of the MAU/PHY with which each is associated.

The requirements for interconnected electrically conducting link segments that are partially or fully external to a single building environment may require additional protection against lightning strikes or other hazards. Protection requirements for such hazards are beyond the scope of this standard. Guidance on these requirements may be found in Section 6 of IEC 60950-1 and IEC 62368-1~~:2001~~, as well as any local and national codes related to safety.

33.4.2 Fault tolerance

Each wire pair of the PI, when it is also an MDI (e.g., an Endpoint PSE or PD), shall meet the fault tolerance requirements of the appropriate specifying clause. (See 14.3.1.2.7, 25.4, and 40.8.3.4.) When a PI is not an MDI (e.g., a Midspan PSE), the PSE PI shall meet the fault tolerance requirements of this subclause.

The PSE PI shall withstand without damage the application of short circuits of any wire to any other wire within the cable for an indefinite period of time. The magnitude of the current through such a short circuit shall not exceed I_{LIM} max as defined in Table 33–11.

Each wire pair shall withstand, without damage, a 1000 V common-mode impulse applied at E_{cm} of either polarity. The shape of the impulse shall be (0.3/50) μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060, where E_{cm} is an externally applied AC voltage as shown in Figure 33–19.

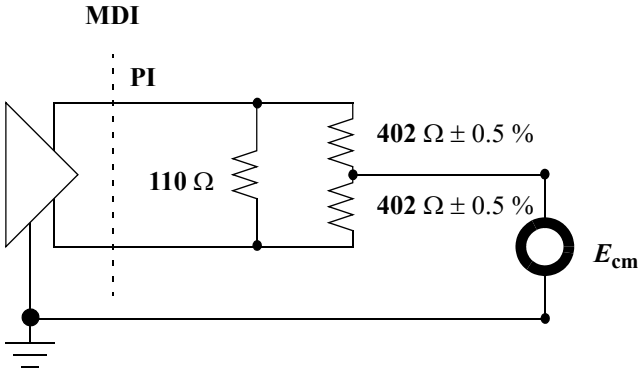

Figure 33–19—PI fault tolerance test circuit

33.4.3 Impedance balance

Change text in section 33.4.3 as follows:

Impedance balance is a measurement of the common-mode-to-differential-mode offset of the PI. The common-mode-to-differential-mode impedance balance for the transmit and receive pairs shall exceed:

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$$\left\{29.0 - 17.0 \times \log_{10}\left(\frac{f}{10.0}\right)\right\}_{\text{dB}} \quad (33\text{–}15)$$

where

f is the frequency in MHz from 1.00 MHz to 20.0 MHz for a 10 Mb/s MAU

$$\left\{34.0 - 19.2 \times \log_{10}\left(\frac{f}{50.0}\right)\right\}_{\text{dB}} \quad (33\text{–}16)$$

where

f is the frequency in MHz from 1.00 MHz to 100.0 MHz for a 100 Mb/s or greater PHY

$$\left\{\begin{array}{ll} 48 & 1 \le f < 30MHz \\ 44.0 - 19.2 \times \log_{10}\left(\frac{f}{50.0}\right) & 30 \le f < 500MHz \end{array}\right\}_{\text{dB}} \quad (33\text{–}16a)$$

The impedance balance is defined as shown in Equation (33–17):

$$\left\{20.0 \times \log_{10}\left(\frac{E_{\text{cm}}}{E_{\text{dif}}}\right)\right\}_{\text{dB}} \quad (33\text{–}17)$$

where

E_{cm} is an externally applied sinusoidal voltage as shown in Figure 33–20

E_{dif} is the voltage of the resulting waveform due only to the applied sine wave measured as shown in Figure 33–20

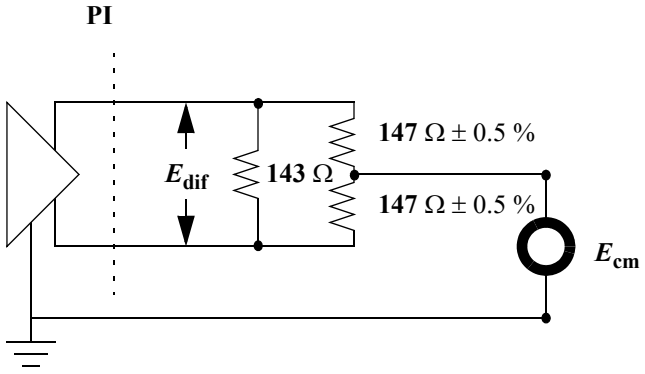

Figure 33–20—PI impedance balance test circuit

33.4.4 Common-mode output voltage

Change text of Section 33.4.4 as follows:

The magnitude of the common-mode AC output voltage measured according to Figure 33–21 and Figure 33–22 at the transmit PI while transmitting data and with power applied, $E_{\text{cm_out}}$, shall not exceed 50 mV peak when operating at 10 Mb/s, and 50 mV peak-to-peak when operating at 100 Mb/s or greater. The

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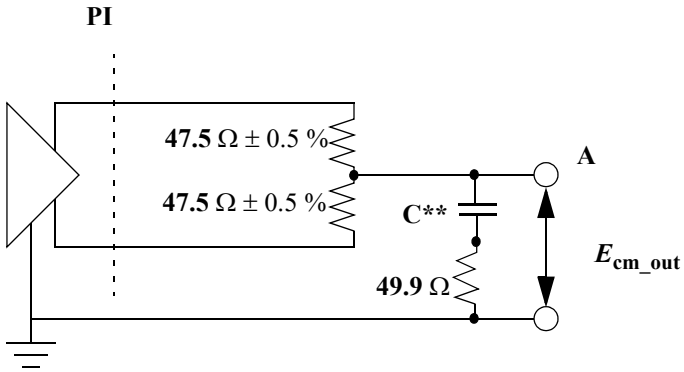
frequency of the measurement shall be from 1 MHz to 100 MHz. For 10GBASE-T systems, 50 mVpp (TBD), for 1 MHz to 500 MHz.

Editor's Note: 10GBASE-T requirement is TBD and needs contributions to fill in relevant details.



**Capacitor impedance less than 1 Ω
from 1 MHz to 100 MHz

Figure 33–21—Common-mode output voltage test

The common-mode AC output voltage shall be measured while the PHY is transmitting data, the PSE or PD is operating with the following PSE load or PD source:

1) For a PSE, the PI that supplies power is terminated as illustrated in Figure 33–22. The PSE load, R, in Figure 33–22 is adjusted so that the PSE output current, I_{out}, is 10 mA and then 350 mA, while measuring E_{cm_out} on the PI.
2) For a PD, the PI that requires power shall be terminated as illustrated in Figure 33–22. V_{source} in Figure 33–22 is adjusted to 36 Vdc and 57 Vdc, while measuring E_{cm_out} on the PI.

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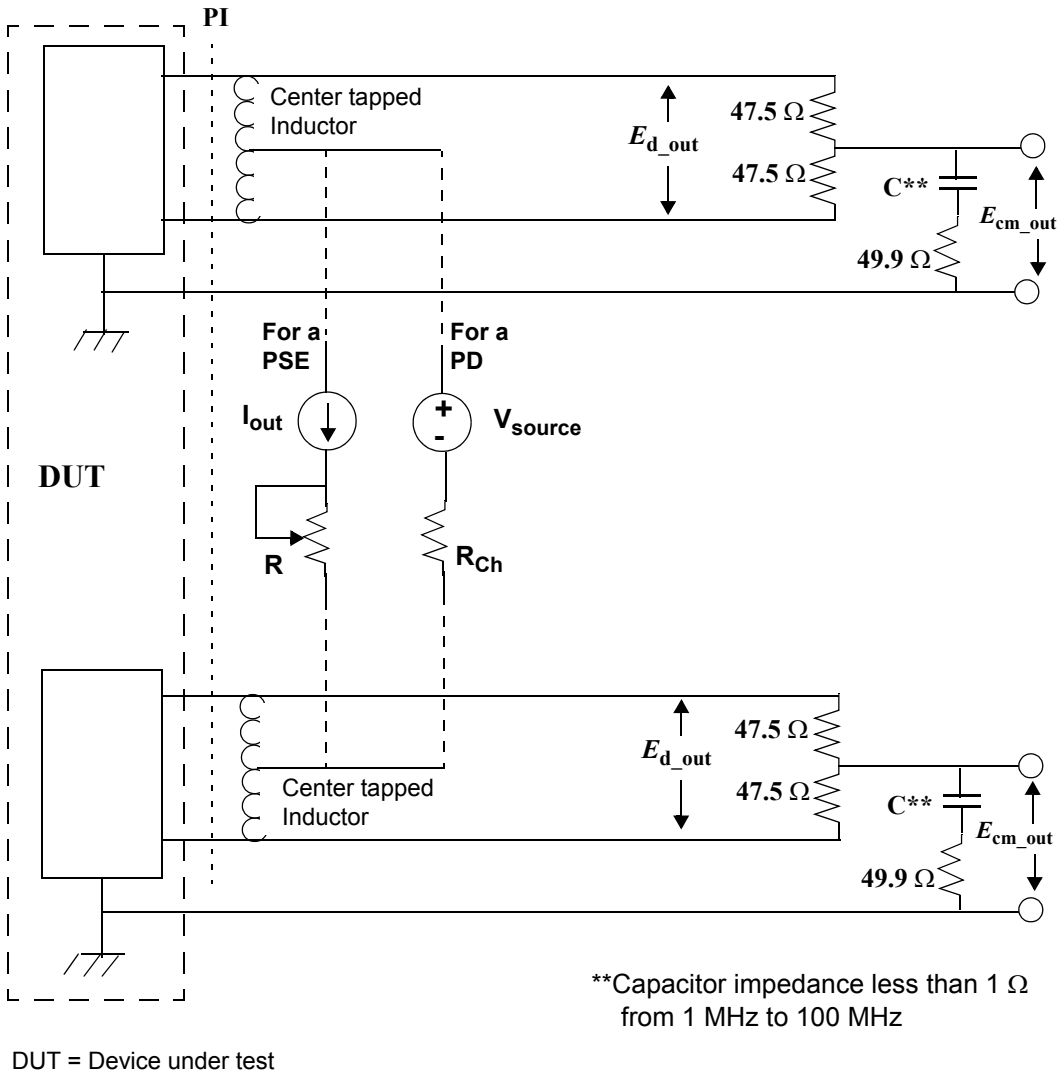

Figure 33–22—PSE and PD terminations for common-mode output voltage test

NOTE—The implementer should consider any applicable local, national, or international regulations that may require more stringent specifications. One such specification can be found in the European Standard EN 55022:1998.

33.4.5 Pair-to-pair output noise voltage

The pair-to-pair output noise voltage (see Figure 33–23) is limited by the resulting electromagnetic interference due to this AC voltage. This AC voltage can be ripple from the power supply (Table 33–11, item 3) or from any other source. A system integrating a PSE shall comply with applicable local and national codes for the limitation of electromagnetic interference.

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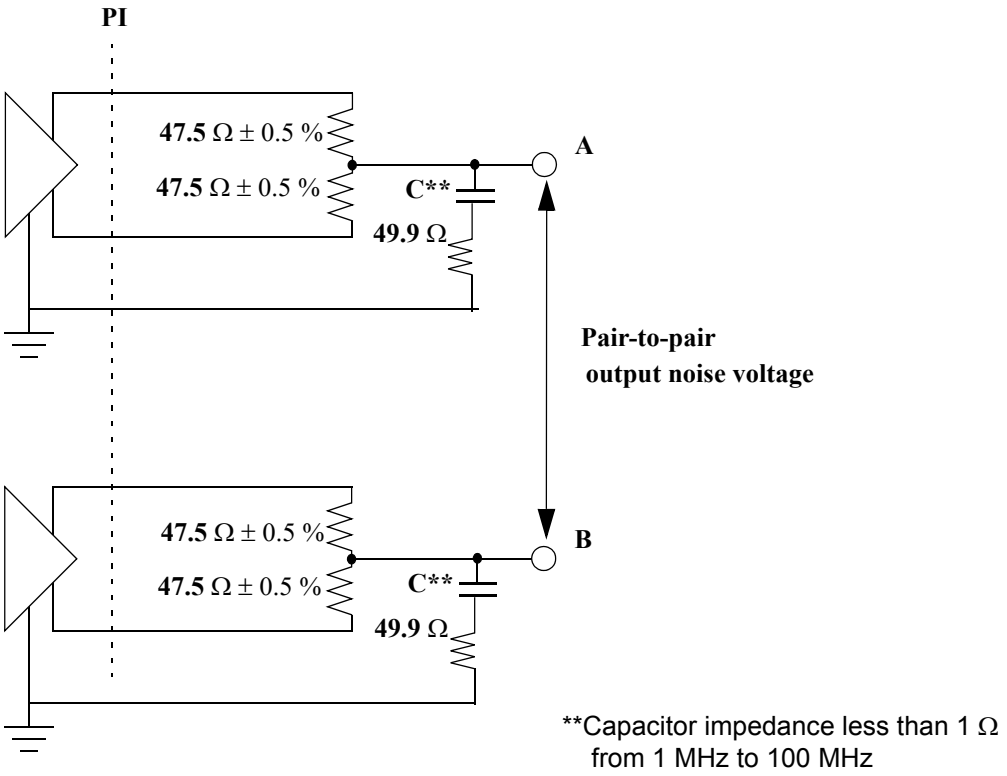

Figure 33–23—Pair-to-pair output noise voltage test

33.4.6 Differential noise voltage

Change text of Section 33.4.6 as follows:

For 10/100/1000 Mb/s, the coupled noise, E_{d_out} in Figure 33–22, from a PSE or PD to the differential transmit and receive pairs shall not exceed 10 mV peak-to-peak when measured from 1 MHz to 100 MHz under the conditions specified in 33.4.4, item 1) and item 2).

For 10GBASE-T, the coupled noise, E_{d_out} in Figure 33–22, from a PSE or PD to the differential transmit and receive pairs shall not exceed the ~~following~~ requirements Equation (33–17a) under the conditions specified in 33.4.4, item 1) and item 2).

Insert the new equation 33-17a as follows:

$$E_{d_out} = \begin{cases} \frac{10 mVpp}{f} & \text{for } (1 \le f < 10) \\ 1 mVpp & \text{for } (10 \le f < 500) \end{cases} \qquad (33\text{–}17a)$$

where

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f is the frequency in MHz for a 10 Gb/s PHY

33.4.7 Return loss

The differential impedance of the transmit and receive pairs at the PHY's MDI shall be such that any reflection shall meet the return loss requirements as specified in 14.3.1.3.4 for a 10 Mb/s PHY, in ANSI X3.263:1995 for a 100 Mb/s PHY, and 40.8.3.1 for a 1000 Mb/s PHY. In addition, all pairs terminated at an MDI should maintain a nominal common-mode impedance of 75 Ω. The common-mode termination is affected by the presence of the power supply, and this should be considered to determine proper termination.

33.4.8 100BASE-TX transformer droop

Change first paragraph of section 33.4.8 as follows:

100BASE-TX systems may contain a legacy PHY receiver that expects to be connected to a PHY transmitter with 350 μH open circuit inductance (OCL). Alternative A Type 2 Midspan PSEs that support 100BASE-TX shall enforce channel current unbalance ~~currents~~ less than or equal to Type 1 I_{unb} (see Table 33–11) or meet 33.4.9.2.

100BASE-TX Type 2 Endpoint PSEs and 100BASE-TX Type 2 PDs shall meet the requirements of Clause 25 in the presence of (I_{unb}/2).

33.4.9 Midspan PSE device additional requirements

Change section 33.4.9 as follows:

The cabling specifications for 100 Ω balanced cabling are described in ISO/IEC 11801-2002. Cable conforming to ANSI/TIA-568-C.2 also meets these requirements. Some cable category specifications that only appear in earlier editions are also supported. The configuration of "channel" and "permanent link" is defined in Figure 33–24. Type 2, 3 and 4 Midspan PSE cabling system requirements are specified in 33.1.4.1.

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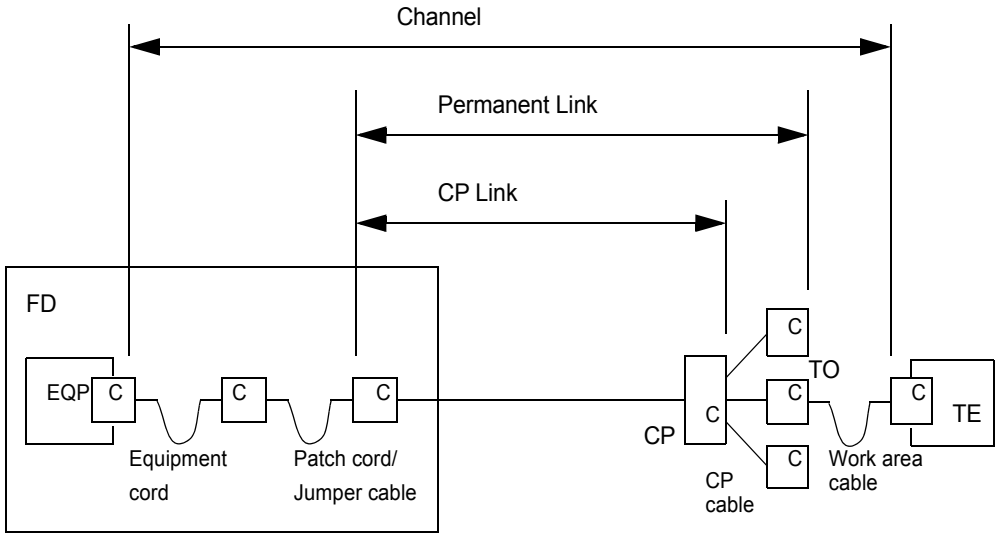

FD = floor distributor; EQP = equipment; C = connection (mated pair);
CP = consolidation point; TO = telecommunications outlet;
TE = terminal equipment

Figure 33–24—Floor distributor channel configuration

ISO/IEC 11801 defines in 5.6.1 two types of Equipment interface to the cabling system: "Interconnect model" and the "cross-connect model." An equivalent "Interconnect model" and "cross-connect model" can be found in ~~ANSI/TIA-568-C.0, 4.2~~ ANSI/TIA-568.D-0, 5.1. See Figure 33–25.

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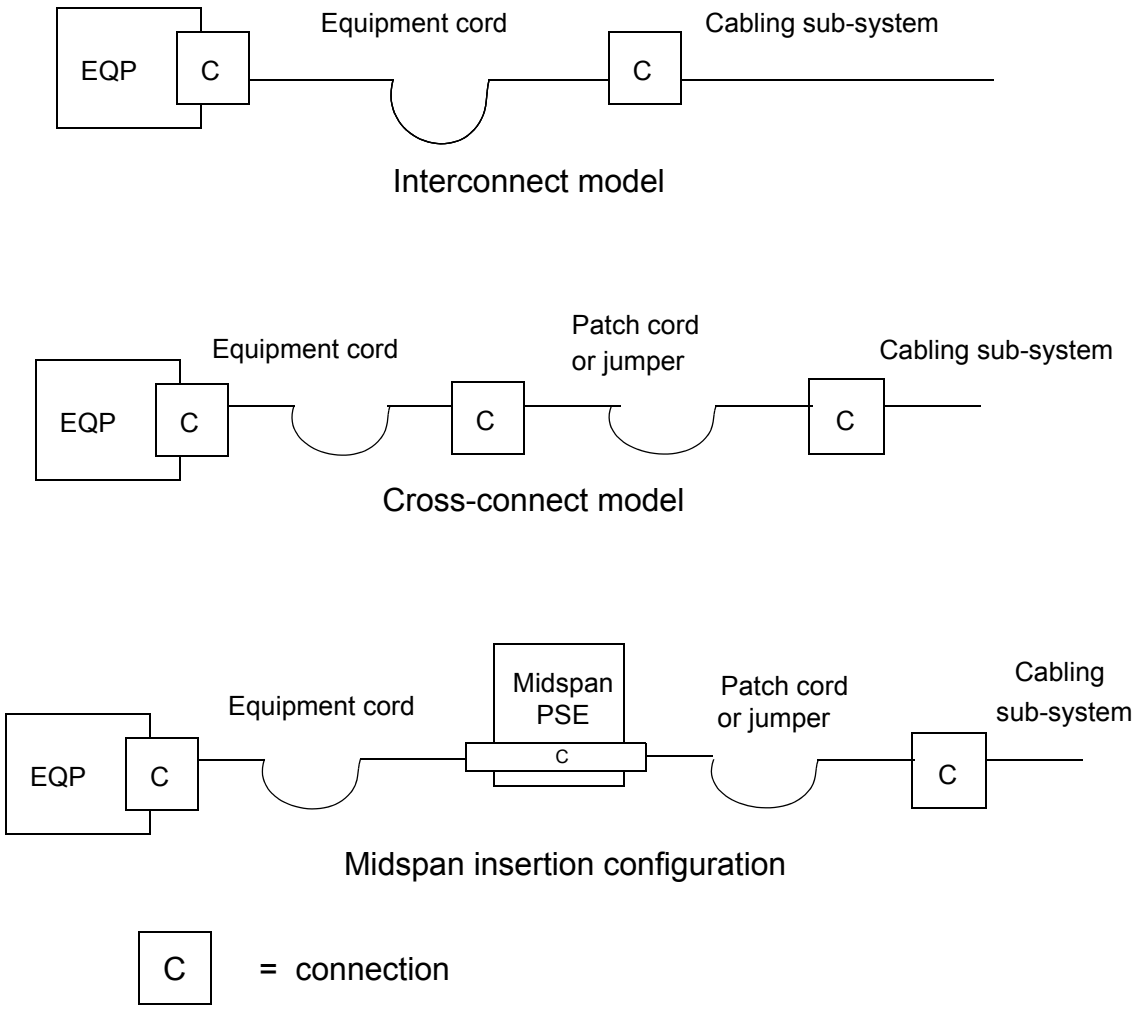

Figure 33–25—Interconnect model, cross-connect model, and midspan insertion configuration

The insertion of a Midspan PSE at the Floor Distributor (FD) shall comply with the following guidelines:

a) If the existing FD configuration is of the "Interconnect model" type, the Midspan PSE can be added, provided it does not increase the length of the resulting "channel" to more than specified 100 m as defined in ISO/IEC 11801 or ANSI/TIA-568-C.0.

b) If the existing FD configuration is of the "Cross-connect model" type, the Midspan PSE needs to be installed instead of one of the connection pairs in the FD. In addition, the installation of the Midspan PSE shall not increase the length of the resulting "channel" to more than specified 100 m as defined in ISO/IEC 11801 or ANSI/TIA-568-C.0.

Configurations with the Midspan PSE in the cabling channel shall not alter the transmission requirements of the "permanent link." A Midspan PSE shall not provide DC continuity between the two sides of the segment for the pairs that inject power.

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The requirements for the two pair Category 5 channel are found in 25.4.9. The specification of Midspan PSE operation on a two pair cable is beyond the scope of this document.

NOTE—Appropriate terminations may be applied to the interrupted pairs on both sides of the Midspan device.

33.4.9.1 "Connector" or "telecom outlet" Midspan PSE device transmission requirements

The Midspan PSE equipment to be inserted as "connector" or "telecom outlet" shall meet the following transmission parameters. These parameters should be measured using the test procedures of ISO 11801:2002 or ANSI/TIA-568-C.2 for connecting hardware.

Change second paragraph of Section 33.4.9.1 as follows:

There are ~~four~~ six variants ~~types~~ of Midspan PSEs defined with respect to transmission requirements:

1) 10BASE-T/100BASE-TX connector or telecom outlet Midspan PSE
2) 10BASE-T/100BASE-TX work area or equipment cable Midspan PSE
3) 1000BASE-T connector or telecom outlet Midspan PSE
4) 1000BASE-T work area o~~r~~f equipment cable Midspan PSE
5) 10GBASE-T connector or telecom outlet Midspan PSE
6) 10GBASE-T work area or equipment cable Midspan PSE

33.4.9.1.1 Near End Crosstalk (NEXT)

Change text of Section 33.4.9.1.1 as follows:

NEXT loss is a measure of the unwanted signal coupling from a transmitter at the near-end into neighboring pairs measured at the near-end. NEXT loss is expressed in dB relative to the received signal level. For operation with 1000BASE-T and lower rates, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–18) when measured for the transmit and receive pairs from 1 MHz to 100 MHz. However, for frequencies that correspond to calculated values greater than 65 dB, the requirement reverts to the minimum requirement of 65 dB.

$$\{NEXTconn\}_{\text{dB}} \geq 40.0 - 20.0 \times \log_{10}\left(\frac{f}{100}\right) \qquad (33\text{–}18)$$

where

NEXTconn is the Near End Crosstalk loss in dB
f is the frequency expressed in MHz

For 10GBASE-T operation, NEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–18a) when measured for the transmit and receive pairs from 1 MHz to 500 MHz. However, for frequencies that correspond to calculated values greater than 75 dB, the requirement reverts to the minimum requirement of 75 dB.

$$\{NEXTconn\}_{\text{dB}} \leq \left\{ \begin{array}{ll} 54.0 - 20.0 \times \log_{10}\left(\frac{f}{100}\right) & \text{for } (1 \leq f \leq 250) \\ 46.04 - 40.0 \times \log_{10}\left(\frac{f}{250}\right) & \text{for } (250 < f \leq 500) \end{array} \right\}_{dB} \qquad (33\text{–}18a)$$

where

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NEXTconn is the Near End Crosstalk loss in dB
f is the frequency expressed in MHz

33.4.9.1.2 Insertion loss

Change text of Section 33.4.9.1.2 as follows:

Insertion loss is a measure of the signal loss between the transmitter and receiver, expressed in dB relative to the received signal level. For other than 10GBASE-T operation, insertion loss for Midspan PSE devices shall meet the values determined by Equation (33–19) when measured for the transmit and receive pairs from 1 MHz to 100 MHz. ~~However, f~~

For frequencies that correspond to calculated values less than 0.1 dB, the requirement reverts to the maximum requirement of 0.1 dB.

$$\{ILconn\}_{\text{dB}} \le 0.040 \times \sqrt{f} \qquad (33–19)$$

where

ILconn is the insertion loss in dB
f is the frequency expressed in MHz

For 10GBASE-T operation, insertion loss for Midspan PSE devices shall meet the values determined by Equation (33–19a) when measured from the transmit and receive pairs from 1 MHz to 500 MHz.

$$\{ILconn\}_{\text{dB}} \le 0.020 \times \sqrt{f} \qquad (33–19a)$$

where

ILconn is the insertion loss in dB
f is the frequency expressed in MHz

33.4.9.1.3 Return loss

Change text of Section 33.4.9.1.3 and Table 33–20 as follows:

Return loss is a measure of the reflected energy caused by impedance mismatches in the cabling system and is expressed in dB relative to the reflected signal level. Return loss for Midspan PSE devices shall meet or exceed the values specified in Table 33–20~~when measured for the transmit and receive pairs from 1 MHz to 100 MHz~~.

Table 33–20—Connector return loss

Midspan PSE Variant	Frequency	Return loss
10/100/1000BASE-T	1 MHz ≤ *f* < 20 MHz	23 dB
	20 MHz ≤ *f* ≤ 100 MHz	14 dB
10GBASE-T	1 MHz ≤ *f* < 79 MHz	30 dB
	79 MHz ≤ *f* ≤ 500 MHz	28 - 20 $\log_{10}$(f/100)

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33.4.9.1.4 Work area or equipment cable Midspan PSE

Change 33.4.9.1.4 as follows:

Replacing the work area or equipment cable with a cable that includes a Midspan PSE should not alter the requirements of the cable. This cable shall meet the requirements of this clause and the specifications for a Category 5 (jumper) cord as specified in ISO/IEC 11801:2002 or ~~ANSI/TIA-568-C.2~~ ANSI/TIA/EIA-568-A:1995 for insertion loss, NEXT, and return loss for the transmit and receive pairs.

Insert Sections 33.4.9.1.4a, 33.4.9.1.4b, 33.4.9.1.4c, 33.4.9.1.4d and 33.4.9.1.4e after 33.4.9.1.4 as follows:

33.4.9.1.5 Maximum link delay

The propagation delay contribution of the Midspan PSE device shall not exceed 2.5 ns from 1 MHz to the highest referenced frequency.

33.4.9.1.6 Maximum link delay skew

The propagation delay contribution of the Midspan PSE device shall not exceed 1.25 ns from 1 MHz to the highest referenced frequency.

33.4.9.1.7 Coupling parameters between link segments

Midspan PSEs intended for operation with 10GBASE-T (~~types~~variants 5 and 6 in 33.4.9.1) are additionally required to meet the following parameters for coupling signals between ports relating to different link segments. Noise coupled between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is referred to as alien crosstalk noise. To ensure the total alien NEXT loss and alien FEXT loss coupled between link segments is limited, multiple disturber alien near-end crosstalk (MDANEXT) loss and multiple disturber alien FEXT (MDAFEXT) loss is specified.

33.4.9.1.8 Multiple disturber power sum alien near-end crosstalk (PSANEXT) loss

PSANEXT loss for 10GBASE-T capable Midspan PSE devices shall meet or exceed the values determined using the equations shown in Table 33–20a for all specified frequencies. Calculations that result in PSANEXT loss values greater than 67 dB shall revert to a requirement of 67 dB minimum.

Table 33–20a—PSANEXT Loss

Frequency	Return Loss (dB)
1 MHz ≤ f ≤ 500 MHz	70.5 - 20 $\log_{10}$ (f/100)

33.4.9.1.9 Multiple disturber power sum alien far-end crosstalk (PSAFEXT) loss

PSAFEXT loss for 10GBASE-T capable Midspan PSE devices shall meet or exceed the values determined using the equations shown in Table 33–20b for all specified frequencies. Calculations that result in PSANEXT loss values greater than 67 dB shall revert to a requirement of 67 dB minimum.

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Table 33–20b—PSAFEXT Loss

Frequency	PSAFEXT Loss (dB)
1 MHz ≤ f ≤ 500 MHz	67 - 20 $\log_{10}$ (f/100)

Insert Section 33.4.9.1a after Section 33.4.9.1 as follows:

33.4.9.1a Transmission parameters for Midspan PSEs with a link segment

In order to maintain the transmission parameters for a link segement, the transmission parameters of the Midspan PSE are defined. These include insertion loss, delay parameters, nominal impedance, NEXT loss, FEXT and return loss. In addition, for 10GBASE-T operation, the requirements for the alien cross talk coupled "between" link segments are specified.

33.4.9.2 Midspan signal path requirements

An Alternative A Midspan PSE transfer function gain shall be greater than that expressed by Equation (33–20) for the frequency range from 0.1 MHz to 1 MHz, at the pins of the PI used as 100BASE-TX transmit pins.

$$\left\{ -0.100 + 37.5 \times \log_{10}\left(\frac{22.4 \times f}{\sqrt{1.00 + 521 \times f^2}} \right) \right\}_{\text{dB}} \qquad (33\text{–}20)$$

where

f is the frequency expressed in MHz.

The requirements shall be met with a DC bias current, I_{bias}, between 0 mA and (I_{unb}/2) mA (I_{unb} is defined in Table 33–11).

33.4.9.2.1 Alternative A Midspan PSE signal path transfer function

The transfer function is measured by applying a test signal to the Midspan PSE signal input through a source impedance of 100 Ω ± 1 %. The Midspan PSE signal input and output may be connected to a 0.5 m maximum length of cable, meeting the requirements of 25.4.9, terminated with 100 Ω ± 1 %.

The transfer function is defined from the output termination to the Midspan PSE input. See Figure 33–26.

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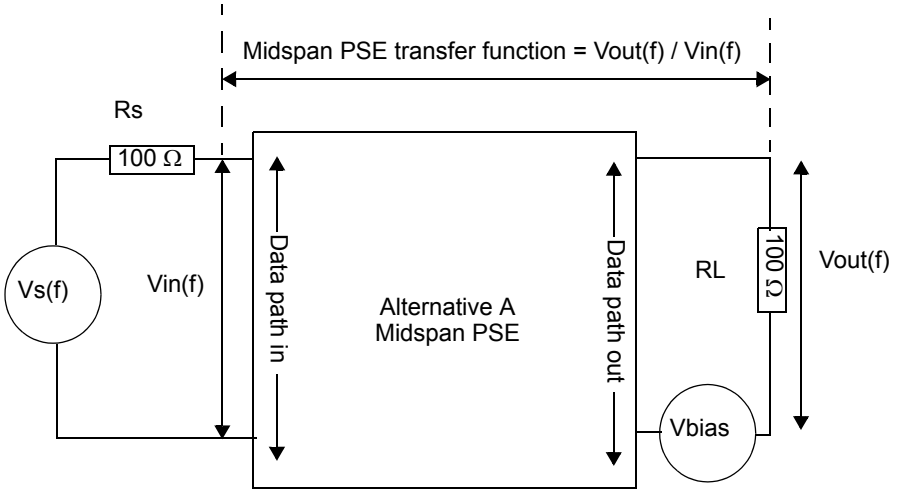

Vin(f) is the sine wave signal to be used to measure the Midspan PSE transfer function.
Vbias is the DC offset voltage to be applied in series with RL in order to generate I_{bias}.
Vout(f) is the Midspan PSE response to Vin(f).
Some test equipment may require isolation between measurement ports.

Figure 33–26—Measurement setup for Alternative A Midspan PSE transfer function

33.5 Management function requirements

If the PSE is implemented with a management interface described in 22.2.4 or 45.2 (MDIO), then the management access shall use the PSE register definitions shown in 33.5.1. Where no physical embodiment of the Clause 22 or Clause 45 management is supported, equivalent management capability shall be provided. Managed objects corresponding to PSE and PD control parameters and states are described in Clause 30.

33.5.1 PSE registers

A PSE implementing either Clause 22 or Clause 45 management interface shall use register address 11 for its control and register address 12 for its status functions. The full set of management registers is listed in Table 22–6.

Some of the bits within registers are defined as latching high (LH). When a bit is defined as latching high and the condition for the bit to be high has occurred, the bit shall remain high until after it has been read via the management interface. Once such a read has occurred, the bit shall assume a value based on the current state of the condition it monitors.

33.5.1.1 PSE Control register (Register 11) (R/W)

The assignment of bits in the PSE Control register is shown in Table 33–21. The default value for each bit of the PSE Control register should be chosen so that the initial state of the PSE upon power up or reset is a normal operational state without management intervention.

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Change Table 33-21 as follows:

Table 33–21—PSE Control register bit definitions

Bit(s)	Name	Description	R/W[1]
11.15:8~~6~~	Reserved	Ignore when read	RO
11.7:6	Force Power Test Mode Pairset Selection	(11.7) (11.6) 1 1 = Both Alternative A and Alternative B powered when Force Power Test Mode enabled 1 0 = Alternative B powered when Force Power Test Mode enabled 0 1 = Alternative A powered when Force Power Test Mode enabled 0 0 = Reserved	R/W
11.5	Data Link Layer Classification Capability	1 = Data Link Layer classification capability enabled 0 = Data Link Layer classification capability disabled	R/W
11.4	Enable Physical Layer Classification	1 = Physical Layer classification enabled 0 = Physical Layer classification disabled	R/W
11.3:2	Pair Control	(11.3) (11.2) 1 1 = ~~Reserved~~PSE pinout Alternative A and Alternative B 1 0 = PSE pinout Alternative B 0 1 = PSE pinout Alternative A 0 0 = Reserved	R/W
11.1:0	PSE Enable	(11.1) (11.0) 1 1 = Reserved 1 0 = Force Power Test Mode 0 1 = PSE Enabled 0 0 = PSE Disabled	R/W

[1]R/W = Read/Write, RO = Read Only

Change text in section 33.5.1.1.1 as follows:

33.5.1.1.1 Reserved bits (11.15:~~6~~8)

Bits 11.15:~~6~~7 are reserved for future standardization. They shall not be affected by writes and shall return a value of zero when read. For compatibility with future use of reserved bits and registers, if the management entity writes to a reserved bit, it should use a value of zero. If it reads a reserved bit, it should ignore the results.

Insert new section 33.5.1.1.1a after section 33.5.1.1.1 as follows:

33.5.1.1.1a Force Power Test Mode Pairset Selection (11.7:6)

Bits 11.7:6 determine which PSE Alternative or Alternatives are enabled when Force Power Test Mode is enabled.

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33.5.1.1.2 Data Link Layer Classification capability (11.5)

Bit 11.5 controls a PSEs capability of performing Data Link Layer classification as specified in 33.6.

A PSE that does not support Data Link Layer classification shall ignore writes to bit 11.5 and shall return a value of zero when read. A PSE that supports Data Link Layer classification, but does not allow the capability to be disabled, shall ignore writes to bit 11.5 and shall return a value of one when read.

A PSE that supports Data Link Layer classification and supports the ability to enable and disable it shall enable Data Link Layer classification by setting bit 11.5 to one and disable it by setting bit 11.5 to zero.

33.5.1.1.3 Enable Physical Layer classification (11.4)

Bit 11.4 controls Physical Layer classification as specified in 33.2.6. A PSE that indicates support for Physical Layer classification in register 12.13 may also provide the option of disabling Physical Layer classification through bit 11.4.

A PSE that does not support Physical Layer classification shall ignore writes to bit 11.4 and shall return a value of zero when read. A PSE that supports Physical Layer classification, but does not allow the function to be disabled, shall ignore writes to bit 11.4 and shall return a value of one when read.

The Physical Layer classification function shall be enabled by setting bit 11.4 to one and disabled by setting bit 11.4 to zero.

33.5.1.1.4 Pair Control (11.3:2)

Change text in section 33.5.1.1.4 as follows:

Bits 11.3:2 report the supported PSE Pinout Alternative specified in 33.2.3. A PSE may also provide the option of controlling the PSE Pinout Alternative through these bits. Provision of this option is indicated through the Pair Control Ability (12.0) bit. A PSE that does not support this option shall ignore writes to these bits and shall return the value that reports the supported PSE Pinout Alternative.

When read as ‘01’, bits 11.3:2 indicate that only PSE Pinout Alternative A is supported by the PSE. When read as ‘10’, bits 11.3:2 indicate that only PSE Pinout Alternative B is supported by the PSE. When read as ‘11’, bits 11.3:2 indicate that both Pinout Alternative A and Pinout Alternative B are supported by the PSE.

Where the option of controlling the PSE Pinout Alternative through these bits is provided, setting bits 11.3:2 to ‘01’ shall force the PSE to use only PSE Pinout Alternative A and setting bits 11.3:2 to ‘10’ shall force the PSE to use only PSE Pinout Alternative B. Setting bits 11.3:2 to '11' shall allow the PSE to use both PSE Pinout Alternative A and PSE Pinout Alternative B.

If bit 12.0 is one, writing to these register bits shall set mr_pse_alternative to the corresponding value: ‘01’ = A, ~~and~~ ‘10’ = B, and '11' = BOTH. The combinations ‘00’ ~~and ‘11’~~ for bits 11.3:2 are reserved~~ and will never be assigned~~. Reading bits 11.3:2 returns an unambiguous result of ‘01’, ~~or~~ ‘10’, or ‘11’ that may be used to determine the presence of the PSE Control register.

33.5.1.1.5 PSE enable (11.1:0)

The PSE function shall be disabled by setting bit 11.1 to zero and bit 11.0 to zero. When the PSE function is disabled, the MDI shall function as it would if it had no PSE function. The PSE function shall be enabled by setting bits 11.1 to a zero and 11.0 to a one. When bit 11.1 is a one, and bit 11.0 is a zero, a test mode is enabled. This test mode supplies power without regard to PD detection.

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Writing to these register bits shall set mr_pse_enable to the corresponding value: '00' = disable, '01' = enable and '10' = force power. The combination '11' for bits 11.1:0 has been reserved for future use.

CAUTION

Test mode may damage connected non-PD, legacy, twisted pair Ethernet devices, or other non-Ethernet devices, especially in split application wiring schemes.

33.5.1.2 PSE Status register (Register 12) (R/W)

The assignment of bits in the PSE Status register is shown in Table 33–22.

Table 33–22—PSE Status register bit definitions

Bit(s)	Name	Description	R/W[1]
12.15	PSE Type Electrical Parameters	1 = PSE is using Type 2 PSE electrical parameters 0 = PSE is using Type 1 PSE electrical parameters	RO
12.14	Data Link Layer Classification Enabled	1 = Data Link Layer classification is enabled 0 = Data Link Layer classification is not supported or is not enabled	RO
12.13	Physical Layer Classification Supported	1 = PSE supports Physical Layer classification 0 = PSE does not support Physical Layer classification	RO
12.12	Power Denied or Removed	1 = Power has been denied or removed due to fault 0 = Power has not been denied or removed	RO/ LH
12.11	Valid Signature	1 = Valid PD signature detected 0 = No valid PD signature detected	RO/ LH
12.10	Invalid Signature	1 = Invalid PD signature detected 0 = No invalid PD signature detected	RO/ LH
12.9	Short Circuit	1 = Short circuit condition detected 0 = No short circuit condition detected	RO/ LH
12.8	Overload	1 = Overload condition detected 0 = No overload condition detected	RO/ LH
12.7	MPS Absent	1 = MPS absent condition detected 0 = No MPS absent condition detected	RO/ LH
12.6:4	PD Class	(12.6) (12.5) (12.4) 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = Invalid Class 1 0 0 = Class 4 0 1 1 = Class 3 0 1 0 = Class 2 0 0 1 = Class 1 0 0 0 = Class 0	RO

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Table 33–22—PSE Status register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[1]
12.3:1	PSE Status	(12.3) (12.2) (12.1) 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = implementation-specific fault 1 0 0 = Test error 0 1 1 = Test mode 0 1 0 = Delivering power 0 0 1 = Searching 0 0 0 = Disabled	RO
12.0	Pair Control Ability	1 = PSE pinout controllable by Pair Control bits 0 = PSE Pinout Alternative fixed	RO

[1]RO = Read Only, LH = Latched High

Editor's Note: Table 33-22 requires new fields to support new Types and features. Reviewers are encouraged to provide the required definitions. Status register bits are used up, and clause 22 address space is used up as well. Contributions requested as to how to expand status, at a minimum to report Class 8 PD and Autoclass.

33.5.1.2.1 PSE Type electrical parameters (12.15)

When read as a zero, bit 12.15 indicates that the PSE is operating with Type 1 PSE electrical parameters. When read as a one, bit 12.15 indicates that the PSE is operating with Type 2 PSE electrical parameters. This bit shall be set to zero when the PSE state diagram sets the state variable set_parameter_type to 1. This bit shall be set to one when the PSE state diagram sets set_parameter_type to 2.

33.5.1.2.2 Data Link Layer Classification Enabled (12.14)

When read as a one, bit 12.14 indicates the PSE supports Data Link Layer classification as defined in 33.2.6 and that it is enabled. When read as a zero, bit 12.14 indicates that the PSE lacks support for Data Link Layer classification or that Data Link Layer classification is not enabled. If supported, the Data Link Layer classification may be enabled or disabled through the state diagram variable pse_dll_enabled (see 33.2.4.4).

This bit shall be set to one when the PSE state diagram (Figure 33–9) sets true the state variable pse_dll_enabled. This bit shall be set to zero when the PSE state diagram sets false the state variable pse_dll_enabled.

33.5.1.2.3 Physical Layer Classification Supported (12.13)

When read as a one, bit 12.13 indicates that the PSE supports Physical Layer classification as defined in 33.2.6. When read as a zero, bit 12.13 indicates that the PSE lacks support for Physical Layer classification. If supported, the function may be enabled or disabled through the Enable Physical Layer Classification bit (11.4).

33.5.1.2.4 Power Denied or Removed (12.12)

When read as a one, bit 12.12 indicates that power has been denied or has been removed due to a fault condition. This bit shall be set to one when the PSE state diagram (Figure 33–9) enters the states

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'POWER_DENIED' or 'ERROR_DELAY.' The Power Denied bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.5 Valid Signature (12.11)

When read as a one, bit 12.11 indicates that a valid signature has been detected. This bit shall be set to one when mr_valid_signature transitions from FALSE to TRUE. The Valid Signature bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.6 Invalid Signature (12.10)

When read as a one, bit 12.10 indicates that an invalid signature has been detected. This bit shall be set to one when the PSE state diagram (Figure 33–9) enters the state 'SIGNATURE_INVALID'. The Invalid Signature bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.7 Short Circuit (12.9)

When read as a one, bit 12.9 indicates that a short circuit condition has been detected. This bit shall be set to one when the PSE state diagram (Figure 33–9) enters the state 'ERROR_DELAY.' The Short Circuit bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.8 Overload (12.8)

When read as a one, bit 12.8 indicates that an overload condition has been detected. This bit shall be set to one when the PSE state diagram (Figure 33–9) enters the state 'ERROR_DELAY_OVER'. The Overload bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.9 MPS Absent (12.7)

When read as a one, bit 12.7 indicates that an MPS Absent condition has been detected. The MPS Absent bit shall be set to one when the PSE state diagram (Figure 33–9) transitions directly from the state POWER_ON to IDLE due to tmpdo_timer_done being asserted. The MPS Absent bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.10 PD Class (12.6:4)

Bits 12.6:4 report the PD Class of a detected PD as specified in 33.2.5 and 33.2.6. The value in this register is valid while a PD is connected, i.e., while the PSE Status (12.3:1) bits are reporting "delivering power." The combinations '110' and '111' for bits 12.6:4 have been reserved for future use.

33.5.1.2.11 PSE Status (12.3:1)

Bits 12.3:1 report the current status of the PSE. When read as '000', bits 12.3:1 indicate that the PSE state diagram (Figure 33–9) is in the state DISABLED. When read as '010', bits 12.3:1 indicate that the PSE state diagram is in the state POWER_ON. When read as '011', bits 12.3:1 indicate that the PSE state diagram is in the state TEST_MODE. When read as '100', bits 12.3:1 indicate that the PSE state diagram is in the state TEST_ERROR. When read as '101', bits 12.3:1 indicate that the PSE state diagram is in the state IDLE due to the variable error_condition = true. When read as '001', bits 12.3:1 indicate that the PSE state diagram is in a state other than those listed above.

The combinations '111' and '110' for bits 12.3:1 have been reserved for future use.

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33.5.1.2.12 Pair Control Ability (12.0)

When read as a one, bit 12.0 indicates that the PSE supports the option to control which PSE Pinout Alternative (see 33.2.3) is used for PD detection and power through the Pair Control (11.3:2) bits. When read as a zero, bit 12.0 indicates that the PSE lacks support of the option to control which PSE Pinout Alternative is used for PD detection and power through the Pair Control (11.3:2) bits.

Change text in Section 33.6 as follows:

33.6 Data Link Layer classification

Additional control and classification functions are supported using Data Link Layer classification using frames based on the IEEE 802.3 Organizationally Specific TLVs defined in Clause 79. ~~Type 2 PDs that require more than 13.0 W support Data Link Layer classification (see 33.3.5).~~ Single signature PDs advertising a Class 4 signature or higher ~~and Type 3 and Type 4 dual-signature PDs~~ support Data Link Layer classification (see 33.3.5). Data Link Layer classification is optional for all other devices.

All reserved fields in transmitted Power via MDI TLVs shall contain zero, and all reserved fields in received Power via MDI TLVs shall be ignored.

33.6.1 TLV frame definition

Change 33.6.1 as follows:

Implementations that support Data Link Layer classification shall comply with all mandatory parts of IEEE Std 802.1AB-2009; shall support the Power via MDI Type, Length, Value (TLV) defined in 79.3.2 and the Power via MDI Measurements TLV defined in 79.3.7; and shall support the control state diagrams defined in 33.6.3.

33.6.2 Data Link Layer classification timing requirements

Change text in paragraph 1 and paragraph 3 of Section 33.6.2 as follows:

Type 2, 3, and 4 PSEs shall send an LLDPDU containing a Power via MDI TLV within 10 seconds of Data Link Layer classification being enabled in the PSE as indicated by the variable pse_dll_enabled (33.2.4.4, 33.6.3.3).

A Type 1 PSE that implements Data Link Layer classification shall send an LLDPDU containing a Power via MDI TLV when the PSE Data Link Layer classification engine is ready as indicated by the variable pse_dll_ready (33.6.3.3).

All Type 1 PDs that implement Data Link Layer classification and Type 2, 3, and 4 PDs shall set the state variable pd_dll_ready within 5 minutes of Data Link Layer classification being enabled in a PD as indicated by the variable pd_dll_enabled (33.3.3.3, 33.6.3.3).

Under normal operation, an LLDPDU containing a Power via MDI TLV with an updated value for the “PSE allocated power value” field shall be sent within 10 seconds of receipt of an LLDPDU containing a Power via MDI TLV where the “PD requested power value” field is different from the previously communicated value.

Under normal operation, an LLDPDU containing a Power via MDI TLV with an updated value for the “PD requested power value” field shall be sent within 10 seconds of receipt of an LLDPDU containing a Power

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via MDI TLV where the "PSE allocated power value" field is different from the previously communicated value.

33.6.3 Power control state diagrams

The power control state diagrams for PSEs and PDs specify the externally observable behavior of a PSE and PD Data Link Layer classification respectively. PSE Data Link Layer classification shall provide the behavior of the state diagram as shown in Figure 33–27. PD Data Link Layer classification shall provide the behavior of the state diagram as shown in Figure 33–28.

33.6.3.1 Conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5.

33.6.3.2 Constants

Change variables PD_DLLMAX_VALUE, PD_INITIAL_VALUE and PSE_INITIAL_VALUE in Section 33.6.3.2 as follows:

PD_DLLMAX_VALUE

This value is derived from pd_max_power variable (33.3.3.3) described as follows:

pd_max_power	PD_DLLMAX_VALUE
0	130
1	39
2	65
3	130
4	255
5	400
6	600
7	620
8	710

PD_INITIAL_VALUE

This value is derived as follows from the pd_max_power (33.3.3.3) variable used in the PD state diagram (Figure 33–16):

pd_max_power	PD_INITIAL_VALUE
0	≤ 130
1	≤ 39
2	≤ 65
3	≤ 130
4	≤ 255
5	≤ 400
6	≤ 600
7	≤ 620
8	≤ 710

PSE_INITIAL_VALUE

This value is derived as follows from parameter_type and the mr_pd_class_detected (33.2.4.6) variable used in the PSE state diagram (Figure 33–9):

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parameter_type	mr_pd_class_detected	PSE_INITIAL_VALUE
1	0	130
1	1	39
1	2	65
1	3	130
1	4	130
2	4	255
3	5	400
3	6	510
4	7	620
4	8	710

Variables PD_DLL_MAX_VALUE, PD_INITIAL_VALUE, and PSE_INITIAL_VALUE, are quantized to fit the available resolution. Additional information on power levels for Classes 6 and 8 may be found in 33.3.7.2.

33.6.3.3 Variables

The PSE power control state diagram (Figure 33–27) and PD power control state diagram (Figure 33–28) use the following variables:

Change variable MirroredPDRequestedPowerValue, MirroredPSEAllocatedPowerValue, PDRequested-PowerValueEcho, PSEAllocatedPowerValue and PSEAllocatedPowerValueEcho in Section 33.6.3.3 as follows:

MirroredPDRequestedPowerValue

The copy of PDRequestedPowerValue that the PSE receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValue attribute (30.12.3.1.17). Actual power numbers are represented using an integer value that is encoded according to Equation (79–1), where *X* is the decimal value of MirroredPDRequestedPowerValue.

Values:~~0~~ 1 through ~~255~~710

MirroredPDRequestedPowerValueEcho

The copy of PDRequestedPowerValueEcho that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValue attribute (30.12.3.1.17).

MirroredPSEAllocatedPowerValue

The copy of PSEAllocatedPowerValue that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute (30.12.3.1.18). Actual power numbers are represented using an integer value that is encoded according to Equation (79–2), where *X* is the decimal value of MirroredPSEAllocatedPowerValue.

Values:~~0~~ 1 through ~~255~~710

MirroredPSEAllocatedPowerValueEcho

The copy of PSEAllocatedPowerValue that the PSE receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute (30.12.3.1.18).

PDRequestedPowerValueEcho

This variable is updated by the PSE state diagram. This variable maps into the aLldpXdot3LocPDRequestedPowerValue attribute (30.12.2.1.17).

Values:~~0~~ 1 through ~~255~~710

PDMaxPowerValue

Integer that indicates the actual PD power value of the local system. The actual PD power value for a PD is the maximum input average power (see 33.3.7.2) the PD ever draws under the current power allocation. Actual power numbers are represented using an integer value that is encoded according to Equation (79–1), where *X* is the decimal value of PDMaxPowerValue.

PDRequestedPowerValue

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Integer that indicates the PD requested power value in the PD. The value is the maximum input average power (see 33.3.7.2) the PD requests. This power value is encoded according to Equation (79–1), where *X* is the decimal value of PDRequestedPowerValue. This variable is mapped from the aLldpXdot3LocPDRequestedPowerValue attribute (30.12.2.1.17).

Values:~~0~~ 1 through PD_DLLMAX_VALUE

PSEAllocatedPowerValue

Integer that indicates the PSE allocated power value in the PSE. The value is the maximum input average power (see 33.3.7.2) the PD ever draws. The power value for a PSE is the maximum input average power the PD may ever draw. This power value is encoded according to Equation (79–2), where *X* is the decimal value of PSEAllocatedPowerValue. This variable is mapped from the aLldpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.18).

Values:~~0~~ 1 through ~~255~~710

PSEAllocatedPowerValueEcho

This variable is updated by the PD state diagram. This variable maps into the aLldpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.18).

Values:~~0~~ 1 through ~~255~~710

TempVar

A temporary variable used to store Power Value. Actual power numbers are represented using an integer value that is encoded according to Equation (79–1) or Equation (79–2), where *X* is the decimal value of TempVar.

local_system_change

An implementation-specific control variable that indicates that the local system wants to change the allocated power value. In a PSE, this indicates it is going to change the power allocated to the PD. In a PD, this indicates it is going to request a new power allocation from the PSE.

Values:FALSE:The local system does not wants to change the power allocation.
TRUE:The local system wants to change the power allocation.

Change variable parameter_type in Section 33.6.3.3 as follows:

parameter_type

A control variable output by the PSE state diagram (Figure 33–9) used by a Type 2, Type 3, or Type 4 PSE to choose operation with Type 1, Type 2, Type 3, or Type 4 ~~2~~ PSE output PI electrical requirement parameter values defined in Table 33–11.

Values: 1: Type 1 PSE parameter values (default).
2: Type 2 PSE parameter values.
3: Type 3 PSE parameter values.
4: Type 4 PSE parameter values.

pd_dll_enabled

A variable output by the PD state diagram (Figure 33–16) to indicate if the PD Data Link Layer classification mechanism is enabled.

Values: FALSE:PD Data Link Layer classification is not enabled.
TRUE:PD Data Link Layer classification is enabled.

Change variable pd_dll_power_type in Section 33.6.3.3 as follows:

pd_dll_power_type

A control variable that indicates the Type of PD that is connected to the PSE as advertised through Data Link Layer classification.

Values: 1: PD is a Type 1 PD (default).
2: PD is a Type 2 PD.
3: PD is a Type 3 PD.
4: PD is a Type 4 PD.

pd_dll_ready

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An implementation-specific control variable that indicates that the PD has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).
Values:FALSE:Data Link Layer classification has not completed initialization.
TRUE:Data Link Layer classification has completed initialization.

pse_dll_enabled

A variable output by the PSE state diagram (Figure 33–9) to indicate if the PSE Data Link Layer classification mechanism is enabled.
Values: FALSE:PSE Data Link Layer classification is not enabled.
TRUE:PSE Data Link Layer classification is enabled.

Change variable pse_dll_power_type in Section 33.6.3.3 as follows:

pse_dll_power_type

A control variable that indicates the Type of the PSE by which the PD is being powered.
Values: 1: PSE is a Type 1 PSE (default).
2: PSE is a Type 2 PSE.
3: PSE is a Type 3 PSE.
4: PSE is a Type 4 PSE.

pse_dll_ready

An implementation-specific control variable that indicates that the PSE has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).
Values:FALSE:Data Link Layer classification has not completed initialization.
TRUE:Data Link Layer classification has completed initialization.

~~pse_power_type~~

pse_power_level

A control variable output by the PD state diagram (Figure 33–16) to indicate the Type of PSE by which it is being powered.

A summary cross-references between the DTE Power via MDI classification local and remote object class attributes and the PSE and PD power control state diagrams, including the direction of the mapping, is provided in Table 33–23.

Change text in Section 33.6.3.4 as follows:

33.6.3.4 Functions

pse_power_review

This function evaluates the power allocation or budget of the PSE based on local system changes. The function returns the following variables:
PSE_NEW_VALUE:
The new maximum power value that the PSE expects the PD to draw. Actual power numbers are represented using an integer value that is encoded according to Equation (79–2), where *X* is the decimal value of PSE_NEW_VALUE.

pd_power_review

This function evaluates the power requirements of the PD based on local system changes and/or changes in the PSE allocated power value. The function returns the following variables:
PD_NEW_VALUE:
The new maximum power value that the PD wants to draw. Actual power numbers are represented using an integer value that is encoded according to Equation (79–1), where *X* is the decimal value of PD_NEW_VALUE.

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Table 33–23—Attribute to state diagram variable cross-reference

Entity	Attribute	Mapping	State diagram variable
oLldpXdot3LocSystemsGroup Object Class			
PSE	aLldpXdot3LocPDRequestedPowerValue	⇐	PDRequestedPowerValueEcho
	aLldpXdot3LocPSEAllocatedPowerValue	⇐	PSEAllocatedPowerValue
	aLldpXdot3LocReady	⇐	pse_dll_ready
PD	aLldpXdot3LocPDRequestedPowerValue	⇐	PDRequestedPowerValue
	aLldpXdot3LocPSEAllocatedPowerValue	⇐	PSEAllocatedPowerValueEcho
	aLldpXdot3LocReady	⇐	pd_dll_ready
oLldpXdot3RemSystemsGroup Object Class			
PSE	aLldpXdot3RemPDRequestedPowerValue	⇒	MirroredPDRequestedPowerValue
	aLldpXdot3RemPSEAllocatedPowerValue	⇒	MirroredPSEAllocatedPowerValueEcho
	aLldpXdot3RemPowerType Value[1] 11 01	 Þ Þ	pd_dll_power_type Value[a][1] 01 10
PD	aLldpXdot3RemPSEAllocatedPowerValue	⇒	MirroredPSEAllocatedPowerValue
	aLldpXdot3RemPDRequestedPowerValue	⇒	MirroredPDRequestedPowerValueEcho
	aLldpXdot3RemPowerType Value[a][1] 10 00	 ⇒ ⇒	pse_dll_power_type Value[a][1] 01 10

[1]Other value combinations mapping from aLldpXdot3RemPowerType to pd_dll_power_type or pse_dll_power_type are not possible.

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33.6.3.5 State diagrams

Editor's Note: New Type 3 and Type 4 LLDP features Request power down and Autoclass need to be included in state diagrams.

The general state change procedure for PSEs is shown in Figure 33–27.

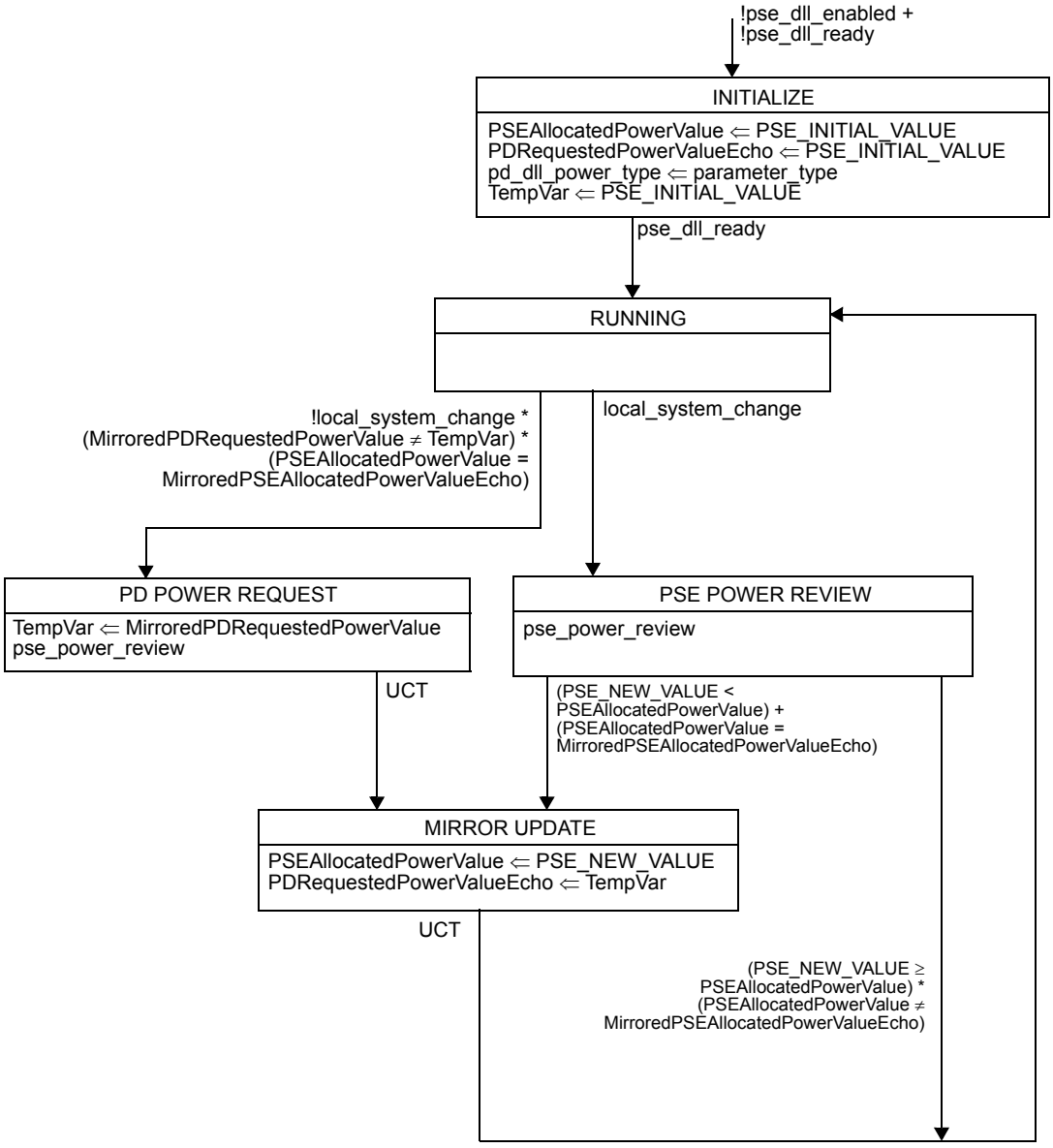

Figure 33–27—PSE power control state diagram

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The general state change procedure for PDs is shown in Figure 33–28.

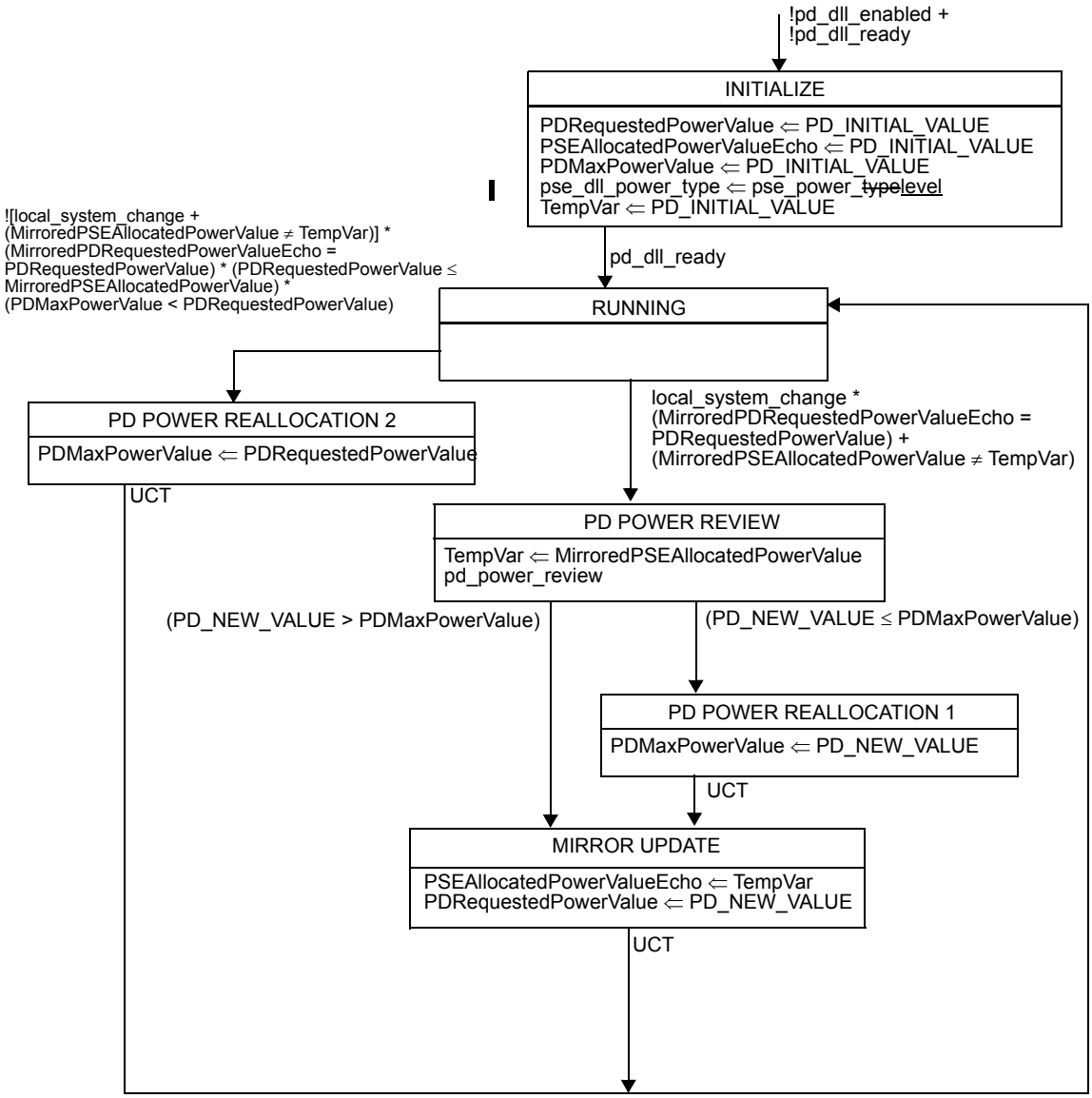

Figure 33–28—PD power control state diagram

33.6.4 State change procedure across a link

The PSE and PD utilize the LLDPDUs to advertise their various attributes to the other entity.

The PD may request a new power value through the aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17) attribute in the oLldpXdot3LocSystemsGroup object class. The request appears to the PSE as a change to the aLldpXdot3RemPDRequestedPowerValue (30.12.3.1.17) attribute in the oLldpXdot3RemSystemsGroup object class.

The PSE responds to the PD's request through the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.18) attribute in the oLldpXdot3LocSystemsGroup object class. The PSE also copies the value of the aLldpXdot3RemPDRequestedPowerValue (30.12.3.1.17) in the oLldpXdot3RemSystemsGroup object class

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to the aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17) in the oLldpXdot3LocSystemsGroup object class. This appears to the PD as a change to the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.18) attribute in the oLldpXdot3RemSystemsGroup object class.

The PSE may allocate a new power value through the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.18) attribute in the oLldpXdot3LocSystemsGroup object class. The request appears to the PD as a change to the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.18) attribute in the oLldpXdot3RemSystemsGroup object class. The PD responds to a PSE's request through the aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17) attribute in the oLldpXdot3LocSystemsGroup object class. The PD also copies the value of the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.18) attribute in the oLldpXdot3RemSystemsGroup object class to the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.18) attribute in the oLldpXdot3LocSystemsGroup object class. This appears to the PSE as a change to the aLldpXdot3RemPDRequestedPowerValue (30.12.3.1.17) attribute in the oLldpXdot3RemSystemsGroup object class.

The state diagrams describe the behavior above.

33.6.4.1 PSE state change procedure across a link

A PSE is considered to be in sync with the PD when the value of PSEAllocatedPowerValue matches the value of MirroredPSEAllocatedPowerValueEcho. When the PSE is not in sync with the PD, the PSE is only allowed to decrease its power allocation.

During normal operation, the PSE is in the RUNNING state. If the PSE wants to initiate a change in the PD allocation, the local_system_change is asserted and the PSE enters the PSE POWER REVIEW state, where a new power allocation value, PSE_NEW_VALUE, is computed. If the PSE is in sync with the PD or if PSE_NEW_VALUE is smaller than PSEAllocatedPowerValue, it enters the MIRROR UPDATE state where PSE_NEW_VALUE is assigned to PSEAllocatedPowerValue. It also updates PDRequestedPowerValueEcho and returns to the RUNNING state.

If the PSE sees a change to the previously stored MirroredPDRequestedPowerValue, it recognizes a request by the PD to change its power allocation. It entertains this request only when it is in sync with the PD. The PSE examines the request by entering the PD POWER REQUEST state. A new power allocation value, PSE_NEW_VALUE, is computed. It then enters the MIRROR UPDATE state where PSE_NEW_VALUE is assigned to PSEAllocatedPowerValue. It also updates PDRequestedPowerValueEcho and returns to the RUNNING state.

33.6.4.2 PD state change procedure across a link

A PD is considered to be in sync with the PSE when the value of PDRequestedPowerValue matches the value of MirroredPDRequestedPowerValueEcho. The PD is not allowed to change its maximum power draw or the requested power value when it is not in sync with the PSE.

During normal operation, the PD is in the RUNNING state. If the PD sees a change to the previously stored MirroredPSEAllocatedPowerValue or local_system_change is asserted by the PD so as to change its power allocation, it enters the PD POWER REVIEW state. In this state, the PD evaluates the change and generates an updated power value called PD_NEW_VALUE. If PD_NEW_VALUE is less than PDMaxPowerValue, it updates PDMaxPowerValue in the PD POWER REALLOCATION 1 state. The PD finally enters the MIRROR UPDATE state where PD_NEW_VALUE is assigned to PDRequestedPowerValue. It also updates PSEAllocatedPowerValueEcho and returns to the RUNNING state.

In the above flow, if PD_NEW_VALUE is greater than PDMaxPowerValue, the PD waits until it is in sync with the PSE and the PSE grants the higher power value. When this condition arises, the PD enters the PD

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POWER REALLOCATION 2 state. In this state, the PD assigns PDMaxPowerValue to PDRequestedPowerValue and returns to the RUNNING state.

33.7 Environmental

33.7.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1. In particular, the PSE shall be classified as a Limited Power Source in accordance with IEC 60950-1.

Equipment shall comply with all applicable local and national codes related to safety.

33.7.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns. The list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to verify compliance with the appropriate requirements. LAN cabling systems described in this clause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cabling and components.
c) High-energy transients coupled onto the LAN cabling system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards should be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures should be taken to verify that the intended safety features are not negated during installation of a new network or during modification of an existing network.

33.7.3 Installation and maintenance guidelines

It is a mandatory requirement that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

It is a mandatory requirement that, during installation of the cabling plant, care be taken to verify that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

33.7.4 Patch panel considerations

It is possible that the current carrying capability of a cabling cross-connect may be exceeded by a PSE. The designer should consult the manufacturers' specifications to verify compliance with the appropriate requirements.

33.7.5 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to a PSE or PD. Other than voice signals, the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard, the following maximums generally apply:

Battery voltage to a telephone line is generally 56 Vdc, applied to the line through a balanced 400 Ω source impedance. Ringing voltage is a composite signal consisting of an AC component and a DC component. The

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AC component is up to 175 Vp at 20 Hz to 60 Hz with a 100 Ω source resistance. The DC component is 56 Vdc with 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Application of any of the above voltages to the PI of a PSE or a PD shall not result in any safety hazard.

33.7.6 Electromagnetic emissions

The PD and PSE powered cabling link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

33.7.7 Temperature and humidity

The PD and PSE powered cabling link segment is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling. Specific requirements and values for these parameters are beyond the scope of this standard.

33.7.8 Labeling

It is recommended that the PSE or PD (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Power classification and power level in terms of maximum current drain over the operating voltage range, 36 V to 57 V, applies for PD only
b) Port type (e.g., 100BASE-TX, TIA Category, or ISO Class)
c) Any applicable safety warnings
d) “PSE” or “PD” as appropriate
e) Type (e.g., “Type 1” or “Type 2”)

33.8 Protocol implementation conformance statement (PICS) proforma for Clause 33, DTE Power via MDI[1]

33.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 33, DTE Power via MDI, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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33.8.2 Identification

33.8.2.1 Implementation identification

Change text in 33.8.2.1 as follows:

Supplier[1]	
Contact point for ~~e~~inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

33.8.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-201x, Clause 33, DTE Power via MDI
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-201x.)	
Date of Statement	

33.8.2.3 PD Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PDT2	Type 2 PD implementation	33.3.2	PD is Type 2	O	Yes [ ] No [ ]
*PDCL	PD Classification	33.3.5	PD supports classification	PDT2:M	Yes [ ] No [ ]
*PDCL2	Implementation supports 2-Event class signature	33.3.5	PD supports 2-Event class signature	PDT2:M	Yes [ ] No [ ]
*DLLC	Implementation supports Data Link Layer classification	33.6	PD supports Data Link Layer classification	PDT2:M	Yes [ ] No [ ]

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33.8.2.4 PSE Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PSET1	Type 1 PSE implementation	33.1.4	Optional	O	Yes [ ] No [ ]
*PSET2	Type 2 PSE implementation	33.1.4	Optional	O	Yes [ ] No [ ]
*MID	Midspan PSE	33.2.1	PSE implemented as a midspan device	O/1	Yes [ ] No [ ]
*MIDA	Alternative A Midspan PSE	33.2.2	Midspan PSE implements Alternative A	MID:O:2	Yes [ ] No [ ]
*MAN	PSE supports management registers accessed through MII Management Interface	33.5	Optional	O	Yes [ ] No [ ]
*CL	Implementation supports Physical Layer classification	33.2.6	Optional	O/1	Yes [ ] No [ ]
*DLLC	Implementation supports Data Link Layer classification	33.6	PSE supports Data Link Layer classification	O	Yes [ ] No [ ]
*1EPLC	Implementation supports ~~1-Event~~Single-Event Physical Layer classification	33.2.6.1	Optional	O	Yes [ ] No [ ]
*2EPLC	Implementation supports 2-Event Physical Layer classification	33.2.6.2	Optional	O	Yes [ ] No [ ]
*PA	Power Allocation	33.2.8	PSE implements power supply allocation	O	Yes [ ] No [ ]
*PCA	Pair control ability—PSE supports the option to control which PSE Pinout is used	33.5.1.1.5	Optional	O	Yes [ ] No [ ]
*AC	Monitor AC MPS	33.2.9.1.1	PSE monitors for AC MPS	O.3	Yes [ ] No [ ]
*DC	Monitor DC MPS	33.2.9.1.2	PSE monitors for DC MPS	O.3	Yes [ ] No [ ]

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33.8.3 PICS proforma tables for DTE Power via MDI

33.8.3.1 Common device features

Item	Feature	Subclause	Value/Comment	Status	Support
COM1	Compatibility considerations.	33.1.2	PDs and PSEs compatible at their PIs	M	Yes [ ]
COM2	Type 2 operation cabling		DC loop resistance 25 Ω or less. Requirement satisfied by category 5e components (cables, cords, and connectors)	M	Yes [ ]
COM3	Resistance unbalance	33.1.4.2	3 % or less	M	Yes [ ]

33.8.3.2 Power sourcing equipment

Item	Feature	Subclause	Value/Comment	Status	Support
PSE1	PSE location	33.2.1	Requirements apply equally to Endpoint and Midspan PSE unless otherwise stated	M	Yes [ ]
PSE2	Alternative A and Alternative B	33.2.3	Implement either Alternative A or Alternative B or both but not operate on same link segment simultaneously	M	Yes [ ] N/A [ ]
PSE3	PSE behavior	33.2.4	In accordance with state diagrams shown in Figure 33–9, Figure 33–9 continued, and Figure 33–10e	M	Yes [ ]
PSE4	Detection, classification, and turn on timing	33.2.4.1	In accordance with Table 33–4, Table 33–10, and Table 33–11	M	Yes [ ]
PSE5	Backoff voltage	33.2.4.1	Not greater than V_{Off}	M	Yes [ ]
PSE6	PSE variable definition permutations	33.2.4.4	Meet at least one allowable definition described in Table 33–3	M	Yes [ ]
PSE7	Type 2 PSE mutual identification	33.2.4.6	When powering a Type 2 PD, assigns a value of '2' to parameter_type if mutual identification is complete	PSET2: M	Yes [ ] N/A [ ]
PSE8	Type 2 PSE powering a Type 1 PD	33.2.4.6	Meets the PI electrical requirements of a Type 1 PSE, but may choose to meet the electrical requirements of a Type 2 PSE for I_{Con}, I_{LIM}, T_{LIM}, and P_{Type}	PSET2: M	Yes [ ] N/A [ ]
PSE9	Applying power	33.2.5	Not until a PD requesting power has been successfully detected	M	Yes [ ]
PSE10	Power pairs	33.2.5	Power supplied on the same pairs as those used for detection	M	Yes [ ]
PSE11	Detecting PDs	33.2.5.1	Performed via the PSE PI	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSE12	PSE presents non-valid signature	33.2.5.1	As defined in Table 33–15	M	Yes [ ]
PSE13	Open circuit voltage and short circuit current	33.2.5.1	Meet specifications for V_{oc} and I_{sc} in Table 33–4	M	Yes [ ]
PSE14	Backdriven current	33.2.5.1	Not be damaged by up to 5 mA over the range of V_{Port_PSE}	M	Yes [ ]
PSE15	Output capacitance	33.2.5.1	C_{out} in Table 33–11	M	Yes [ ]
PSE16	Detection voltage with a valid PD signature connected	33.2.5.2	Meets V_{valid} in Table 33–4	M	Yes [ ]
PSE17	Detection voltage measurements	33.2.5.2	At least two that create at least ΔV_{test} difference	M	Yes [ ]
PSE18	Control slew rate when switching detection voltages	33.2.5.2	Less than V_{slew} in Table 33–4	M	Yes [ ]
PSE19	Accept as a valid signature	33.2.5.3	R_{good} and C_{good}, with up to V_{os} max and I_{os} max as defined in Table 33–5	M	Yes [ ]
PSE20	Reject as an invalid signature	33.2.5.4	Resistance less than R_{bad} min, resistance greater than R_{bad} max, or capacitance greater than C_{bad} min	M	Yes [ ]
PSE21	Classification permutations	33.2.6	Meet one allowable permutation in Table 33–8	M	Yes [ ]
PSE22	Type 1 PSE does not implement Physical Layer classification	33.2.6	Assign all PDs to Class 0	PSET1: M	Yes [ ] N/A [ ]
PSE23	Type 1 PSE failure to complete classification	33.2.6	Return to IDLE state or assign PD to Class 0	PSET1: M	Yes [ ] N/A [ ]
PSE24	Type 2 PSE failure to complete classification	33.2.6	Return to IDLE state	PSET2: M	Yes [ ] N/A [ ]
PSE25	Provide V_{Class} for ~~1-Event~~Single-Event Physical Layer classification	33.2.6.1	Limited to I_{Class_LIM} as defined by Table 33–10	1EPLC: M	Yes [ ] N/A [ ]
PSE26	Classification polarity for ~~1-Event~~Single-Event Physical Layer classification	33.2.6.1	Same as V_{Port_PSE}	1EPLC: M	Yes [ ] N/A [ ]
PSE27	Classification timing for ~~1-Event~~Single-Event Physical Layer classification	33.2.6.1	In accordance with T_{pdc} in Table 33–10	1EPLC: M	Yes [ ] N/A [ ]
PSE28	Measurement result of ~~1-Event~~Single-Event Physical Layer classification I_{Class}	33.2.6.1	Classify PD according to observed current based on Table 33–9	1EPLC: M	Yes [ ] N/A [ ]
PSE29	Measurement timing of ~~1-Event~~Single-Event Physical Layer classification I_{Class}	33.2.6.1	Measurement taken after the minimum relevant class event timing in Table 33–10	1EPLC: M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSE30	Class 4 result for ~~1-Event~~Single-Event Physical Layer classification with a Type 1 PSE	33.2.6.1	Assign the PD to Class 0	PSET1: M	Yes [ ] N/A [ ]
PSE31	Type 1 PSE ~~1-Event~~Single-Event Physical Layer classification if I_{Class} is in the range of I_{Class_LIM}	33.2.6.1	Return to IDLE state or assign PD to Class 0	PSET1: M	Yes [ ] N/A [ ]
PSE32	Type 2 PSE ~~1-Event~~Single-Event Physical Layer classification if I_{Class} is in the range of I_{Class_LIM}	33.2.6.1	Return to IDLE state	PSET2: M	Yes [ ] N/A [ ]
PSE33	In the CLASS_EV1 and CLASS_EV2 states, provide V_{Class}	33.2.6.2	As defined in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE34	Classification timing in CLASS_EV1 state	33.2.6.2	In accordance with T_{CLE1} in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE35	In the CLASS_EV1 and CLASS_EV2 states, measurement result I_{Class}	33.2.6.2	Classify PD according to Table 33–9	2EPLC: M	Yes [ ] N/A [ ]
PSE36	In the MARK_EV1 and MARK_EV2 states, provide V_{Mark}	33.2.6.2	In accordance with Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE37	Classification timing in MARK_EV1	33.2.6.2	In accordance with T_{ME1} in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE38	Classification timing in CLASS_EV2 state	33.2.6.2	In accordance with T_{CLE2} in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE39	Classification timing in MARK_EV2 state	33.2.6.2	In accordance with T_{ME2} in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE40	Type 2 PSE 2-Event Physical Layer classification if I_{Class} is greater than or equal to I_{Class_LIM} min	33.2.6.2	Returns to IDLE state	2EPLC: M	Yes [ ] N/A [ ]
PSE41	Current limitation during class events	33.2.6.2	Meet I_{Class_LIM}	2EPLC: M	Yes [ ] N/A [ ]
PSE42	Current limitation during mark events	33.2.6.2	Meet I_{Mark_LIM}	2EPLC: M	Yes [ ] N/A [ ]
PSE43	Measurement timing of 2-Event Physical Layer classification I_{Class}	33.2.6.2	Taken after the minimum relevant class event timing in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE44	Class event and mark event voltages polarity	33.2.6.2	Same as V_{Port_PSE}	2EPLC: M	Yes [ ] N/A [ ]
PSE45	Voltage level at PI when transition to POWER_ON state	33.2.6.2	Completes 2-Event classification and transitions to POWER_ON with PI voltage greater than or equal to V_{Mark} min	2EPLC: M	Yes [ ] N/A [ ]
PSE46	Return to IDLE state	33.2.6.2	Maintains PI voltage at V_{Reset} for at least T_{Reset} min before starting new detection cycle	2EPLC: M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSE47	Power supply output		When the PSE provides power to the PI, conforms with Table 33–11	M	Yes [ ]
PSE48	Load regulation	33.2.7.1	Met with (I_{Hold} max × V_{Port_PSE} min) to P_{Type} min load step at a rate of change of at least 15 mA/µs max	M	Yes [ ]
PSE49	Voltage transients	33.2.7.1	Limited to 3.5 V/µs max for load changes up to 35 mA/µs	M	Yes [ ]
PSE50	Voltage transients (30 µs to 250 µs)	33.2.7.2	No less than K_{Tran_lo} below V_{Port_PSE} min and meet requirements of 33.2.7.7.	PSET2: M	Yes [ ]
PSE51	Voltage transients (greater than 250 µs)	33.2.7.2	Meet V_{Port_PSE} specification	M	Yes [ ]
PSE52	Power feeding ripple and noise	33.2.7.3	Met for common-mode and/or pair-to-pair noise values for power outputs from (I_{Hold} max × V_{Port_PSE} min) to P_{Type} min at static operating V_{Port_PSE}	M	Yes [ ]
PSE53	AC current waveform parameters	33.2.7.4	I_{Peak} minimum equals Equation (33–4) for T_{CUT} minimum and 5% duty cycle minimum.	M	Yes [ ]
PSE54	Inrush current limit	33.2.7.5	PSE limits the maximum current sourced at the PI	M	Yes [ ]
PSE55	Inrush current template	33.2.7.5	Current sourced does not exceed the PSE inrush template in Figure 33–13	M	Yes [ ]
PSE56	Short circuit condition	33.2.7.7	Remove power from PI before I_{PSEUT} is exceeded. Equation (33–6) and Figure 33–14.	M	Yes [ ]
PSE57	Short circuit current and time	33.2.7.7	In accordance with I_{LIM} and T_{LIM} in Table 33–11	M	Yes [ ]
PSE58	Short circuit power removal	33.2.7.7	Begins within T_{LIM} in Table 33–11	M	Yes [ ]
PSE59	Turn off time	33.2.7.8	Applies to the discharge time from V_{Port_PSE} to V_{Off} with a test resistor of 320 kΩ attached to the PI.	M	Yes [ ]
PSE60	Turn off voltage	33.2.7.9	Applies to the PI voltage in the IDLE state	M	Yes [ ]
PSE61	Current unbalance	33.2.7.11	Applies to the two conductors of a power pair over the current load range in accordance with I_{unb} in Table 33–11.	M	Yes [ ]
PSE62	Type 2 PSEs in the presence of (I_{unb} / 2)	33.2.7.11	Meet the requirements of 25.4.5	PSET2: M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSE63	Power allocation	33.2.8	Not be based solely on historical data of power consumption of the attached PD	PA:M	Yes [ ] N/A [ ]
PSE64	PSE monitoring AC MPS component	33.2.9.1.1	Meets "AC Signal parameters" and "PSE PI voltage during AC disconnect detection" parameters in Table 33–12	AC:M	Yes [ ] N/A [ ]
PSE65	PSE AC MPS component present	33.2.9.1.1	When AC impedance at the PI is equal to or lower than $\|Z_{ac1}\|$ in Table 33–12	AC:M	Yes [ ] N/A [ ]
PSE66	PSE AC MPS component absent	33.2.9.1.1	When AC impedance at the PI equal to or greater than $\|Z_{ac2}\|$ in Table 33–12	AC:M	Yes [ ] N/A [ ]
PSE67	Power removal	33.2.9.1.1	When AC MPS has been absent for a time duration greater than T_{MPDO}	AC:M	Yes [ ] N/A [ ]
PSE68	PSE DC MPS component present	33.2.9.1.2	I_{Port} is greater than or equal to I_{Hold} max for at least T_{MPS} min as specified in Table 33–11	DC:M	Yes [ ] N/A [ ]
PSE69	PSE DC MPS component absent	33.2.9.1.2	I_{Port} is less than or equal to I_{Hold} min as specified in Table 33–11	DC:M	Yes [ ] N/A [ ]
PSE70	Power removal	33.2.9.1.2	When DC MPS has been absent for a time duration greater than T_{MPDO}	DC:M	Yes [ ] N/A [ ]
PSE71	Not remove power	33.2.9.1.2	When the DC current is greater than or equal to I_{Hold} max continuously for at least T_{MPS} every $T_{MPS} + T_{MPDO}$	DC:M	Yes [ ] N/A [ ]

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33.8.3.3 Powered devices

Change text in section 33.8.3.3 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
PD1	Accept power	33.3.1	On either set of PI conductors	M	Yes [ ]
PD2	Polarity insensitive	33.3.1	Both Mode A and Mode B per Table 33–13	M	Yes [ ]
PD3	Source power	33.3.1	The PD does not source power on its PI	M	Yes [ ]
PD4	Voltage tolerance	33.3.1	Withstand 0 V to 57 V at the PI indefinitely without permanent damage	M	Yes [ ]
PD5	Underpowered Type 2 PD	33.3.2	If PD does not successfully observe 2-Event Physical Layer classification or Data Link Layer classification, conforms to Type 1 PD power restrictions and provides the user with an active indication if underpowered	PDT2:M	Yes [ ] N/A [ ]
PD6	Current unbalance	33.3.2	Type 2 PDs meet the requirements of 25.4.5 in presence of (I_{unb}/2)	PDT2:M	Yes [ ] N/A [ ]
PD7	PD behavior	33.3.3	According to state diagram shown in Figure 33–16	M	Yes [ ]
PD8	Valid and non-valid detection signatures	33.3.4	Presented between positive V_{PD} and negative V_{PD} on each set of pairs defined in 33.3.1	M	Yes [ ]
PD9	Non-valid detection signature	33.3.4	When powered, present an invalid signature on the set of pairs not drawing power	M	Yes [ ]
PD10	Valid detection signature	33.3.4	Characteristics defined in Table 33–14	M	Yes [ ]
PD11	Non-valid detection signature	33.3.4	Exhibit one or both of the characteristics described in Table 33–15	M	Yes [ ]
PD12	PD classifications	33.3.5	Meets at least one permutation listed in Table 33–8	PDCL:M	Yes [ ]
PD13	PD implementing 2-Event class signature	33.3.5.1	Returns Class 4	PDCL2:M	Yes [ ] N/A [ ]
PD14	Type 2 PD classification behavior	33.3.5.1	Conforms to electrical specifications in Table 33–17	PDT2:M	Yes [ ] N/A [ ]
PD15	Classification signature	33.3.5.1	As defined in Table 33–16	PDCL:M	Yes [ ] N/A [ ]
PD16	Classification signature	33.3.5.1	One classification signature during classification	PDCL:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PD17	2-Event class signature	33.3.5.2	Class 4 in accordance with the maximum power draw as specified in Table 33–18	PDCL2:M	Yes [ ] N/A [ ]
PD18	2-Event class signature behavior	33.3.5.2	As defined in Table 33–17	PDCL2:M	Yes [ ] N/A [ ]
PD19	Type 2 PD electrical requirements	33.3.5.2	As defined by Table 33–18 of the Type defined in its pse_power_type state variable	PDT2:M	Yes [ ] N/A [ ]
PD20	Mark event current and 2-Event class signature	33.3.5.2.1	Draw I_{Mark} and present a non-valid detection signature as defined in Table 33–15	PDCL2:M	Yes [ ] N/A [ ]
PD21	Mark event current limits	33.3.5.2.1	Not exceed I_{Mark} when voltage at the PI enters V_{Mark} as defined in Table 33–17	PDCL2:M	Yes [ ] N/A [ ]
PD22	PD current draw	33.3.5.2.1	I_{Mark} until the PD transitions from DO_MARK_EVENT state to the IDLE state	PDCL2:M	Yes [ ] N/A [ ]
PD23	PSE identification	33.3.6	Identify as Type 1 or Type 2 (see Figure 33–16)	PDT2:M	Yes [ ]
PD24	PD power supply	33.3.7	Operate within the characteristics in Table 33–18	M	Yes [ ]
PD25	PD turn on voltage	33.3.7.1	PD turns on at a voltage less than or equal to V_{On_PD}	M	Yes [ ]
PD26	PD stay on voltage	33.3.7.1	Stay on for all voltages in the range of V_{Port_PD}	M	Yes [ ]
PD27	PD turn off voltage	33.3.7.1	Turn off at a voltage less than V_{Port_PD} min and greater than V_{Off_PD}	M	Yes [ ]
PD28	Startup oscillations	33.3.7.1	Shall turn on or off without startup oscillations and within the first trial at any load value	M	Yes [ ]
PD29	P_{Port_PD} definition	33.3.7.2.1	When PD is fed by V_{Port_PD} min to V_{Port_PD} max with R_{Ch} (as defined in Table 33–1) in series	M	Yes [ ]
PD30	Type 2 PD input inrush current	33.3.7.3	With pse_power_type state set to 2 prior to power-on, operate as a Type 1 PD for at least T_{delay} min	PDT2:M	Yes [ ] N/A [ ]
PD31	Input inrush current	33.3.7.3	Limited by the PD if C_{port} is greater than or equal to 180 µF so that I_{Inrush_PD} max is satisfied.	M	Yes [ ]
PD32	Peak power	33.3.7.4	Not to exceed P_{Class_PD} max for more than T_{CUT} min and 5% duty cycle	M	Yes [ ]
PD33	Peak operating power	33.3.7.4	Not to exceed P_{Peak} max	M	Yes [ ]
PD34	RMS, DC, and ripple current	33.3.7.4	Bounded by Equation (33–10)	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PD35	Maximum I_{Port} for all operating V_{Port_PD}	33.3.7.4	Defined by Equation (33–11)	M	Yes [ ]
PD36	Peak transient current	33.3.7.5	Not to exceed 4.70 mA/µs in either polarity	M	Yes [ ]
PD37	Specifications for I_{PDUT}	33.3.7.5	Operate below upperbound template defined in Figure 33–18	M	Yes [ ]
PD38	Behavior during transients at the PSE PI	33.3.7.6	As specified in 33.3.7.6	M	Yes [ ]
PD39	Ripple and noise	33.3.7.7	As specified in Table 33–18 for the common-mode and/or differential pair-to-pair noise at the PD PI	M	Yes [ ]
PD40	Ripple and noise specification	33.3.7.7	For all operating voltages in the range defined by V_{Port_PD} in Table 33–18	M	Yes [ ]
PD41	Ripple and noise presence	33.3.7.7	Operates in the presence of ripple and noise generated by the PSE that appears at the PD PI	M	Yes [ ]
PD42	Classification stability	33.3.7.8	Class signature valid within T_{class} and remains valid for the duration of the classification period	M	Yes [ ]
PD43	Backfeed voltage	33.3.7.9	Mode A and Mode B per 33.3.7.9	M	Yes [ ]
PD44	Maintain power signature		PD provides a valid MPS at the PI as defined in	M	Yes [ ]
PD45	No longer require power		Remove both components of the Maintain Power Signature	M	Yes [ ]

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33.8.3.4 Electrical specifications applicable to the PSE and PD

Item	Feature	Subclause	Value/Comment	Status	Support
EL1	Conductor isolation	33.4.1	Provided between accessible external conductors including frame ground and all MDI leads	M	Yes [ ]
EL2	Strength tests for electrical isolation	33.4.1	Withstand at least one of the electrical strength tests specified in 33.4.1	M	Yes [ ]
EL3	Insulation breakdown	33.4.1	No breakdown of insulation during electrical isolation tests	M	Yes [ ]
EL4	Isolation resistance	33.4.1	At least 2 MΩ, measured at 500 Vdc after electrical isolation tests	M	Yes [ ]
EL5	Isolation and grounding requirements	33.4.1	Conductive link segments that have different requirements have those requirements provided by the port-to-port isolation of the NID	M	Yes [ ]
EL6	Environment A requirements for multiple instances of PSE and/or PD	33.4.1.1.1	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated	!MID:M	Yes [ ] N/A [ ]
EL7	Environment A requirement	33.4.1.1.1	Switch more negative conductor	M	Yes [ ] N/A [ ]
EL8	Environment B requirements for multiple instances of PSE and/or PD	33.4.1.1.2	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated	!MID:M	Yes [ ] N/A [ ]
EL9	Fault tolerance for PIs encompassed within the MDI	33.4.2	Meet requirements of the appropriate specifying clause	!MID:M	Yes [ ] N/A [ ]
EL10	Fault tolerance for PSE PIs not encompassed within an MDI	33.4.2	Meet the requirements of 33.4.2	M	Yes [ ] N/A [ ]
EL11	Common-mode fault tolerance	33.4.2	Each wire pair withstands without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity	M	Yes [ ]
EL12	The shape of the impulse for item common-mode fault tolerance	33.4.2	0.3/50 µs (300 ns virtual front time, 50 µs virtual time of half value)	M	Yes [ ]
EL13	Common-mode to differential-mode impedance balance for transmit and receive pairs	33.4.3	Exceeds Equation (33–15) for 10Mb/s PHYs and Equation (33–16) for 100Mb/s or greater PHYs	M	Yes [ ]
EL14	Common-mode AC output voltage	33.4.4	Magnitude while transmitting data and with power applied does not exceed 50 mV peak when operating at 10 Mb/s and 50 mV peak-to-peak when operating at 100 Mb/s or greater	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
EL15	Frequency range for common-mode AC output voltage measurement	33.4.4	From 1 MHz to 100 MHz	M	Yes [ ]
EL16	Common-mode AC output voltage measurement	33.4.4	While the PHY is transmitting data, the PSE or PD is operating, and with the enumerated PSE load or PD source	M	Yes [ ]
EL17	Noise from an operating PSE or PD to the differential transmit and receive pairs	33.4.6	Does not exceed 10 mV peak-to-peak measured from 1 MHz to 100 MHz under the conditions specified in 33.4.4	M	Yes [ ]
EL18	Return loss requirements	33.4.7	Specified in 14.3.1.3.4 for a 10 Mb/s PHY, in ANSI X3.263:1995 for a 100 Mb/s PHY, and 40.8.3.1 for a 1000 Mb/s PHY	M	Yes [ ]
EL19	100BASE-TX Type 2 Endpoint PSE and PD channel unbalance	33.4.8	Meet requirements of Clause 25 in the presence of (I_{unb}/2)	M	Yes [ ] N/A [ ]

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33.8.3.5 Electrical specifications applicable to the PSE

Change section 33.8.3.5 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL1	Short circuit fault tolerance	33.4.2	Any wire pair withstands any short circuit to any other pair for an indefinite amount of time	M	Yes [ ]
PSEEL2	Magnitude of short circuit current	33.4.2	Does not exceed I_{LIM} max	M	Yes [ ]
PSEEL3	Limitation of electromagnetic interference.	33.4.5	PSE complies with applicable local and national codes	M	Yes [ ]
PSEEL4	Alternative A Type 2 Midspan PSEs that support 100BASE-TX	33.4.8	Enforce channel unbalance currents less than or equal to Type 1 Iunb (see Table 33–11) or meet 33.4.9.2.	MIDA: M	Yes [ ] N/A [ ]
PSEEL5	Insertion of Midspan at FD	33.4.9	Comply with the guidelines specified in 33.4.9 items a) and b)	MID:M	Yes [ ] N/A [ ]
PSEEL6	Resulting “channel”	33.4.9	Installation of a Midspan PSE does not increase the length to more than 100 m as defined in ISO/IEC 11801.	MID:M	Yes [ ] N/A [ ]
PSEEL7	Configurations with Midspan PSE	33.4.9	Not alter transmission requirements of the “permanent link”	MID:M	Yes [ ] N/A [ ]
PSEEL8	DC continuity in power injecting pairs	33.4.9	Does not provide DC continuity between the two sides of the segment for the pairs that inject power	MID:M	Yes [ ] N/A [ ]
PSEEL9	Midspan PSE inserted as a “connector” or “telecom outlet”	33.4.9.1	Meet transmission parameters NEXT, insertion loss, and return loss	MID:M	Yes [ ] N/A [ ]
PSEEL10	Midspan PSE NEXT	33.4.9.1.1	Meet values detemined by Equation (33–18) from 1 MHz to 100 MHz, but not greater than 65 dB	MID:M	Yes [ ] N/A [ ]
PSEEL11	Midspan PSE Insertion Loss	33.4.9.1.2	Meet values determined by Equation (33–19) from 1 MHz to 100 MHz, but not less than 0.1 dB	MID:M	Yes [ ] N/A [ ]
PSEEL12	Midspan PSE Return Loss	33.4.9.1.3	Meet or exceed values in Table 33–20 for transmit and receive pairs from 1 MHz to 100 MHz	MID:M	Yes [ ] N/A [ ]
PSEEL13	Work area or equipment cable Midspan PSE	33.4.9.1.4	Meet the requirements of this clause and the specifications for a Category 5 (jumper) cord as specified in ISO/IEC 11801-2002 or ~~ANSI/TIA-568-C.2~~ ANSI/TIA/EIA-568-A:1995 for insertion loss, NEXT, and return loss for transmit and receive pairs	MID:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL14	Alternative A Midspan PSE signal path requirements	33.4.9.2	Exceed transfer function gain expressed in Equation (33–20) from 0.10 MHz to 1 MHz at the pins of the PI used as 100BASE-TX transmit pins	MIDA: M	Yes [ ] N/A [ ]
PSEEL15	Alternative A Midspan PSE signal path requirements bias current	33.4.9.2	Met with DC bias current between 0 mA and (I_{unb}/2)	MIDA: M	Yes [ ] N/A [ ]

33.8.3.6 Electrical specifications applicable to the PD

Item	Feature	Subclause	Value/Comment	Status	Support
PDEL1	PD common-mode test requirement	33.4.4	The PIs that require power terminated as illustrated in Figure 33–22	M	Yes [ ]

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33.8.3.7 Management function requirements

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Management capability	33.5	Access to register definitions defined in 33.5.1 via interface described in 22.2.4 or 45.2 or equivalent	MAN:M	Yes [ ] N/A [ ]
MF2	PSE registers	33.5.1	Register address 11 for control functions and register address 12 for status functions	MAN:M	Yes [ ] N/A [ ]
MF3	Register bits latching high (LH)	33.5.1	Remain high until read via the management interface	MAN:M	Yes [ ] N/A [ ]
MF4	Latching register bit after read	33.5.1	Assumes a value based on the current state of the condition it monitors	MAN:M	Yes [ ] N/A [ ]
MF5	PSE Control register reserved bits (11.15:6)	33.5.1.1.1	Not affected by writes and return a value of zero when read	MAN:M	Yes [ ] N/A [ ]
MF6	Data Link Layer classification not supported	33.5.1.1.2	Ignore writes to bit 11.5 and return a value of zero when read	MAN* !DLLC: M	Yes [ ] N/A [ ]
MF7	Data Link Layer classification supported	33.5.1.1.2	Ignore writes to bit 11.5 and return a value of one when function cannot be disabled	MAN* DLLC: M	Yes [ ] N/A [ ]
MF8	Enable/disable Data Link Layer classification capability	33.5.1.1.2	Capability enabled by setting bit 11.5 to one and disabled by setting bit 11.5 to zero	MAN* DLLC: M	Yes [ ] N/A [ ]
MF9	Physical Layer classification not supported	33.5.1.1.3	Ignore writes to bit 11.4 and return a value of zero when read	MAN* !CL:M	Yes [ ] N/A [ ]
MF10	Physical Layer classification supported	33.5.1.1.3	Ignore writes to bit 11.4 and return a value of one when function cannot be disabled	MAN* CL:M	Yes [ ] N/A [ ]
MF11	Enable/disable Physical Layer classification	33.5.1.1.3	Function enabled by setting bit 11.4 to one and disabled by setting bit 11.5 to zero	MAN* CL:M	Yes [ ] N/A [ ]
MF12	Pair Control Ability not supported	33.5.1.1.4	Ignore writes to bits 11.3:2	MAN* !PCA:M	Yes [ ] N/A [ ]
MF13	Writes to 11.3:2 when Pair Control Ability not supported	33.5.1.1.4	Return the value that reports the supported PSE Pinout Alternative	MAN* !PCA:M	Yes [ ] N/A [ ]
MF14	Bits 11.3:2 set to '01'	33.5.1.1.4	Forces the PSE to use Alternative A	MAN* PCA:M	Yes [ ] N/A [ ]
MF15	Bits 11.3:2 set to '10'	33.5.1.1.4	Forces the PSE to use Alternative B	MAN* PCA:M	Yes [ ] N/A [ ]
MF16	Pair control ability bit (12.0)	33.5.1.1.4	A value of one sets the mr_pse_alternative variable	MAN* PCA:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MF17	PSE function disabled	33.5.1.1.5	Setting PSE Enable bits 11.1:0 to a '00', also the MDI shall function as it would if it had no PSE function	MAN:M	Yes [ ] N/A [ ]
MF18	PSE function enabled	33.5.1.1.5	Setting PSE Enable bits 11.1:0 to a '01'	MAN:M	Yes [ ] N/A [ ]
MF19	PSE enable bits (11.1:0)	33.5.1.1.5	Writing to these register bits shall set mr_pse_enable to the corresponding value: '00' = disable, '01' = enable and '10' = force power	MAN:M	Yes [ ] N/A [ ]
MF20	PSE Type electrical parameters bit (12.15)	33.5.1.2.1	Set to zero when the PSE state diagram sets the state variable set_parameter_type to 1. Set to one when set_parameter_type is set to 2	MAN:M	Yes [ ] N/A [ ]
MF21	Data Link Layer classification enabled bit (12.14)	33.5.1.2.2	Set to one when the PSE state diagram sets true pse_dll_enabled. Set to zero when the PSE state diagram sets false pss_dll_enabled	MAN:M	Yes [ ] N/A [ ]
MF22	Power denied bit (12.12)	33.5.1.2.4	A value of one indicates power has been denied or removed due to an error condition	MAN:M	Yes [ ] N/A [ ]
MF23	Power denied bit implementation	33.5.1.2.4	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]
MF24	Valid signature bit (12.11)	33.5.1.2.5	One indicates a valid signature has been detected. Set to one when mr_valid_signature transitions from FALSE to TRUE.	MAN:M	Yes [ ] N/A [ ]
MF25	Valid signature bit implementation	33.5.1.2.5	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]
MF26	Invalid signature bit (12.10)	33.5.1.2.6	One indicates an invalid signature has been detected. Set to one entering SIGNATURE_INVALID state	MAN:M	Yes [ ] N/A [ ]
MF27	Invalid signature bit implementation	33.5.1.2.6	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]
MF28	Short circuit bit (12.9)	33.5.1.2.7	Bit indicates a short circuit condition has been detected. Set to one entering ERROR_DELAY state.	MAN:M	Yes [ ] N/A [ ]
MF29	Short circuit bit implementation	33.5.1.2.7	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MF30	Overload bit (12.8)	33.5.1.2.8	Bit indicates an overload condition has been detected. Set to one when entering the ERROR_DELAY_OVER state	MAN:M	Yes [ ] N/A [ ]
MF31	Overload bit implementation	33.5.1.2.8	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]
MF32	MPS absent bit (12.7)	33.5.1.2.9	Bit indicates an MPS Absent condition has been detected. Set to one when transitions directly from POWER_ON to IDLE state when MPS is absent for a duration greater than T_{MPDO} as specified in 33.2.9	MAN:M	Yes [ ] N/A [ ]
MF33	MPS Absent bit implementation	33.5.1.2.9	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]

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33.8.3.8 Data Link Layer classification requirements

Item	Feature	Subclause	Value/Comment	Status	Support
DLL1	Reserved fields	33.6	Reserved fields in Power via MDI TLV transmitted as zeroes and ignored upon receipt	M	Yes [ ] N/A [ ]
DLL2	Data Link Layer classification standards compliance	33.6.1	Meet mandatory parts of IEEE Std 802.1AB-2009	DLLC:M	Yes [ ] N/A [ ]
DLL3	TLV frame definitions	33.6.1	Meet requirements for Type, Length, and Value (TLV) defined in 79.3.2	DLLC:M	Yes [ ] N/A [ ]
DLL4	Control state diagrams	33.6.1	Meet state diagrams defined in 33.6.3	DLLC:M	Yes [ ] N/A [ ]
DLL5	Type 2 PSE LLDPDU	33.6.2	Transmitted within 10 seconds of Data Link Layer classification being enabled as indicated by pse_dll_enabled	DLLC:M	Yes [ ] N/A [ ]
DLL6	Type 1 PSE LLDPDU	33.6.2	Transmitted when Data Link Layer classification is ready as indicated by pse_dll_ready	DLLC:M	Yes [ ] N/A [ ]
DLL7	PD Data Link Layer classification ready	33.6.2	Set state variable pd_dll_ready within 5 min of Data Link Layer classification being enabled as indicated by pd_dll_enabled	DLLC:M	Yes [ ] N/A [ ]
DLL8	PD requested power value change	33.6.2	LLDPDU with updated “PSE allocated power value” sent within 10 seconds	DLLC:M	Yes [ ] N/A [ ]
DLL9	PSE allocated power value change	33.6.2	LLDPDU with updated “PD requested power value” sent within 10 seconds	DLLC:M	Yes [ ] N/A [ ]
DLL10	PSE power control state diagrams	33.6.3	Meet the behavior shown in Figure 33–27	DLLC:M	Yes [ ] N/A [ ]
DLL11	PD power control state diagrams	33.6.3	Meet the behavior shown in Figure 33–28	DLLC:M	Yes [ ] N/A [ ]

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33.8.3.9 Environmental specifications applicable to PSEs and PDs

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Safety	33.7.1	Conforms to IEC 60950-1:2001	M	Yes [ ]
ES2	PSE classified as a limited power source	33.7.1	In accordance with IEC 60950-1:2001	M	Yes [ ]
ES3	Safety	33.7.1	Comply with all applicable local and national codes	M	Yes [ ]
ES4	Telephony voltages	33.7.5	Application thereof described in 33.7.5 not result in any safety hazard	M	Yes [ ]
ES5	Limitation of electromagnetic interference	33.7.6	PD and PSE powered cabling comply with applicable local and national codes	M	Yes [ ]

33.8.3.10 Environmental specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEES1	Safety	33.7.1	Limited Power Source in accordance with IEC 60950-1:2001	M	Yes [ ]

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Annex 33A

(informative)

PSE-PD stability

Editor's Note: (to be removed prior to Working Group ballot) - All annexes are to be at the end of the draft. Prior to Working Group ballot, editor should move Clause 79 before Annex 33A in the frame book.

Insert 33A.3 and 33A.4 after 33A.2 as follows:

33A.3 Intra Pair Resistance Unbalance

Operation for all Types requires that the resistance unbalance be 3% or less. Resistance unbalance is a measure of the difference between the two conductors of a twisted pair in the 100 Ω balanced cabling system. Resistance unbalance is defined as in Equation (33A–1):

$$\left\{\frac{(R_{\max}-R_{\min})}{(R_{\max}+R_{\min})}\times 100\right\}_{\%} \qquad \text{(33A–1)}$$

where

$R_{\max}$ is the resistance of the channel conductor with the highest resistance

$R_{\min}$ is the resistance of the channel conductor with the lowest resistance

33A.4 Recommended Channel Requirement For pair-to-pair Resistance Unbalance in 4-Pair Operation

Four pair operation requires the specification of resistance unbalance between each two pairs of the channel, not greater than 100 milliohms or resistance unbalance of 7% whichever is a greater unbalance. Resistance unbalance between the channel pairs is a measure of the difference of resistance of the common mode pairs of conductors used for power delivery. Channel pair-to-pair resistance unbalance is defined by Equation (33A–2):

$$\left\{\frac{(R_{ch_\max}-R_{ch_\min})}{(R_{ch_\max}+R_{ch_\min})}\times 100\right\}_{\%} \qquad \text{(33A–2)}$$

Channel pair-to-pair resistance difference is defined by Equation (33A–3):

$$\{R_{ch_max}-R_{ch_min}\} \qquad \text{(33A–3)}$$

where

$R_{\text{ch_max}}$ is the sum of channel pair elements with highest common mode resistance

$R_{\text{ch_min}}$ is the sum of channel pair elements with lowest common mode resistance

Common mode resistance is the resistance of the two wires in a pair (including connectors), connected in parallel.

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NOTE—7% is the worst case pair-to-pair resistance unbalance at 100 milliohms of channel pair-to-pair resistance difference. At 100 meter channel length, the cable and connectors ensures 5.5% maximum channel pair-to-pair resistance unbalance.

33A.5 PD PI pair-to-pair current unbalance requirements

The following design guide lines may be implemented to ensure PD PI P2P_Iunb requirements are met:

$$R_{\text{Pair_PD_max}} = \left\{ \begin{array}{ll} 1.750 \times R_{\text{Pair_PD_min}} + 0.080 & \text{for PD Type 3, Class 5} \\ 1.800 \times R_{\text{Pair_PD_min}} + 0.080 & \text{for PD Type 3, Class 6} \\ 2.010 \times R_{\text{Pair_PD_min}} + 0.105 & \text{for PD Type 3, Class 7} \\ 2.200 \times R_{\text{Pair_PD_min}} + 0.125 & \text{for PD Type 3, Class 8} \end{array} \right\}_{\Omega} \quad \text{(33A–4)}$$

For PD power above the values shown in Table 33–18 and up to P_{Class}, stringent requirement will be needed to not exceed $I_{Con\text{-}2P_unb}$ by means of smaller constants α and β in the equation $R_{Pair_PD_max} = \alpha \times R_{Pair_PD_min} + \beta$.

$R_{Pair_PD_max}$ and $R_{Pair_PD_min}$ represent PD common mode input effective impedance of pairs of the same polarity. The effective resistance Z_i is the measured voltage $V_{eff_pd_i}$, divided by the current through the path as described below and as shown in the example in Figure 33A–4.

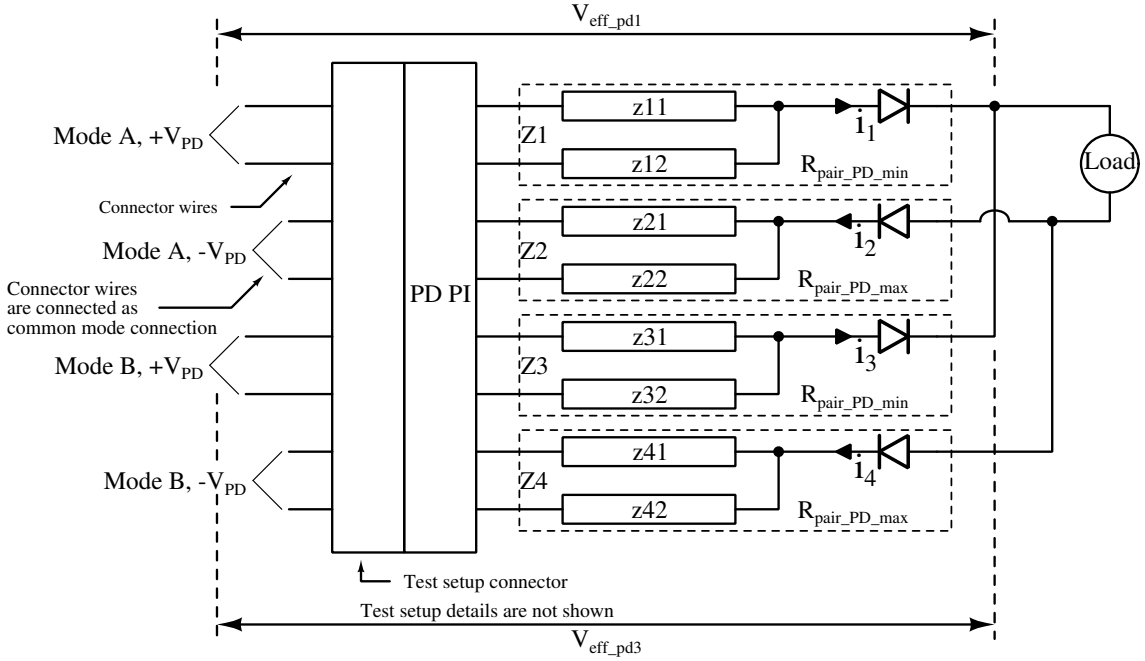

Figure 33A–4—PSE PI unbalance specification and E2EP2PRunb

Positive pairs:

$Z_1 = R_{Pair_PD_min} = V_{eff_pd1}/i_1$

$Z_3 = R_{Pair_PD_max} = V_{eff_pd3}/i_3$

Negative pairs:

$Z_2 = R_{Pair_PD_min} = V_{eff_pd2}/i_2$

$Z_4 = R_{Pair_PD_max} = V_{eff_pd4}/i_4$

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Annex 33B

(normative)

PSE PI pair-to-pair resistance/current unbalance

Editor's Note (remove prior to D2.0): Yair working to move the shalls to Clause 33. Readers are encouraged to participate.

Pair-to-pair current unbalance refers to current differences in powered pairs of the same polarity. Current unbalance can occur in positive and negative powered pairs when a PSE uses all four pairs to deliver power to a PD.

Current unbalance of a PSE shall be met with R_{load_max} and R_{load_min} as specified by Table 1. The details for derivation of R_{load_max} and R_{load_min} can be found in Annex 33E.

A compliant unbalanced load consists of the channel (cables and connectors) and the PD effective resistances.

Equation (33–4f) is described in 33.2.7.4.1, specified for the PSE, assures that E2EP2PRunb will be met in a compliant 4-pair powered system. Figure 1 illustrates the relationship between PSE PI Equation (33–4f) and R_{load_min} and R_{load_max} as specified in Table 1.

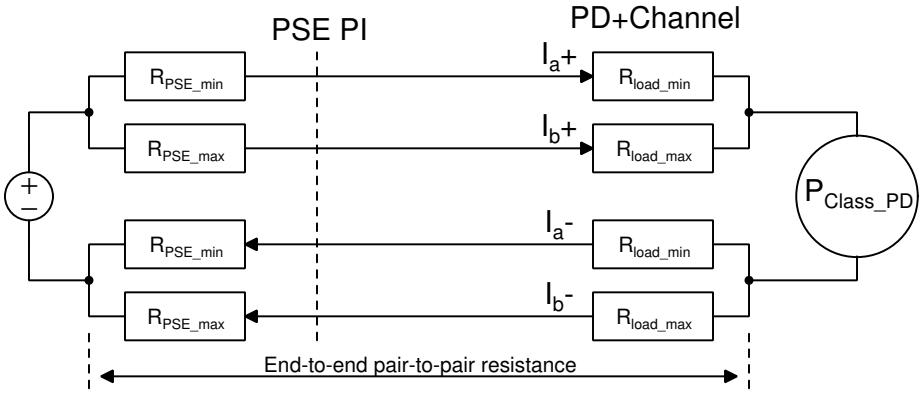

Figure 33B–1—PSE PI unbalance specification and E2EP2PRunb

Table 33B–1—R_{load_max} and R_{load_min} requirements

PSE Class	R_{load_min} (Ω)	R_{load_max} (Ω)
5	0.723	1.628
6	0.623	1.289
7	0.590	1.090
8	0.544	0.975

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Equation (33–4f) specifies the PSE effective resistances required to meet E2EP2PRunb in the presence of all compliant, unbalanced loads attached to the PSE PI. There are three alternate test methods for R_{PSE_max} and R_{PSE_min} and determining conformance to Equation (33–4f).

Measurement methods to determine R_{PSE_max} and R_{PSE_min} are defined in 33B.1, 33B.2, and 33B.3.

33B.1 Direct R_{PSE} measurement

If there is access to internal circuits, effective resistance may be determined by sourcing current in each path corresponding to maximum P_{Class} operation, and measuring the voltage across all components that contribute to the effective resistance, including circuit board traces and all components passing current to the PSE PI output connection. The effective resistance is the measured voltage V_{eff}, divided by the current through the path e.g. the effective value of $R_{PSE_min} = V_{eff1}/i_1$ as shown in Figure 2.

The two sections that follow, 33B.2 and 33B.3 illustrate two other possible measurements of PSE effective resistances for R_{pse_max} and R_{pse_min} Equation (33–4f) verification, if the internal circuits are not accessible.

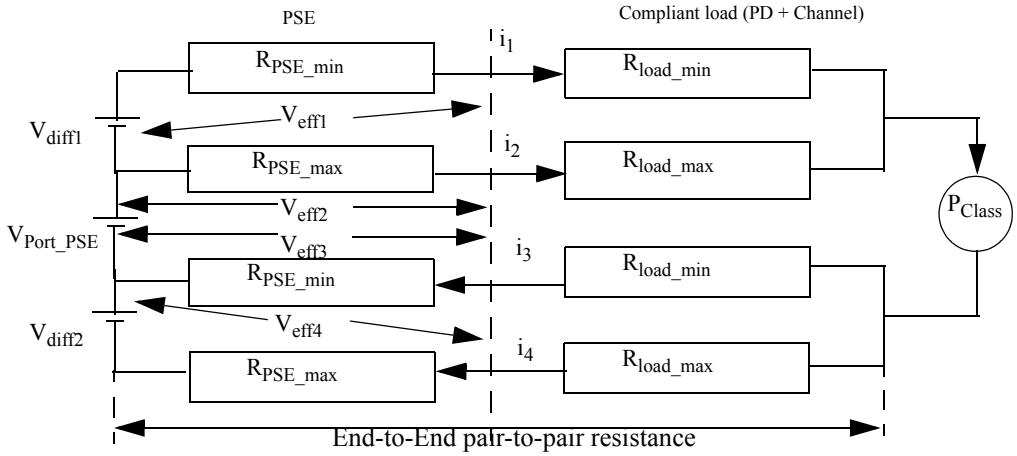

Figure 33B–2—Direct measurements of effective R_{pse_max} and R_{pse_min}

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33B.2 Effective resistance R_{PSE} measurement

Figure 3 shows a possible test circuit for effective resistance measurements on a PSE port for evaluating conformance to Equation (33–4f).

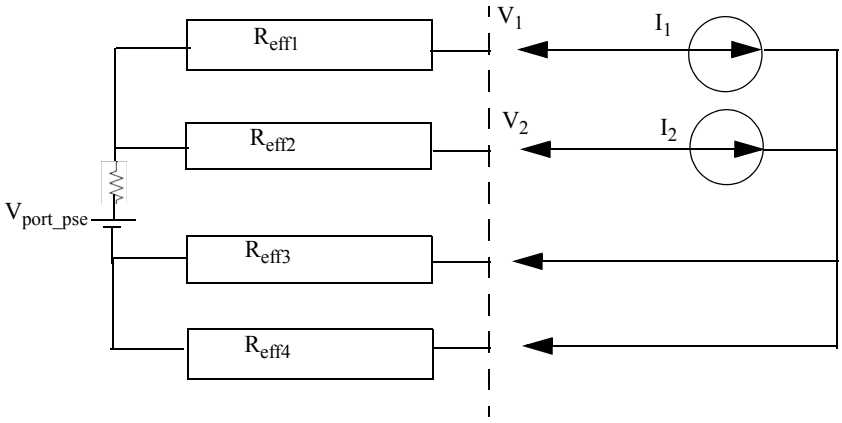

Figure 33B–3—Effective resistance test circuit

The Effective Resistance Test Procedure is described below:

1) With the PSE powered on, set the following current values
   a. 10 mA < I_2 < 50 mA
   b. $I_1 = 0.5 \times (P_{max}/V_{port}) - I_2$
2) Measure V_{diff} across V_1, V_2.
3) Reduce I_1 by 20% (=I_1'). Ensure I_2 remains unchanged.
4) Measure V_{diff}' across V_1, V_2.
5) Calculate R_{eff1}:
   $R_{eff1} = [(V_{diff}) - (V_{diff}')] / (I_1 - I_1')$
7) Repeat procedure for R_{eff2}, with I_1, I_2 values swapped.
8) Repeat procedure for R_{eff3}, R_{eff4}.
9) Evaluate compliance with Equation (33–4f).

The effective resistance test method applies to the general case. If pair-to-pair balance is actively controlled in a manner that changes effective resistance to achieve balance, then the current unbalance measurement method described in 33B.3 should be used.

33B.3 Current unbalance R_{PSE} measurement

Unbalanced load resistances must be selected per Table 1. Current unbalance must be met for any pair-to-pair resistances meeting the equation. Selected resistance values which provide adequate verification are

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dependent upon PSE circuit implementation and as such are left to the designer. Figure 4 shows a test circuit for the current unbalance measurement.

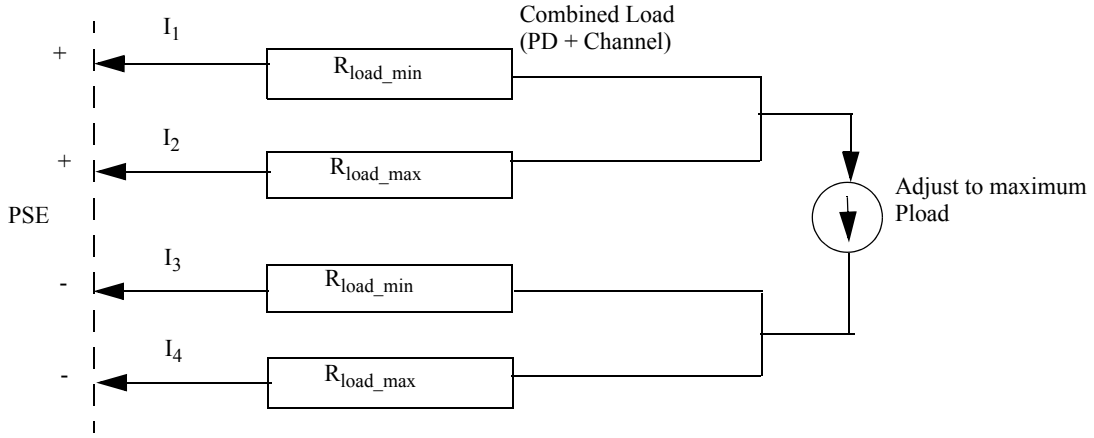

Figure 33B–4—Current unbalance test circuit

The current unbalance test method is described below:

1) Use R_{load_min} and R_{load_max} from Table 1.
2) With the PSE powered on, adjust the load for maximum power at the PSE.
3) Measure I_1, I_2.
4) Swap $R_{_max}$, $R_{_min}$, repeat steps 1 and 2.
5) Repeat for I_3, I_4.
6) Verify that the current unbalance in each case does not exceed $I_{con\text{-}2P_unb}$ minimum in Table 33–11 item 4a.

Verification of $I_{con\text{-}2P_unb}$ in step 6 confirms PSE R_{Pair_max} and R_{Pair_min} are in conformance to Equation (33–4f).

33B.4 Channel resistance with less than 0.1Ω

$I_{con_2P_unb}$ max is specified for total channel common mode pair resistance from 0.1Ω to 12.5Ω and worst case unbalance contribution by a PD. When the PSE is tested for channel common mode resistance less than 0.1 Ω, i.e. 0 Ω < R_{ch_x} < 0.1 Ω, the PSE shall be tested with (R_{load_min} - R_{ch_x}) and (R_{load_max} - R_{ch_x}).

Editor's Note: To consider the value of adding informative section to present R_{load_max} and R_{load_min} equation derivation and values.

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Annex 33C

(informative)

Autoclass

Editor's Note: Annex 33C needs information on:
- Explanation of the measurement method
- Guideline for what PDs need to do for reliable measurement
- Explain combination of L1 and LLDP Autoclass
- Simplified margin calculation

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Annex 33D

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Derivation of R_{load_max} and R_{load_min}

Editor Note: To consider the value of adding informative Annex 33E to present Rload_max and Rload_min equation derivation and values

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Annex 33E

(informative)

PD Design Guidelines for MPS

Editor's Note: This Annex to be filled with PD design guidelines for MPS.

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79. IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements

79.1 Overview

The Link Layer Discovery Protocol (LLDP) specified in IEEE Std 802.1AB-2009 is a MAC Client protocol that allows stations attached to an IEEE 802 LAN to advertise to all other stations attached to the same IEEE 802 LAN: the major capabilities provided by the system incorporating that station, the management address or addresses of the entity or entities that provide management of those capabilities, and the identification of the station's point of attachment to the IEEE 802 LAN.

The information fields in each LLDP frame are contained in a Link Layer Discovery Protocol Data Unit (LLDPDU) as a sequence of short, variable length, information elements known as TLVs that each include a type, length, and value field.

Organizationally Specific TLVs can be defined by either the professional organizations or the individual vendors that are involved with the particular functionality being implemented within a system. The basic format and procedures for defining Organizationally Specific TLVs are provided in subclause 9.6 of IEEE Std 802.1AB-2009.

79.1.1 IEEE 802.3 LLDP frame format

The IEEE 802.3 LLDP frame format is illustrated in Figure 79–1.

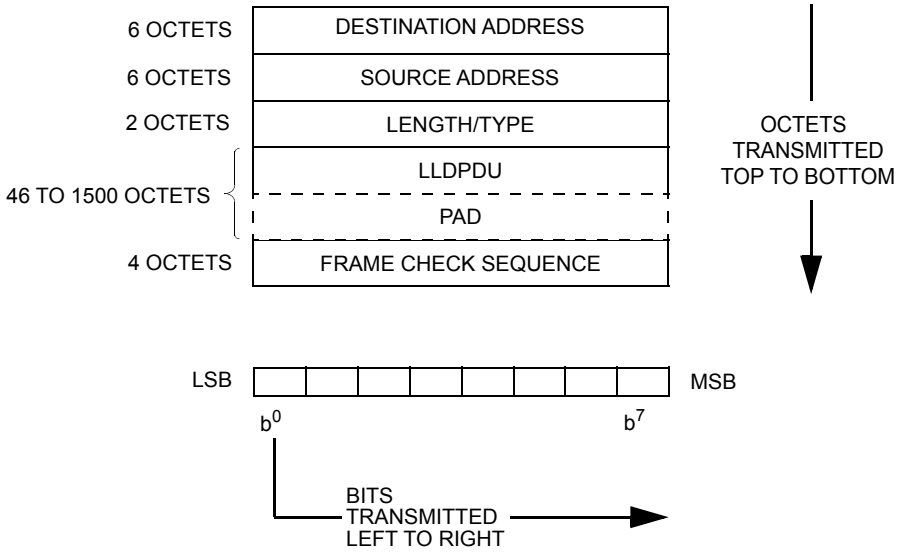

Figure 79–1—IEEE 802.3 LLDP frame format

NOTE—The illustration shows the simplest form of an IEEE 802.3 LLDP frame; i.e., where the frame has no IEEE Std 802.1Q™ tag header, or IEEE Std 802.1AE™ security tag, or any other form of encapsulation applied to it.[2]

[2]NOTES in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

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79.1.1.1 Destination Address field

The Destination Address field of an IEEE 802.3 LLDP frame contains a MAC address specified by 7.1 of IEEE Std 802.1AB-2009 (see 79.2).

79.1.1.2 Source Address field

The Source Address field of an IEEE 802.3 LLDP frame contains the 48-bit individual address of the station sending the frame.

79.1.1.3 Length/Type field

The Length/Type field of an IEEE 802.3 LLDP frame is a 2-octet field that contains the hexadecimal value: 88-CC. This value carries the Type interpretation (see 3.2.6), and has been universally assigned for LLDP.

79.1.1.4 LLDPDU field

The LLDPDU field of an IEEE 802.3 LLDP frame contains the LLDPDU which is a sequence of short, variable length, information elements known as TLVs that each include type, length, and value fields.

79.1.1.5 Pad field

A minimum MAC frame size is required for correct operation and, if necessary, a Pad field is appended after the LLDPDU field as defined in 3.2.8.

79.1.1.6 Frame Check Sequence field

The Frame Check Sequence (FCS) field contains the Frame Check Sequence, as defined in 3.2.9.

79.2 Requirements of the IEEE 802.3 Organizationally Specific TLV set

All IEEE 802.3 Organizationally Specific TLVs shall conform to the LLDPDU bit and octet ordering conventions of 8.1 of IEEE Std 802.1AB-2009.

79.3 IEEE 802.3 Organizationally Specific TLVs

The currently defined IEEE 802.3 Organizationally Specific TLVs are listed in Table 79–1. Any additions or changes to these TLVs will be included in this clause.

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Change Table 79-1 as follows:

Table 79–1—IEEE 802.3 Organizationally Specific TLVs

IEEE 802.3 subtype	TLV name	Subclause reference
1	MAC/PHY Configuration/Status	79.3.1
2	Power Via Medium Dependent Interface (MDI)	79.3.2
3	Link Aggregation (deprecated)	79.3.3
4	Maximum Frame Size	79.3.4
5	Energy-Efficient Ethernet	79.3.5
6	EEE fast wake	79.3.6
TBD	Power Via MDI Measurements	79.3.7
TBD ~~7~~–255	Reserved	—

79.3.1 MAC/PHY Configuration/Status TLV

The MAC/PHY Configuration/Status TLV is an optional TLV that identifies the following:

a) The duplex and bit-rate capability of the sending IEEE 802.3 LAN node that is connected to the physical medium.
b) The current duplex and bit-rate settings of the sending IEEE 802.3 LAN node.
c) Whether the current duplex and bit-rate settings are the result of auto-negotiation during link initiation or of manual set override action.

Figure 79–2 shows the format of this TLV.

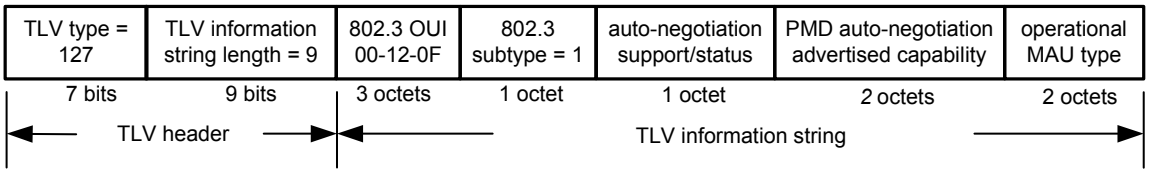

Figure 79–2—MAC/PHY configuration/status TLV format

79.3.1.1 Auto-negotiation support/status

The auto-negotiation support/status field shall contain a bitmap that identifies the auto-negotiation support and current status of the local IEEE 802.3 LAN station as defined in Table 79–2. If the auto-negotiation support bit (bit 0) is one and the auto-negotiation status bit (bit 1) is zero, the IEEE 802.3 physical media dependent sublayer (PMD) operating mode is determined by the operational Medium Attachment Unit (MAU) type field value rather than by auto-negotiation.

79.3.1.2 PMD auto-negotiation advertised capability field

The ‘PMD auto-negotiation capability’ field shall contain a 2-octet value that provides a bitmap of the ifMauAutoNegCapAdvertisedBits object, defined in IETF RFC 4836, of the sending device. Bit zero is the high order (left-most) bit in an octet string.

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Table 79–2—IEEE 802.3 auto-negotiation support/status

Bit	Function	Value/meaning	IETF RFC 4836 reference
0	Auto-negotiation support	1 = supported 0 = not supported	ifMauAutoNegSupported
1	Auto-negotiation status	1 = enabled 0 = not enabled	ifMauAutoNegAdminStatus
2–7	—	Reserved for future standardization	—

79.3.1.3 Operational MAU type

The operational MAU type field contains an integer value indicating the MAU type of the sending device. This value shall be derived from the list position of the corresponding dot3MauType as listed in IETF RFC 4836 (or subsequent revisions) and is equal to the last number in the respective dot3MauType Object Identifier (OID). For example, if the ifMauType object is dot3MauType1000BaseTHD which corresponds to {dot3MauType 29}, the numerical value of this field is 29. For MAU types not listed in IETF RFC 4836 (or subsequent revisions), the value of this field shall be set to zero.

79.3.1.4 MAC/PHY Configuration/Status TLV usage rules

An LLDPDU should contain no more than one MAC/PHY Configuration/Status TLV.

79.3.2 Power Via MDI TLV

Clause 33 defines two option power entities: a Powered Device (PD) and Power Sourcing Equipment (PSE). These entities allow devices to draw/supply power over the sample generic cabling as used for data transmission. The Power Via MDI TLV allows network management to advertise and discover the MDI power support capabilities of the sending IEEE 802.3 LAN station. This TLV is also required to perform Data Link Layer classification as defined in 33.6. Figure 79–3 shows the format of this TLV.

Replace Figure 79-3 with the following:

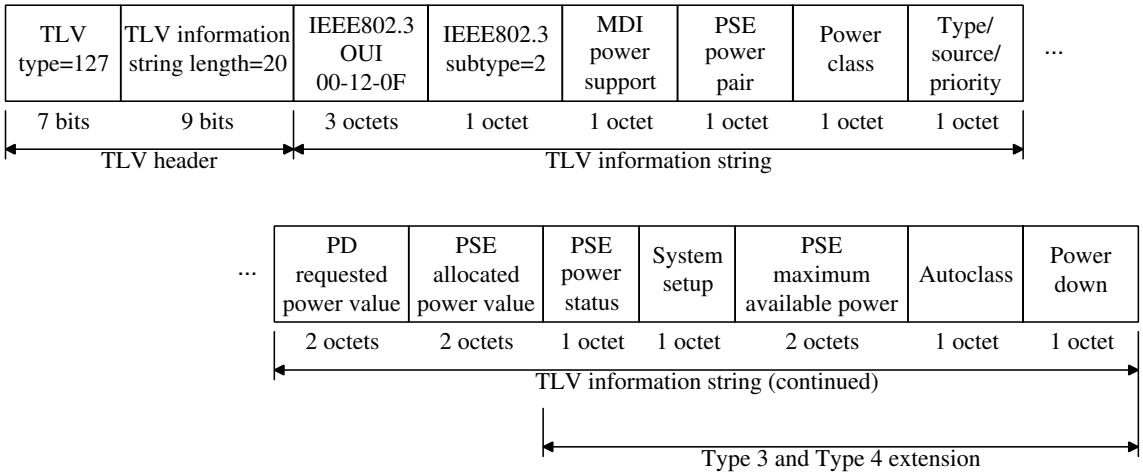

Figure 79–3—Power Via MDI TLV format

The TLV shown in Figure 79–3 is a revision of the legacy Power via MDI TLV originally defined in IEEE Std 802.1AB-2009 Annex F.3. The legacy TLV had only the first three fields of the TLV shown in the

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figure. These three fields enable discovery and advertisement of MDI power support capabilities. The newly added fields provide Data Link Layer classification capabilities. The revised TLV can be used by the PSE only when it is supplying power to a PI encompassed within an MDI and by the PD only when it is drawing power from the PI. Power entities may continue to use the legacy TLV prior to supplying/drawing power to/from the PI. If the power entity implements Data Link Layer classification, it shall use the Power via MDI TLV shown in Figure 79–3 after the PI has been powered.

79.3.2.1 MDI power support

The MDI power support field shall contain a bitmap of the MDI power capabilities and status as defined in Table 79–3.

Table 79–3—MDI power capabilities/status

Bit	Function	Value/meaning	IETF RFC 3621 object reference
0	Port class	1 = PSE 0 = PD	See Note 1
1	Power Sourcing Equipment (PSE) MDI power support	1 = supported 0 = not supported	See Note 2 and Note 3
2	PSE MDI power state	1 = enabled 0 = disabled	pethPsePortAdminEnable
3	PSE pairs control ability	1 = pair selection can be controlled 0 = pair selection can not be controlled	pethPsePortPowerPairContolAbility
4–7	Reserved for future standardization	—	—

NOTE 1—Port class information is implied by the support of the PSE or PD groups.

NOTE 2—MDI power support information is implied by support of IETF RFC 3621.

NOTE 3—If bit 1 is zero, bit 2 has no meaning.

79.3.2.2 PSE power pair

The PSE power pair field shall contain an integer value as defined by the pethPsePortPowerPairs object in IETF RFC 3621. Type 3 or Type 4 PSEs that are furnishing power on a single pairset shall use the value that defines that pairset (signal=Alternative A, spare=Alternative B). Either pairset may be indicated when furnishing power on both pairsets, as that condition is communicated by the PSE power status value field defined in 79.3.2.6a.

79.3.2.3 Power class

The power class field shall contain an integer value as defined by the pethPsePortPowerClassifications object in IETF RFC 3621.

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79.3.2.4 Requested power type/source/priority

Change text in section 79.3.2.4 as follows:

The power type/source/priority field shall contain a bit-map of the power type, source and priority defined in Table 79–4 and is reported for the device generating the TLV.

Table 79–4—Power type/source/priority field

Bit	Function	Value/meaning
7:6	power type	7 6 1 1 = Type 1 PD 1 0 = Type 1 PSE 0 1 = Type 2 PD 0 0 = Type 2 PSE
5:4	power source	Where power type = PD 5 4 1 1 = PSE and local 1 0 = Reserved 0 1 = PSE 0 0 = Unknown Where power type = PSE 5 4 1 1 = Reserved 1 0 = Backup source 0 1 = Primary power source 0 0 = Unknown
3:2	Reserved	Transmit as zero, ignore on receive
1:0	power priority	1 0 1 1 = low 1 0 = high 0 1 = critical 0 0 = unknown (default)

79.3.2.4.1 Power type

Change text in 79.3.2.4.1 as follows:

This field shall be set according to Table 79–4. Type 3 or Type 4 PSEs shall set this field to the value corresponding with Type 2 PSEs. Type 3 or Type 4 PDs shall set this field to the value corresponding with Type 2 PDs.

79.3.2.4.2 Power source

When the power type is PD, this field shall be set to 01 when the PD is being powered only through the PI; to 11 when the PD is being powered from both; and to 00 when this information is not available.

When the power type is PSE, this field shall be set to 01 when the PSE is sourcing its power through the PI from its primary supply; to 10 when the PSE is sourcing its power through the PI from a backup source; and to 00 when this information is not available.

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79.3.2.4.3 Power priority

When the power type is PD, this field shall be set to the power priority configured for the device. If a PD is unable to determine its power priority or it has not been configured, then this field shall be set to 00.

When the power type is PSE, this field reflects the PD priority that the PSE advertises to assign to the PD.

79.3.2.5 PD requested power value

The PD requested power value field shall contain the PD's requested power value defined in Table 79–5

Change Table 79-5 as follows:

.

Table 79–5—PD requested power value field

Bit	Function	Value/meaning
15:0	PD requested power value	Power = 0.1 × (decimal value of bits) Watts. Valid values for these bits are decimal 1 through ~~255~~999.

The PD requested power value is encoded according to Equation (79–1).

$$Power = \{0.1 \times X\}_{\mathrm{W}} \qquad (79–1)$$

where

Power is the effective requested PD power value

X is the decimal value of the power value field, bits 15:0

"PD requested power value" is the maximum input average power (see 33.3.7.2) the PD wants to draw. "PD requested power value" is the power value at the input to the PD's PI.

79.3.2.6 PSE allocated power value

The PSE allocated power value field shall contain the PSE's allocated power value defined in Table 79–6

Change Table 79-6 as follows:.

Table 79–6—PSE allocated power value field

Bit	Function	Value/meaning
15:0	PSE allocated power value	Power = 0.1 × (decimal value of bits) Watts. Valid values for these bits are decimal 1 through ~~255~~999.

The PSE allocated power value is encoded according to Equation (79–2).

$$Power = \{0.1 \times X\}_{\mathrm{W}} \qquad (79–2)$$

where

Power is the effective allocated PSE power value

X is the decimal value of the power value field, bits 15:0

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"PSE allocated power value" is the maximum input average power (see 33.3.7.2) the PSE expects the PD to draw. "PSE allocated power value" is the power at the input to the PD's PI. The PSE uses this value to compute Pas defined in 33.2.6.

Insert Sections 79.3.2.6a, 79.3.2.6b, 79.3.2.6c, 79.3.2.6d and 79.3.2.6e after Section 79.3.2.6 as follows:

79.3.2.6a PSE power status

The PSE power status value field shall contain the PSE's bit-map of the PSE power pair and PSE power class, defined in Table 79-6a, and is reported for the device generating the TLV.

Table 79–6a—PSE power status value field

Bit	Function	Value/meaning
7	Reserved	Transmit as zero. Ignore on receive.
6:5	PSE power pair	6 5 1 1 = Both Alternatives 1 0 = Alternative B 0 1 = Alternative A 0 0 = Reserved/Ignore
4	Reserved	Transmit as zero. Ignore on receive.
3:0	PSE power class	3 2 1 0 1 1 1 1 = Reserved/Ignore 1 1 1 0 = Reserved/Ignore 1 1 0 1 = Reserved/Ignore 1 1 0 0 = Reserved/Ignore 1 0 1 1 = Reserved/Ignore 1 0 1 0 = Reserved/Ignore 1 0 0 1 = Reserved/Ignore 1 0 0 0 = 8 0 1 1 1 = 7 0 1 1 0 = 6 0 1 0 1 = 5 0 1 0 0 = 4 0 0 1 1 = 3 0 0 1 0 = 2 0 0 0 1 = 1 0 0 0 0 = 0

79.3.2.6a.1 PSE power pair

The PSE power pair field shall contain an integer value for PSE power pairs defined by 33.2. A TLV generated by a PD shall set the field to 00.

79.3.2.6a.2 PSE power class

The power class field shall contain an integer value for PSE ~~classes~~ Classes defined by 33.2.6. A TLV generated by a PD shall set the field to 0000.

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79.3.2.6b System setup

The System setup value field shall contain the device bit-map of the Power type, PD 4P-ID, and PD PI defined in Table 79-6b and is reported for the device generating the TLV.

Table 79–6b—System setup value field

Bit	Function	Value/meaning
7:4	Power type	7 6 5 4 1 1 1 1 = Reserved/Ignore 1 1 1 0 = Reserved/Ignore 1 1 0 1 = Reserved/Ignore 1 1 0 0 = Reserved/Ignore 1 0 1 1 = Reserved/Ignore 1 0 1 0 = Reserved/Ignore 1 0 0 1 = Type 4 PD 1 0 0 0 = Type 4 PSE 0 1 1 1 = Type 3 PD 0 1 1 0 = Type 3 PSE 0 1 0 1 = Type 2 PD 0 1 0 0 = Type 2 PSE 0 0 1 1 = Type 1 PD 0 0 1 0 = Type 1 PSE 0 0 0 1 = Reserved/Ignore 0 0 0 0 = Reserved/Ignore
3	PD 4P-ID	1 = PD supports powering of both modes 0 = PD does not support powering of both modes
2	PD PI	1 = Physical layer P_{Class_PD} is the sum of the indicated PD mode power class values. 0 = Physical layer P_{Class_PD} is indicated by either PD mode power class values.
1	Reserved	Transmit as zero. Ignore on receive.
0	Reserved	Transmit as zero. Ignore on receive.

79.3.2.6b.1 Power type

This field shall be set according to Table 79-6b.

79.3.2.6b.2 PD 4P-ID

This field shall be set according to Table 79-6b when the power type is PD. This field shall be set to 0 when the power type is PSE.

79.3.2.6b.3 PD PI

This field shall be set according to Table 79-6b when the power type is PD. This field shall be set to 0 when the power type is PSE.

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79.3.2.6c PSE maximum available power

The PSE maximum available power field shall contain the highest power the PSE can grant as defined in Table 79–6c. The PSE shall set the value of this field taking available power budget and hardware capabilities into account.

Table 79–6c—PSE maximum available power field

Bit	Function	Value/meaning
15:0	PSE maximum available power value	Power = 0.1 × (decimal value of bits) Watts. Valid values for these bits are 1 through 999.

79.3.2.6d Autoclass

The Autoclass field shall contain the bits defined in Table 79–6d to control Autoclass. See 33.2.6.3, 33.3.5.3 and Annex 33C for details on Autoclass. Using the Autoclass field to trigger a new Autoclass measurement allows a PD to change maximum power consumption.

Table 79–6d—Autoclass

Bit	Function	Value/meaning
7:3	Reserved	Transmit as zero. Ignore on receive.
2	PSE Autoclass support	1 = PSE supports Autoclass 0 = PSE does not support Autoclass
1	Autoclass completed	1 = Autoclass measurement completed 0 = Autoclass idle
0	Autoclass request	1 = PD requests Autoclass measurement 0 = Autoclass idle

The sequence of Autoclass as triggered by LLDP is listed in Table 79–6e.

79.3.2.6e Request power down

The request power down field shall be set as defined in Table 79–6f. This field may be set to value 0xDD by a PD that no longer requires power from the PI.

79.3.2.7 Power Via MDI TLV usage rules

An LLDPDU should contain no more than one Power Via MDI TLV.

79.3.3 Link Aggregation TLV (deprecated)

The Link Aggregation TLV is an optional TLV that indicates whether the link is capable of being aggregated, whether the link is currently in an aggregation, and if in an aggregation, the port identification of the aggregation. Figure 79–4 shows the format for this TLV.

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Table 79–6e—Sequence of events for Autoclass triggered via LLDP

Sequence	Function
1	PD switches to a mode where maximum power is consumed
2	PD sends LLDP frame with request_autoclass=1
3	PSE receives frame with request_autoclass=1 and performs the measurement and power budget reduction
4	PSE sends LLDP frame with completed_autoclass=1
5	PD receives LLDP frame with completed_autoclass=1 and sets request_autoclass=0
6	PSE receives LLDP frame with request_autoclass=0 and sets completed_autoclass=0

Table 79–6f—PD request power down field

Bit	Function	Value/meaning
7:0	Power down	Value = 0xDD triggers a power down. Any other value is ignored.

NOTE—As the Link Aggregation specification has now been removed from IEEE Std 802.3 and is now standardized as IEEE Std 802.1AX, new implementations of this standard are encouraged to make use of the Link Aggregation TLV that is now part of the IEEE 802.1 extension MIB specified in Annex E of IEEE Std 802.1AB-2009.

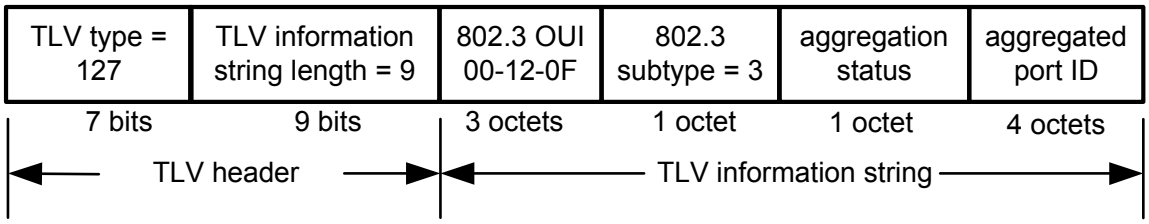

Figure 79–4—Link Aggregation TLV format

79.3.3.1 Aggregation status

The link aggregation status field shall contain a bitmap of the link aggregation capabilities and the current aggregation status of the link as defined in Table 79–7.

79.3.3.2 Aggregated port ID

The aggregated port ID field shall contain the IEEE 802.3 aggregated port identifier, aAggPortID, derived from the ifNumber in the ifIndex for the interface (see 30.7.2.1.1).

79.3.3.3 Link Aggregation TLV usage rules

An LLDPDU should contain no more than one Link Aggregation TLV.

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Table 79–7—Link aggregation capability/status

Bit	Function	Value/meaning
0	Aggregation capability	0 = not capable of being aggregated 1 = capable of being aggregated
1	Aggregation status	0 = not currently in aggregation 1 = currently in aggregation
2–7	reserved for future standardization	—

79.3.4 Maximum Frame Size TLV

The Maximum Frame Size TLV is an optional TLV that indicates the maximum frame size capability of the implemented MAC and PHY. Figure 79–5 shows the format of this TLV.

NOTE—MAC and PHY support for a given frame size doesn't necessarily mean that the upper layers support that frame size.

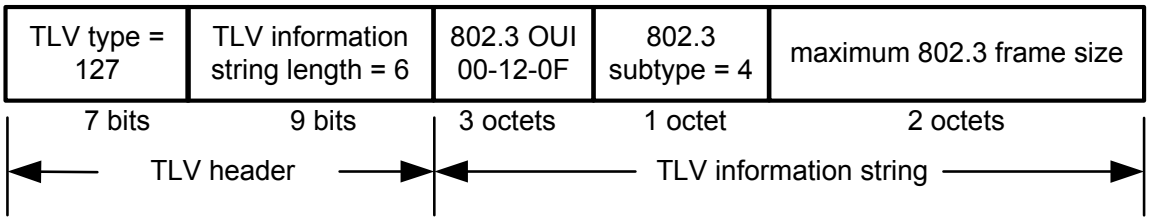

Figure 79–5—Maximum Frame Size TLV format

79.3.4.1 Maximum frame size

The maximum frame size field shall contain an integer value indicating the maximum supported frame size in octets as determined by the following:

a) If the MAC/PHY supports only basic frames (see 3.2.7) the maximum frame size field shall be set to 1518.
b) If the MAC/PHY supports Q-tagged frames (see 3.2.7) the maximum frame size field shall be set to 1522.
c) If the MAC/PHY supports envelope frames (see 3.2.7) the maximum frame size field shall be set to 2000.

79.3.4.2 Maximum Frame Size TLV usage rules

An LLDPDU should contain no more than one Maximum Frame Size TLV.

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79.3.5 EEE TLV

The EEE TLV is used to exchange information about the EEE Data Link Layer capabilities. Figure 79–6 shows the format of this TLV.

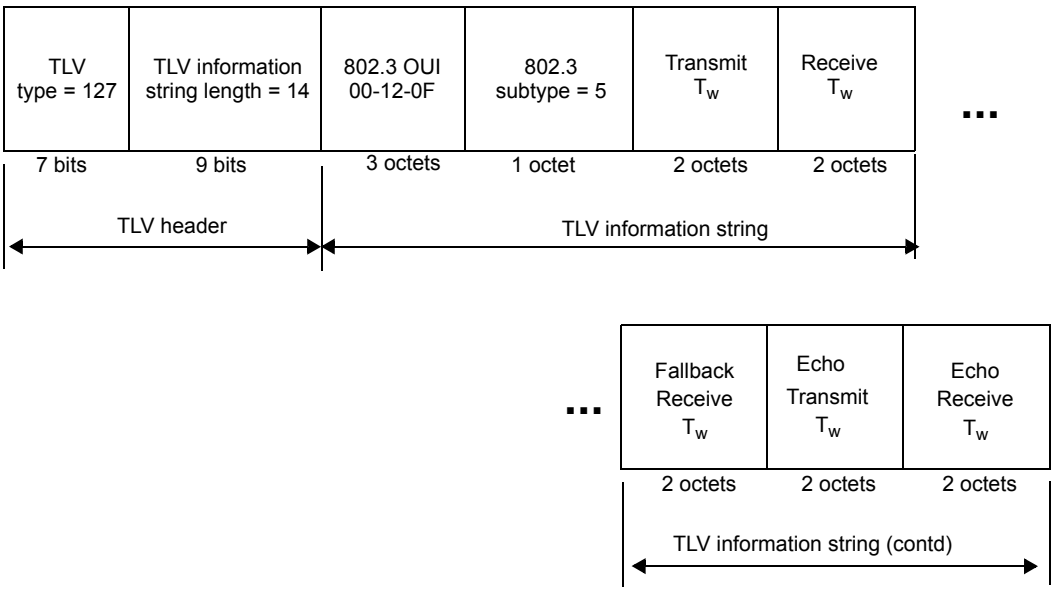

Figure 79–6—EEE TLV format

79.3.5.1 Transmit T_w

Transmit $T_{w_sys_tx}$ (2 octets wide) shall be defined as the time (expressed in microseconds) that the transmitting link partner will wait before it starts transmitting data after leaving the Low Power Idle (LPI) mode. This is a function of the transmit system design and may be constrained, for example, by the transmit path buffering. The default value for Transmit $T_{w_sys_tx}$ is the T_{w_phy} defined for the PHY that is in use for the link. The Transmitting link partner expects that the Receiving link partner will be able to accept data after the time delay Transmit $T_{w_sys_tx}$ (expressed in microseconds).

79.3.5.2 Receive T_w

Receive $T_{w_sys_tx}$ (2 octets wide) shall be defined as the time (expressed in microseconds) that the receiving link partner is requesting the transmitting link partner to wait before starting the transmission data following the LPI. The default value for Receive $T_{w_sys_tx}$ is the T_{w_phy} defined for the PHY that is in use for the link. The Receive $T_{w_sys_tx}$ value can be larger but not smaller than the default. The extra wait time may be used by the receive link partner for power-saving mechanisms that require a longer wake-up time than the PHY-layer definitions.

79.3.5.3 Fallback T_w

A receiving link partner may inform the transmitter of an alternate desired $T_{w_sys_tx}$. Since a receiving link partner is likely to have discrete levels for savings, this provides the transmitter with additional information that it may use for a more efficient allocation. As with the Receive $T_{w_sys_tx}$, this is 2 octets wide. Systems that do not implement this option default the value to be the same as that of the Receive $T_{w_sys_tx}$.

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79.3.5.4 Echo Transmit and Receive T_W

The respective echo values shall be defined as the local link partner's reflection (echo) of the remote link partner's respective values. When a local link partner receives its echoed values from the remote link partner it can determine whether or not the remote link partner has received, registered, and processed its most recent values. For example, if the local link partner receives echoed parameters that do not match the values in its local MIB, then the local link partner infers that the remote link partner's request was based on stale information.

79.3.5.5 EEE TLV usage rules

An LLDPDU should contain no more than one EEE TLV.

79.3.6 EEE Fast Wake TLV

The EEE Fast Wake TLV is used to exchange information about the EEE fast wake capabilities. This TLV is only used by systems with links operating at speeds greater than 10 Gb/s. Figure 79–7 shows the format of this TLV.

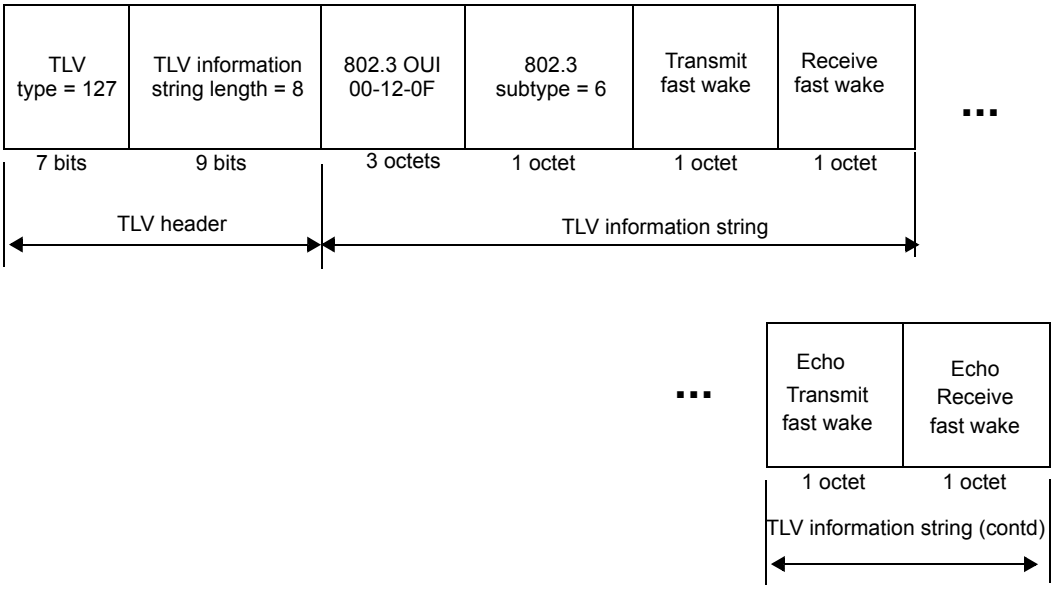

Figure 79–7—EEE Fast Wake TLV format

79.3.6.1 Transmit fast wake

Transmit fast wake (1 octet wide) is a logical indication that the transmit LPI state diagram intends to use the fast wake function (corresponding to the variable LPI_FW in 82.2.19.2.2). Transmit fast wake = 1 corresponds to LPI_FW being TRUE; Transmit fast wake = 0 corresponds to LPI_FW being FALSE. The default value for Transmit fast wake is 1 (TRUE). Transmit fast wake is set to TRUE unless the PHY is capable of deep sleep operation as determined by the PHY type and the results of auto-negotiation.

79.3.6.2 Receive fast wake

Receive fast wake (1 octet wide) is a logical indication that the receive LPI state diagram is expecting its link partner to use the fast wake function (corresponding to the variable LPI_FW in 82.2.19.2.2). Receive fast

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wake = 1 corresponds to LPI_FW being TRUE; Receive fast wake = 0 corresponds to LPI_FW being FALSE. The default value for Receive fast wake is 1 (TRUE). Receive fast wake is set to TRUE unless the PHY is capable of deep sleep operation as determined by the PHY type and the results of auto-negotiation.

79.3.6.3 Echo of Transmit fast wake and Receive fast wake

The respective echo values are the local link partner's reflection (echo) of the remote link partner's respective values. When a local link partner receives its echoed values from the remote link partner, it can determine whether or not the remote link partner has received, registered, and processed its most recent values. For example, if the local link partner receives echoed parameters that do not match the values in its local MIB, then the local link partner infers that the remote link partner's request was based on stale information.

79.3.6.4 EEE Fast Wake TLV usage rules

An LLDPDU should contain no more than one EEE Fast Wake TLV.

Insert new section 79.3.7 after 79.3.6.4 as follows:

79.3.7 Power via MDI Measurements TLV

Clause 33 defines two option power entities: a Powered Device (PD) and Power Sourcing Equipment (PSE). These entities allow devices to draw/supply power over the sample generic cabling as used for data transmission. The Power Via MDI Measurement TLV allows network management to read electrical measurement data from the sending IEEE 802.3 LAN station. Figure 79–7a shows the format of this TLV.

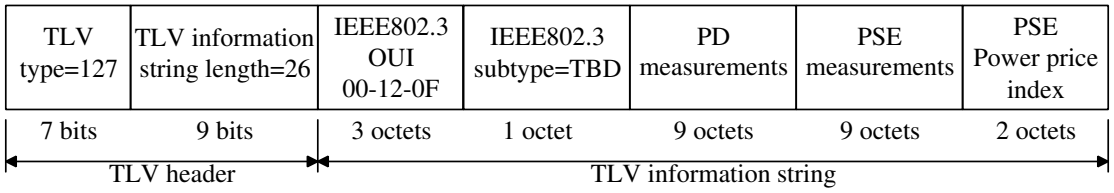

Figure 79–7a—Power Via MDI Measurements TLV format for Type 3 and Type 4

79.3.7.1 PD measurements

The PD measured voltage value field may be included to carry the PD's measured voltage value at the port defined in Table 79–7a. The PD measured current value field may be included to carry the PD's measured current value at the port defined in Table 79–7a. The PD measured energy value field may be included to carry the PD's measured energy consumption value at the port defined in Table 79–7a.

Measurement values (Voltage measurement, Current measurement and Energy measurement shall be set to 0 in case the corresponding request bit is 0. If a device does not support a particular measurement, the corresponding measurement value shall be set to 0.

Insert Table 79-7a as follows:

79.3.7.2 PSE measurements

The PSE measured voltage value field may be included to carry the PSE's measured voltage value at the port defined in Table 79–7b. The PSE measured current value field may be included to carry the PSE's measured

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Table 79–7a—PD measurements

Bit	Function	Value/meaning
95	Voltage support	1 = PD supports voltage measurement 0 = PD does not support voltage measurement
94	Current support	1 = PD supports current measurement 0 = PD does not support current measurement
93	Energy support	1 = PD supports energy measurement 0 = PD does not support energy measurement
92:91	Measurement source	Determine where the measurement is to be taken. 92 91 0 0 No request 0 1 Pairset Alternative A 1 0 Pairset Alternative B 1 1 Port total
90	Voltage request	Request voltage measurement Where power type = PSE 1 = PSE request for voltage measurement 0 = No request for voltage measurement Where power type = PD 1 = Voltage measurement contains valid data 0 = Voltage measurement disabled
89	Current request	Request current measurement Where power type = PSE 1 = PSE request for current measurement 0 = No request for current measurement Where power type = PD 1 = Current measurement contains valid data 0 = Current measurement disabled
88	Energy request	Request energy measurement Where power type = PSE 1 = PSE request for energy measurement 0 = No request for energy measurement Where power type = PD 1 = Energy measurement contains valid data 0 = Energy measurement disabled
87:80	Voltage accuracy	Number of useful significant bits in Voltage measurement data field (decimal value of bits). Valid values for these bits are decimal 1 through 16
79:72	Current accuracy	Number of useful significant bits in Current measurement data field (decimal value of bits). Valid values for these bits are decimal 1 through 16
71:64	Energy accuracy	Number of useful significant bits in Energy measurement data field (decimal value of bits). Valid values for these bits are decimal 1 through 32

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Table 79–7a—PD measurements

Bit	Function	Value/meaning
63:48	Voltage measurement	V_{Port_PD} = (decimal value of bits) mV Valid values for these bits are decimal 1 through 65000
47:32	Current measurement	I_{Port} or $I_{Port\text{-}2P}$ = 0.1 × (decimal value of bits) mA Valid values for these bits are decimal 0 through 20000
31:0	Energy measurement	Total energy consumed at the port or pairset value = 0.1 × (decimal value of bits) in kJ since power on.

current value at the port defined in Table 79–7b. The PSE measured energy value field may be included to carry the PSE's measured energy consumption value at the port defined in Table 79–7b.

Measurement values (voltage, current or energy) shall be set to 0 in case the corresponding request bit is 0. If a device does not support a particular measurement, the corresponding measurement value shall be set to 0.

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Insert Table 79-7b as follows:

Table 79–7b—PSE measurements

Bit	Value	Meaning
95	Voltage support	1 = PSE supports voltage measurement 0 = PSE does not support voltage measurement
94	Current support	1 = PSE supports current measurement 0 = PSE does not support current measurement
93	Energy support	1 = PSE supports energy measurement 0 = PSE does not support energy measurement
92:91	Measurement source	Determine where the measurement is to be taken. 92 91 0 0 No request 0 1 Pairset Alternative A 1 0 Pairset Alternative B 1 1 Port total
90	Voltage request	Request voltage measurement Where power type = PD 1 = PD request for voltage measurement 0 = No request for voltage measurement Where power type = PSE 1 = Voltage measurement contains valid data 0 = Voltage measurement disabled
89	Current request	Request current measurement Where power type = PD 1 = PD request for current measurement 0 = No request for current measurement Where power type = PSE 1 = Current measurement contains valid data 0 = Current measurement disabled
88	Energy request	Request energy measurement Where power type = PD 1 = PD request for energy measurement 0 = No request for energy measurement Where power type = PSE 1 = Energy measurement contains valid data 0 = Energy measurement disabled
87:80	Voltage accuracy	Number of useful significant bits in voltage measurement data field (decimal value of bits). Valid values for these bits are decimal 1 through 16.
79:72	Current accuracy	Number of useful significant bits in current measurement data field (decimal value of bits). Valid values for these bits are decimal 1 through 16.

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Table 79–7b—PSE measurements

Bit	Value	Meaning
71:64	Energy accuracy	Number of useful significant bits in energy measurement data field (decimal value of bits). Valid values for these bits are decimal 1 through 32.
63:48	Voltage measurement	V_{PORT_PSE} = (decimal value of bits) mV. Valid values for these bits are decimal 1 through 65000.
47:32	Current measurement	I_{PORT} or $I_{PORT-2P}$ = 0.1 x (decimal value of bits) mA. Valid values for these bits are decimal 0 through 20000.
31:0	Energy measurement	Total energy consumed at the port or pairset. Value = 0.1 x (decimal value of bits) in kJ since power on.

79.3.7.3 PSE power price index

The PSE power price index field shall contain a linear index to the current value of electricity within the PSE. This is a 16 bit unsigned integer in the range 0 through 65,535, with 1,000 as a nominal value as defined in Table 79–7c. The PSE shall set the value of this field taking the availability of power from any external and internal resources, and the relative supply and demand balance, into account. A value of zero means that no power price index is available.

Insert Table 79-7c as follows:

Table 79–7c—

Bit	Function	Value/meaning
15:0	Power price index	Power price index = decimal value of bits. Valid values for these bits are decimal 1 through65535.

79.3.7.4 Power Via MDI Measurements TLV usage rules

An LLDPDU should contain no more than one Power Via MDI Measurements TLV.

79.4 IEEE 802.3 Organizationally Specific TLV selection management

TLV selection management consists of providing the network manager with the means to select which specific IEEE 802.3 Organizationally Specific TLVs are enabled for inclusion in an LLDPDU. The following LLDP variable cross references the LLDP local systems configuration MIB tables (see Clause 11 of IEEE Std 802.1AB-2009) to indicate which specific TLVs are enabled for the particular port(s) on the system. The specific port(s) through which each TLV is enabled for transmission may be set (or reset) by the network manager:

a) **mibXdot3TLVsTxEnable:** This variable lists the single-instance use IEEE 802.3 Organizationally Specific TLVs, each with a bitmap indicating the system ports through which the referenced TLV is enabled for transmission.

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79.4.1 IEEE 802.3 Organizationally Specific TLV selection variable/LLDP Configuration managed object class cross reference

Table 79–8 lists the relationship both between IEEE 802.3 TLV selection variable and the corresponding LLDP Configuration managed object class (see 30.12.1) attribute.

Table 79–8—IEEE 802.3 Organizationally Specific TLV selection variable/LLDP MIB object cross reference

IEEE 802.3 TLV selection variable	LLDP Configuration managed object class attribute
mibXdot3TLVsTxEnable	aLldpXdot3PortConfigTLVsTxEnable

79.4.2 IEEE 802.3 Organizationally Specific TLV/LLDP Local and Remote System group managed object class cross references

The cross references between the IEEE 802.3 TLVs and the LLDP Local System Group managed object class (see 30.12.2) attributes are listed in Table 79–9. The cross references between the IEEE 802.3 TLVs and the LLDP Remote System Group managed object class (see 30.12.3) attributes are listed in Table 79–10.

The cross-references between the EEE TLV, the EEE Fast Wake TLV, and the EEE local (30.12.2) and remote (30.12.3) object class attributes are listed in Table 79–9 and Table 79–10.

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Change Table 79-9 and Table 79-10 as follows:

Table 79–9—IEEE 802.3 Organizationally Specific TLV/LLDP Local System Group managed object class cross references

TLV name	TLV variable	LLDP Local System Group managed object class attribute
MAC/PHY Configuration/Status	Auto-negotiation support	aLldpXdot3LocPortAutoNegSupported
	Auto-negotiation status	aLldpXdot3LocPortAutoNegEnabled
	PMD auto-negotiation advertised capability	aLldpXdot3LocPortAutoNegAdvertisedCap
	Operational MAU type	aLldpXdot3LocPortOperMauType
Power via MDI	Port class	aLldpXdot3LocPowerPortClass
	PSE MDI power support	aLldpXdot3LocPowerMDISupported
	PSE MDI power state	aLldpXdot3LocPowerMDIEnabled
	PSE pairs control ability	aLldpXdot3LocPowerPairControlable
	PSE power pair	aLldpXdot3LocPowerPairs
	Power class	aLldpXdot3LocPowerClass
	Power type	aLldpXdot3LocPowerType
	Power source	aLldpXdot3LocPowerSource
	Power priority	aLldpXdot3LocPowerPriority
	PD requested power value	aLldpXdot3LocPDRequestedPowerValue
	PSE allocated power value	aLldpXdot3LocPSEAllocatedPowerValue
	PSE power pair	aLldpXdot3LocPowerPairs
	Power class	aLldpXdot3LocPowerClass
	Power type	aLldpXdot3LocPowerType
	PD 4P-ID	aLldpXdot3Loc4PID
	PD PI	aLldpXdot3LocPDPI
	PSE available power	aLldpXdot3LocPSEMaxAvailPower
	PSE Autoclass support	aLldpXdot3LocPSEAutoclassSupport
	Autoclass completed	aLldpXdot3LocAutoclassCompleted
	Autoclass request	aLldpXdot3LocAutoclassRequest
	Power down	aLldpXdot3LocPowerDownRequest
Link Aggregation (deprecated)	aggregation status	
	aggregated port ID	
Maximum Frame Size	maximum frame size	

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Table 79–9—IEEE 802.3 Organizationally Specific TLV/LLDP Local System Group managed object class cross references *(continued)*

TLV name	TLV variable	LLDP Local System Group managed object class attribute
EEE	Transmit $T_{w_sys_tx}$	aLldpXdot3LocTxTwSys
	Receive $T_{w_sys_tx}$	aLldpXdot3LocRxTwSys
	Echo Transmit $T_{w_sys_tx}$	aLldpXdot3LocTxTwSysEcho
	Echo Receive $T_{w_sys_tx}$	aLldpXdot3LocRxTwSysEcho
	Fallback $T_{w_sys_tx}$	aLldpXdot3LocFbTwSys
EEE Fast Wake	Transmit fast wake	aLldpXdot3LocTxFw
	Receive fast wake	aLldpXdot3LocRxFw
	Echo Transmit fast wake	aLldpXdot3LocTxFwEcho
	Echo Receive fast wake	aLldpXdot3LocRxFwEcho
Power via MDI Measurements	PD Voltage support	aLldpXdot3LocPDMeasVoltageSupport
	PD Current support	aLldpXdot3LocPDMeasCurrentSupport
	PD Energy support	aLldpXdot3LocPDMeasEnergySupport
	PD Measurement source	aLldpXdot3LocPDMeasurementSource
	PD Voltage measurement	aLldpXdot3LocPDMeasurementVoltage
	PD Current measurement	aLldpXdot3LocPDMeasurementCurrent
	PD Energy measurement	aLldpXdot3LocPDMeasurementEnergy
	PSE Voltage support	aLldpXdot3LocPSEMeasVoltageSupport
	PSE Current support	aLldpXdot3LocPSEMeasCurrentSupport
	PSE Energy support	aLldpXdot3LocPSEMeasEnergySupport
	PSE Measurement source	aLldpXdot3LocPSEMeasurementSource
	PSE Voltage measurement	aLldpXdot3LocPSEMeasurementVoltage
	PSE Voltage measurement	aLldpXdot3LocPSEMeasurementVoltage
	PSE Current measurement	aLldpXdot3LocPSEMeasurementCurrent
	PSE Energy measurement	aLldpXdot3LocPSEMeasurementEnergy
	PSE Power price index	aLldpXdot3LocPSEPowerPriceIndex

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Table 79–10—IEEE 802.3 Organizationally Specific TLV/LLDP Remote System Group managed object class cross references

TLV name	TLV variable	LLDP Remote System Group managed object class attribute
MAC/PHY Configuration/Status	Auto-negotiation support	aLldpXdot3RemPortAutoNegSupported
	Auto-negotiation status	aLldpXdot3RemPortAutoNegEnabled
	PMD auto-negotiation advertised capability	aLldpXdot3RemPortAutoNegAdvertisedCap
	Operational MAU type	aLldpXdot3RemPortOperMauType
Power via MDI	Port class	aLldpXdot3RemPowerPortClass
	PSE MDI power support	aLldpXdot3RemPowerMDISupported
	PSE MDI power state	aLldpXdot3RemPowerMDIEnabled
	PSE pairs control ability	aLldpXdot3RemPowerPairControlable
	PSE power pair	aLldpXdot3RemPowerPairs
	Power class	aLldpXdot3RemPowerClass
	Power type	aLldpXdot3RemPowerType
	Power source	aLldpXdot3RemPowerSource
	Power priority	aLldpXdot3RemPowerPriority
	PD requested power value	aLldpXdot3RemPDRequestedPowerValue
	PSE allocated power value	aLldpXdot3RemPSEAllocatedPowerValue
	PSE power pair	aLldpXdot3RemPowerPairs
	Power class	aLldpXdot3RemPowerClass
	Power type	aLldpXdot3RemPowerType
	PD 4P-ID	aLldpXdot3Rem4PID
	PD PI	aLldpXdot3RemPDPI
	PSE available power	aLldpXdot3RemPSEMaxAvailPower
	PSE Autoclass support	aLldpXdot3RemPSEAutoclassSupport
	Autoclass completed	aLldpXdot3RemAutoclassCompleted
	Autoclass request	aLldpXdot3RemAutoclassRequest
	Power down	aLldpXdot3RemPowerDownRequest
Link Aggregation (deprecated)	aggregation status	aLldpXdot3RemLinkAggStatus
	aggregated port ID	aLldpXdot3RemLinkAggPortId
Maximum Frame Size	maximum frame size	aLldpXdot3RemMaxFrameSize

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Table 79–10—IEEE 802.3 Organizationally Specific TLV/LLDP Remote System Group managed object class cross references *(continued)*

TLV name	TLV variable	LLDP Remote System Group managed object class attribute
EEE	Transmit $T_{w_sys_tx}$	aLldpXdot3RemTxTwSys
	Receive $T_{w_sys_tx}$	aLldpXdot3RemRxTwSys
	Echo Transmit $T_{w_sys_tx}$	aLldpXdot3RemTxTwSysEcho
	Echo Receive $T_{w_sys_tx}$	aLldpXdot3RemRxTwSysEcho
	Fallback $T_{w_sys_tx}$	aLldpXdot3RemFbTwSys
EEE Fast Wake	Transmit fast wake	aLldpXdot3RemTxFw
	Receive fast wake	aLldpXdot3RemRxFw
	Echo Transmit fast wake	aLldpXdot3RemTxFwEcho
	Echo Receive fast wake	aLldpXdot3RemRxFwEcho
Power via MDI Measurements	PD Voltage support	aLldpXdot3RemPDMeasVoltageSupport
	PD Current support	aLldpXdot3RemPDMeasCurrentSupport
	PD Energy support	aLldpXdot3RemPDMeasEnergySupport
	PD Measurement source	aLldpXdot3RemPDMeasurementSource
	PD Voltage measurement	aLldpXdot3RemPDMeasurementVoltage
	PD Current measurement	aLldpXdot3RemPDMeasurementCurrent
	PD Energy measurement	aLldpXdot3RemPDMeasurementEnergy
	PSE Voltage support	aLldpXdot3RemPSEMeasVoltageSupport
	PSE Current support	aLldpXdot3RemPSEMeasCurrentSupport
	PSE Energy support	aLldpXdot3RemPSEMeasEnergySupport
	PSE Measurement source	aLldpXdot3RemPSEMeasurementSource
	PSE Voltage measurement	aLldpXdot3RemPSEMeasurementVoltage
	PSE Voltage measurement	aLldpXdot3RemPSEMeasurementVoltage
	PSE Current measurement	aLldpXdot3RemPSEMeasurementCurrent
	PSE Energy measurement	aLldpXdot3RemPSEMeasurementEnergy

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79.5 Protocol implementation conformance statement (PICS) proforma for IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements[3]

79.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 79, IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

79.5.2 Identification

79.5.2.1 Implementation identification

Change text in section 79.5.2.1 as follows:

Supplier[1]	
Contact point for ~~e~~inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTES 1—Required for all implementations. 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

79.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-201x, Clause 79, IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-201x.)	
Date of Statement	

[3]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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79.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*MP	MAC/PHY Configuration/Status TLV	79.3.1		O	Yes [ ] No [ ]
*PV	Power Via MDI TLV	79.3.2		O	Yes [ ] No [ ]
*LA	Link Aggregation TLV	79.3.3	TLV deprecated	O	Yes [ ] No [ ]
*FS	Maximum Frame Size TLV	79.3.4		O	Yes [ ] No [ ]
*EE	EEE TLV	79.3.5		O	Yes [ ] No [ ]
*EEFW	EEE Fast Wake TLV	79.3.6		O	Yes [ ] No [ ]

79.5.4 IEEE 802.3 Organizationally Specific TLV

Item	Feature	Subclause	Value/Comment	Status	Support
TLV1	Group MAC addresses	79.2	*Nearest device* group MAC addresses listed in Table 7-1 of IEEE Std 802.1AB-2009	M	Yes [ ]
TLV2	LLDPDU bit and octet ordering	79.2	Defined in subclause 8.1 of IEEE Std 802.1AB-2009	M	Yes [ ]

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79.5.5 MAC/PHY Configuration/Status TLV

Item	Feature	Subclause	Value/Comment	Status	Support
MPT1	auto-negotiation support/status field	79.3.1.1	Identifies support and current status as defined in Table 79–2	MP:M	Yes [ ] N/A [ ]
MPT2	PMD auto-negotiation capability field	79.3.1.2	Bitmap of the ifMauAutoNeg-CapAdvertisedBits object defined in IETF RFC 4836	MP:M	Yes [ ] N/A [ ]
MPT3	operational MAU type field	79.3.1.3	Derived from the list position of the corresponding dot3Mau-Type as listed in IETF RFC 4836 (or subsequent revisions)	MP:M	Yes [ ] N/A [ ]
MPT4	operational MAU type field	79.3.1.3	Set to zero for MAU types not listed in IETF RFC 4836 (or subsequent revisions)	MP:M	Yes [ ] N/A [ ]
MPT5	Usage rules	79.3.1.4	LLDPDU contains no more than one MAC/PHY Configuration/Status TLV	MP:O	Yes [ ] No [ ] N/A [ ]

79.5.6 EEE TLV

Item	Feature	Subclause	Value/Comment	Status	Support
EET1	Transmit T_w field	79.3.5.1	2 octets representing time (expressed in microseconds) that the transmitting link partner will wait before it starts transmitting data after leaving the LPI mode	EE:M	Yes [ ] N/A [ ]
EET2	Receive T_w field	79.3.5.2	2 octets representing time (expressed in microseconds) that the receiving link partner is requesting the transmitting link partner to wait before it starts transmitting data following the LPI	EE:M	Yes [ ] N/A [ ]
EET3	Fallback field	79.3.5.3	2 octets representing time (expressed in microseconds)	EE:O	Yes [ ] N/A [ ]
EET4	Echo Transmit and Receive T_w fields	79.3.5.4	2 octets representing time (expressed in microseconds)	EE:M	Yes [ ] N/A [ ]
EET5	Usage rules	79.3.5.5	LLDPDU contains no more than one EEE TLV	EE:O	Yes [ ] No [ ] N/A [ ]

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79.5.7 EEE Fast Wake TLV

Item	Feature	Subclause	Value/Comment	Status	Support
EFW1	Transmit fast wake field	79.3.6.1	1 octet representing fast wake option for transmit LPI function	EEFW: M	Yes [ ] N/A [ ]
EFW2	Receive fast wake field	79.3.6.2	1 octet representing fast wake option for receive LPI function	EEFW: M	Yes [ ] N/A [ ]
EFW3	Echo Transmit and Receive fast wake fields	79.3.6.3	2 octets representing received fast wake options	EEFW: M	Yes [ ] N/A [ ]

79.5.8 Power Via MDI TLV

Item	Feature	Subclause	Value/Comment	Status	Support
PVT1	MDI power support field	79.3.2.1	Bit map of the MDI power capabilities and status as defined in Table 79–3	PV:M	Yes [ ] N/A [ ]
PVT2	PSE power pair field	79.3.2.2	Integer value as defined by the pethPsePortPowerPairs object in IETF RFC 3621	PV:M	Yes [ ] N/A [ ]
PVT3	power class field	79.3.2.3	Integer value as defined by the pethPsePortPowerClassifications object in IETF RFC 3621	PV:M	Yes [ ] N/A [ ]
PVT4	Power type/source/priority field	79.3.2.4	Contains a bit-map of the power type, source, and priority defined in Table 79–4	PV:M	Yes [ ] N/A [ ]
PVT5	Power type field	79.3.2.4.1	Set according to Table 79–4	PV:M	Yes [ ] N/A [ ]
PVT6	Power source field when power type is PD	79.3.2.4.2	Set to ‘01’ when powered only through the PI; set to ‘11’ when powered from both; set to ‘00’ when information is not available	PV:M	Yes [ ] N/A [ ]
PVT7	Power source field when power type is PSE	79.3.2.4.2	When sourcing power through the PI, set to ‘01’ when using primary supply; set to ‘10’ when using backup source; set to ‘00’ when information is not available	PV:M	Yes [ ] N/A [ ]
PVT8	Power priority field when power type is PD	79.3.2.4.3	Set to the power priority configured for the device; set to ‘00’ if power priority is undetermined	PV:M	Yes [ ] N/A [ ]
PVT9	PD requested power value field	79.3.2.5	Contains the PD’s requested power value defined in Table 79–5	PV:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PVT10	PSE allocated power value field	79.3.2.6	Contains the PSE's allocated power value defined in Table 79–6	PV:M	Yes [ ] N/A [ ]
PVT11	Usage rules	79.3.2.7	LLDPDU contains no more than one Power Via MDI TLV	PV:O	Yes [ ] No [ ] N/A [ ]

79.5.9 Link Aggregation TLV

Item	Feature	Subclause	Value/Comment	Status	Support
LAT1	link aggregation status field	79.3.3.1	Bitmap of the link aggregation capabilities and the current aggregation status as defined in Table 79–7	LA:M	Yes [ ] N/A [ ]
LAT2	aggregated port ID	79.3.3.2	IEEE 802.3 aggregated port identifier, aAggPortID	LA:M	Yes [ ] N/A [ ]
LAT3	Usage rules	79.3.3.3	LLDPDU contains no more than one Link Aggregation TLV	LA:O	Yes [ ] No [ ] N/A [ ]

79.5.10 Maximum Frame Size TLV

Item	Feature	Subclause	Value/Comment	Status	Support
FST1	maximum frame size field	79.3.4.1	Integer value indicating the maximum supported frame size	FS:M	Yes [ ] N/A [ ]
FST2	maximum frame size field	79.3.4.1	1518 for basic frames	FS:O/1	Yes [ ] No [ ] N/A [ ]
FST3	maximum frame size field	79.3.4.1	1522 for Q-tagged frames	FS:O/1	Yes [ ] No [ ] N/A [ ]
FST4	maximum frame size field	79.3.4.1	2000 for envelope frames	FS:O/1	Yes [ ] No [ ] N/A [ ]
FST5	Usage rules	79.3.4.2	LLDPDU contains no more than one Maximum Frame Size TLV	FS:O	Yes [ ] No [ ] N/A [ ]

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