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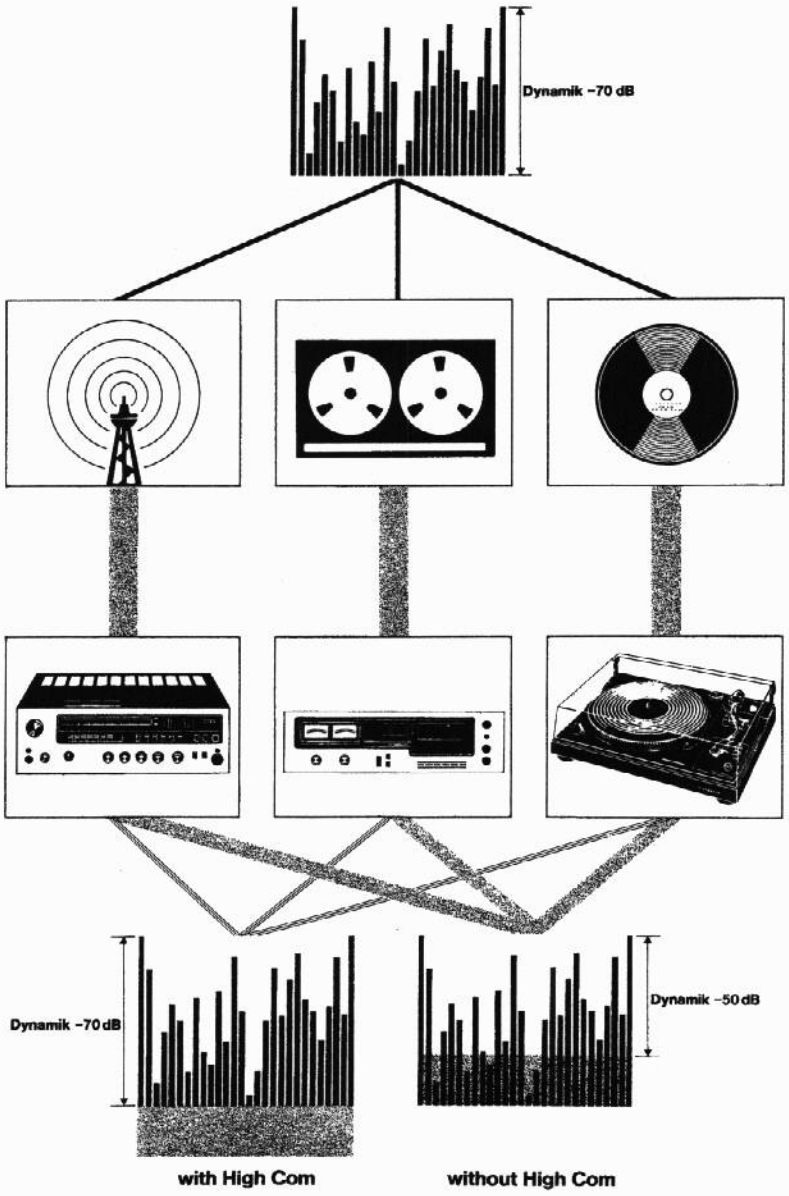
HIGH ( ) COM

The HIGH COM broadband compander utilizing the integrated circuit U 401 BR



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1. Introduction

The usable dynamic range of a transmission channel or a storage medium is limited by onset of overdrive at one end and by the intrinsic noise level at the other end. Thus, it is not possible to transmit a signal with extensive dynamic range without either frequent overdrive excursions at peak signal levels or losing important signal components in the noise background. However, if the transmission channel is complemented with a compander consisting of an input dynamic range compressor and output complementary dynamic range expander (Fig. 1), then correspondingly greater dynamic range of the signal can be handled without the aforementioned limitations, since the compressor boosts low-level signal components enough to bring them above the noise level. Provided that precisely opposite operations are performed by the expander, the original dynamic range, as present at the output of the signal source, can be restored at the output of the reproduction system.

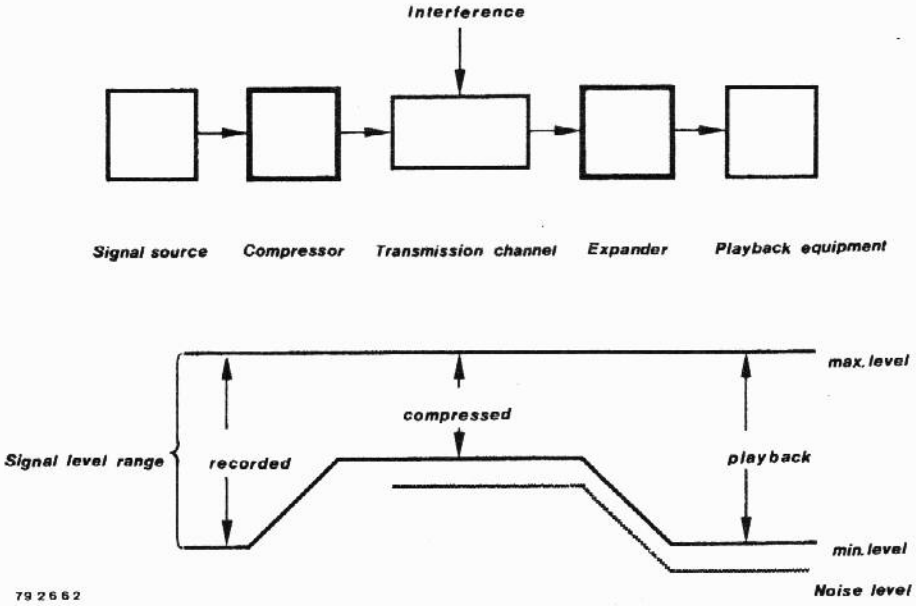


Fig. 1:
Principle of operation of a companding transmission link.

2. Theoretical principles

When using a compander circuit as shown in Fig. 2, the generalized transfer function A of the compressor depends on the form of its output voltage E_2:

$$\frac{E_2}{E_1} = A\,(E_2) \tag{2.1}$$

Correspondingly, the transfer function B of the expander depends on the input voltage E_3 applied to the latter:

$$\frac{E_4}{E_3} = B\,(E_3) \tag{2.2}$$

Two conditions must be satisfied in order to make the output signal of the expander identical to the input signal applied to the compressor:

$$B\,(E_3) = A^{-1}\,(E_2) \tag{2.3}$$

$$E_3\,(t) = E_2\,(t\text{-}t_o) \tag{2.4}$$

Condition (2.3) can be fulfilled in several ways. A particularly good method is to use an operational compressor configuration, where the expander is placed in the negative feedback path of the operational amplifier (Fig. 3).

According to the known relationship, the transfer function of this circuit configuration is given by the expression:

$$A = \frac{A_o}{1 + A_o B} \tag{2.5}$$

where A_o is the open loop gain of the operational amplifier. If A_o is sufficiently large, the expression simplifies to:

$$\lim_{A_o \to \infty} A = B^{-1} \tag{2.6}$$

Thus, this method imposes the only fundamental condition that **the open loop gain of the operational amplifier must be adequately greater than the reciprocal of the maximum expander attenuation factor.**

Condition (2.4) demands that the input and the output voltages of the complete transmission channel be identical except for a constant given shift in time. A real transmission channel can meet this requirement only approximately, since every real channel not only exhibits a finite bandwidth, but also introduces both linear and non-linear distortion components and superimposes background noise on the processed signal.

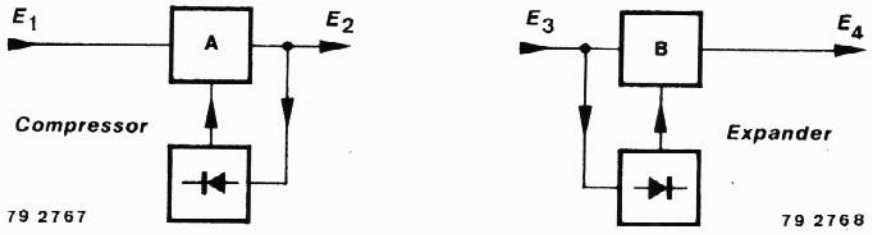


Fig. 2:
Basic configurations of compressing/expanding circuits.

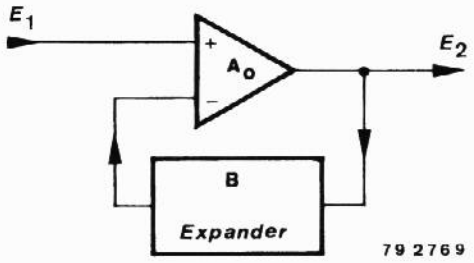


Fig. 3:
The complementary compressor is formed by placing an expander in the negative feedback loop of an operational amplifier.

Differences between E_2 and E_3 subsequently lead to differences between the transfer functions A and B, resulting in so-called **mistracking.** The manner in which non-ideal performance of the transmission channel affects the reproduced signal form E_4, depends on the individual parameters of a given compander system.

Limited channel bandwidth makes it necessary to prevent the compressor from being driven by signals which cannot reach the expander. A simple way to meet such requirement is to place a bandwidth restriction circuit similar to that of the transmission channel ahead of the compressor. It is furthermore important to ensure that the intrinsic channel noise level E_R is sufficiently lower than the lowest compressed signal level E_2 which must be transmitted. Since the expander receives the sum of E_2 and background noise:

$$E_3 = E_2 + E_R, \tag{2.7}$$

this may lead to mistracking for small signals.

If E_2 and E_3 differ by a constant factor (which means that the transmission channel has a non-unity gain), a non-complementary behavior of compressor and expander (mistracking as a result of signal level incongruency) may result.

Such an effect, however, can be made negligible by choosing appropriate forms for the compander characteristics. For example, the following stipulations can be made for the transfer functions A and B:

$$A = \frac{E_2}{E_o}^{-(k-1)} \tag{2.8}$$

$$B = \frac{E_3}{E_o}^{(k-1)} \tag{2.9}$$

These conditions define straight lines in the logarithmic signal level diagram. The constant "k" defines the compression factor, while the voltage E_o represents the reference drive level at which compressor and the expander go to unity gain.

If E_2 and E_3 differ by a constant factor "a", such that:

$$E_3 = E_2 \cdot a \tag{2.10}$$

we obtain

$$E_4 = B \cdot E_3 = B \cdot a \cdot E_2 = a \cdot A \cdot B \cdot E_1 \tag{2.11}$$

and

$$E_4 = a^k \cdot E_1 \tag{2.12}$$

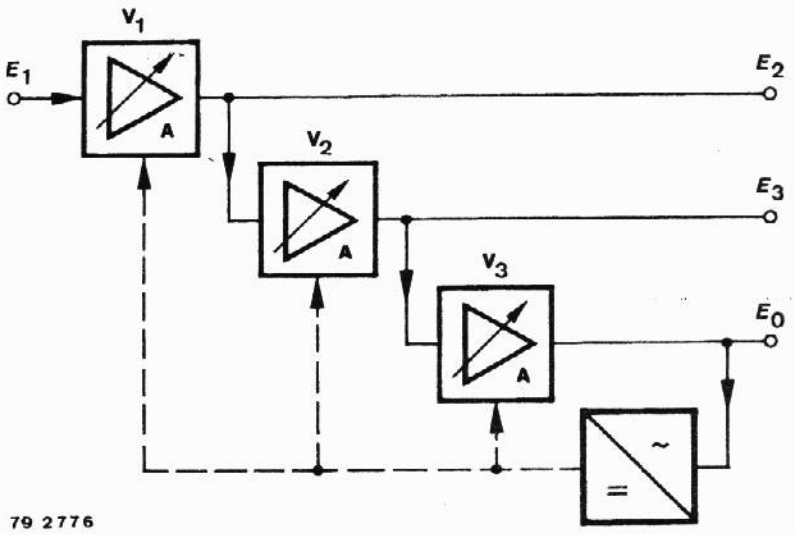
In terms of logarithmic representation this means that a constant level error in the channel equal to log a produces merely a k-time greater constant output level error (k being the compression factor). Thus, the output signal E_4 will remain unchanged except for a volume level error.

3. Implementation of the cascaded amplifier chain principle

The principles outlined in the previous paragraph prove that it is particularly advantageous to provide the compander with the characteristics leading to straight lines in logarithmic representation. The resultant compression factor is then determined by characteristics of the control circuit shown in Fig. 2.

Perfect linearity of the characteristics in the logarithmic representation may be achieved only when both the compressor and expander process the signals very accurately and behave in accordance with the equations (2.8) and (2.9) over the entire dynamic range of E_2 and E_3.

Moreover, if a signal level error is to affect only the overall volume level, it is also necessary to make sure that the dynamic response of the control circuit is constant and independent of the starting point on the characteristic. Thus, high performance characteristics on the part of the rectifier and control circuit are necessary.



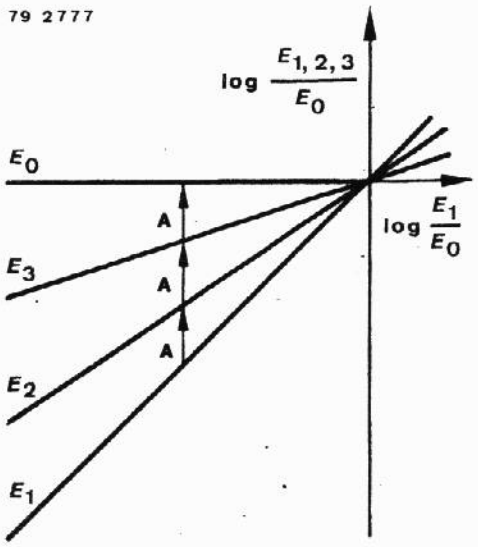


Fig. 4:
Cascaded amplifiers principle (a) and its operating characteristics (b).

If n identical amplifiers are cascaded, and their gain factor A is controlled so that the output voltage of the last amplifier is constant and equal to E_o (Figure 4), the following expression is true:

$$E_O = A^n \cdot E_1 \qquad (3.1)$$

Hence, if the output of the v^{th} amplifier is now considered an output, then:

$$E_O = A^{n-v} \cdot E_V \qquad (3.2)$$

and the corresponding compressor gain will be:

$$A^v = \left(\frac{E_v}{E_o}\right)^{-\frac{v}{n-v}} \qquad (3.3)$$

When comparing this with equation (2.8), we can see that the compression factor k is expressed here as:

$$k = \frac{n}{n-v} \qquad (3.4)$$

Expression (3.4) shows that the described procedure can lead to any compression factor represented as a function of the integer numbers n and v. In Fig. 4 an example of a circuit configuration for n = 3 and v = 1 has been shown. One advantage of such arrangement is that the rectifier is expected to handle a signal E_o with an essentially constant magnitude. Therefore, the dynamic responses will be always the same, regardless of any particular starting point on the characteristic. Moreover, since the compander characteristic is not determined by the behavior of any particular rectifier but rather the cascaded arrangement of the identical amplifier components, this approach becomes highly suitable for monolithic integration.

4. Static Characteristics of the HIGH COM compander

A large compression factor "k" is vital for the most effective compander performance. However, excessively high "k" is also undesirable since the signal level errors of the transmission channel are also amplified by the factor "k" at the expander's output (see 2.12). A value of k = 2 constitutes a convenient compromise, while preventing excessive circuit complexity (two gain-controlled amplifiers are employed, i.e. n = 2 and v = 1 in accordance with the requirements of (3.4).

In order to ensure sufficient suppression of high frequency spectral noise components generated during recording on tape, a fixed pre-emphasis in the compressor and corresponding de-emphasis in the expander are used in addition to the linear gain control in the compressor and the expander. Thus, each amplifier block in Fig. 4 consists of a gain-controlled amplifier and a treble boost network (1) (see Fig. 5). Accordingly, the expander contains a complementary-function gain controlled amplifier and a network (2) for treble cut. This way, the treble boost in the compressor cannot lead to channel overdrive in the case of a treble-dominant wanted signal, since in this case the gain controlled compressor amplifier would reduce the overall gain by the corresponding amount.

Two further measures to reduce effective tape drive level at high frequencies are adopted on account of the rather limited treble frequency drive capability of the cassette tapes. Treble boost (3) (see Fig. 5, ahead of the rectifier) provides for a frequency-dependent reduction of the reference voltage E_o in Fig. 4. This displaces the compander characteristics towards the angular bisector of the third quandrant at high frequencies. Furthermore, a fixed treble cut (4) is also performed at the compressor output, thus displacing the compander characteristic in Fig. 6 in the negative direction on the vertical axis. A corresponding treble boost (5) is provided ahead of the expander. The treble boost (3) is also placed ahead of the rectifier. Fig. 6 shows the resulting compander characteristics for three different signal frequencies.

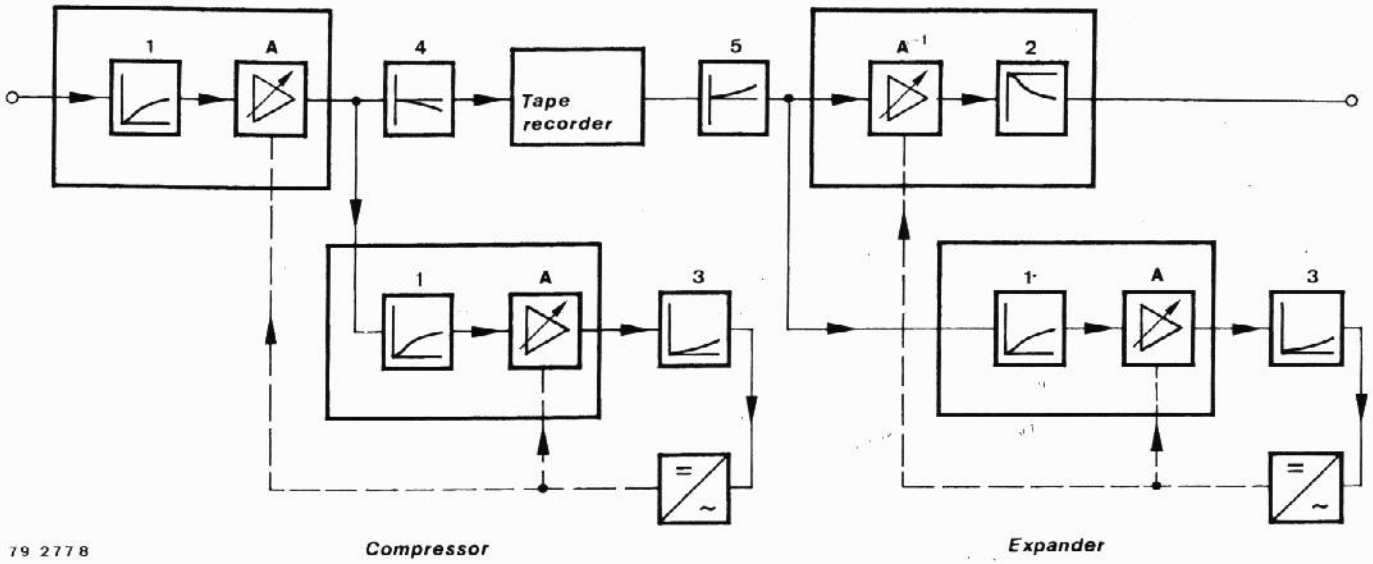


Fig. 5:
Block diagram of the HIGH COM companding circuitry.

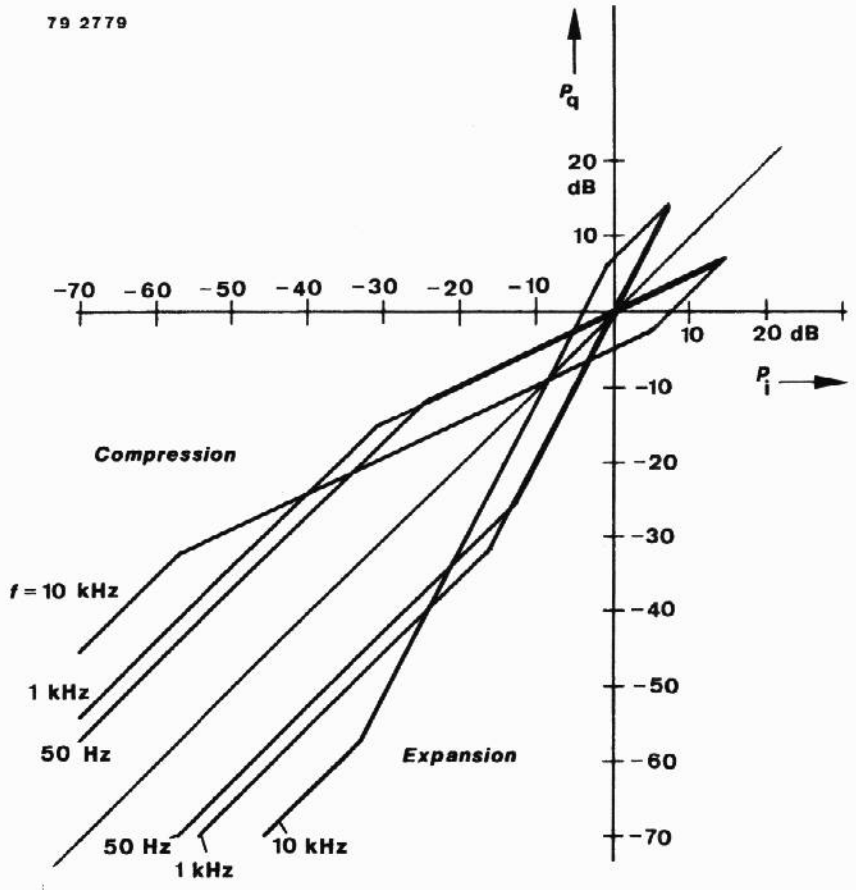


Fig. 6:
HIGH COM compander characteristics.

The noise suppression degree achieved by the HIGH COM compander is illustrated in Fig. 7. The noise reduction factor attained is 20 dB (rms, curve A) and about 15 dB for the low frequency disturbances.

Fig. 8 shows the effect of a ± 6 dB level error between compressor and expander on the overall frequency response characteristic. While the latter remains unchanged, the primary level error is doubled in accordance with (2.12).

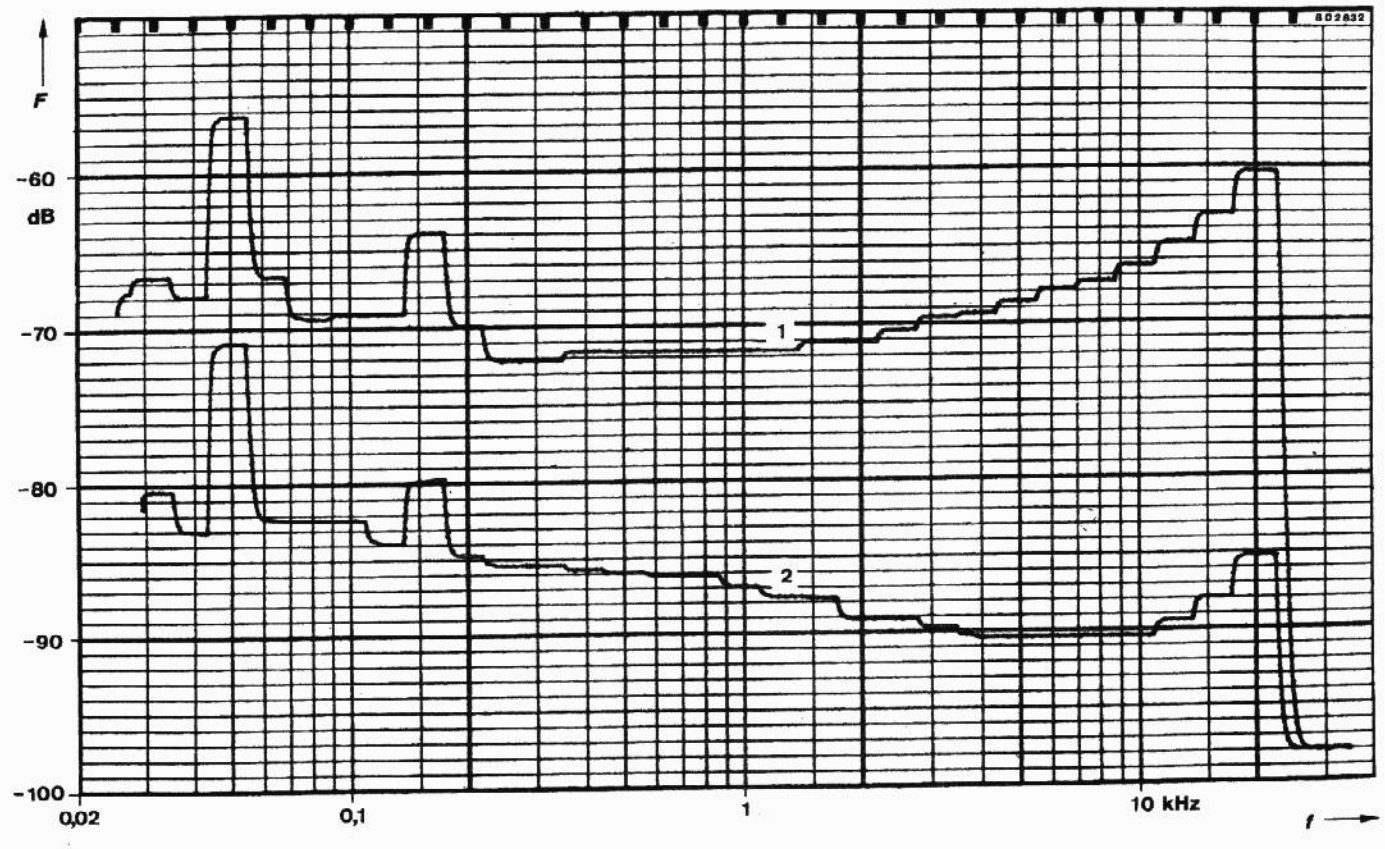


Fig. 7:
Noise spectrum characteristics of a cassette tape: Without compander (1), and with the HIGH COM compander (2).

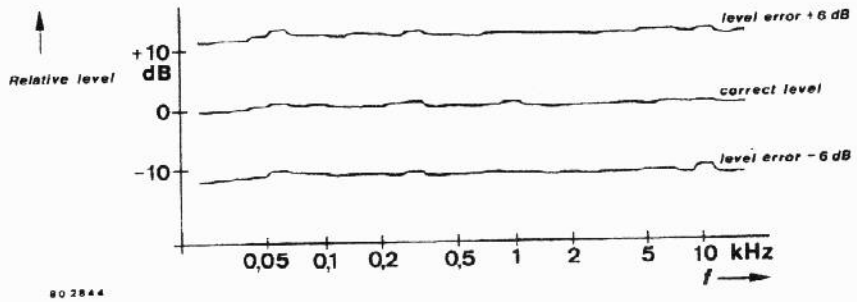


Fig. 8:
Frequency response of a transmission channel incorporating HIGH COM: with no level error (1) with + 6 dB level error (2), and with – 6 dB level error between compressor and expander. (Measurements made with pink noise generator and 1/3 octave analysis).

5. The U401BR HIGH COM IC.

The following description of the circuit refers to the U401BR IC shown in Fig. 9.

5.1 Supply voltage

The supply voltage V_{cc} in the range of 12V... 20V is applied between pins 2 ($+V_{cc}$) and 1 (ground). This voltage is halved at pin 21 by means of two 12K resistors and a filter capacitor C 20. A reference voltage (pin 23) with a very low source impedance is generated internally from the voltage at C 20 by the operational voltage follower X1 with a built-in current limiter. Pin 23 is also capacitively decoupled to ensure overall stability.

The reference voltage V_R appearing at pin 4 is produced from the voltage an pin 1 with the aid of a Zener diode; the V_R is always maintained 6 V above the voltage at pin 23. With a 10 μF capacitor connected to pin 21, the maximum permissible 100 Hz ripple on the supply voltage is 10 mV rms when the amplifier A is not used; otherwise it should not exceed 3 mV rms. In Fig. 10 a typical characteristic of the supply current I_S versus supply voltage V_{cc} has been shown.

A single-ended supply is shown in Fig. 9, but the application of a split supply ($\pm$ 6 ... $\pm$ 10V) is also possible. The midpoint of a supply should then be connected to pin 21. The capacitors C_6 and C_7 must remain connected to pin 1 of the U 401 B.

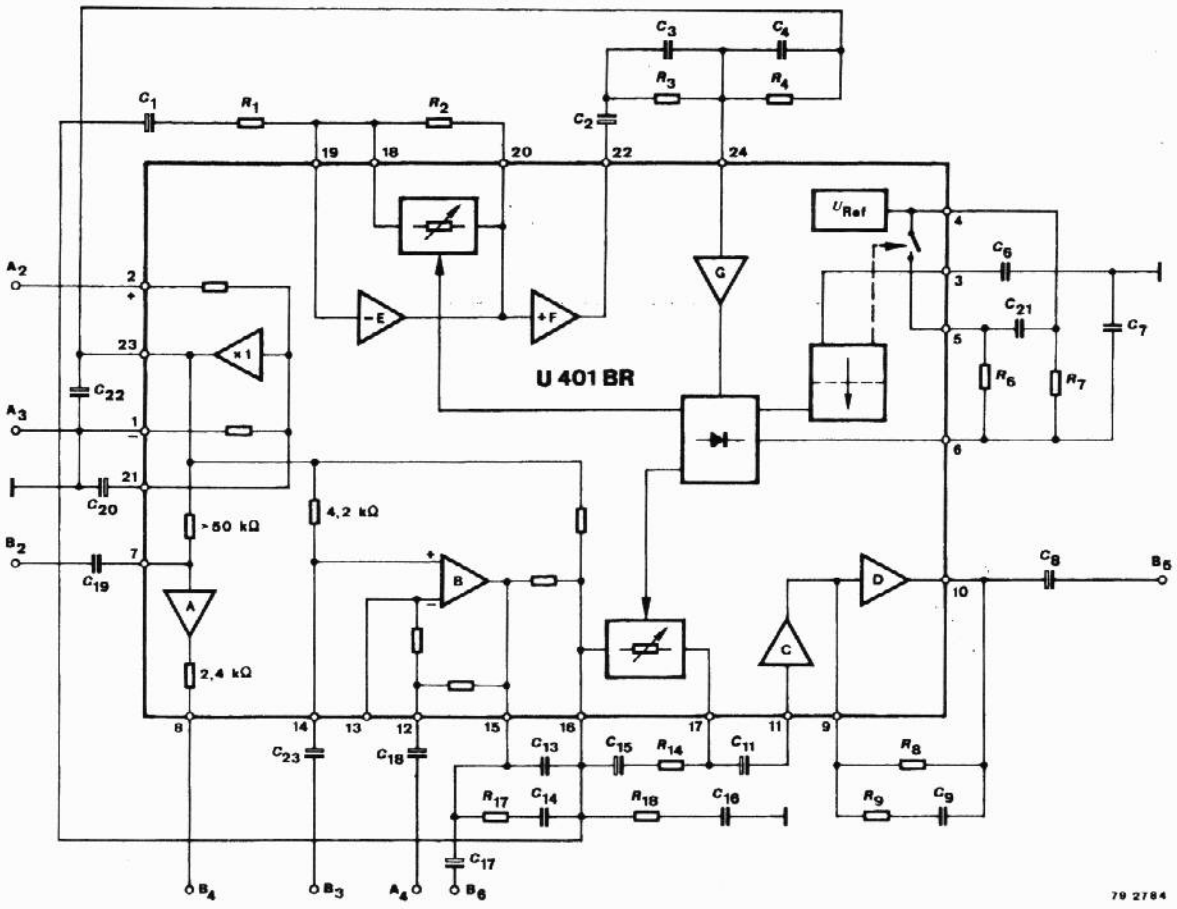


Fig. 9:

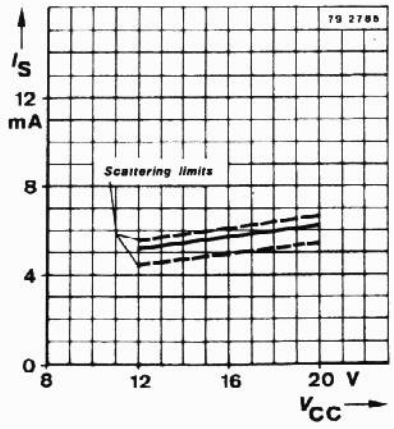


Fig. 10:
Typical current consumption characteristics of the U401B HIGH COM IC.

5.2 Input amplifier

The internal low noise input amplifier A is connected between pins 7 and 8. The amplifier has a 30 dB gain and a typical input impedance of 80 K; thus, direct capacitive coupling is possible. The external signal source impedance should be less than 10 K to ensure amplifier's stability and prevent spurious signal injection from other circuit sections.

The output of A (pin 8) and the input of the next amplifier (pin 14) have built-in terminating resistors for insertion of a multiplex filter (Fig. 11). The resistors attenuate the output signal of A to maintain the overall gain between pin 7 and pin 14 at the 26 dB level.

The maximum rms output voltage of the amplifier A for 1% THD is shown in Fig. 12.

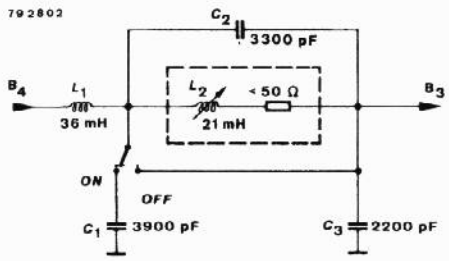


Fig. 11:
19 kHz multiplex filter.

5.3 Amplifier B

A non-inverting operational amplifier with internal unity gain negative feedback loop is connected between pins 14 and 15. Since the amplifier has built-in output current limiter, it is therefore short circuit-protected; its output impedance is less than 10 ohms. In Figure 13 the behavior of the maximum output voltage versus V_{cc} has been shown for two different values of the load R_L and for 1 KHz 1% THD.

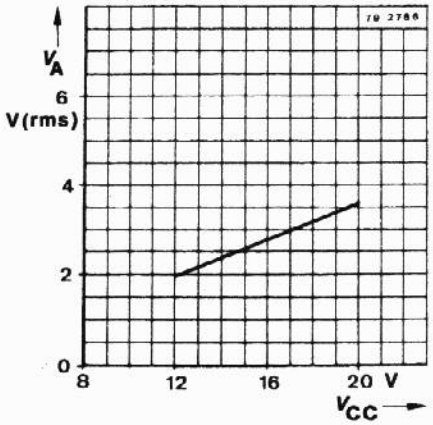


Fig. 12:
Maximum rms output voltage of the amplifier A for 1% THD as a function of the power supply voltage V_{cc} (pins 8 and 14 linked).

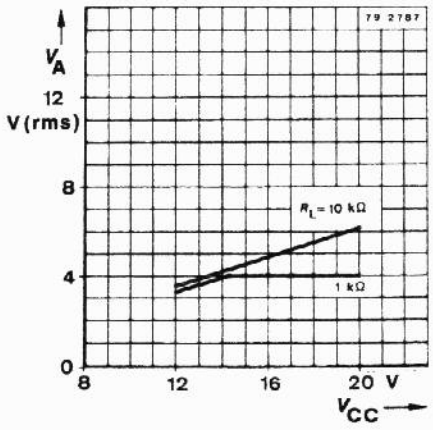


Fig. 13:
Maximum rms output voltage of the amplifier B for 1% THD as a function of the power supply voltage V_{cc} and varying load resistances.

5.4 The C and D amplifiers

C and D are the inverting amplifiers operating in a cascaded configuration. The input at pin 11 has a current sensitive characteristic. The output of the D (pin 10) has a built-in current limiter and output impedance similar to that of B. The gain of both amplifiers is determined by the resistor R_{14} at pin 11 and the resistor R_8 connected between pins 10 and 9 in the following manner:

$$K_{C,D} = 2.55 \cdot \frac{R_8}{R_{14}} \qquad (5.1)$$

5.5 Expander

The cascaded network consisting of the amplifier B, the first control network between pins 16 and 17 and the amplifiers C and D constitutes expander's essential signal path. The R_8-R_9-C_9 network reduces the effective gain at higher frequencies and forms an active low-pass filter for expander de-emphasis (See 2 in Fig. 5).

The first control resistor R_{C1} is internally connected in parallel with the resistor R_{14}, so that the gain $K_{C,D}$ increases when the R_{C1} is decreased.

The external C_{13}-C_{14}-C_{16}-R_{17}-R_{18} network connected between pins 15 and 16 corresponds to the block (5) in Fig. 5.

The gain between pins 14 and 10 is equal to 1 at low frequencies, when the total impedance seen between pins 16 and 17 is 3K. The capacitors C_{11} and C_{15} prevent DC fluctuations caused by control resistance changes.

5.6 Generation of the control voltage

In order to generate proper control signal, part of the processed signal is tapped off at pin 16 at the output network (5), (but ahead of the gain controlled expander amplifier - Fig. 5) and delivered via C_1 to the amplifiers E and F. The gain of the inverting amplifier E is determined by the ratio of the parallel combination of R_2 and the control element R_{C2} to R_1. Consequently, the gain decreases as the resistance of the control element R_{C2} decreases. Thus, the behavior of the gain controlled amplifier E is opposite to that of amplifier C, as implied by the configuration shown in Fig. 5.

Subsequently, the amplifier F boosts the signal by a factor of 10. The F's output (pin 22) is connected to the input of the rectifier amplifier (pin 24) via a passive high-pass filter which combines the functions of the networks (1) and (3) from Fig. 5. Since the rectifier operates at the center point voltage, pin 24 must also be tied via R_4 to the center point voltage at pin 23.

5.7 Rectifier

The rectifier produces the gain control voltage according to a full wave threshold principle. When the voltage at pin 24 differs by more than ± 70 mV DC from the center point voltage at pin 23, a current sink circuit is switched on at pin 6. The current delivered internally to pin 1 is proportional to the threshold overshoot at pin 24 until the maximum value of 2.5 mA is reached, and is used to discharge the storage capacitor C_7 at pin 6, thus changing the voltage at this pin.

The capacitor C_7 is recharged towards more positive voltages from the reference voltage source at pin 4, via the R_6-R_7 network.

The equilibrium at pin 6 will be reached when the integral of current flow into pin 6 produced by threshold overshoots is equal to the charging current delivered through R_7 and R_6. This implies that the magnitude of the equilibrium gain control voltage is independent of the magnitude of the voltage at pin 24.

However, in the circuit as the whole, the gain control voltage depends on both the input voltage of the expander and the output voltage of the compressor, since they are related through the gain A of the amplifier E to the constant input voltage at pin 24. The gain A is determined by the value of the second control element which, in turn, is dependent on the control voltage. Thus, in spite of constant input voltage to the rectifier, the gain control voltage depends on the input signal level of

the circuit and an unambiguous control state is established. The gain control voltage can assume values between:

$$E_{6max} = E_{23} + 1.5\,V \quad (5.2)$$

in the absence of a signal and:

$$E_{6min} = E_{23} - 2.0\,V \quad (5.3)$$

with increasing signal level.

For E_{6max} the control elements have their maximum resistance values in excess of 100 K, while for E_{6min} the minimum resistance is 450 ohm. In conjunction with the 15 K parallel resistors R_2 and R_7, a gain control range of 30 dB is thus attained for C and E amplifiers.

The shortest response time of the rectifier to a positive step change of input voltage is determined by the value of the storage capacitor C_7 and the maximum current of the current sink at pin 6. This time reaches 0.3 ms for full swing of the gain control voltage. Since virtually all natural sound effects have longer transient times, the compander is thus capable of accurate processing and reproduction of such transients.

5.8 One shot circuit

The gain control voltage decay time is determined by the value of the capacitor C_7 and the charging current flowing through the resistors R_7 and R_6. A short decay time is naturally desirable for good performance of the compander in order to prevent audible noise trailers after an abrupt termination of wanted signal. On the other hand, an unduly short decay time produces variations of the gain control voltage in response to a low frequency wanted signal leading to signal distortion via the gain control loop. Theoretically (see paragraph 2), such distortion would be cancelled again in the expander, but this is true only when the transmission channel has ideal performance characteristics. In the real channel, however, it is important that the distortion be kept as low as possible already in the compressor; this requirement, in turn, calls for a long decay time. A delay circuit in the form of retriggerable monoflop is provided to meet these two contradictory requirements.

In the passive state, pins 4 and 5 are linked internally. The monoflop is fired each time an applied signal exceeds the rectifier threshold, and this, in turn, opens the switch between pins 4 and 5. Thus, the decay will be determined by C_7 and R_7 when a signal is present, and these components have been dimensioned to keep distortion at low frequencies at minimum level. The pulse-width of the one shot circuit has been chosen so that each half cycle of a 20 Hz signal is still able to retrigger the circuit.

If the wanted signal terminates abruptly, the internal switch connects the resistor R_6 in parallel with the resistor R_7 after elapsing of the "HOLD" time, thus considerably shortening the decay time so that noise trailers remain inaudible.

The capacitor between pins 4 and 5 shortens the decay time even further when the wanted signal is shorter than the "HOLD" time of the one shot. At the moment the switch is being open, C_{21} holds pin 5 to the level of pin 4 momentarily and for a short time the charging current continues to flow through R_6. This way the decay time does not increase abruptly upon signal commencement but rather rises slowly through C_{21}.

Figure 14 shows the gain control voltage response characteristics at the compressor for a 10 kHz signal burst at a 600 mV level (pin 14).

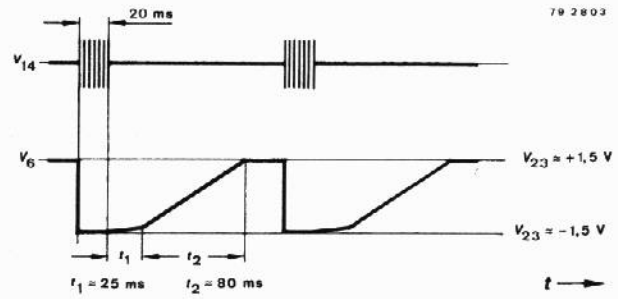


Fig. 14:
The gain control voltage characteristics for the compressor stage (pin 6) measured for a 10 kHz, 600 mV input burst.

5.9 The compressor circuit

According to Fig. 2, the expander comprises the circuitry between pins 15 and 10, and the branch path from pin 16. As shown in Fig. 3, the associated complementary compressor is formed by placing the expander in the negative feedback loop of the amplifier B (external link between pins 10 and 12). If such a connection ensures adequately low resistance, the internal negative feedback resistor between pin 15 and pin 12 has no longer any effect on the gain of B. In order to secure this condition, C_8 and C_{18} should have a relatively large value (e.g. 47 μF in the circuit shown). Any additional resistance implemented to the link between pins 10 and 12 must not exceed 70 ohms. Negative feedback signal should be fed to pin 12 since the internal auxiliary network is contained between pins 12 and 13 (to suppress closed loop parasitic oscillation).

5.10 Circuit outputs

The output signals of the compressor and the expander are available at their respective low impedance ($R_i < 10$ ohms) short circuit protected outputs. As long as the corresponding functions are not switched off, the compressed signal is present at pin 15 and the expanded signal at pin 10 (see also Section 6).

5.11 Characteristics

The compander characteristics as referred to signal level diagram, have already been shown in Fig. 6. In Fig. 15 the level characteristics for the compressor as a function of signal frequency were given while Table 1 presents the output levels of the compressor for three different frequencies and various input levels.

It should be noted that the depicted curves shown in Fig. 15 do not represent frequency response characteristics in the conventional sense. Frequency response measurement of a circuit utilizing a sweep signal is permissible only when the circuit characteristics do not change during the measurement, i.e. in the course of the actual sweep. During the measurements reflected in Fig. 15, however, the circuit characteristics do change, since the gain control state of the compressor not only depends on the input level, but also on the frequency of the test signal. Consequently, a correct measurement of the frequency response would call for a test signal with which measurements are possible without changing the gain control state. One possibility is to use pink noise as a test signal and interpret the measurements by means of 1/3 octave analysis.

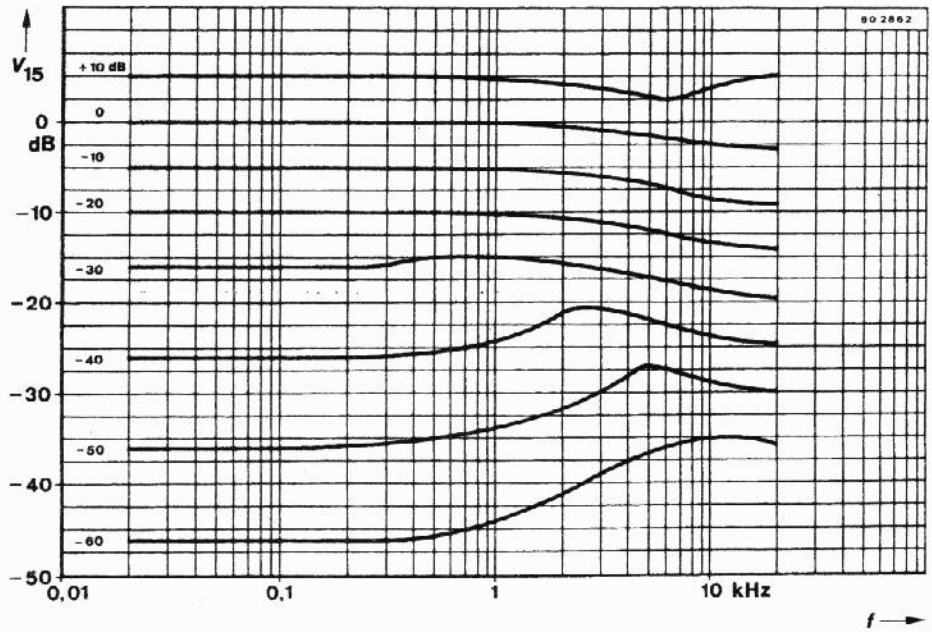


Fig. 15:
Signal level characteristics at the compressor output (pin 15) for various input signal levels.

TABLE 1

Hz \ dB	+10	0	−10	−20	−25	−30	−40	−50	−60
315 Hz	+ 5,0	±0	− 5,0	−10,0	−12,5	−16,0	−26,0	−36,0	−46,0
5 kHz	+ 3,0	− 2,5	− 7,5	−12,5	−15,0	−17,5	−22,5	−27,5	−37,0
20 kHz	+ 5,5	− 4,0	− 9,5	−14,5	−17,0	−19,5	−24,5	−29,5	−35,0

The block diagram of Fig. 5 implies that the frequency response of the compressor is determined by the cascaded filters (1) and (4) for every fixed gain control state. This fact is confirmed by the characteristics shown in Fig. 16, where the 1/3 octave analysis has been performed after the measurements of the compressor output signal with an input pink noise test signal.

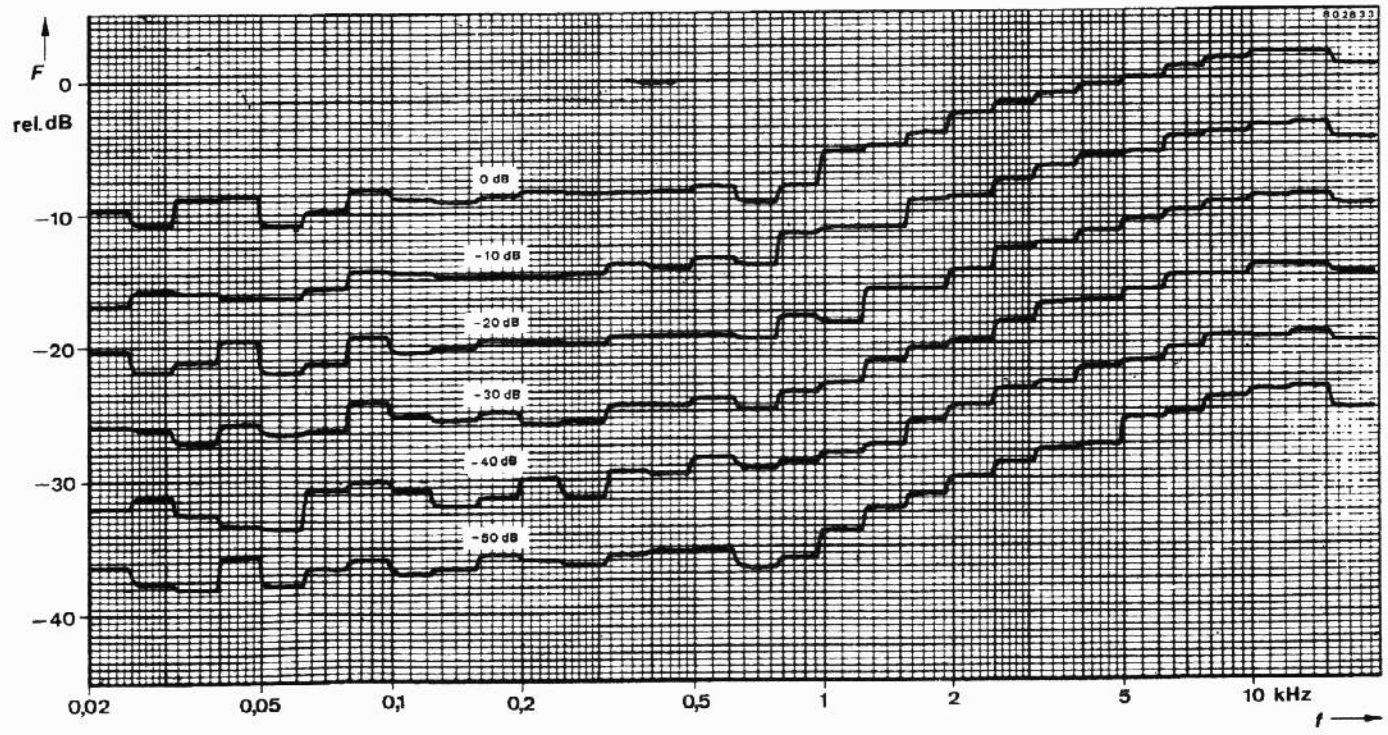


Fig. 16:
Frequency response of HIGH COM compressor for various input levels measured with pink noise input signal (1/3 octave analysis).

5.12 Alignment

The point of intersection of the characteristics shown in Fig. 6 corresponds the 315 Hz/600 mV signal level at pin 15. This value has been chosen as a 0 dB reference level for all other level specifications corresponding to expected magnetization of 200 nWb/m when recording on cassette tape. Consequently, the expander should be aligned so that reproduction of a 200 nWb/m recording produces a 600 mV signal level at pin 15. Test tapes with standard magnetization of 200 nWb/m are available from various manufacturers. Table 2 lists some of these sources although no claim is made as to its comprehension. The difference between a 400 Hz recording and the previously specified 315 Hz test signal frequency is negligible.

The location of the 0 dB intersection point (corresponding to 600 mV) is determined by the magnitude of the rectifier threshold voltage at pin 24 and the gain between pins 16 and 24. According to Fig. 17, the rectifier threshold voltage at pin 24 depends on the supply voltage V_{cc} (Fig. 18). Alignment is performed by varying the value of the resistor R_1 according to Fig. 19.

TABLE 2

BASF Badische Anilin- und Sodafabrik D-6700 Ludwigshafen West Germany	RCA Special Products 6550 E. 30th Street Indianapolis, Indiana 46219 USA (part no. 127)
TEAC Corporation 3-7-3 Naka-cho Musashino Tokyo, Japan (part no. MTT-150)	TEAC Corporation of America 7733 Telegraph Road Montebello, CA 90640 USA (part no. MTT-150)

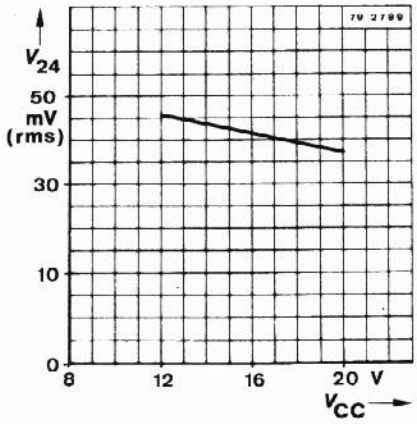


Fig. 17:
The dependence of the rectifier threshold voltage rms, pin 24 on supply voltage V_{cc}.

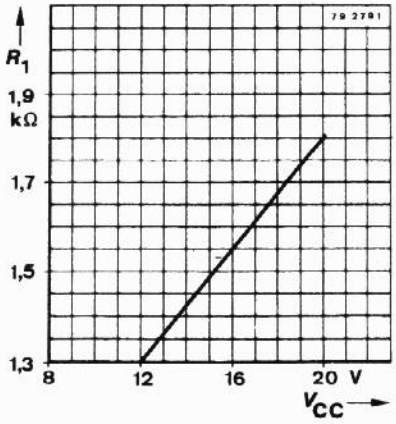


Fig. 19:
Typical values of R_1 vs. V_{cc}, as required to correct, the deviation shown in Fig.18.

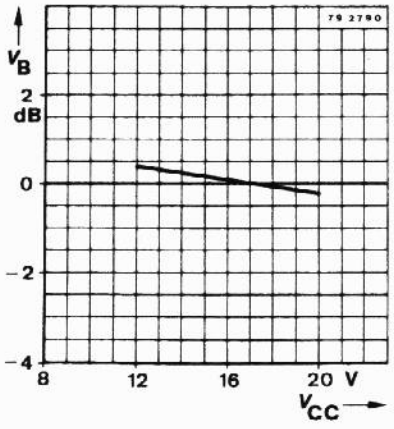


Fig. 18:
Compressor's output level deviation (0 dB reference) as a function of a supply voltage V_{cc} for 315 kHz, 0 dB input signal at pin 14.

6. Design examples

6.1 Circuit layout

A typical layout of the complete HIGH COM broadband compander module (as shown in Fig. 9), has been shown in Figures 20 and 21. In Table 3 all the necessary external components have been listed. The interfacing connections of the terminal points A_1 to A_4 and B_1 to B_6 are described in the following paragraphs.

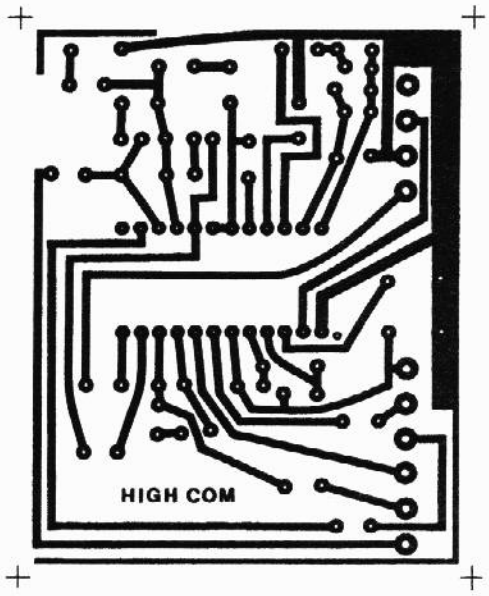


Fig. 20:
PC layout of the HIGH COM test module.

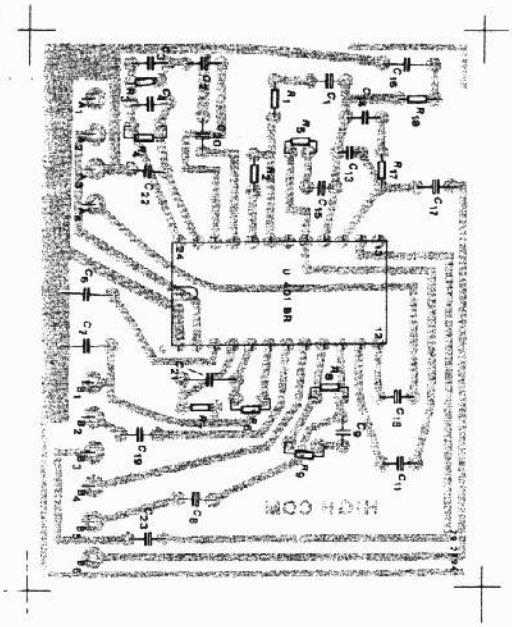


Fig. 21:
Components layout of the HIGH COM test module.

List of components

R_1 = see Fig. 19	C_1 = 22 µF 6,3V	C_{14} = 0.01µF 5%
R_2 = 15 kΩ 2%	C_2 = 4.7 µF 16V	C_{15} = 2.2 µF 16V
R_3 = 47 kΩ 2%	C_3 = 3.3 nF 5%	C_{16} = 0.033µF 10%
R_4 = 5.6 kΩ 2%	C_4 = 1000pF 10%	C_{17} = 10 µF 16V
R_6 = 820 kΩ 2%	C_6 = 0.68µF 5%	C_{18} = 47 µF 16V
R_7 = 8.2MΩ 5%	C_7 = 0.22µF 5%	C_{19} = 0.15µF 10%
R_8 = 33 kΩ 2%	C_8 = 47 µF 16V	C_{20} = 10 µF 16V
R_9 = 5.6 kΩ 2%	C_9 = 3300pF 5%	C_{21} = 0.015µF 5%
R_{14} = 15 kΩ 2%	C_{11} = 47 µF 16V	C_{22} = 100 µF 16V
R_{17} = 1.5 kΩ 2%	C_{13} = 1000pF 10%	C_{23} = 2.2 µF 16V
R_{18} = 56 kΩ 5%		

TABLE 3

6.2 Switched compander

Fig. 22 shows the interfacing connections of the circuit shown in Fig. 9 for a complete switched compander module. Respective DPST switches are required for the control functions "ON/OFF" and "Record/Playback".

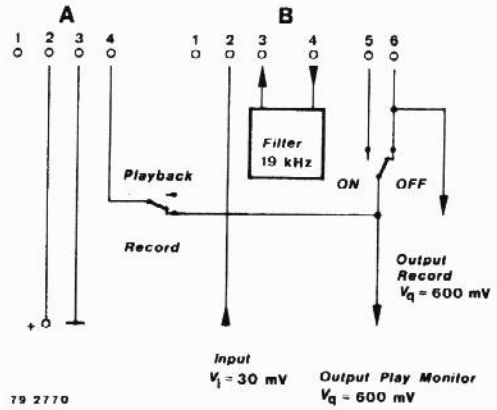


Fig. 22:
External connections for a switched compander module.

6.3 Non-switched compressor/expander

For applications such as triple head units with tape monitor, the respective circuits for "compressor-only" (Fig. 23) and "expander-only" (Fig. 24) may be obtained by slight modification of the circuit shown in Fig. 22.

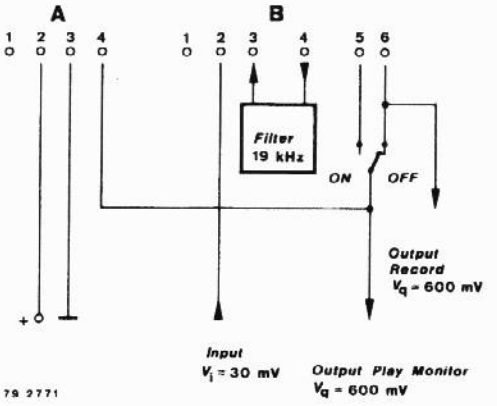


Fig. 23:
External connections for the »compressor-only« HIGH COM configuration.

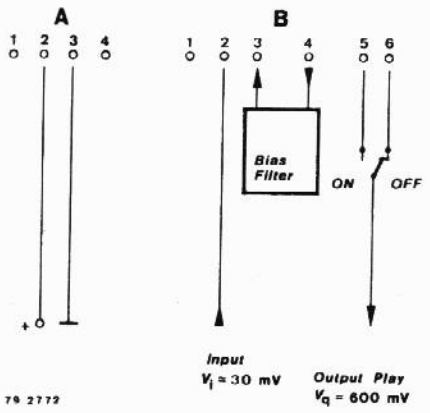


Fig. 24:
External connections for the »expander-only« HIGH COM configuration.

6.4 Operation with high input signal levels.

If a signal level of 0 dB = 600 mV, or greater, is already available for driving the compressor and/or the expander, the amplifier A can be omitted in the signal path (Fig. 25) and the signal may be fed to pin 14 directly through the terminal point B_3. Otherwise Fig. 25 fully corresponds to Fig. 22.

It should be noted that the input impedance at pin 14 is 4.2 K and the signals must be fed to this pin through a bandwidth-restricting (or multiplex) filter.

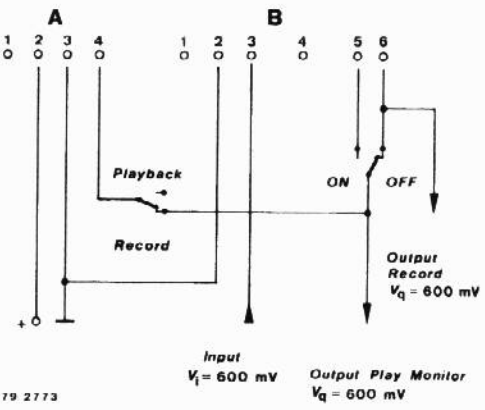


Fig. 25:
External connections for a switched compander module with the amplifier A not used.

6.5 Output decoupling

If the terminating impedance is lower than 5 K at the monitor or playback output it should be decoupled with a separate isolating capacitor to prevent low frequency oscillation. In this case, external wiring should be performed in accordance with Fig. 26.

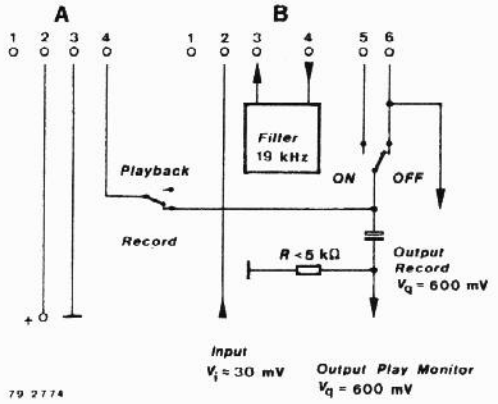


Fig. 26:
External connections for a switched compander module with the load resistance at the playback/monitor output lower than 5K.

6.6 "DNR" expander

With a simple additional circuit comprising only a few components, the HIGH COM expander can be also employed as expander for signals compressed up to 10 dB and commencing from several hundred Hz. For example, Dolby® processed cassettes can be thus reproduced.

Fig. 27 shows the circuit modifications (with respect to Fig. 9) neccessary to incorporate this feature.

® Dolby is a registered trademark of Dolby Laboratories Inc.

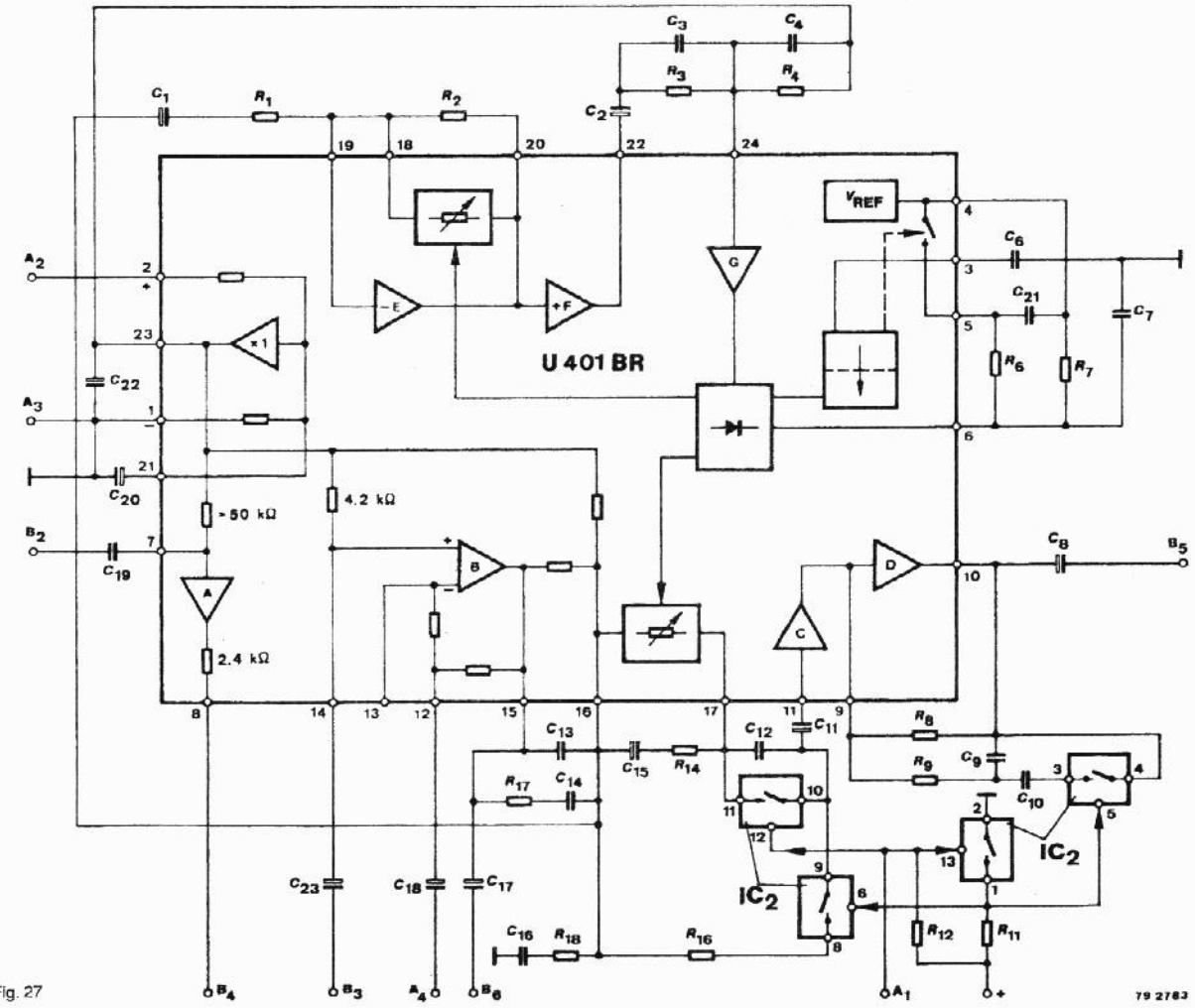


Fig. 27

In Fig. 28 a recommended printed circuit board layout has been shown; Fig. 29 shows the corresponding layout of components, while the additional required components are listed in Tab. 4. The external wiring (Fig. 30) differs from that in Fig. 22 only by the additional switch at terminal A_1.

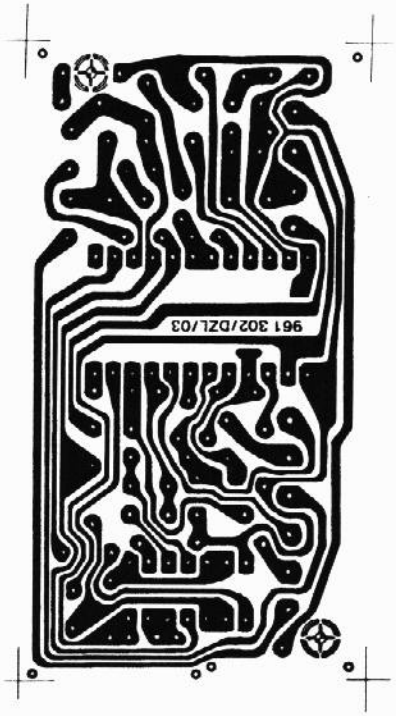


Fig. 28

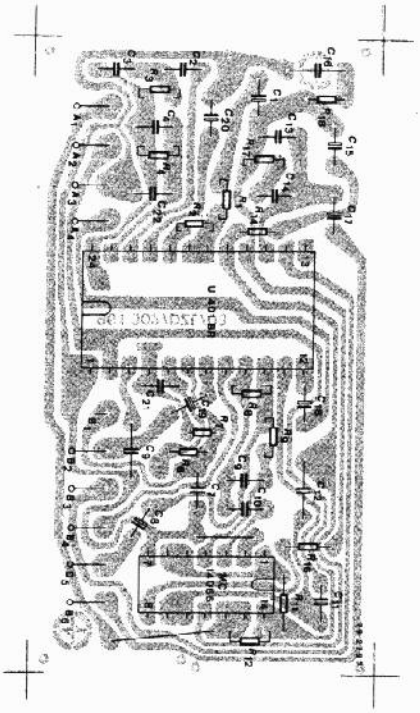


Fig. 29

Also, another design configuration based on Fig. 24 or

Fig. 25 is possible.
The "Playback", "ON" and "DNR expander" functions must be switched on simultaneously for "DNR expander" playback mode (see Fig. 30).

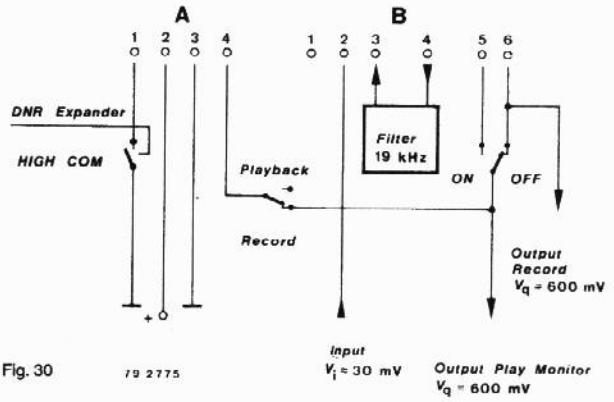


Fig. 30

R_{11} = 10 kΩ 20%	C_{12} = 0.068 μF 5%	IC 2 (CMOS switch IC):
R_{12} = 10 kΩ 20%	C_{10} = 1200 pF 5%	MC 14066 ($V_{cc\,max}$ = 18 V)
R_{16} = 3.3 kΩ 2%		CD 4066 ($V_{cc\,max}$ = 15 V)

TABLE 4

7. Rectifier offset

The second-order harmonic distortion (a_{K_2}) at low frequencies can be lowered by compensating the rectifier offset voltage at PIN 24. A suitable additional circuit is shown in Fig. 31 (Measurement e.g. at 40 Hz and reference level).

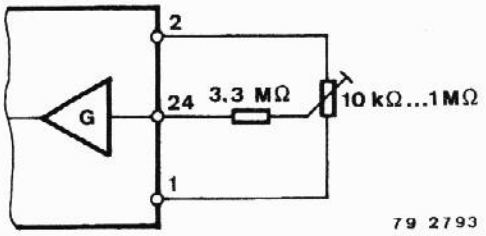


Fig. 31:
Rectifier input offset compensation (pin 24).

8. Other technical specifications

Figure 32 shows the maximum tolerable high-frequency signal levels relative to 0 dB ≙ 600 mV at PIN 14, such that compressor action is controlled by the wanted signals only and not by these high-frequency signals. High-frequency interfering signals at the input of the expander should not exceed −40 dB.

Rumble noise at the input of the compressor shall not exceed the following levels: $f \leq 12$ Hz $U \leq 600$ mV −30 dB
$f \leq 7$ Hz $U \leq 600$ mV −40 dB

Overall technical characteristics of the U401BR HIGH COM integrated circuit have been compiled in Table 5.

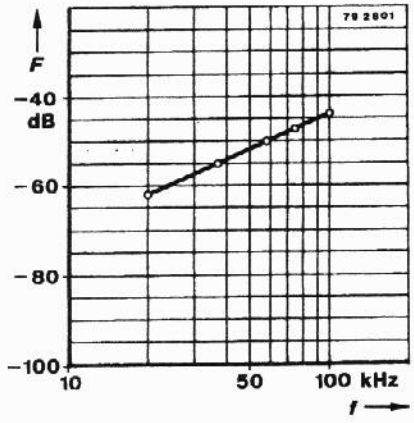


Fig. 32:
Maximum acceptable limits of high frequency interfering voltages at the input of the compressor as referred to 0 dB = 600 mV at pin 14.

Absolute maximum ratings

Reference point pin 1, unless otherwise specified

Supply voltage	pin 2	V_{cc}	24	V
Ambient temperature range		t_{amb}	0...+70	°C
Storage temperature range		t_{stg}	−55...+125	°C

Electrical characteristics

$V_{cc} = 15$ V, $f = 20$ Hz...20 kHz, $t_{amb} = 25$ °C, Reference point pin 1, unless otherwise specified.
All levels refer to $V_2 = 600\ mV_{rms} = 0$ dB, at pin 15.

			Min.	Typ.	Max.	
Supply voltage range	pin 2	V_{cc} 12	12		20	V
Supply current	pin 2	I_S		7		mA
Voltage gain f = 1 kHz, pins 8 and 14 are not connected Position: Playback	 pin 7-8 pin 7-15	 A_u A_u		 30 26		 dB dB
Distortion f = 1 kHz, Position: Record	 pin 15	 k		 0,2		 %
Overload reserve $V_{cc} = 12$ V, f = 1 kHz, k ≦ 1%	 pin 8	 $+A_u$		 12		 dB
Signal to noise ratio according to DIN 45511 (DIN 45633 rms, A-weighted) $R_G = 10$ kΩ (pin 7)	 pin 8	 $\frac{U_q}{U_{qn}}$		 80		 dB
Compander gain A-weighted		A_{uwtd}		20		dB
Compander gain unweighted		A_u		14		dB
Input resistance Output resistance	pin 7 pin 14 pin 8 pin 10 pin 15	R_i R_i R_q R_q R_q	50	100 4,2 2,4 <10 <10		kΩ kΩ kΩ Ω Ω

TABLE 5