# *Upgrade to a PDP11 Single Board Computer*

## *AE 24675*

## AE Abstract

Mentec Limited is a computer systems company, which employs 175 people in various countries and has an annual turnover in the region of 25 mECU. Mentec Limited has designed and delivered a number of electronic sub-systems (Single Board Computers) over the last ten years based on Intel and DEC microprocessors. The company has specialised in delivering PDP11 type processors for use in embedded processor/Real Time systems. Mentec Limited has implemented these Single Board Computers by using modern programmable logic and microprocessor technology.

Mentec Limited's market segment is a robust one because many large organisations have invested millions in PDP based software systems. While the option of upgrading these systems' performance exists, these companies are not inclined to completely redesign their systems. Some examples of these application areas include, Telecom Switches, Power Station Controls, Paper Control Systems and Financial Networks. By utilising an ASIC based design, Mentec Limited can offer greater performance over its existing Bit Slice Technology offering.

The economic benefits of such an undertaking will result in continued sales and reduced production costs. If the technical goals of the Application Experiment can be achieved the commercial risk will be small. The main technical risk was associated with the ASIC itself. The advice we have received from our consultants is that the ASIC requirements are not over complex and therefore the risk is low.

Beginning in April 1997 the Application Experiment was expected to take 12 months for completion at a cost of 183K ECU's. The Payback period for the initial investment return is immediate as the first orders received for the new product cover the investment costs. The ROI for the product is an estimated increase of 53% of board sales for the year 1999. There fore the time to market for this higher performance ASIC based computer is of great importance as the market demand for it already exists. As this was Mentec Limited's first ASIC design a close working relationship with Mentec Limited's consultant partners would be central to the success of the Application Experiment. This Application Experiment will allow Mentec Limited to undertake further ASIC design projects involving its other product lines in the future.

## 1. Company Name and Address

Mentec Limited
Dun Laoghaire Industrial Estate
Pottery Road
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Co. Dublin Ireland

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Mentec Limited.
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## 2. Company size

Mentec Limited employs 175 people at four sites, Dublin Ireland (120), Manchester UK (35), London UK (5) and Boston USA (15). This Application Experiment was carried out at the Dublin Head Quarters and within the Research and Development Group. The design team included three Hardware Design Engineers and one Software Engineer, all with previous experience in the Digital Design environment. The main design team consisted of:

| | | | |
|---|---|---|---|
| Martin Collins | MEng. | Project | Leader |
| Michael Byrne | BEng. | Design Engineer | |
| Brendan McGreen | MSc. | Design Engineer | |
| Dave Carroll | | Software Engineer Microcode | |

Additional team members who contributed as required were,

| | | |
|---|---|---|
| Helen Griffin | BEng. | Production Engineer |
| Brian Farrell | Dip.EE | R & D Technician |

## 3. Company business description

Mentec Limited, a private Irish-based company was founded in 1978 by Dr. Michael Peirce, to address perceived business opportunities arising from the application of computers to industrial processes and environments. The company now addresses a number of segments within the IT market, has a turnover of 25mECU approx. (only 25% generated in Ireland) and employs 175 people located on four sites, Dublin Ireland (120), Manchester UK (35), London UK (5) and Boston USA (15). The company also has 10+ distributors/agents in different locations throughout the world. Three different product areas are addressed and these are as follows:-

1. A **software/**systems integration business activity which delivers complete IT solutions to companies in manufacturing and distribution. These solutions include Mentec Limited's and other vendor's packages as well as customised software and services ( projects range in cost between 125kECU -175kECU). The development and support of these software systems is labour intensive and over half of the people in the company are engaged in this activity. This resource must reside close to the customer and hence almost all the customer base for this area in Ireland (6mECU) and UK (6mECU). The company is considered to have a strong position with a significant market share in Ireland but is a small player in the UK.

2. A range of Single Board Computer boards (SBC's), **specialist hardware** products (mainly DEC compatible) are designed manufactured in Ireland and marketed by Mentec to large international companies throughout the world who incorporate them into their products. These products are easily transportable and international customers are supported through a network of specialist distributors after an initial "technical sell" by Mentec. Turnover in this area is approximately 9mECU per year, all generated outside Ireland. The company is well placed in this niche market with its main competitor (DEC) withdrawing from this market. This **FUSE** Application Experiment applies to the SBC business of Mentec.

3. Mentec has recently diversified into the emerging **Desktop Videoconferencing** market by investing early in the development of some products in this area. This market is perceived to be one of high growth. Sales are running at a rate of approximately 2.5mECU per annum (the majority in the US). As videoconferencing is moving from a professional marketplace into a cost sensitive consumer marketplace Mentec must in future implement elements of its videoconferencing products in ASIC to maintain competitiveness.

## 4. Company Markets and competitive position at the start of the AE

In 1991 as demand for higher performance continued. The company set out to implement a PDP11 architecture using bit slice technology (from TI) and a micro-programmed system, the M11 was introduced in 1993. It is now necessary to use ASIC technology to deliver the performance demanded by customers. No competitor has introduced ASIC technology so far although we believe some American competitors will be doing so in the near future**,** (see marketing Table). The time to market for this product is extremely important as a high performance non-ASIC based competitors product will be available during the life of this Application Experiment, impacting on Mentec Limited's market.

**Table 1** gives an overview of the previous five years sales figures and projections for the next 3 years

5 Years Actual
3 Years Projected

| | Actual | | | | | Projected | | |
|---|---|---|---|---|---|---|---|---|
| | 92 | 93 | 94 | 95 | 96 | 97 | 98 | 99 |
| M100 | 3.9 | 5.2 | 2.92 | 1.95 | 1.62 | 1.30* | 0.97 | - |
| M11 | - | 0.35 | 2.6 | 3.9 | 6.18 | 7.15* | 6.5 | 4.55 |
| M1 | | | | | | - | 1.95* | 5.2 |
| Total | 3.9 | 5.55 | 5.52 | 5.85 | 7.72 | 8.45 | 9.42 | 9.7 |

**TABLE 1 Sales Figures/ Projections in ECU's (Millions).**

End of Financial Year (June)

*1. Orders on hand for 80% of these figures already
*2. Initial commitment for 0.75m subject to performance (50% increase over current System)

The key issue for Mentec Limited's customers is performance and currently, Mentec Limited's product is matching the best performance available. **Table 2** indicates the market position of the main competitors. In order to hold and grow our market share we must deliver a higher performance product ahead of our active competitors.

| **Competitor** | **Status** | **Technology/ Production** | **Estimated Market Share Worldwide** |
|---|---|---|---|
| DEC (US) | No longer competitive in this Niche<br>Withdrawing from Market. | J11 Based 11/93<br>No future enhancements | 25% Reducing |
| German Competitor | Lower Performance<br>(Loosing Market share) | J11 Based 11/93 Type | 15%Reducing |
| US Competitor #1 | Similar Performance to M11 | Bit slice based processor | 15% Growing |
| US Competitor #2 | Currently J11 Based<br>Developing high performance product | J11 Going to ASIC | 5% Growing |
| MENTEC (IRL) | M11 Bit Slice going for Higher Performance | Bit Slice going to ASIC | 35% Growing |
| (Others) | | | 5% |

**TABLE 2 Sales Figures/ Market Share relative to Competitors**

Mentec Limited's product costs have always been highly competitive. Against its three main competitors, the M11 pricing compared very favourably. These prices range from being approximately the same as US competitor #2 to being 30-40% cheaper than US competitor #1.

## 5. Product to be improved and its Industrial Sectors

Mentec Limited design and market high performance PDP11 compatible Single Board Computers. The current top of the range product, the M11 is based on standard IC's (from TI and Intel) and some FPGA's. There is no further scope for performance increase with the current design the aim of this proposed project is to deliver 50% plus performance increase over the current figure by employing ASIC technology, as demanded by current customers.

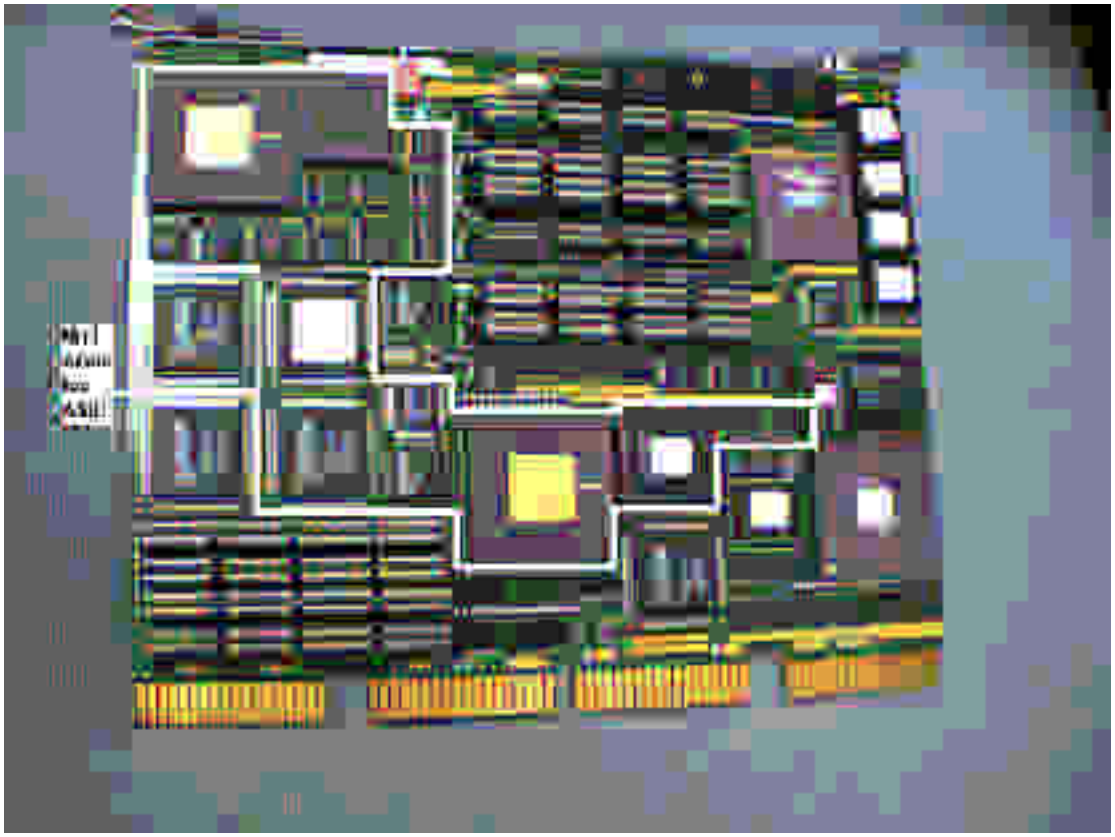
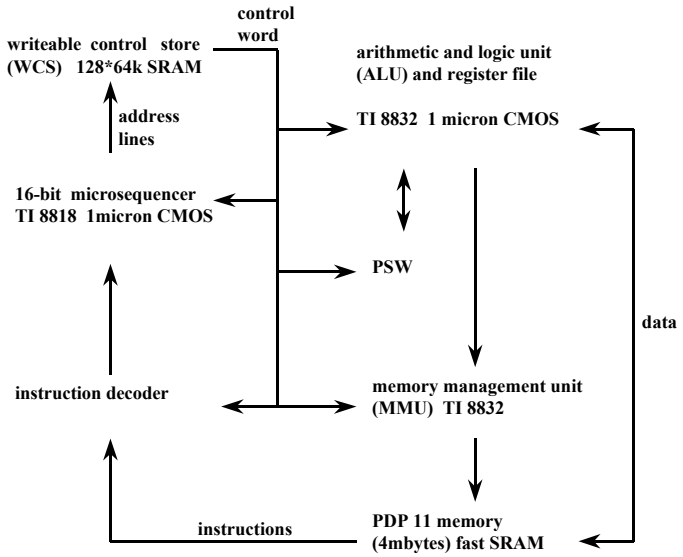


**Figure Shows M11 real estate to be incorporated into ASIC**

This 50% target increase figure means that customers using the ASIC based CPU can expect their system to perform 50% faster assuming that their application software is CPU bound. Because the applications to which the CPU can be put are many, it is difficult to give specific examples. However, in a very simplistic example where CPU performance translates directly to process output performance, a company currently processing 100 items per hour with an M11, could expect an increase to 150 items per hour. This will be Mentec's first ASIC design project.

**Existing Product**

The M11 processor board is essentially a 16-bit machine with a 22-bit memory management unit (MMU), the core of which is implemented using standard parts. The figure below is a simplified overview of the core design. The arithmetic and logic unit (ALU) and the register stack are implemented using a TI-8832, a 40 nsec cycle time, registered ALU is implemented using 1 micron CMOS technology. This unit is driven by a 16-bit microsequencer, a TI-8818 with a microcode wordsize of 128-bits wide, the microcode resident in fast SRAM. The MMU is implemented using a second TI-8832 (only 25% of its functionality is used). Other elements of the core are implemented in GAL's and FPGA's.




Both the microcode and the clock speed of the processor have been optimised and further performance enhancements are not possible using the current core elements. The essential limitation is that a number of timing loops within the core have been pushed to the limit, for example the timing for a register to register operation is currently about 65 nsecs, made up by the internal and on/off chip delays of the TI-8832 etc. In order to achieve this performance increase it is envisaged a figure of 40-45 nsec is required for this particular loop.

Because Mentec Limited's customers require even greater performance to remain competitive, it was required to produce an ASIC based design to overcome the performance limitations as described previously. This allows the applications areas such as Telecom Switches and Financial Networks, which comprise a large proportion of Mentec Limited's product market to remain productive and revenue generating.

## 6. Description of the technical product improvements

Before proposing the ASIC approach, Mentec Limited had considered other ways of increasing the performance of its single board computers. These included more pipelining, more parallelism, emulating with even faster microprocessors and utilising faster FPGA's. However it was found that that the centralising on a single chip of the core elements of Mentec Limited's M11 processor card would deliver the optimum solution.

ASIC Components
By centralising the core elements of the M11 (ALU, Sequencer, MMU and Instruction Decoder) many of the critical path, on/off chip delays were eliminated and internal timings were speeded up. VHDL logic was used to design these core elements and Mentec Limited targeted to a 0.6 micron CMOS technology ASIC device. This fabrication technology was selected as it appeared to guarantee the necessary speed requirements for the design. Mentec Limited estimates a performance increase on its previous processor cards of between 50-60%. The main functional blocks required for the ASIC included,

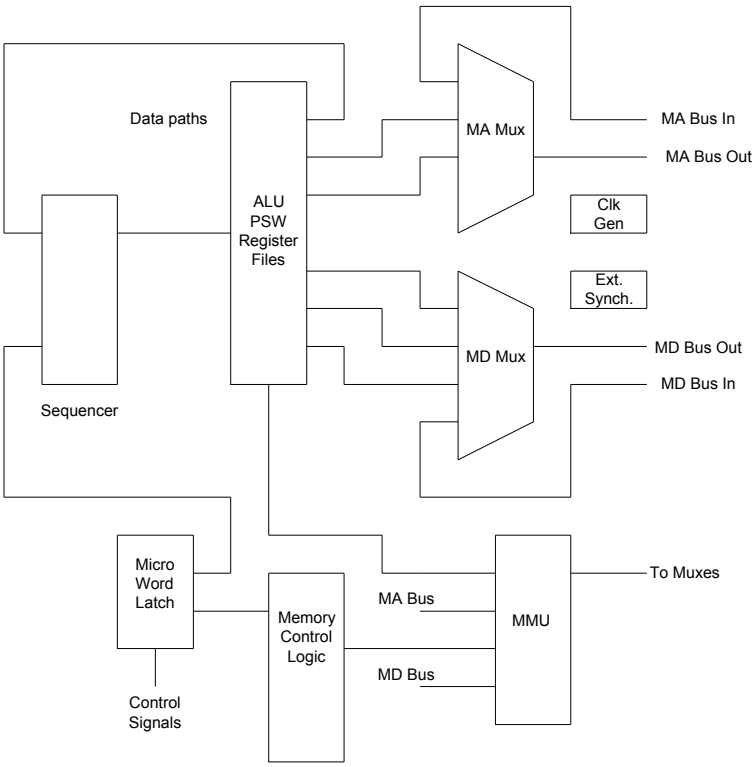
1. A 16 bit ALU function
2. 22 bit memory management units
3. A 16 bit microsequencer and instruction decoder
4. A Processor Status Word (PSW) function with register file

These blocks were implemented within the ASIC core as shown in the following figure. This formed the basis of the design hierarchy. Other smaller blocks within the ASIC provided clock-generation, clock synchronisation and sram latching control for the ASIC's Writeable Control Store. An estimate of the gate count indicated that approximately 50,000 gates were required. The I/O count indicated that a 313 pin BGA package was required.

The complexity of the ASIC in fact was more than the 50K gate estimate. The ASIC contained 80400 gates in a 112 square mm, 0.8 micron CMOS technology. The design is I/O limited so the 313 pin BGA package was required. The design contains only 70% active area. The benefits and improvements were better than targeted, namely the critical timing path was reduced from 65 ns to 36 ns which gave a performance increase of up to 80% in certain applications. The complexity of the resulting PCB was also greatly reduced with a decrease in required components and a decrease in PCB complexity from 12 to 10 layers.

Because this was the first occasion that a BGA package device was used in a Mentec Limited design, some form of BGA pad to PCB connectivity check was required. For this reason, a partial Boundary Scan was included. Full Boundary Scan option was not included, as this would have resulted in a timing degradation.

**Figure 1. ASIC Core Block Diagram.**




**Design Methodology Decision**

One of the central requirements of the ASIC design was to determine the selection of either a multiplex or tri-state design methodology. After consultations with our sub-contractor, a multiplex architecture was selected. A multiplex architecture avoids the issue of bus contention, which can arise within tri-state architectures. Because bus contention internal to a device can be fatal, tri-state architectures require secure VHDL code to guard against this. Given that this was the first occasion that Mentec Limited are to write synthesizable VHDL code the risk was greatly reduced by opting for the multiplex architecture approach.

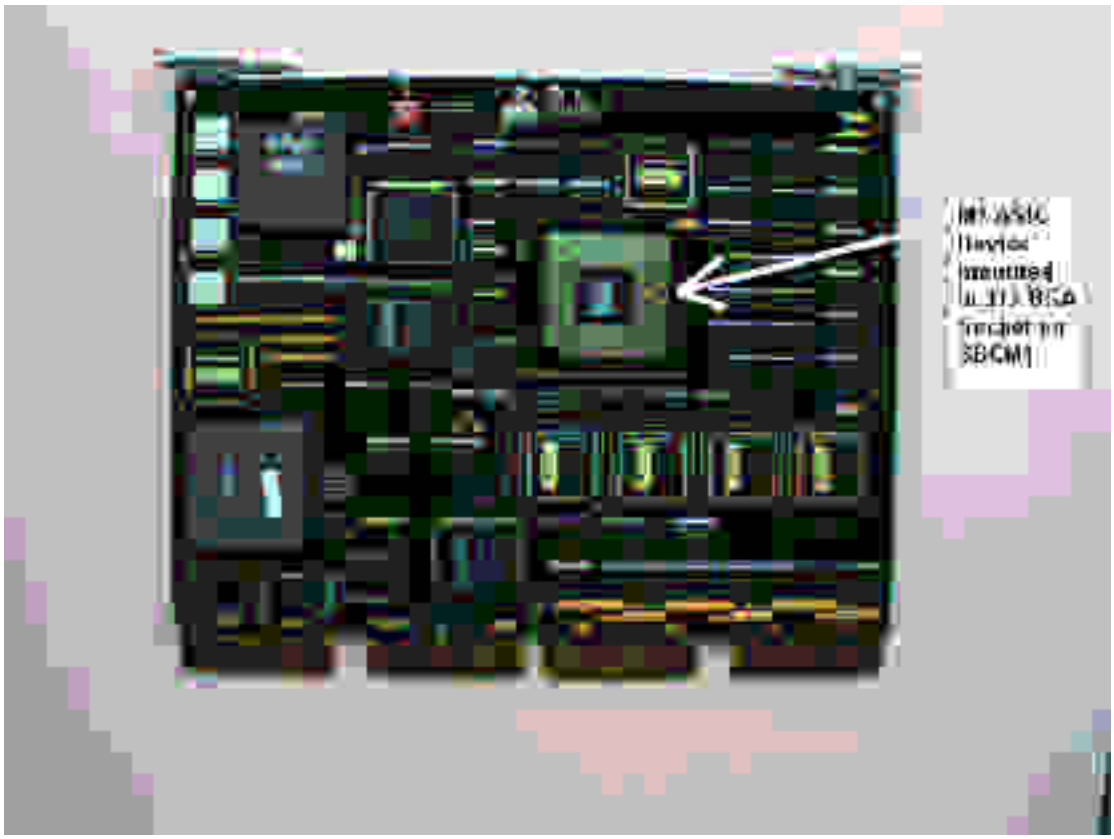
**Benefits and improvements resulting from the ASIC implementation**

The improvements that will accrue to Mentec Limited as a result of this ASIC design are varied. Firstly the use of an ASIC will reduce the cost of manufacturing of the associated Single Board Computer. Many high cost components will no longer be required as a result of the ASIC implementation. The Single Board Computer (SBC) itself is easier and hence cheaper to manufacture as its PCB is now single sided and a reduction in layer count has been achieved. The reduction in the Bill of Materials alone for the ASIC implementation is 30% cheaper. The cost of testing the new SBC has also been reduced. The level of complexity of the board has been reduced with the decrease in component count and this facilitates testing and debugging. There are also benefits in both process throughput and yield with the increasing ease of manufacture that occurs as a result of the ASIC usage. These have a positive impact on production

costs. Although the new customer markets that the ASIC implementation has created have also created an increase in testing for specific applications.

The greatest benefits however occur as a result of the performance of the ASIC device itself. It has greatly improved the speed performance of the SBC in excess of the original projected estimates. This increase in performance should guarantee continued sales growth for the product. The SBC will also be more maintainable and supportable as the ASIC chip replaces many components, which were approaching their end of availability. This in turn will assist Mentec Limited to guarantee supply to its market, of high-speed, high quality PDP11 Single Board Computers.

The main motivation for attempting this project was to provide an increase in product performance. By so doing this would give Mentec Limited a competitive edge in the market place. In achieving these goals the competitive market in which Mentec Limited trades will continue to provide opportunities. Opportunities not only to protect existing business, but to increase its market share by targeting new markets and new sectors for the product which heretofore where unattainable. By developing this ASIC Mentec Limited has produced the fastest ever PDP11 SBC, which can now be marketed competitively throughout the world. This Unique Selling Point will be a major factor in Mentec Limited's continued success.



## 7. Choices and rationale for technologies, tools and methodologies

Before proposing the ASIC design approach, Mentec Limited had investigated alternative ways of speeding up its M11 PDP11 processor.

- More pipelining- Mentec Limited had already achieved as much pipelining as possible within its M11 SBC implementation. Because the PDP11 architecture allows self modifying code the processor may modify the next instruction to be executed. This means the maximum feasible pipeline is very short.
- More parallelism- Mentec Limited considered a design where a separate Memory Management Unit could be implemented. It was estimated that this would yield about a 20% performance gain which, was below what the market was demanding. It would also incur significant manufacturing costs, requiring extra board space on an already densely populated SBC.
- Emulation with a very fast processor- Of the emulation products that Mentec Limited had considered developing, a PDP11 instruction set operating on a DEC alpha platform was a factor of two slower than Mentec Limited's existing product.
- FPGA Technology- The speed performance of an FPGA based architecture was not fast enough. To reach the required performance increase targets, the Arithmetic and Logic Unit (ALU) must perform 16 bit additions in 12nS. This was not currently practical with FPGA technology at that time. However Mentec Limited was advised that these cycle times could be achieved using standard cell CMOS technology.

**Digital ASIC Design**

After considering the above technologies, Mentec Limited decided that an ASIC design was the best way to achieve the required performance increase for its product. Mentec Limited had been designing its products using Mentor Graphics CAD tools for five years. Mentor Graphics are a world reknowned supplier of Computer Automated Design software packages. A top down design methodology was always used by Mentec Limited when working with Mentor Graphics CAD software. The M11 SBC had been fully simulated using Mentor Graphics' Quicksim II product. The ASIC design was fully implemented in VHDL. Autologic II synthesis tools were used to synthesise this VHDL. This synthesised code was then targeted to a 0.6 micron CMOS technology. The use of this logic synthesis will ensure that the cost of porting the design to future finer geometries in later years will be minimised.

It was anticipated that a volume of approximately 1000 ASIC parts would be required over the entire sales life of the product. Such volumes impacted on the choice of available Technology to be used. Having identified the various project phases required for this Application Experiment the economic factors for such a project were considered. The costs for foundry and design assistance were obtained. These costs are as shown below.

Planned Foundry Costs.

| *Description* | *Price ECU* |
|---|---|
| *Prototyping of ASIC* | 7419 |
| *Place & Route Service* | 22258 |
| *Production of Prototypes* | 44516 |
| *Tooling Costs* | 21774 |
| *Total* | 95967 |

A detailed cost proposal was studied by Mentec Limited and its sub-contractors. It was agreed that the costs were in line with industry norms and cost effective for this development project. These decisions were justified as the performance increase required were achieved while also the costs associated with the resulting product were reduced.

## 8. Expertise and experience in Microelectronics of the company and staff on the project

Mentec Limited had experience in top-down design flow methodologies and were very familiar with the Mentor Graphics CAD tool environment. Having designed the M11 board, Mentec had obtained a high knowledge of FPGA and CPLD technologies and the synthesis tools required to target towards such devices. Mentec Limited also had extensive experience in VHDL design environments. Mentec were also fully committed to simulation of designs where possible. Mentec had no ASIC design experience and this was the company's first venture into the world of ASIC design. To this end, Mentec required help in a number of ways. By selecting an experienced ASIC sub-contractor as design consultants, Mentec Limited were provided with valuable design guidance and training during the project design phase and later with the tasks of layout, floor planning and routing of the ASIC. Working with the subcontractors provided the Mentec Limited design team with invaluable knowledge about ASIC development flows and toolsets.

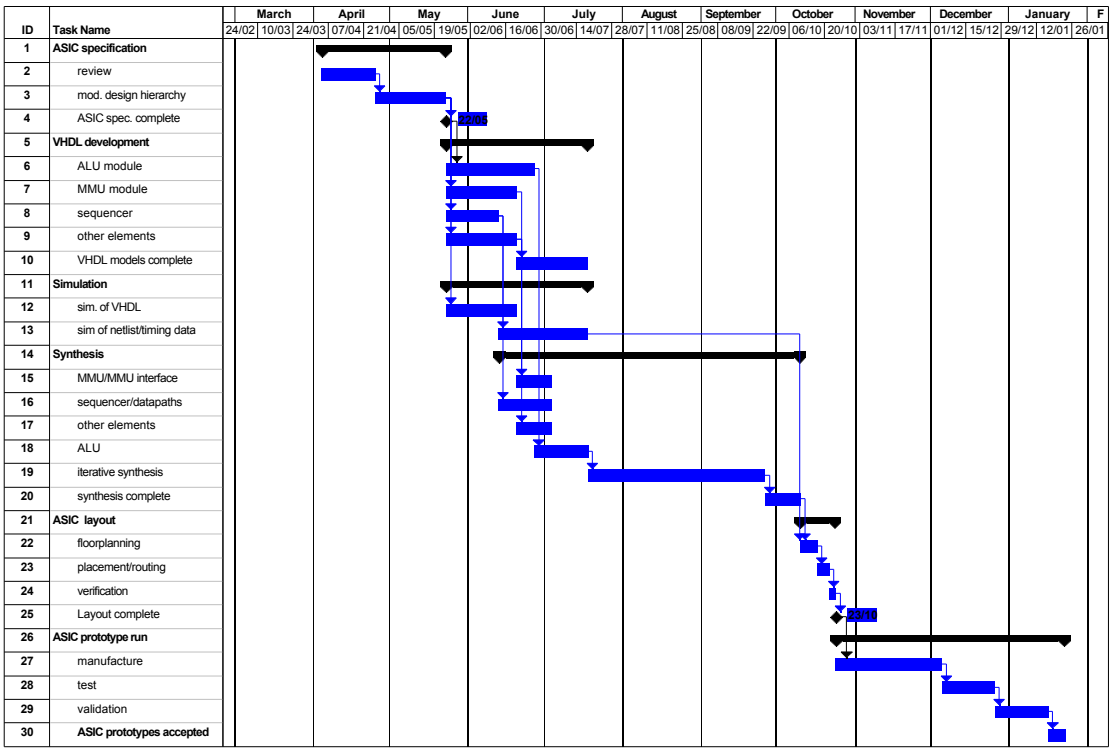
It was actively designed into the project plan that Mentec Limited's design personnel and the sub-contractor personnel should work closely together. In that way Mentec Limited gained the knowledge and experience of the techniques and tools required for the implementation of ASICs. This allows further ASIC projects to be undertaken by Mentec to improve the company's competitive position with its other product lines in the future.

Mentec Limited envisaged three areas where its design engineers needed to learn. Firstly it needed to acquire the know how to get high speeds out of digital CMOS. The company already knew how to get high speeds out of standard components on printed circuit boards. This knowledge was particularly required in the logic synthesis tasks. Secondly, Mentec Limited's design team needed to learn about IC layout. Mentec Limited learned these particular skills by working closely with the ASIC manufacturer. Finally, Mentec Limited needed to learn about the total costs of "owning" an IC. These included issues such as foundry management, test development, quality and reliability.

This ASIC acts as the CPU engine for the M1 SBC. As with its previous SBC designs the PCB for the M1 board will be manufactured by Sub-contractors. The same PCB manufactures that produced Mentec's M11 PCB will produce the M1 PCB.

## 9. Work plan and rationale

In this particular Application Experiment, project completion times were extremely important. This is because there was a demand for a higher performance product within the marketplace and Mentec was committed to filling that need before any competitors could do so. In this regard, Mentec could bear the overrun in costs in order to have as soon as possible a working ASIC. Due to the issues outlined in the following section, an extra effort was required to meet the project time-scales. The engineers allocated to the project work more than full time and this extra project effort incurred a cost of 70KECU.




The complexity of the final ASIC circuitry was also greater than originally estimated. The completed ASIC contained 80400 gates as opposed to the estimated 50,000. However this had no impact on the ASIC size and cost, as the design had always been I/O bounded requiring a 313 pin device. The original workplan for the project is

included below.

The key review milestones were:

- **Month 4** – Completion of VHDL models
- **Month 8** – Completion of simulation and layout of ASIC
- **Month 11** – Testing of prototypes complete

The Main activities were :

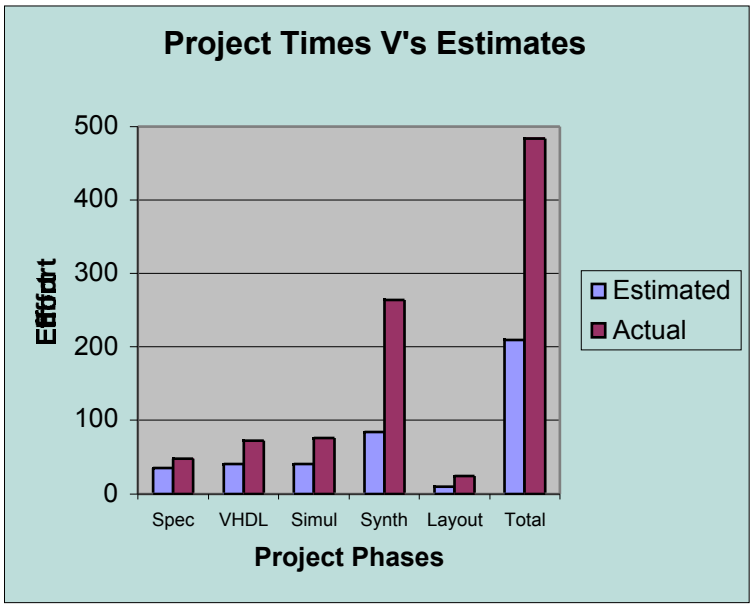
1. **Specification** To determine the architectural requirements of the ASIC
2. **VHDL Design** To produce optimised VHDL for ASIC implementation.
3. **Synthesis** To optimise design for speed and testability
4. **Simulation** To simulate for gate level and VHDL implementations
5. **ASIC Layout** To implement floorplan, place and route, test vectors.
6. **Prototype Run** To gain experience in foundry management.

The main Project Milestones are summarised below.

- ASIC specification completed
- Pre-Simulation VHDL modules completed
- Pre-Synthesis Simulation complete
- Synthesis completed
- ASIC Layout complete
- Acceptance of prototypes

**ASIC Design Phases**

The following Graph illustrates the original project estimates versus the actual effort:




The following Table illustrates the original project estimates versus the actual targets achieved. It also describes the "Estimated" subcontractor involvement against the "Actual" subcontractor involvement. Following on from this is an explanation for the extra effort required for completing the tasks described.

***Project Times V's Estimates***

| Task Name | Estimated | Actual | Sub Est | Sub Act | Note |
|---|---|---|---|---|---|
| *Specification* | 35 | 48 | 5 | 2 | 1 |
| *VHDL Development* | 40 | 72 | 2 | 2 | 2 |
| *Simulation* | 40 | 76 | 5 | 2 | 3 |
| *Synthesis* | 84 | 264 | 5 | 1 | 4 |
| *Layout* | 10 | 24 | 3 | 3 | 5 |
| **Totals** | 209 | 484 | 20 | 10 | |

**Split of Effort For Subcontractors**

In the original estimate, it was foreseen that the subcontractors would have a specific role to play in lending expertise to the Application Experiment. This turned out to be the case however, the amount of design assistance required was overestimated particularly with regard to SSD. During most phases, initial input was required and then once the phase was "up and running", Mentec Limited was able to proceed unassisted. Mentec Limited had a "consultancy on demand" arrangement with SSD which are explained in Section 10, Sub Contractor information.

**Note 1**

**Specification**
This phase determined the architectural requirements of the ASIC being designed. One of the important decisions from this phase was the choice of a Multiplex or Tri-state architecture.

Two issues needed to be resolved during the specification phase. Firstly the choice of a Multiplex architecture for the device. The second issue, which necessitated the extra time commitment, was the decision to move from a 0.6 micron process to a 0.85 micron process. The reasons for this were two-fold. Firstly 0.6 micron silicon requires a 3.3V core. This would mean adding 3.3V regulatory circuitry to the SBC. Also, an dmore importantly the utilisation on this 0.6 process was less than 50%. On advice from both sub-contractors, it was decided that moving to a 0.85 micron process would be more appropiate. This process utilises 5V technology throughout and Mentec Limited was assured that for the application it was designing no performance degradation would occur. The extra consideration for these changes accounted for the project phase time that occurred.

**Note 2**

**VHDL Design**
Having selected the elements that were to be implemented in the ASIC and having determined the Architecture of the ASIC, Mentec Limited produced optimised VHDL code for the ASIC implementation. The design of synthesisable VHDL code was a new experience for Mentec Limited and one in which training was provided. The design entry tool was Design Architect from Mentor Graphics.

Mentec Limited had experience in writing VHDL code for CPLD and FPGA logic. However writing synthesizable VHDL code was a new experience. Previously Mentec Limited had combined combinational and sequential logic within VHDL code targeted to I/O limited package types. However in this case for the ASIC design it was required to separate combinational and sequential logic sections in order to push combinational logic speeds

The estimated effort for this phase as submitted in the First User Submission was 30 person days. The actual effort was 72 person days. The effort was under estimated

primarily due to the complexity of the models and the extra effort required for combinational and sequential logic separation and generation.

**Note 3**

**Simulation**
Mentec Limited used the Mentor Graphics tool QVPRO for the simulation exercises. QVPRO provides a combination of gate level simulation (QUICKSIM II) and a VHDL simulator QVSIM. As QVSIM was a new tool to Mentec Limited. Training was provided for its use by Mentor Graphics.

Previous Mentec Limited design projects have been simulated using Mentor Graphics Quicksim II tool. For this project a new system was utilised. The QVPRO tool from Mentor Graphics was used. This tool acts like a back-plane to provide simulation linkage between hardware models, (Quicksim II) and VHDL models (QVSIM). This allowed the core elements written in VHDL to be included as required within the overall simulation. Individual VHDL core elements were added one at a time and then in logical groups until the entire set of models was validated.

The original estimate for simulation as submitted in the First User Submission, grouped together the simulation required for VHDL and synthesis into one category. Estimating 40 days in total. However the VHDL simulation phase it self took 76 man days to complete.

**Note 4**

**Synthesis**
In this phase the design was optimised for speed and testability. Autologic II from Mentor Graphics was used for this task. A second tool called DFT advisor was used to provide scan path insertion for test purposes. The ASIC synthesis was an iterative process, it continues throughout a large section of the project process.

This was by far the most complex section of the project and the phase that was most under-estimated in the initial project plan. It was estimated that the synthesis phase including iterative simulation and training would take 84 man days. In fact it took 264 man days. The reasons for this were two-fold. Initially synthesis was being performed within each block or leaf of the synthesis tree. However during one of the training sessions for synthesis it transpired that inter-block relationships were not being correctly accounted for. When this was realised much of the work done to that point had to be re-done. However the growing familiarity with the Software Tools and task in hand meant that it was quickly recovered from.

The second obvious delay was the discovery of a library error within software supplied by the ASIC vendor. This meant that certain back-annotations were not being effectively carried out when user changes were made. Again once corrected libraries had been received this set back was overcome. By this time however the design team were very familiar with what was required and the stage was completed effectively.

## Note 5

**ASIC Layout**

The initial skills in this phase concerned the floor planning of the device itself. Consultation with the ASIC Vendor and Mentec Limited's sub-contractors was essential during this phase. Mentec Limited identified various logical blocks which should reside in close proximity on the silicon for speed reasons. In parallel with this Mentec Limited worked with Mentor Graphics to produce Automatic Test Program Generation vectors (ATPG) for use by the ASIC manufacturer for verifying the place and route process.

Having verified the functional and timing elements of the ASIC the next stage was to design the layout and floor plan for the device itself. The ASIC is being implemented within a 313 pin plastic BGA device. In consultation with our ASIC sub-contractors, the design team outlined the proposed floor-plan. Logical blocks were placed together. The pin out was defined. Pin placement was implemented so as to logically group related I/O's together. For example an I/O bus that would interface to SRAM was positioned so that it would be physically close to the SRAM on the completed M1 card.

The power requirements for the device were detailed. The ASIC is heavily I/O orientated so extra VCC/GND pins were placed to meet the necessary power consumption requirements. The drive capability of the various I/O's was also detailed. This process was performed using the Mentor Graphics tool, Boardstation 500 for physical board layout and ATMEL's ES2 packaging tool was used for I/O pin-out, power consumption etc.

Once the layout was completed it was sent to ATMEL for place and route verification. ATMEL's tools verify the layout and calculate the net capacitance (delay) for each net. This is used to generate a Standard Delay Format (SDF) file. This SDF file was returned to Mentec Limited and used to re-simulate the design with real delays within the netlist. The simulation is carried out for minimum and maximum delays. These delays include transistor level delays and net connection delays.

The initial estimate for this phase as submitted within the First User Submission was for 10 days. The actual layout phase took 24 man-days to complete. The disparity is accounted for by the extra time required in using the ES2 packaging tool's from ATMEL

The total planned effort for the project was 166 person days. The actual project effort took 484 person days. The extra effort put in meant that the calendar finish for the project was completed in 12 months as originally estimated.

# 10. Subcontractor information

Mentec have no ASIC design experience and this will be the company's first venture into the world of ASIC design. To this end Mentec will contract Silicon Systems Design (SSD) to help in specific ways where Mentec Limited is lacking in the particular knowledge areas required for this project. SSD are an ASIC design house and have in-depth knowledge of ASIC design. They provided Mentec with valuable design guidance and training during the project design phase. They provided further consultancy and help with the task layout, floor planning, routing of the ASIC. Working with SSD provided the Mentec design team with invaluable knowledge about ASIC development flows and toolsets. Mentec planed a close working relationship with SSD as they were situated about fifteen kilometres apart.

Given the close proximity of SSD to Mentec, the relationship was not incorporated within a formal contract, instead it was a "consultation on demand" arrangement. This arrangement worked well in this particular Application Experiment. The risks associated with this approach could have involved issues, such as the unavailability of personnel for consultation at crucial project times. However, given the long-standing relationship of both companies, it was perceived as a small risk. In the end it was a justifiable one as no such issues arose during the Application Experiment.

**Silicon Systems Design Ltd. –Profile**

**Company size**

120 people.

**Company business description**

Full custom IC design centre

**Companies' markets**

Telecoms, EDP/Computer, Consumer Audio, Automotive

**Expertise and experience of the company**

SSD have the capability for design of full custom digital, analog, and mixed signal devices. 80 Design engineers are currently employed each with access to full layout facilities.

**Description of personnel and Rationale for choosing SSD**

80 Design Engineers, 20 Sales staff, 20 Administration staff. SSD's design centre HQ is in Dublin Ireland. They also have additional design centres in San Jose and Cork. They provide full customIC design and support for Digital, Analog, DSP and RISC technologies. Their experience expertise and location made them an excellent choice as consultants on this Application Experiment.

Mentec Limited chose ATMEL/ES2 as its ASIC manufacturer. ATMEL's ability to deal with small projects, (Mentec's volume requirements were low) the time scales they offered, costs and flexibility were all advantages in choosing them as a sub-contractor. Mentec Limited agreed a contract for the supply of ASIC chips with ATMEL and in that way the risk of manufacture was shared. The cost of unpredictability was factored into the contract with a higher unit price agreed for risk samples. The contract that was made with ATMEL incorporated sign-off procedures, non-performance penalty procedures and a purchase order details.

**ATMEL/ES2 Ltd. –Profile**

**Company size**

3000 people

**Company business description**

Design and Manufacture of IC's

**Relevant expertise and experience of the company**

ATMEL manufactures a broad-line of high-performance non-volatile memory ICs, microcontrollers and logic devices. The highly differentiated nature of ATMEL's product lines results in greater profit margins and more secure customer relations than commodity semiconductor manufacturers. The company's products are used in telecommunications, computer and consumer automotive systems. The company's non-volatile memory products consist primarily of EPROMs, EEPROMs (parallel and serial- interface) and Flash memory devices, and its logic products consist of programmable logic devices (EPLDs and FPGAs), application specific integrated circuits and microcontrollers. Headquartered in San Jose, California, ATMEL has manufacturing facilities in Colorado Springs, Colorado and Rousset, France, where it fabricates silicon wafers using its proprietary CMOS technologies, and manufactures circuits having feature sizes as small as 0.35 microns

**Description of personnel involved**

The majority of the 3000 employees are invovled in both production and design engineering. The balance is made up of administration and sales.

**Rationale for choosing / evaluation of this subcontractor**

ATMEL's earnings and revenue growth rates exceed that of the industry, reflecting the company's strong new product acceptance. In the most recent second quarter, revenue continued to be driven by expanding international demand for ATMEL's products in the telecommunications and consumer markets.ATMEL's assorted product offerings and extensive list of customers dramatically reduce the risk of individual customer or product line brinkmanship.

## 11. Barriers perceived by the company in the first use of the AE technology

This Application Experiment was Mentec Limited's first ever ASIC design. Although Mentec Limited has extensive previous design experience, this project still produced many challenges. Mentec Limited as a company has a philosophy of understanding that technical innovation is necessary to improve products and competitiveness. There were no cultural or inertia barriers to be overcome in relation to this project. Mentec Limited has always understood the need for enthusiastically pursuing new technology in order to remain competitive. Mentec Limited also has extensive experience in running its own design projects and all the work and effort that is associated with those projects. Therefore, it was technical challenges that were the main perceived barriers for Mentec Limited to overcome, namely it was its lack of experience in the areas specific to ASIC design.

These areas would include,

- Writing and generation of synthesizable VHDL code
- Synthesis of VHDL code for performance and testability
- The Layout of an IC
- The Mastering of new CAD tools associated with the above items

**Writing Synthesizable VHDL**

Mentec Limited has previous experience in writing VHDL code targeted for CPLD and FPGA devices. However writing synthesizable VHDL would present a different challenge. VHDL was designed as a simulation language; synthesizers make an interpretation of the VHDL code based on the mapping of constructs onto hardware. As a result of this, the coding approach must use VHDL constructs that have available hardware equivalents.

**Synthesis of VHDL**

For the synthesis phase of the project Mentor Graphics' Autologic II would be used. When all the synthesis for every stage is completed, (ASIC Core), a netlist will need to be generated. This netlist will be used to simulate the design. Errors that arise will need to be identified and removed by re-synthesizing the relevant sections and re-simulating. This iterative process will need to continue until all constraints are met.

**The Layout of an IC**

The ASIC is being implemented within a 313 pin plastic BGA device. The design team need to outline the proposed floorplan. Logical blocks will need to be placed together. The pin out for the device will have to be defined.

**Mastering of new CAD tools**

Several new CAD tools will be used by Mentec Limited's engineers to achieve the various tasks that were outlined above. By successfully mastering these tools many of the knowledge barriers will be overcome.

## 12. Steps taken to overcome the barriers and arrive at an improved product

In relation to the four knowledge barriers referred to in the previous section, Mentec Limited overcame these perceived barriers by the careful selection of 3rd party sub-contractors who can deliver the particular training expertise required. This process of knowledge transfer will allow Mentec Limited to meet the future technological challenges in ASIC design technology as they arise. With particular reference to the points raised in the previous section they are explained in detail below.

**Writing Synthesizable Code**

The VHDL blocks required were written using Mentor Graphics QuickVHDL package. The hierarchical nature of the design meant that a tree structure was to be used. The Mentor design package allows sub-levels of the VHDL design hierarchy to be combined in higher level VHDL blocks and so on up to a top level. Mentec Limited received instruction in the management of this type of VHDL "tree" by the Mentor Graphics training group. When some of the VHDL blocks had been written a consultant from Mentor Graphics examined them. These blocks were synthesized as a test. It was found that the performance in synthesis was below expectations. On advise from Mentor Graphics, the VHDL blocks were re-written, this time separating *Combinational Logic* from *Sequential Logic*. Within ASIC VHDL design environments this approach is recommended. This method provides a higher level of synthesis performance during the latter synthesis stages. Mentec Limited re-tested the modified VHDL blocks and found a large improvement in the synthesis results. This combinational/sequential VHDL approach was therefore adopted throughout the design hierarchy.

The knowledge transfer during this VHDL phase worked very well. Mentor Graphics training assistance being of particular importance.

**Synthesis of VHDL**

Autologic II was the tool that Mentec Limited engineers were trained on. Mentor Graphics consultants provided the training on these tools as well as providing very helpful guidance on general synthesis approached and methodologies. This software provided details on the longest slowest path through any block of synthesized code. Reducing these path delays forms part of the iterative process of the synthesis stage. VHDL was modified or re-written as required to assist in reducing path delays. This process continued up through the various levels of the hierarchy until the top level (known as ASIC Core on the M1 project) was reached.

Testability was designed in from the lowest level using a tool called DFTAdviser from Mentor Graphics. This tool adds the necessary testability onto the logic during the synthesis process. DFTAdviser is called during the execution of the synthesis script. It in turn calls a separate script file, which contains the test parameters for the block under synthesis. Therefore any additional test logic is added at this stage and subsequent path delays include this test logic.

During one of the training sessions that were conducted by Mentor Graphics it emerged that inter-block relationships were not being correctly accounted for as the synthesis progressed up through the hierarchy tree. This meant that the majority of work done to that point had to be re-done. However once the error had been realised the growing familiarity with the software tools meant that this set back was quickly overcome.

The second and more damaging problem that arose was one beyond Mentec Limited's immediate control. An error was discovered in one of the libraries that had been supplied by the ASIC vendor. This meant that certain back annotations where not being carried out when user changes were being made. Mentec Limited engineers discovered this discrepancy when certain synthesis results were at variance with those expected. The debugging of this problem and the subsequent issue of the corrected libraries lost Mentec Limited time. However once the ammended libraries where received this set back was overcome. The design team, were by this time very familiar with the software tools, the synthesis process and the task in hand. This project phase then moved quickly to completion. The synthesis phase was by the far the most complex individual section of the project. This was Mentec Limited's first synthesis experience. There was a sharp learning curve required for the engineering team and the assistance provided by Mentor Graphics was extremely useful. It was also the most underestimated phase in terms of effort/person days.

**The Layout of an IC**

In consultation with our ASIC sub-contractors, the design team outlined the proposed floorplan. Logical blocks were placed together. The pin out was defined. Pin placement was implemented so as to logically group related I/O's together. For example an I/O bus that would interface to SRAM was positioned so that it would be physically close to the SRAM on the completed SBC card. The power requirements for the device were detailed. The ASIC is heavily I/O orientated so extra VCC/GND pins needed to be placed to meet the necessary power consumption requirements. The drive capability of the various I/O's was also detailed. This process was performed using the Mentor Graphics tool, Boardstation 500 for physical board layout. ATMEL's ES2 packaging tool was used for I/O pinout, power consumption etc.

Once the layout was completed it was sent to ATMEL for place and route verification. ATMEL's tools verified the layout and calculated the net capacitance (delay) for each net. This was used to generate a Standard Delay Format (SDF) file. This SDF file was returned to Mentec Limited and used to re-simulate the design with real delays within the netlist. The simulation is carried out for minimum and maximum delays. These delays include transistor level delays and net connection delays.

The knowledge transfer for this phase worked very well. ATMEL provided advice and support throughout the phase with regard to the layout and their ES2 packaging tool. As the ASIC will form part of a Single Board Computer, its pinout was dependent to a large extent on how the related devices on the SBC were to be placed. The SBC's printed circuit board layout was therefore laid out at this time.

**Mastering of new CAD tools**

Several new CAD tools were used by Mentec Limited's engineers to achieve the various tasks. By successfully mastering these tools many of the knowledge barriers were overcome. Mentor Graphics provided training and support on all the new tools that were required on the ASIC Application Experiment. Namely on packages such as, QVPRO, AutologicII, FastScan. and DFTAdvisor. ATMEL provided training on their ES2 packaging tool. Particular emphasis was placed on training for these tools. This was because the training is a key element in guaranteeing the successful achievement of the other knowledge challenges associated with the project.

## 13. Knowledge and experience acquired

One of the key aspects of this Application Experiment was to ensure that skills and knowledge that were previously lacking by Mentec Limited were obtained. One way that this was achieved was by working closely with the two selected sub-contractors.

Selection of Subcontractors

The first sub-contractor chosen by Mentec Limited was Silicon Systems Design Limited (SSD). SSD's design centre HQ is based locally in Dublin, Ireland. SSD have the capability for designing full custom digital, analog and mixed signal devices. 80 design engineers are currently employed each with access to full layout facilities. Their proximity and expertise made them an ideal choice as a subcontractor.

Mentec Limited's second sub-contractor was ATMEL. ATMEL manufacture a wide-range of high performance IC's and logic devices. ATMEL has over 3000 employees in the US and Europe. Its manufacturing facility in Rousset France is where ATMEL will produce Mentec's ASIC. At this facility ATMEL fabricates silicon wafers using its proprietary CMOS technologies and is capable of fabricating circuits with feature sizes as small as 0.35 microns.

As Mentec Limited used some new CAD tools to implement its ASIC design, Mentor Graphics supplied the support and training required on these new tools.

Key Knowledge Transfers through the Project Phases

Specification Phase
During the specification phase SSD played a significant role in guiding Mentec Limited's choice of fabrication technology and design methodology.

VHDL Design Phase
During this phase training assistance from Mentor Graphics led to the splitting of Combinational and Sequential logic blocks for better synthesis results.

Simulation Phase
During the various simulation phases Mentor Graphics provided training on the new simulation tools. ATMEL provided assistance throughout and were the prominent sub-contractor during this phase.

Synthesis Phase
The synthesis phase was the most complex individual section of the project. There was a sharp learning curve required for the engineering team and all three sub-contractors were involved during this phase. Mentor Graphics provided training on their synthesis tools and ATMEL were required to provide support on their library releases.

Layout Phase
During this phase the knowledge transfer worked very well. ATMEL provided advice and support on layout and their ES2 packaging tool.

Prototype Run
During this phase ATMEL provided assistance and expertise to provide Mentec Limited with an understanding of the processes involved in producing an ASIC and Mentec Limited gained experience in foundry management.

Knowledge Base after Application Experiment completion

The engineering design team has learned a great deal as a result of this project. From producing an ASIC specification, learning to use new software tools, producing synthesizable VHDL code that meets performance criteria, managing the synthesis process and producing required timing. Designing testability into an ASIC, obtaining the optimum simulation results, laying out of an ASIC floor plan and power requirements, understanding the prototyping stages. Mentec Limited have also acquired the necessary Tools such as QuickVHDL, Autologic and DFT Adviser, so that it is possible in future to design an ASIC up to the netlist level. All these areas and Tools were covered in great depth and the design team obtained a detailed knowledge both of the individual and collective phases involved. This process of knowledge transfer will allow Mentec Limited to meet future technological challenges in ASIC design technology as they arise.

## 14. Lessons Learned

On completion of this Application Experiment, it is possible to see areas where lessons have been learned.

ASIC design projects require a high level of resources to achieve the required time-scales. The Synthesis Phases was the most demanding stage of the Project. Gaining experience in this synthesis was a key factor in reaching the project goals.

1. A close engineering working relationship is required with the ASIC manufacturer. In this Application Experiment fully understanding how the foundry process works was a key lesson that was learned. Incorporated with that is the effect that implementing layout changes causes and its impact in time-scales.

2. Developing and implementing a company's first ASIC design is a project which tests the design teams abilities and involves team work throughout the enterprise. During this Application Experiment Mentec Limited found that the assistance offered by the selected sub-contractors was still a vital and intrinsic part of the success of the project.

Point 1 above, was common to just about all the phases of the project, was that each phase had been under resourced. It took an increase in effort for Mentec Limited to stay as close as it did in calendar terms to its original timescales.

Of all the project phases, the Synthesis Phase of the project was by far the most demanding and required the most amount of effort. One of the issues, which caused a delay, was a Vendor Library File problem which was beyond Mentec Limited's immediate control. Issues like that can not be foreseen, yet by working with the sub-contractor involved and highlighting the exact problem, the issue was resolved in a reasonable time frame. The synthesis phase is one area where experience counts for a great deal. Gaining this experience was a key element in passing beyond this phase successfully. Synthesis is by its nature an iterative process and a lot of effort can be expended on reaching the optimised requirements. Familiarity with the synthesis tools is essential to efficiently generating results. Mentec Limited in some ways learned from experience and lost some time accordingly. For example sample synthesis was being performed before it was realised that, by splitting combinational from sequential logic the design achieved far better optimisation results. This methodology could be included as a prerequisite on any future ASIC design implementations. Therefore to receive as much training as possible in the synthesis area prior to starting the project would have helped to prevent some of these issues from arising. Perhaps Mentec Limited under estimated the value of this specific technical training, by carrying it out during the project phase. In hindsight synthesis training before the project phase, would have been more beneficial.

The second major lesson learned, point 2 above, concerned the foundry process. A detailed understanding of the various process stages, revisions and task implementations would be a distinct advantage. It is not practically possible for a First User to control the fabrication process of a sub-contractor. Therefore it is important to fully understand the manner in which the sub-contractor works. An example would be in relation to the handling of ECR's and the effect that this will likely have on timescales etc. Engineering Change Recommendations (ECR's) were required when Mentec Limited engineers needed to amend the ATMEL generated Standard Delay Format (SDF) file. These amendments were required when vector tests carried out using the SDF were found. It took between two and three weeks per ECR, allowing for the relay-out of the ASIC. Mentec Limited had not adequately allowed for these issues during the Layout project phase.

In summary again the two main lessons learned were,

1. ASIC design projects require a higher level of engineering resource to achieve the required development timescales.
2. A very close engineering working relationship is required with the ASIC manufacturer.

**Conclusions**

Because of the increase in effort required to finish the project within the 12 months, costs were a lot higher than anticipated. However, Mentec Limited was confident that the demand for this product was in the marketplace and that the return would be immediate once the product was released. With this knowledge, the extra costs could be borne for a short period in order to guarantee and achieve the return. This turned out to be the case with initial orders more than covering the additional costs.

Despite these minor issues, the project was extremely successful. Mentec Limited has achieved a very good return for the effort expended during the project. As a result of this particular Application Experiment Mentec Limited now has the acquired skill set to confidently propose and deliver future ASIC based products. This project has also moved Mentec Limited onto a different level of expertise and as an ASIC capable design company, will hopefully allow the company to embrace future business opportunities, which heretofore were beyond its technical ability.

**Lessons Learned Relating to Sub Contractors**

A successful working relationship with shrewdly chosen sub-contractors also assisted Mentec Limited greatly in the pursuit of this ASIC project. Our close working relationship with SSD proved highly beneficial. (Even though there was no formal contract between Mentec Limited and SSD). Our existing relationship with Mentor Graphics was further enhanced during this project. ATMEL provided us with good ASIC foundry production. Despite one or two issues that arose, the relationship was a beneficial one. When using sub-contractors control for some project aspects invariable passes temporarily outside of the company. Understanding how these periods progress and planning for contingencies that may arise would be one area that Mentec Limited would envisage paying particular close attention to in future.

Overall the great success of the Application Experiment is due to the hard work of the Mentec Limited design team, the close collaboration with the sub-contractors and the specific transfer of knowledge from existing experts in the project field.

This strategic approach is to be highly recommended to potential future Application Experiment participants.

## 15. Resulting product, its industrialisation and internal replication

The result of this Application Experiment is that Mentec Limited has a working ASIC chip, packaged as a 313 pin Ball Grid Array device. This ASIC will act as a dedicated CPU for Mentec Limited's next generation of Single Board Computer product, The M1. This SBC has been developed in parallel with the ASIC device using the standard micro-electronic methodologies previously employed by Mentec Limited on its Single Board Computer products. The M1 SBC has been designed in such a way as to fully utilise the performance and functionality of the ASIC acting at its CPU core.

The initial testing that has been carried out indicates that the Application Experiment has been a great success. The M1 SBC complete with the Application Experiment ASIC is delivering a performance increase above that originally targeted for in the project plan. Initial figures are showing an increase in performance of between 60% and 80% (depending on the application) over that of the product to be improved the M11 SBC. These prototype devices are currently being tested in a range of scenarios including customer specific applications. It is planned that the ASIC will be re-used to produce a lower performance version where slower memory can be used for the product to appeal to an even wider market segment.

With an ASIC design project the key areas for success involve a large and concentrated effort during the design phases. An ASIC chip must be "right first time" and the various design phases act as checks and balances towards this aim.

## 16. Economic impact and improvement in competitive position

The total investment for the Application Experiment is approximately 250KECU. Despite the cost overrun associated with the extra effort required, Mentec Limited had expected to re-coup all development costs within the first year of sales. In fact the orders received to date for the new product already pay back the investment made. There fore the Payback Period is achieved immediately. The availability of such an immediate Payback was why the time factor in this Application Experiment was so important and the extra commitment of resources was justified to keep the project on schedule.

One of the other economic benefits is a reduction in costs from previous Mentec SBC's of approximately 1200 ECU. This has been achieved by replacing many of the high cost components used for implementing the processor architecture with the single ASIC device. The Table below summarises the sales figures associated with M-Series Single Board Computer product lines.

**Table 3** gives an overview of the previous five years sales figures and projections for the next 3 years

5 Years Actual
3 Years Projected

| | Actual | | | | | Projected | | |
|---|---|---|---|---|---|---|---|---|
| | 92 | 93 | 94 | 95 | 96 | 97 | 98 | 99 |
| M100 | 3.9 | 5.2 | 2.92 | 1.95 | 1.62 | 1.30* | 0.97 | - |
| M11 | - | 0.35 | 2.6 | 3.9 | 6.18 | 7.15* | 6.5 | 4.55 |
| M1 | | | | | | - | 1.95* | 5.2 |
| Total | 3.9 | 5.55 | 5.52 | 5.85 | 7.72 | 8.45 | 9.42 | 9.7 |

**TABLE 3 Sales Figures/ Projections in ECU's (Millions).**

End of Financial Year (June)

*1. Orders on hand for 80% of these figures already
*2. Initial commitment for 0.75m Subject to performance (50% increase over current System)

In order to get a view of Mentec Limited's position without development of the M1 ASIC product simply remove the sales figures for the M1. It is possible to do this because these sales only exist because Mentec Limited has a higher performance product than the M100 and the M11 products. Therefore the projected increase in sales for 1998 is 1.8m ECU's (21% of sales for the M-Series product line) and 4.8m ECU's in 1999 (53% of total M-Series sales). From the figures it is possible to see that the Return on Investment (ROI) achieved over the life of the product sales is substantial.

A number of other opportunities have arisen since the development of the ASIC. Mentec Limited is planning the development of a low cost board to replace the M100 and M11 products. This lower performance card using slower memory will provide continuity of supply for customers using previous generation SBC's. The build cost of this board will be lower and hence Mentec Limited should be able to supply these products very competitively.

In conclusion, the development of the M1 ASIC has been a very worthwhile and profitable exercise for Mentec Limited. Within Mentec Limited the Application Experiment has been seen as a great success. The Application Experiment was hard won but very worthwhile. Mentec Limited is now a proficient ASIC capable design house and this was made possible in great part by the knowledge transfer mechanism inherent in the FUSE program approach. With the aid of this FUSE program Mentec Limited was provided with a technological roadmap which enabled the designers to develop from a successful digital design house into a successful ASIC design house.

With the increase in Sales revenue that this Application Experiment helped to achieve, Mentec Limited believes that this FUSE program Application Experiment has contributed greatly to the future economic growth and prosperity of the company. Taking these factors into account, this FUSE program has been a great success.

## 17. Target audience for dissemination throughout Europe

This AE describes the development of a digital ASIC for a computer application. The FU was a reasonable size SME (175 employees) who acquired the necessary expertise during the AE to enable them to produce future designs on their own. They had considerable experience in other areas of micro-electronics before the AE, and extended this knowledge as a result of this AE. The project would be particularly interesting to two types of companies:

a) Companies with existing products based on FPGAs and/or standard ICs willing to replace those with an ASIC. By doing so, they can achieve either an improvement in product performance or a reduction in price. This project provides very interesting information for companies thinking about designing their first digital ASIC.
b) Companies with experience in microelectronics interested on the introduction of new (advanced) technologies in their process to improve their product performance. Especially for those companies willing to acquire knowledge on the new technology to be able to carry out the process themselves without the need of a subcontractor.