Media-accelerated Global Information Carrier

Engineering Specification

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Revision History

The following table is a record of all public releases of this document.

Revision	*Release Date*	*Comments*
1.0	09/18/99	Initial proposal to the audio industry at the 107th AES.
1.1	02/02/00	NAMM 2000.
2.0	01/20/01	NAMM 2001. Revised packet format.
2.1	09/21/01	Complete rewrite. Revised control protocol and application layer. New sample rate modification protocol.
2.2	10/18/01	Changed flag order in word 12. Added more figures and improved descriptions of all algorithms. Simplified the CTS/MIP control flow protocol. Fixed bug in control message numbering. Added section on Endian requirements.
2.3	11/16/01	Added MIDI message encapsulation and Timecode, and a Blob component type. Also, added control packet requirement of at least 12 RX buffers on each port to ensure proper flow control.
2.4	01/22/02	Added copy protection bit. Added reset enumeration from any device on the network. Several minor edits to presentation.
2.5	02/18/02	Renamed A and B ports to Send and Receive respectively. Rewrote chapter 8 to incorporate the Device Class and pre-defined Component address. Added several new figures and tables.
2.6	03/04/02	Added: Identify Neighbor control message, device-specific ports, their mnemonic names, channel counts, router configuration, product & vendor id, super toggle source component, auto control links, and error reporting control message. Updated all relevant packet formats to reflect the same.
2.7	04/17/02	Removed super toggle type. Added three channel number enabled control types. Fixed several typos in chapter 8 and appendix G. Reserved port address 0. Reformatted Ret Comp Info and Ret Dev Info. Added tables described component-specific data format for Ret Comp Info and Set New Value.
2.8	05/07/02	Renamed Send and Receive to OUT and IN respectively. Modified power spec to be compliant with IEEE802.3af. Assigned 0 as an invalid component address.
2.9	02/28/03	Added: network layer for transport, control application layer, flexible media channel bandwidth allocation, default slot formats, device address auto-configuration procedure, address conflict resolution, MaGIC device hierarchical structure, control components linking mechanism based on unified control link tables, improved error reporting.
3.0	05/05/03	Changed frame format: excluded UDP/IP header placeholder,

		added IEEE 802.2 LLC-SNAP frame format. Size is now 222 octets. Payload boundaries are aligned to 32 bit words for better performance. Tables represented in octets. Control Packet payload increased to 32 octets. New fragmentation/reassembly of control messages for robust encapsulation of high-level protocols. Redefined CTS handshaking. Updated list of reserved unit addresses. Provided definition of control routing tables of Media Slot routers. Defined control messages for media routing. Introduced hierarchical Attributes and related control messages. List of required attributes. Advertisement on the network layer.

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Terms and Abbreviations

The following section lists and defines commonly used terms and abbreviations used in this specification:

100baseT	The 100-Megabit Ethernet physical layer.
OUT port	A MaGIC port with a one-to-one wiring with respect to the cable.
A/D	Refers to analog-to-digital conversion, the process by which an analog signal is converted to a digital sample.
ADAT	Alesis Digital Audio Tape. See LightPipe.
ADCCP	Abbreviation for Advanced Data Communications Control Protocol. An ANSI standard, bit-oriented, data-link control protocol.
AES/EBU	Abbreviation for the Audio Engineering Society / European Broadcasting Union. Here refers to the 24-bit, 48 kHz, two channel digital audio standard.
ANSI	American National Standards Institute. The coordinating body for voluntary standards groups within the U.S.
AUTODIN	Acronym for Automatic Digital Network. The United States Department of Defense automatic switching network for telecommunications developed in the 1960s.
Audio Slots	MaGIC supports multiple Sample Rates by providing flexible mapping between samples and channels, called audio slots. For example, slots 1 and 2 are mapped to the first samples of channels 1 and 2 at 48 kHz, and to the first and second samples of channel 1 at 92 kHz.
IN port	A MaGIC port with a signal crossover with respect to the cable.
Bandwidth	The measure of data transmitted per unit of time across a given medium. Common units are bits per second (b/s) or bytes per second (B/s).

Bi-directional	Moving simultaneously in both directions. See Full-duplex.
Bit	The smallest unit of digital data. It has two possible values a logical high or one, or a logical low or zero.
Byte	A commonly used unit of data equal to eight bits.
CRC	see Cyclic Redundancy Check.
CTS	Clear To Send. This bit in the MaGIC packet allows devices to determine the flow of control packets from adjacent devices, based on their individual processing capabilities.
CAT-5	The interconnection cable used for Common Instrument Interface MaGIC physical layer. It is based on the IEEE 802.3 protocol.
Category 5	See CAT-5
Component	A unit of control in a MaGIC device that can issue or interpret a control command.
Control Link	A virtual connection established between two Components on a MaGIC network. It allows a Source Component to control a Target Component of the same type.
Control Message	A message sent by one MaGIC device to another in order to provide configuration or control information.
Cyclic Redundancy Check	A technique that employs an algorithm to compute a value for any arbitrary data. This value is then transmitted with the data allowing the recipient to re-compute and check the value to determine if the transmission was free of errors.
D/A	Refers to digital-to-analog conversion, the process by which digital samples are converted into an analog signal.

Daisy Chain	Network topology in which nodes are linked together such that no node is adjacent to more than two other nodes, and no loops may exist.
Device	See MaGIC device.
Device Address	The network-wide unique unsigned integer address assigned to the device by the STM during enumeration.
Device Class	Label applied to a collection of predefined Components. Devices belonging to the class are guaranteed to have those Components.
Ethernet	See IEEE 802.3.
Enumeration	The process by which the STM assigns a unique unsigned integer Device Address to each device on the network.
Firewire	See IEEE 1394.
Full duplex	The simultaneous exchange of data in both directions across a single connection.
Hot-swap switch	A power load monitor. The switch can apply power to the port when necessary and can disconnect it if a short or a disconnection is detected.
MaGIC Control	The native protocol described in this document that allows MaGIC devices to control parameters on one another.
MaGIC Device	Any device equipped with a MaGIC Link that allows it to exchange bi-directional, fixed-length data and control, at a determined network sample rate.
MaGIC Link	The connection between two adjacent devices on a MaGIC network.
MaGIC Packet	A collection of networking headers, audio, and possibly control information transmitted synchronously across a MaGIC network.

MaGIC Port	The physical point of connection between the medium of transport and the MaGIC device.
Gigabit	An advanced 802.x standard that operates at 1000Mbps.
IEEE 802.3	A bus-based broadcast network with decentralized control operating at 10 or 100 Mbps.
IEEE 1394	A digital multimedia peripheral interface developed by Apple for digitally connecting consumer electronics with personal computers.
Inter-NIC	Network Information Center. The central authority that assigns worldwide unique IP addresses.
Jitter	The phase shifts of digital signals caused by mechanical or electrical imperfections. This deviation can lead towards a lack of synchronization of the signals involved.
Latency	Time delay in signal propagation as measured between the source and the target.
Lightpipe	An eight channel, 24-bit, 48 kHz, low-cost optical digital audio standard developed by Alesis. Also known as ADAT Optical and TossLink.
MAC Address	The worldwide unique Medium Access Control addresses.
MIDI	The Musical Instrument Digital Interface standard.
MIP	Message In Progress. This bit in the MaGIC packet allows adjacent devices to determine the flow of control information between them depending upon their individual processing capabilities.
Network Name	A mnemonic name assigned to a configured MaGIC network for easy identification in user interfaces. This name can be requested by and sent to other devices.
Nibble	A commonly-used unit of digital data equal to four bits.

RJ-45 The connector/port used for the connection based on the IEEE 802.3 Ethernet physical layer.

STM System Timing Master. Every network automatically selects one device to be the STM. This device is responsible for enumerating the other devices on the network and for providing the sample clock.

Sample Rate The number of samples transmitted per second. Measured in Hertz (Hz) or kilohertz (kHz).

Source A Component that can issue a control command.

Star MaGIC network topology in which Daisy Chains are connected together using a Routing Hub.

Target A Component that can receive and interpret a control command.

T/DIF The Tascam Digital Audio Interface. An 8-channel digital audio interface used mainly by in Tascam products.

UDP User Datagram Protocol. The standard Internet connectionless transport protocol used for sending raw IP datagrams.

Uplink MaGIC network topology that employs at least two Switching Hubs allowing several MaGIC Links to be multiplexed onto a single cable of a faster physical layer (such as Gigabit).

1. Introduction

1.1 Motivation

The Media-accelerated Global Information Carrier (MaGIC) is motivated by the following goals:

1. **Enhanced real-time digital sonic fidelity:**

   Despite dramatic advances in technology, real-time, high fidelity digital audio has yet to permeate production and live performance. Increasing demand has motivated little effort to apply modern network technology towards producing affordable, yet superior quality real-time media devices.

   MaGIC uses state-of-the-art technology to provide up to 32 channels of 32-bit bi-directional high-fidelity media with sample rates up to 192 kHz. Data and control can be transported up to 30,000 times faster than MIDI. Added cable features include power for instruments, automatic clocking, and network synchronization.

2. **Interoperability**:

   There is a compelling need for an Open Architecture digital interconnect that allows products from different vendors in different industries to seamlessly communicate. MaGIC provides the ability to create such networks appropriate for use in a wide variety of environments including music instruments, professional audio, live performance, postproduction, and home entertainment.

3. **Complete digital solution**:

   Existing digital systems rely on archaic analog interfaces to connect with other devices. The increasing demand for interconnected devices has resulted in diminished sound quality, caused by repeated analog-to-digital and digital-to-analog conversions. These conversions often lead to prohibitive size and power product requirements and create a situation that begs for a universal end-to-end digital solution.

4. **Simple installation and ease-of-use**:

   Most existing systems are difficult to install, lack flexible reconfiguration capabilities, and do not take advantage of user-friendly hardware and software interfaces. MaGIC provides a single cable solution that is trivial to install, requires virtually no maintenance, and offers a data link layer that supports a simple yet sophisticated protocol, capable of offering a superior user experience.

Several digital interconnection specifications such as AES/EBU, S/PDIF, ADAT (Light Pipe), and IEEE 1394 (Fire Wire) have emerged but none satisfy the unique requirements of live performances, particularly in the areas of clocking, distance synchronization, and jitter/latency management.

The Media-accelerated Global Information Carrier was commissioned to overcome these limitations of point-to-point solutions by providing inexpensive, end-to-end, and real-time digital sonic fidelity.

1.2 Scope of the Document

This document is written for manufacturers, hardware and software developers who wish to develop MaGIC-compliant devices.

It describes the physical, mechanical, and electrical interconnection based on the 100-Megabit Ethernet physical layer. The document also specifies the network timing synchronization mechanism, data transport layer, and the control protocol which are independent of the physical layer.

1.3 Historical Background

Henry Juszkiewicz, Executive Director of the MaGIC project, has supported the idea of a digital audio network for nearly a decade. In addition to launching the preliminary Guitar Innovation Group (GIG) studies, Henry has funded extensive research and development in digital audio connectivity at the University of California at Berkeley Center for New Music and Audio Technologies.

The guiding principle of this research was to apply technology invented for computer network products to media equipment, and develop an interconnect that would be:

- Reliable over long distances, locally repairable, trivial to install, and simple to use.
- Capable of supporting multiple channels of advanced fidelity audio and video.
- Fit for enabling installations to scale beyond the capacity of existing multiple cable solutions and meet the requirements of permanent installations such as live venues and recording studios.
- Able to provide power for digital instruments thereby removing the need for batteries.
- Supportive of intuitive control interfaces.
- Successful in providing extreme simplicity and reliability.

The above stated goals were to be accomplished by augmenting, not diminishing the acoustic, electric, or physical characteristics of existing devices.

MaGIC is the result of these efforts.

1.4 Document Organization

Chapters 1 and 2 provide a general introduction to the goals, concept, and architecture of the MaGIC standard. It includes an overview of the various interfaces and protocols that comprise MaGIC without subjecting the reader to rigorous details.

Chapters 3 and 4 are directed at the hardware and mechanical engineers designing the physical layer of a MaGIC device.

Chapter 5 is primarily of interest to the firmware and software engineers implementing the packet framework and Ethernet compatibility.

Chapter 6, 7, 8, and 9 describe the MaGIC network layer and is aimed at software and firmware engineers implementing enumeration, media, control, and other related protocols.

Chapter 10 describes the MaGIC application layer.

2. Architectural Overview

2.1 Devices

A MaGIC-compliant device is equipped with at least one MaGIC port through which it can exchange real-time, bi-directional, fixed-length data and control information, at a determined network sample rate. Unless specified otherwise, the term “device” is to be understood as referring to a MaGIC-compliant device.

2.2 Network Topology

MaGIC networks can be arranged in the following three topologies:

1. **Daisy Chain:** As shown in the figure below, a Daisy Chain network refers to devices connected together to form a single chain.

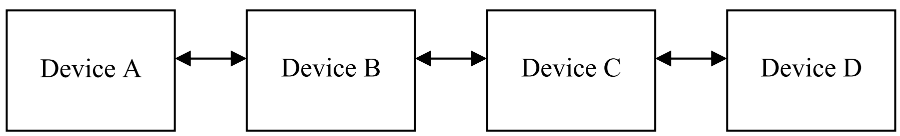

Figure 2-1: Daisy Chain network topology

2. **Star:** As shown in the figure below, a star network is one in which several Daisy Chain networks are connected together using a Routing Hub.

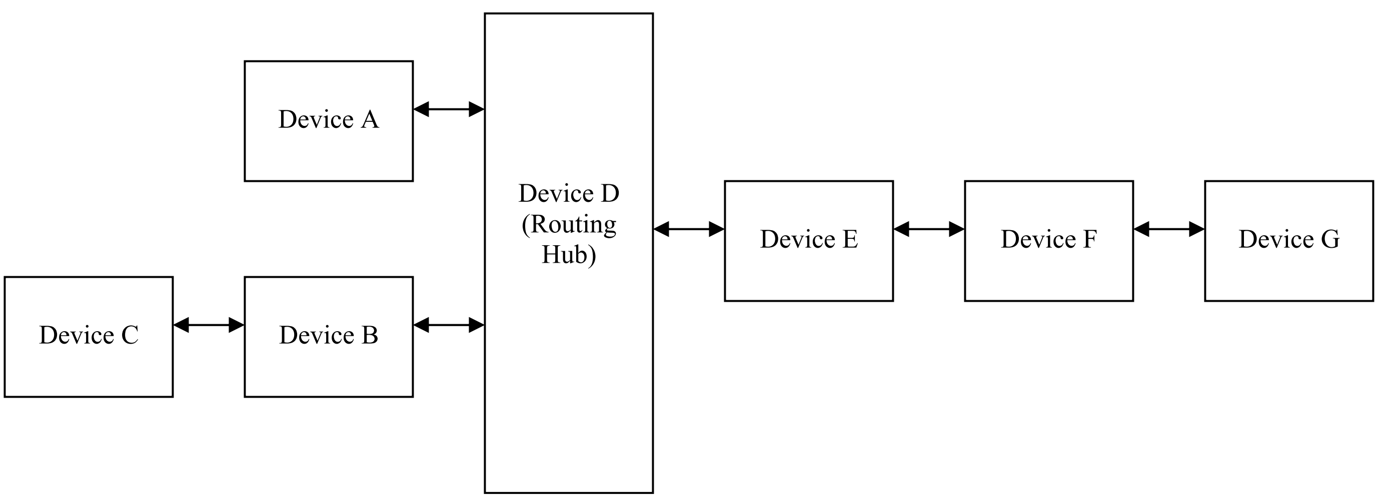

Figure 2-2: Star network topology

3. **Uplink:** As shown in the figure below, an uplink network topology employs at least two routing Hubs that allow data from several MaGIC Links to be multiplexed onto a single cable.

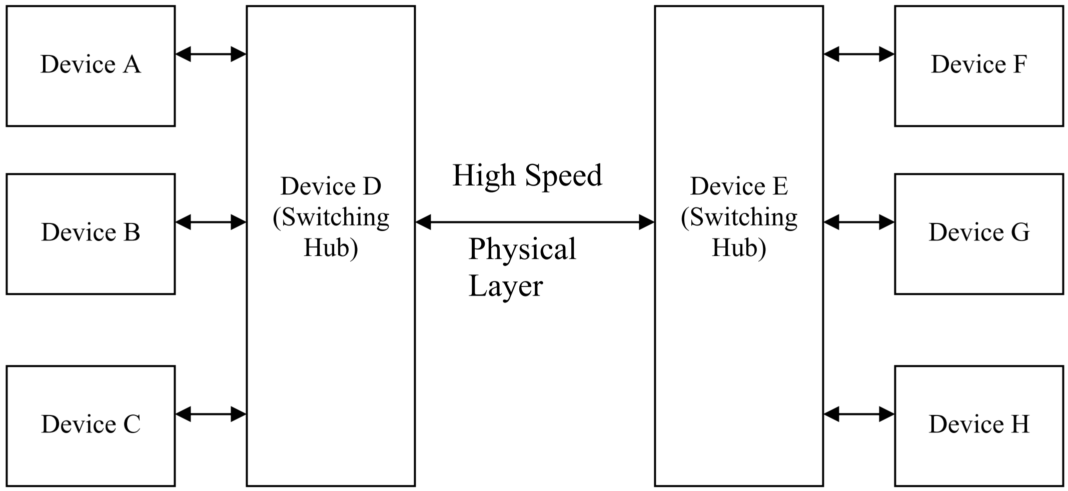

Figure 2-3: Uplink network topology

2.3 Protocol Stack

Not unlike common networking protocols, the MaGIC protocol is stacked into four distinct layers. From the lowest to highest, they are:

1. *Physical Layer*: the mechanical and electrical specifications for the physical network. This layer is compatible with the IEEE 802.3 Fast Ethernet physical layer and the 802.3af Power over Ethernet (PoE) specifications

2. *Data Link Layer*: as defined by the IEEE 802.3 and IEEE 802.2 protocols. It views bits transported by the Physical Layer as defined sequences called frames.

3. *MaGIC Network Layer*: uses frames transported by the Data Link Layer to encapsulate MaGIC-specific information into the payload to enable real-time, bi-directional communication. Media and control are extracted from a received frame, processed on separate paths, and reassembled into the payload of the outgoing frame. Multi-port MaGIC devices route media and control between ports in real-time at this layer.

4. *MaGIC Application Layer*: provides a MaGIC device with media and control data interfaces to user applications by providing transport for communication messages of high-level protocols. As in the network layer, media and control data paths are managed independently.

Each layer is independent of lower layers thereby allowing MaGIC to operate on any available physical transport.

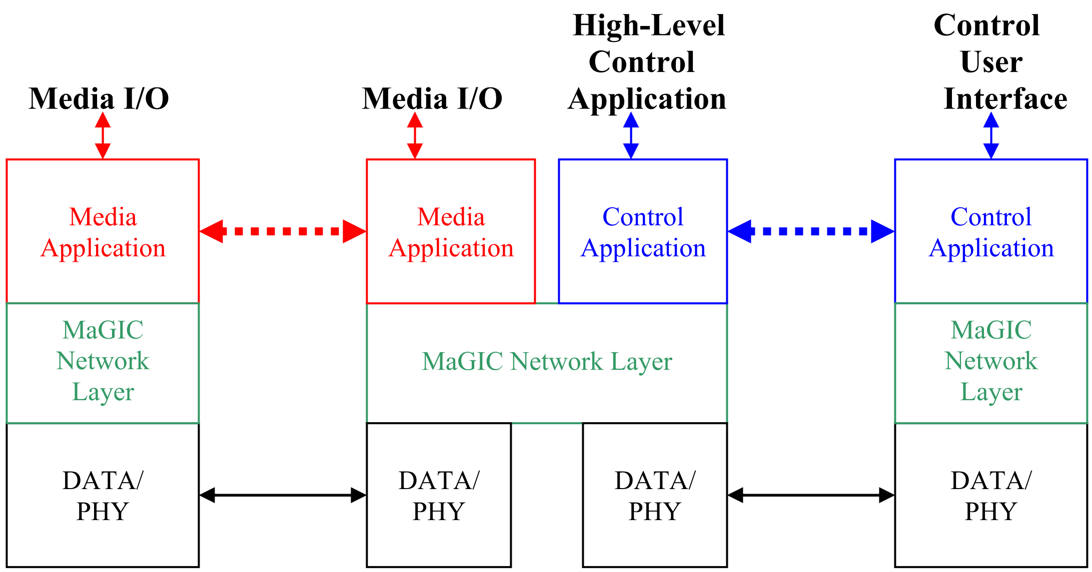

Figure 2-4: Protocol Stack (dashed lines show logical communication links)

2.4 Mechanical Interface

The MaGIC protocol is suitable for a variety of physical interfaces. Examples include: the IEEE 802.3 Ethernet physical layer, the high-speed multi-link Optical Interface, the Ethernet Gigabit-based physical layer, etc.

This specification only describes the MaGIC Link based on the IEEE 802.3 100-Megabit Ethernet physical layer, which uses standard Category 5 (Cat 5) cables, and RJ-45 connectors.

2.5 Electrical Interface

The electrical component of the Ethernet physical layer is based on a 4b/5b data-encoding scheme, scrambled to eliminate RF ‘hot spots’, thereby reducing emissions. This is a well-known data transport with a large installed base.

Four conductors in a Category 5 cable are used for data transport and the remaining four supply at least 300mA at plus 48 volts DC for devices that can operate on limited power in compliance with IEEE 802.3af.

2.6 Data Link Layer

The MaGIC Data Link Layer is based on the IEEE 802.3 Ethernet Data Link Layer. Data is transmitted between devices at a fixed network sample rate in discrete fixed-size frames. Each frame contains a Preamble with Start of Frame, 802.3 MAC header, 802.2 LLC header, SNAP header, a 188 octet payload, and FCS fields which add up to 222 octets.

At the default sample rate of 48 kHz, the useful bandwidth is 72.2 Mbit/sec.

2.7 Network Layer

MaGIC Network layer encapsulates application data into payload fields of MaGIC frames. The payload field has two parts: media and control. As the names suggest, the former is designed for data with low-latency requirements such as audio or video and the latter is for control or other data than may tolerate limited propagation delay.

By regulating channel allocation in the media payload, the MaGIC network layer can transport multiple media streams with varying bandwidth requirements. The protocol itself is agnostic to the transported streams-- compressed or otherwise, provided, the bandwidth requirements do not exceed payload capacity.

The control payload is used for native MaGIC control messages as well as application control, management and information parameters, and even to encapsulate other protocols such as MIDI and X10.

The media and control payload fields are fixed and independent, and therefore bandwidth allocation in one does not affect the other.

2.8 Logical Entities

A MaGIC device is structured around following logical entities:

- Unit
- Components
- Ports
- Media Slot Router

Unit is a logical network access point for MaGIC applications designed to send and receive control messages for basic device operation. Each MaGIC device must contain at least one logical *Unit*.

Components provide access points for control applications. The MaGIC Control Protocol (MCP), a simple messaging system described later in this document, defines inter-component communication messages that allow a Component on a device to communicate with another Component on a different device. User control applications can vary from simple parameters like remote volume control to abstract protocols like TCP/IP. Components are limited to a maximum of 65535.

Ports are of two types: MaGIC ports which are logical representations of physical connections or User Media ports which connect media from user applications into the network layer.

Media Slot Router can route multiple media data streams between applications through the network. It also provides flexible bandwidth allocation for particular media stream requirements.

2.9 MaGIC device structure

As shown in the following diagram, a typical MaGIC device consists of the following:

1. Media Channel Interface (MCI) modules: interfaces to audio or video applications.

2. Application Interface Components (AIC): interfaces to controls from simple power on-off switches to sophisticated graphical user interfaces.

3. Frame Formatter/PHY (FFP) pairs: connections to physical media (MaGIC ports) that extract payloads from inbound frames and assemble data into outbound frames. Each MaGIC device must have at least one FFP.

4. Media Slot Router (MSR): forwards media payload slots from an assigned source channel and port to an assigned destination channel and port.

5. Control Packet Router (CPR): forwards control packets from assigned source to destination

6. Control Protocol Engine (CPE): implements procedures defined in the MaGIC Control Protocol (MCP) that defines how devices establish logical connections between AICs, router data between MSRs and CPRs, and remotely change AIC parameters on another device through the network.

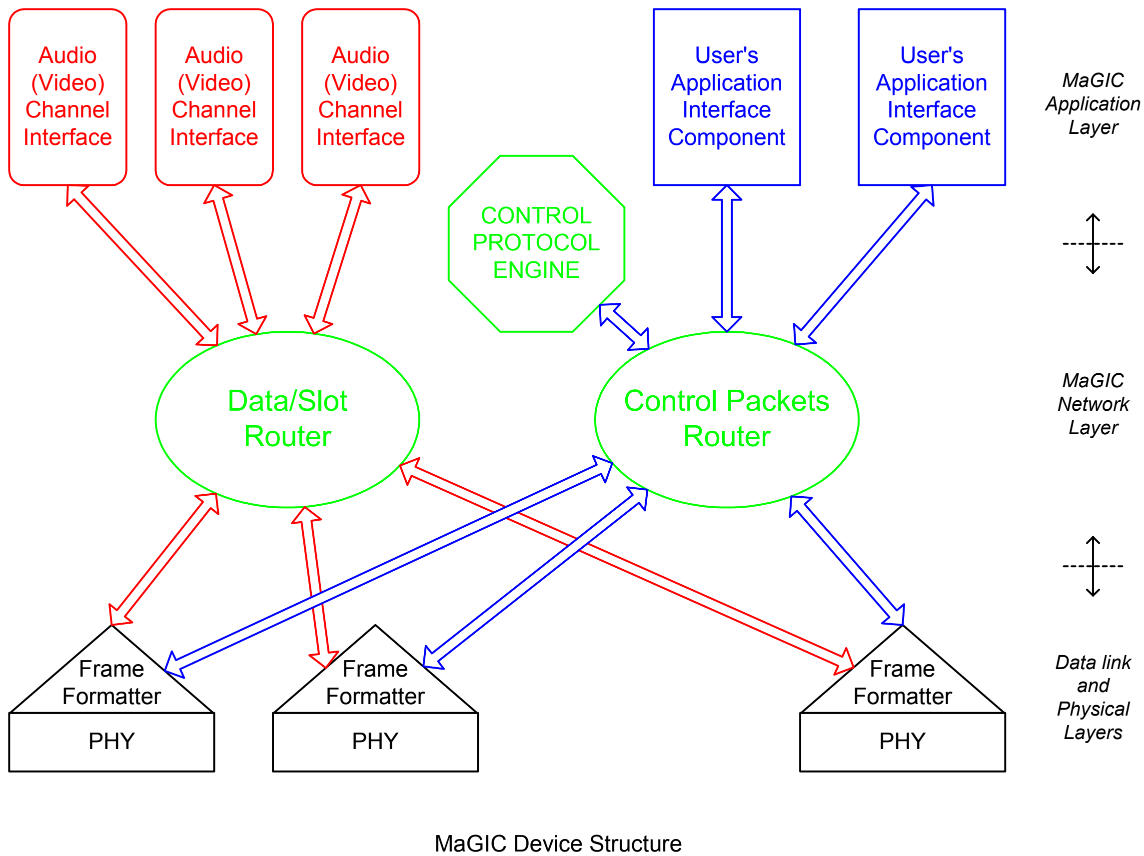

Figure 2-5: Structure of a MaGIC device

2.10 Media and control data flows

While MaGIC devices carry media and control in fixed parts of the same frame their characteristics are inherently different.

Each media stream on the MaGIC network has one source and one or more destinations. Data is transmitted synchronously at the base sampling without buffering thereby ensuring minimal possible latency. All destination devices should be capable of receiving and processing data at the full data stream rate.

On the other hand, control data is not synchronous and therefore does not share the same stringent latency requirements. These messages are generally broadcast to all devices on the network. Each device reads the destination address and decides whether to process it. If the message is addressed to another device then it is forwarded to all neighbors except the one it was received from.

A mandatory handshaking protocol ensures that receiving devices can stop control message flow when low on processing resources, therefore allowing flexibility in the requirements for each device. It is required however, for all devices to be capable of forwarding the control messages to their neighbors at network speed.

2.11 System Timing Master

The System Timing Master (STM) is the source of synchronization on the network allowing all devices to process data in phase with each other. The STM is automatically selected using a set of defined rules.

The STM locally generates a frame timing of 48 kHz with maximum jitter of 80 nanoseconds and worst stability of 100 ppm. All other devices recover and regenerate the same. The signaling rate of the physical layer is asynchronous with the frame transmission rate.

3. Mechanical

3.1 The MaGIC Link

The IEEE 802.3 implementation of the MaGIC Link is comprised of the RJ-45 connector and 100baseT Category 5 cable.

RJ-45 Cable RJ-45 Port

Figure 3-1: RJ-45 cable and port

3.2 The MaGIC Port

3.2.1 Port Specifications

The Category 5 cable consists of four twisted pairs: two are assigned for data transport and two for carrying power. Ports must be wired in a one-to-one configuration allowing each conductor to be connected to the same pin on both ports.

MaGIC requires an internal crossover on one of the two ports as shown in the figure below. This should not be confused with a crossover cable. The port using the standard 568A (one-to-one) wiring is defined as the **OUT** port. And, the port using the standard 568B with the signal crossover is defined as the **IN** port.

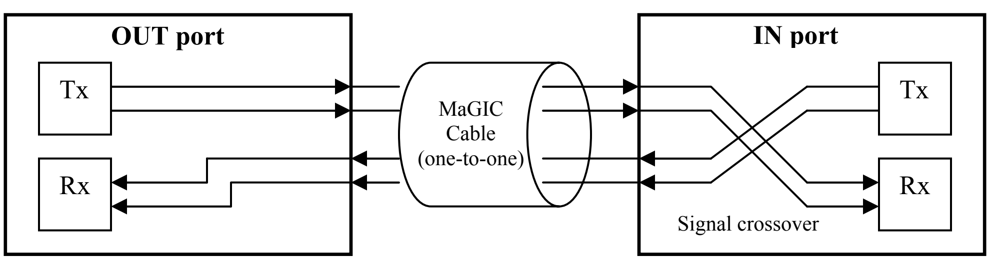

Figure 3-2: OUT and IN ports

3.2.2 Pin Assignments

Signal Name	OUT port pin number	IN port pin number
Transmit Data (TX) +	1	3
Transmit Data (TX) -	2	6
Receive Data (RX) +	3	1
Receive Data (RX) -	6	2
Power Ground	4	4
Power Ground	5	5
Voltage +	7	7
Voltage +	8	8

Table 3-1: Port pin assignments

This pin assignment ensures that

- Signals are transported over twisted pairs
- Transmit and Receive signals on OUT port use the same pins as a standard NIC. In ports are the same pin-outs as a hub.
- The two pairs of wires not used in standard Ethernet networks carry power.

3.2.3 Valid Configurations

A key feature of MaGIC is the automatic determination of the System Timing Master. (See chapter 7 for a detailed description). To make this possible, a device may have any number of IN ports, but no more than one OUT port.

3.3 The MaGIC Cable

3.3.1 Cable Requirements

The MaGIC Link has been designed to use 100baseT Category 5 cables:

- Of lengths up to 100 meters
- That include all four twisted pairs
- With at least 24 gauge stranded wire

It should be noted that MaGIC uses Category 5 patch cords that are always wired as a one-to-one assembly and not special crossover cables. Cables must be connected between OUT and IN ports, not OUT-to-OUT or IN-to-IN.

MaGIC devices should provide a mechanism (such as a green LED) to notify the user of a proper connection. This would allow the user to easily detect and rectify incorrectly connected cables.

A MaGIC network should never be wired such that any loops exist.

3.4 Dominant Data Flow

In most applications, there is almost always a dominant direction to the flow of media. The figure below illustrates a simple audio network consisting of a guitar, an effects box, and an amplifier.

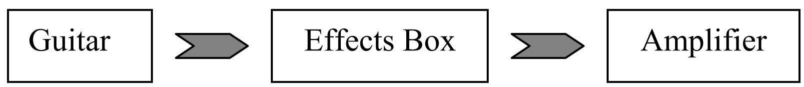

Figure 3-3: Direction of dominant data flow in a simple network

This is notion of dominant flow is the motivation behind the *OUT* and *IN* nomenclature used for MaGIC ports.

It is important to note that this is merely an application abstraction; MaGIC is a truly symmetrical and bi-directional communication protocol. Reversing the above connections would not change data flow because media is both sent and received through OUT and IN ports. Doing so would however, dictate the network synchronization master.

3.5 Robustness and Reliability

Live performance is one of the important applications MaGIC caters to. For such environments, particular attention must be paid to reliability and robustness of the network. The following suggestions can help manufacturers increase the quality of their connection equipment.

- Require highly flexible cables that can sustain repeated twisting, turning, and mechanical stress often experienced in live environments

- Take into account a reasonable amount of mechanical stress typically induced upon ports and over-stretched or tangled cables.

- Employ physical supports such as locking clips and special cable ends for the RJ-45 connector to prevent the clip from breaking or from accidental unplugging.

- Use stranded instead of solid wire cables in all environments except permanent fixed installations.

- Provide adequate protection against high voltage/current cables running nearby or even bundled with a MaGIC cable.

4. Electrical

4.1 IEEE 802.3 Compatibility

MaGIC shares a common physical layer with Ethernet. Each device occupies the entire bandwidth of a discrete 100baseT link in full-duplex mode.

Therefore, MaGIC is compatible with Ethernet at the physical layer.

4.2 Timing Parameters

4.2.1 Sample Clock Recovery

The recovered sample clock is based on the incoming sample rate to ensure synchronous data processing, and, if need be, can be multiplied up to the system sample rate.

With the exception of devices with sample rate conversion capabilities, the STM must supply sample timing for other devices on the network with a maximum frame-to-frame jitter of 80 nanoseconds.

All other devices must generate their outgoing frames in-phase with the stream of incoming frames. The frame-to-frame jitter of the outbound frames from non-STM devices must not exceed 160 nanoseconds. This is not a measure of accumulated jitter.

4.2.2 Latency Limitations

In order for MaGIC to function as a real-time digital link, the transmission latency must be contained to a low deterministic minimum.

There are three sources of latency in a MaGIC network:

1. *Physical Layer*: for a 100baseT physical layer this is usually in the range of 10-40 microseconds.

2. *Digital/Analog conversion*: if present, analog-to-digital (A/D) and digital-to-analog (D/A) converters usually add a significant delay of 1000-5000 microseconds. Therefore, these converters must be carefully chosen particularly for devices intended for live performance.

3. *Device processing*: each MaGIC device should use no more than 250 microseconds to process and forward incoming media. This limit refers specifically to the processing between the two digital MaGIC ports not between a MaGIC port and a Media Channel Interface.

4.2.3 Jitter Management

Minimizing jitter is an important requirement in designing circuits for sample rate recovery. The exact amount will vary depending upon the quality required for the specific application but as a general rule, each device should manage jitter to less than 80 nanoseconds.

4.3 Power

4.3.1 Cable Supply Requirements

A MaGIC cable must be capable of supplying 48 Volts DC (+/- 10%) according to the IEEE 802.3af specification.

The RJ-45 connector pins 4 and 5 are V+, and 7 and 8 pins are V-. This ensures a minimum of 36 Volts DC at greater than 350mA across the maximum cable length of 328 feet, as measured at the cable terminus.

4.3.2 Powered Device Requirements

Devices powered by the cable supply must operate within the range of 36 Volts DC to 54 Volts DC according to IEEE standard 802.3af. For increased efficiency non-linear voltage regulators should be used.

The maximum continuous power draw of a device must not exceed 350mA and inrush current must not exceed 500mA for more than 100ms.

Note that power supplied by one port must not be used by more than one device within a Daisy Chain. Only end point devices are permitted to use the power. Passing power through a device is not permitted.

4.3.3 Electrical Isolation

Devices supplying power to the MaGIC cable are not required to be isolated from one another.

Powered devices housed in non-conductive casing without any external connections except an OUT port do not require isolation. If the casing is conductive or other external connections exist, the DC-DC power supply must be isolated with 1500 Volts AC.

5. Data Link Layer

5.1 Overview

As shown in the table below, the Data Link Layer is based on the IEEE 802.2 standard LLC-SNAP frame:

Octets	Name	Size in Octets
0-7	**Preamble**	**8**
8-13	**Destination MAC Address**	**6**
14-19	**Source MAC Address**	**6**
20-21	**Length = 0xC4**	**2**
22-24	**LLC Header = AA-AA-03**	**3**
25-29	**SNAP Header = 00-00-00-xx-xx**	**5**
30–217	**MaGIC Payload**	**188**
218-221	**FCS**	**4**

Table 5-1: MaGIC Frame format

The frame starts with the 8-octet preamble, followed by the 14-octet long Media Access Control (MAC header), the 3-octet Logical Link Control (LLC), and 5-octet long Sub-Network Access Protocol (SNAP) headers. This defines MaGIC data as a payload of the 802.2 LLC-SNAP frames [2].

The 32-bit FCS field must be calculated using all data except the preamble in accordance with the IEEE 802.3 standard [1].

Since all sections are fixed-size, the MaGIC frame with preamble is always 222 octets.

5.2 Preamble

The frame preamble is described in section 7.2.3.2 and 7.2.3.3 of IEEE 802.3 specification [1].

5.3 MAC Header

As defined in the IEEE 802.3 standard, the 14-octet MAC header immediately follows the preamble and consists of 48-bit destination and source MAC addresses, and a 16-bit Length/Type field.

All MaGIC devices require worldwide unique 48-bit MAC addresses to remain compatible with standard Ethernet network hardware.

The Length/Type field contains the number of MAC payload octets following this field except the FCS. For the fixed-length MaGIC frame, this field always set to 196 (0x00C4).

5.4 IEEE 802.2 LLC and SNAP Headers

A 3-byte IEEE 802.2 Logical Link Control header immediately follows the MAC header.

It contains value DSAP/SSAP = AA and Control = 03 thus defining the use of LLC Type 1 communication with Sub-Network Access Protocol (SNAP). The following 5-byte SNAP header must carry value in 00-00-00-xx-xx format.

5.5 LLC implementation

The IEEE 802.2 standard defines the service provided by Logical Link Control sublayer [2]. A MaGIC device based on a 100-Mbit physical layer is not required to implement this service.

5.6 Frame Check Sequence

Octets 218-221 contain a 32-bit cyclic redundancy check (CRC) value for the data contained in the entire frame. The FCS computation and checking is mandatory.

The computation algorithm must follow IEEE 802.3 chapter 3.2.8 [1]. Appendix A contains a source code example for the FCS calculation function.

5.7 Endian Format

All data on a MaGIC network must be octet-wise Big Endian. This should not be confused with the bit-wise Little Endian format of the underlying Fast Ethernet physical layer.

Any Little Endian devices must accordingly swap necessary bytes before sending and after receiving frames.

6. Network Layer

6.1 Overview

As shown in the table below, the MaGIC frame payload uses 188-octet structure for transporting real-time media and control data. Note that octet indices in the left most column have been preserved with respect to the payload field of the MaGIC frame shown in table 5-1 in the previous chapter.

Frame Octets	Name	Size
30-33	**Configuration**	**4 octets**
34-37	**Frame Count / Timecode**	**One 32-bit word**
38-41	**Media Data Slot Valid Bits**	**One 32-bit word**
42-169	**Media Data Slots**	**Thirty-two 32-bit words**
170-173	**Reserved**	**4 octets**
174–185	**Control Header**	**12 octets**
186-217	**Control Data**	**32 octets**

Table 6-1: MaGIC Frame Payload Format

The MaGIC frame payload can be divided into the following sections:

- *Configuration*: 8-octet field that specifies the context and configuration in which to interpret the payload. It also carries a 32-bit Frame Count/Timecode.

- *Media Data*: fields containing the audio or video samples and related control bits. The Data Slots fields can also contain arbitrary data if needed. This section occupies 132 octets.

- *Control*: fields containing control messages and data being exchanged between MaGIC devices. This section occupies 44 octets.

These sections are described in detail in the following paragraphs.

6.2 Configuration Section

6.2.1 Configuration Section Format

The table below defines the format of the Configuration section located in octets 30-37 of the MaGIC payload.

Frame Octets	B0	B1	B2	B3	B4	B5	B6	B7
30	Frame Version				Slot Format		R	CP
31	Base Frame Rate				Channel Bandwidth			
32	R		Timecode Format					
33	Cable Number				R			
34-37	32-bit Frame Count/Timecode							

Table 6-2: Configuration Section of the MaGIC Payload

The reserved fields in this table are marked with letter R. These fields must be transmitted 0 and ignored on reception.

The Configuration section definition includes the following fields.

- Frame Version
- Default Media Data Slot Format ("Slot Format" in the table above)
- Copy Protection Bit ("CP" in the table)
- Base Frame Rate
- Default Channel Bandwidth Allocation ("Channel Bandwidth" in the table)
- Timecode Format
- Cable Number
- Frame Count/Timecode

These fields are described in details in the following chapters. Each device must verify these fields to ensure proper network operation.

6.2.1.1 Configuration Section: Frame Version (bits 0-3 of octet 30)

A transmitting device must set this field to 3 to indicate that the frame is compliant with this version of MaGIC.

A receiving device must check this field to insure that it properly interprets the received frame.

6.2.1.2 Configuration Section: Default Media Data Slot Format (bits 4-5 of octet 30)

This field defines the default data format carried in Media Data Slots located in octets 42-169 of the frame. The following table describes all possible field values.

Value	Format Type	Description
0	32-bit Integer	Data Slot word carries a 32-bit signed integer value.
1	32-bit Floating Point	Data Slot word carries a signed floating-point value according to IEEE 754 / 854.
2	24-bit with Channel Functions and Status	Data Slot word carries 24-bit audio sample, 4-bit channel status data, and 4-bit channel command
3	Raw	The format of Media Data Slots is defined by applications

Table 6-3: Configuration Word Bits 31-30 – Data Slot Formats

For all formats excluding RAW, 32-bit data must be transmitted in compliance with MaGIC Big Endian architecture (most significant byte first) and a Data Slot must always carry exactly one sample value. If a transmitting device does not generate a full 32-bit value then it must send the actual data value using the most significant bits of the Data Slot word and zero all the unused low bits. The sign value must be transmitted in the most significant bit of the 32-bit Data Slot word.

Format 2 should be used for transporting 24-bit audio samples in the three most significant bytes of the Data Slot word while the least significant byte may carry 4-bit audio channel and 4-bit audio channel command. This format is described in the following table:

Bits of the Data Slot	Format Name	Description
31	Audio sample MSB	Audio sample sign bit
30-8	Audio sample bits	Other audio sample bits. All unused least significant bits must be set to 0. Note: when directly mapped to the AES/EBU sub-frame, bits 11-8 may carry AES/EBU AUX data [4]
7	P	Channel status bits similar to AES/EBU channel status bits [4]
6	C	
5	U	
4	V	
3-1	-	Reserved for user channel commands
0	Express	Express channel command. An audio processing device that receives this command should forward this audio sample unchanged to the mapped output

Table 6-4: 24-bit audio Data Slot format

Use of channel commands is implementation dependent. By definition, the express command feature is not applicable to end points in a network. A hub may or may not respond to the channel command bits depending upon its specific function. For example, the hub must respond when providing an uplink but may choose to ignore it in the case of a mixer.

The RAW format must be used to send unformatted streams of octets between applications on the network. MaGIC devices must preserve the order of octets within the same media channel.

6.2.1.3 Configuration Section: Copy Protection Bit (bit 7 of octet 30)

In compliance with the Serial Copy Management System requirement specified by the 1992 U.S. federal copyright law, this bit denotes whether the data is copy protected.

Upon receiving copy-protected data, a device must not retransmit it to any other ports.

6.2.1.4 Configuration Section: Base Frame Rate (bits 0-3 of octet 31)

All MaGIC devices operate synchronously with a common network clock provided by the System Timing Master. The clock frequency defines the constant base frame rate at which devices transmit frames.

The value of this field indicates the clock frequency chosen by the System Timing Master. The following table lists all possible frequencies:

Base Frame Rate Field Value	Network Synchronization Frequency
0	48 kHz (default)
1	44.1 kHz
2-15	Reserved for future

Table 6-5: Defined Base Frame Rate values

All MaGIC devices must forward this field value that they receive through the OUT port to all their neighbors connected on IN ports.

The STM device must set this field to allow other devices to configure their timing circuits and media application interfaces. All devices must support both 48 and 44.1 kHz network frequencies.

6.2.1.5 Configuration Section: Default Channel Bandwidth Allocation (bits 4-7 of octet 31)

A MaGIC frame can carry data belonging to one or more media channels. The bandwidth of each channel is calculated as a product of the network base frame rate and the number of data slots in frame allocated to the channel. For example, a channel using four data slots on a 44.1 kHz network has 44,100 x 4 x 32 = 5,644,800 Bit/sec useful bandwidth.

The Base Frame Rate configuration field specifies the network base frame rate value. The Default Channel Bandwidth Allocation field provides the default number of media data slots that a device must allocate per channel based on the following table:

Channel Bandwidth value	Bandwidth	Comment
0	Single (1x)	Uses one media data slot word per channel and provides 32 default channels per link.
1	Double (2x)	2 data slots/channel, 16 default channels
2	Quadruple (4x)	4 data slots/channel, 8 default channels
3	8x	8 data slots/channel, 4 default channels
4	16x	16 data slots/channel, 2 default channels
5	32x	Allocates all 32 data slots for a single channel
6-15	-	Reserved

Table 6-6: Default Channel Bandwidth Allocation Field definition

The default channel bandwidth allocation is a part of device auto-configuration that may be overridden by network control applications.

6.2.1.6 Configuration Section: Timecode Format (bits 2-7 of octet 32)

The Timecode Type defined in the three most significant bits of octet 32 determines the content of the 32-bit Frame Count/Timecode word located in octets 34-37. The following table lists the defined options:

Value of Timecode Type bits	Configuration
0	Frame Count
1	MaGIC Timecode
2	MIDI Timecode
3-7	Reserved

Table 6-7: Timecode Type configuration values

Bits 2-4 store the frame rate for Timecode. The following table lists supported rates with corresponding values:

Value of Timecode Frame Rate bits	Timecode Frame Rate (Hz)
0	24
1	24.97
2	25
3	29.97
4	30
5-7	Reserved

Table 6-8: Timecode Frame Rate configuration values

6.2.1.7 Configuration Section: Cable Number (bits 0-3 of octet 33)

The value of this field may be used in the uplink configuration to provide additional routing information.

6.2.2 Frame Count / Timecode word

Bits 2-7 of the frame octet 32 determine the content of the Frame Count/Timecode word in octets 34-37. This 32-bit word can either be used as a counter for the number of transmitted frames transmitted, or to store Timecode.

When used as a counter at 48 kHz, the number stored in this field will reset every 24.86 hours when it reaches the maximum 0xFFFFFFFF value.

6.3 Media Data Section

The media data section is represented in the following table. It consists of thirty-three 32-bit words.

Octets	B0 – B31
38-41	**Data Slot Valid Bits**
42-45	**Data Slot 0**
46-49	**Data Slot 1**
50-53	**Data Slot 2**
54-57	**Data Slot 3**
58-61	**Data Slot 4**
62-65	**Data Slot 5**
66-69	**Data Slot 6**
70-73	**Data Slot 7**
74-77	**Data Slot 8**
78-81	**Data Slot 9**
82-85	**Data Slot 10**
86-89	**Data Slot 11**
90-93	**Data Slot 12**
94-97	**Data Slot 13**
98-101	**Data Slot 14**
102-105	**Data Slot 15**
106-109	**Data Slot 16**
110-113	**Data Slot 17**
114-117	**Data Slot 18**
118-121	**Data Slot 19**
122-125	**Data Slot 20**
126-129	**Data Slot 21**
130-133	**Data Slot 22**
134-137	**Data Slot 23**
138-141	**Data Slot 24**
142-145	**Data Slot 25**
146-149	**Data Slot 26**
150-153	**Data Slot 27**
154-157	**Data Slot 28**
158-161	**Data Slot 29**
162-165	**Data Slot 30**
166-169	**Data Slot 31**

Table 6-9: Media Data section of the MaGIC frame

6.3.1 Data Slot Valid Bits

The first 32-bit word of the MaGIC Media Data section is used to determine which data slots contain valid data. Bits 0-31 of this word are mapped to data slots 0-31 respectively. For example, if bit 0 were set it would denote valid data in slot 0. If bit 1 were set it would denote valid data in slot 1, and so on.

6.3.2 Data Slots

Frame octets 42-169 contain thirty-two 32-bit media data slots. This notion of slots allows MaGIC to support multiple channels and sample rates by providing a flexible mapping between the rate and the channels being transmitted.

At the single rate, each data slot is mapped to a single channel allowing a maximum of thirty-two channels to be transmitted.

In order to achieve higher fidelity, it is usually desirable to operate the media streams at a higher data rate. At the double rate, one channel is assigned to two data slots resulting in a possible transmission of two words each, mapped to sixteen different channels as shown in the figure below:

Octets	B0 – B31
42-45	Data Slot 0 (channel 0 first sample)
46-49	Data Slot 1 (channel 0 second sample)
50-53	Data Slot 2 (channel 1 first sample)
54-57	Data Slot 3 (channel 1 second sample)
58-61	Data Slot 4 (channel 2 first sample)
62-65	Data Slot 5 (channel 2 second sample)
66-169	Data Slot 6-31 (…so on)

Table 6-10: Default Data Slots assignment at the double (2x) channel speed

The next figure illustrates data slots allocation for establishing channels with quadruple bandwidth.

Word	B0 – B31
42-45	**Data Slot 0 (channel 1 first sample)**
46-49	**Data Slot 1 (channel 1 second sample)**
50-53	**Data Slot 2 (channel 1 third sample)**
54-57	**Data Slot 3 (channel 1 fourth sample)**
58-61	**Data Slot 4 (channel 2 first sample)**
62-65	**Data Slot 5 (channel 2 second sample)**
66-69	**Data Slot 6 (channel 2 third sample)**
70-73	**Data Slot 7 (channel 2 fourth sample)**
74-77	**Data Slot 8 (channel 3 first sample)**
78-169	**Data Slot 9-31 (…so on)**

Table 6-11: Default Data Slots assignment at the quadruple (2x) channel speed

The channel can aggregate any number of slots in the available range. For example, following two figures show valid configurations for two channels with 5x and 3x bandwidth respectively.

Word	B0 – B31
42-45	**Data Slot 0 (channel 0 sample 1 of 5)**
46-49	**Data Slot 1 (channel 0 sample 2 of 5)**
50-53	**Data Slot 2 (channel 0 sample 3 of 5)**
54-57	**Data Slot 3 (channel 0 sample 4 of 5)**
58-61	**Data Slot 4 (channel 0 sample 5 of 5)**
62-65	**Data Slot 5 (channel 1 sample 1 of 3)**
66-69	**Data Slot 6 (channel 1 sample2 of 3)**
70-73	**Data Slot 7 (channel 1 sample3 of 3)**
74-169	**Data Slot 8-31 (unused)**

Table 6-12: Example of valid data slots assignment for channels with 5x and 3x speeds

Word	B0 – B31
42-45	**Data Slot 0 (unused)**
46-49	**Data Slot 1 (channel 0 sample 1 of 5)**
50-53	**Data Slot 2 (channel 0 sample 2 of 5)**
54-117	**Data Slot 3-18 (unused)**
118-121	**Data Slot 19 (channel 1 sample 1 of 3)**
122-125	**Data Slot 20 (channel 1 sample2 of 3)**
126-129	**Data Slot 21 (channel 1 sample3 of 3)**
130-133	**Data Slot 22 (channel 0 sample 3 of 5)**
134-137	**Data Slot 23 (channel 0 sample 4 of 5)**
138-141	**Data Slot 24 (channel 0 sample 5 of 5)**
142-169	**Data Slot 25-31 (unused)**

Table 6-13: Another example of valid data slots assignment for channels with 5x and 3x speeds

All samples from a channel must be transmitted in the order they were generated. Therefore inside the frame, samples with larger numbers will be located in the frame words with larger numbers.

Samples from different channels may be arbitrarily interleaved.

All devices that generate media data samples with less than 32-bit resolution must represent samples in the most significant bits of the data slots and zero all unused low bits. This is required for simpler communication between devices that operate with different resolutions.

While data slots can transport data in any format, MaGIC devices should use one data slot per audio sample.

All audio devices that send channel status/command data with audio samples must use the least significant bits of the data slot word for all non-audio data. This minimizes the negative impact that is potentially introduced whenever the control data propagates to the audio path of a connected device.

6.4 Control Section

6.4.1 Control Packet format

MaGIC devices must use the following 44-octet unified structure for carrying control messages in the control section of the MaGIC frame payload. This structure is referred to as a Control Packet as defined in the following table:

Frame Octets	Bits 0-7	
174	**Control Message Code (High 4 Bits)**	**Status Bits (4 bits)**
175	**Control Message Code (Low 8 Bits)**	
176	**Message Length (High 4 Bits)**	**Reserved (4 Bits)**
177	**Message Length (Low 8 Bits)**	
178–179	**Destination Unit Address (2 octets)**	
180–181	**Source Unit Address (2 octets)**	
182–183	**Destination Component Address (2 octets)**	
184–185	**Source Component Address (2 octets)**	
186-217	**Control Data (32 octets)**	

Table 6-14: MaGIC Control Section/Packet Format

The control packet has its own 12-octet header and 32-octet payload that follows the header.

The address fields of the control packet allow a maximum of 65535 functions on a maximum of 65535 devices on the network. The control messages may choose from 4096 independent types/codes and can be up to 4096 octets long.

The following subsections describe the control packet format in detail.

6.4.1.1 Control Packet format: Status Bits (bits 4-7 of octet 174)

The control packet status bits are listed in the following table

Bits	Name	Description
7	CTS	Clear to Send This bit is used for controlling the control packets flow.
6	-	Reserved Must be sent 0 and ignored by the receiver
5	CV	Control Packet Valid bit. When asserted, indicates that the Control section contains a Control packet
4	SOM	Start of Message Indicates the beginning of new control message

Table 6-15: Control Packet Status Bits

The Control Packet Valid bit (CV) indicates whether the frame contains a control packet. When CV is zero all other fields in the control section are undefined. The only exception is the CTS bit which is always valid regardless of CV status.

An asserted CTS bit indicates that the neighbor device is capable of receiving more control packets. This bit is associated with the physical port through which the frame is received and with the device connected through that port.

When a device receives low CTS, it must stop sending control packets immediately. Taking into consideration all pipeline delays between layers; a device must not send more than 8 control packets through a physical port after that port starts receiving a frame with low CTS. In other words, the receiving port must be capable of receiving at least 8 control packets into its input queue after it lowers the CTS.

Note that a pause in transmission of control packets due to lowered CTS must not effect transmission of MaGIC frames. The device must continue sending frames with a lowered CV indicating the absence of control packets in the frames.

The sending device must resume transmission after receiving a frame with asserted CTS.

All devices must use this mechanism for flow control with their neighbors. Flow control must be performed independently on each physical port for both incoming and outgoing control packets.

Control messages may require multiple control packets (frames) to transmit. An asserted Start of Message bit (SOM) indicates the beginning of a transmission. Devices must be capable of reassembling *multi-frame message* using the values of this bit together with Message Length field (octets 176 and 177).

All *single-frame* messages must assert the SOM bit to indicate the transmission of a new control message.

6.4.1.2 Control Packet format: Control Message Code (octets 174 and 175)

The 12-bit Control Message Code (CMC) field is located in octet 175 (low eight bits) and bits 0-3 of octet 174 (high four bits). As defined in the table below, its value determines the type and format of control message:

Range	Name	Description
0-127	Network Management Messages	Defines the control message being sent. Appendix C lists all the standard control messages defined at this time.
128-511	Well Known Application Protocols	Must be used either for encapsulation of well-known high level protocols (like TCP/IP or UDP/IP) or for transporting messages with well-known format and structure (like MIDI).
512-1023	User Control Messages	Users may freely specify their proprietary messages using CMC values from this range.
1024-4095	Reserved	Reserved for future definition. Must not be used.

Table 6-16: Assignment of Control Message Code Value Ranges

The first range of values 0-127 lists network management messages all devices must implement. They are defined in subsequent chapters. Appendix C also lists defined standard control messages.

The second range (128-511) is dedicated for encapsulation of well-known protocols like IP, TCP, or well-known formats like MIDI. Such implementations are discussed at length in the MaGIC Application Layer chapter.

Values from the third range 512-1023 may be freely used to define new device or application specific messages and protocols. Devices must be carefully to only use such messages with other devices known to support them in order to prevent unpredictable behavior.

6.4.1.3 Control Packet format: Reserved (bits 4-7 of octet 176)

Bits 4-7 of octet 176 are reserved for future use. They must be transmitted as zeros, and ignored upon receipt.

6.4.1.4 Control Packet format: Message Length (octets 176 and 177)

The 12-bit Message Length field is located in octet 177 (low eight bits) and bits 0-3 of octet 176 (high four bits).

It carries the length in octets of the control message being transmitted. Size of transmitted message may exceed size of the allowed control packet payload. In such case the message must be sent in several consecutive control packets.

For proper transmission and reception of multi-frame messages, this field must be used with SOM (bit 4 of octet 174) as described in section 6.4.2 of this document.

6.4.1.5 Control Packet format: Destination Unit Addresses (octets 178-179) and Source Unit Address (octets 180-181)

These 16-bit fields allow a device to address a control packet from itself to another device on the network. Each device on network is assigned a unique Unit address. As a control packet is sent from one device to another, each device evaluates the Destination Unit Address field to determine if it should process the packet. If not, it must forward the packet along the network ensuring that the packet will eventually reach it's the intended destination(s).

Control messages can also be multicast or broadcasted. The following table lists reserved addresses (not assigned to any device during address auto-configuration) used for this purpose:

Name	Address	Description
System Broadcast	0xFFFF	All devices on a network must process a message with this destination address.
Local Hub Broadcast	0xFFFE	If a hub generates this broadcast it must forward it to all its IN ports. If it receives the message on one of its ports, it should process it and then forward it on all ports except it's OUT port, and the port it received the message on.
Daisy Chain Broadcast	0xFFFD	All devices on a Daisy Chain must process and forward this broadcast. A hub should only forward it to its IN ports if it generates the message itself or if it receives it on its OUT port.
Startup	0xFFFC	Not used.
Neighbor	0xFFFB	The receiving device must process this message without forwarding it.
Reserved	0xFFF0 - 0xFFFA	Reserved for future use. All devices must forward this broadcast.
Application Broadcasts	0xF000 - 0xFFEF	Reserved for control applications. All devices must forward this broadcast.
STM	0x0000	System Timing Master

Table 6-17: Reserved Unit Addresses

6.4.1.6 Control Packet format: Destination Component Address (octets 182-183) and Source Component Address (octets 184-185)

The 16-bit source and destination component addresses define service access points or interface ports to support multiple higher layer users.

The component address field interpretation must be performed depending on the particular message CMC value. For example, messages carrying encapsulated TCP/IP frames should use component address values to map TCP port numbers.

In other examples, the components may represent physical interfaces like remote audio volume controls or power on/off switches.

MaGIC components are described in MaGIC Application Layer specification.

6.4.1.7 Control Packet format: Control Data (octets 186-217)

These 32 octets transmit supporting data for control packets.

The message length field (octets 176-177) defines the number of used control data octets. When less than or equal to 32, it is the exact number of used control data octets offset from octet 186.

When greater than 32 then the packet carries 32 octets with remaining octets to be expected in the subsequent packets.

Devices are not required to fill unused control data octets.

6.4.2 Multi-Frame control messages

Whenever a control message size exceeds 32 octets, the size of the control data field, the transmitting device must fragment and send the message in consecutive packets. The transmitted message is considered a sequence limited to a maximum of 4096 octets.

Note that the size of each message fragment excluding the last must be exactly 32 octets. The size of the last fragment must equal the number of remaining octets.

The message length field contains the size of the remaining part of message. For example, for a message of size N, the first length field should be N, the second (N-32), the third (N-64), and so on.

The first control packet must raise the SOM bit to indicate the start of message while subsequent fragments must lower it.

The message being transmitted is uniquely identified with the following values:

- Control Message Code
- Destination and Source Unit Addresses
- Destination and Source Component Addresses

Control packets that are carrying fragments with different CMC or addresses may be interleaved during transmission since the recipient can identify each one based on the above-mentioned values.

If a device starts a new transmission before finishing an ongoing one, the receiver must discard all fragments of the unfinished message.

6.4.3 Control Communication Errors

If a recipient detects a control message transmission error it must cancel the operation and discard all previous fragments. The device may then choose to inform the sender about detected errors provided it does not introduce an "avalanche" of messages. Devices must never send notifications about detected broadcast errors.

Possible errors include:

- Recipient lacks sufficient resources to receive and reassemble the message. This is detectable using the message length value.

- Recipient detects a loss of a message fragment. This can be detected by comparing message length fields of packets that carry consecutive fragments. The difference should always be 32, the fragment size.

- Recipient detects a restarted transmission. This can be detected by comparing CMC and address values to ensure that they match those of the previously received message.

6.4.4 Encapsulation of the Internet Protocol

The encapsulation of the Internet Protocol (IP) in MaGIC control messages is accomplished using multi-frame messages mechanism described above. This topic is addressed at length in the MaGIC Application Layer chapter.

7. Device Auto-Configuration

7.1 Overview

Each device must execute the following configuration steps when joining a MaGIC network.

1. Select synchronization source
2. Configure unit address
3. Enable media and control applications

This chapter explains the first two steps in details. The MaGIC Application Layer chapter specifies the third.

7.2 Selecting Synchronization Source: establishing the STM

The System Timing Master (STM) is a device selected to provide the sample clock used by all other devices to achieve synchronized data processing. Selecting the STM is automatic and transparent to the end user.

The following diagram shows an STM device X connected to a slave device Y. Device Y uses the recovered and regenerated sample clock for encoding and decoding frames.

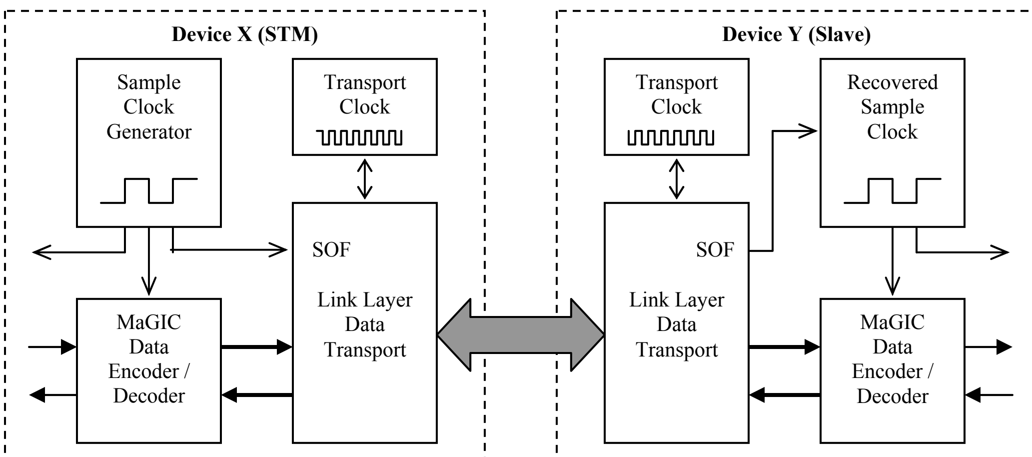

Figure 7-1: Sample and Transport Clock Relationship

The following rules are used to uniquely establish the STM:

1. *A device with only one OUT port can never be the STM.*
2. *A device with only IN ports will always be the STM.*
3. *If all devices contain both OUT and IN ports, then the one not connected on the OUT port will be the STM.*

Subsequent sections continue to refer to these rules as Rule 1, Rule 2, and Rule 3 respectively.

The established STM must notify other devices about the new synchronization source by broadcasting the `Change of STM` control message with Daisy Chain Broadcast destination address to all its connected ports. The broadcast must be repeated at least 5 times with 1 millisecond interval to allow all devices on the network to correctly respond to the change.

The STM device must receive and respond to messages with the reserved destination unit address 0x0. The STM must also continue responding normally to its unit address that it assigned to itself using auto-configuration process. The address auto-configuration is discussed chapter 7.4.

7.2.1 Example: two-device network

The following figure shows a simple network with a Guitar (one OUT port, no IN ports) and an end-point Amplifier (no OUT port, one IN port). Rule 1 above disqualifies the Guitar from being the STM. Rule 2 uniquely identifies the end-point Amplifier as the network STM.

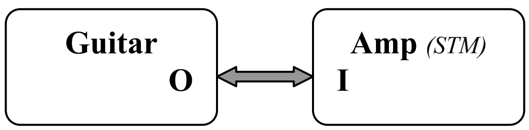

Figure 7-2: Establishing the STM using Rules 1 and 2

7.2.2 Example: daisy-chain network

Consider below another simple network consisting of a Guitar (one OUT port, no IN ports), a Stomp Box (one OUT port, one IN port), and an Amplifier (one OUT port, one IN port). As in the previous example, Rule 1 disqualifies the Guitar and Rule 2 is not applicable. Rule 3 however, disqualifies the Stomp Box (because it is connected on the OUT port) in favor of the Amplifier, which becomes the unambiguous STM.

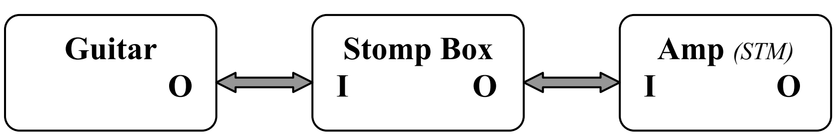

Figure 7-3: Establishing the STM using Rules 1 and 3

7.2.3 Example: hub-based networks

The following example consists of a Routing Hub (no OUT port, and three IN ports) connected to three devices. Again, Rule 1 disqualifies the Instruments and Rule 2 uniquely identifies the Routing Hub as the STM.

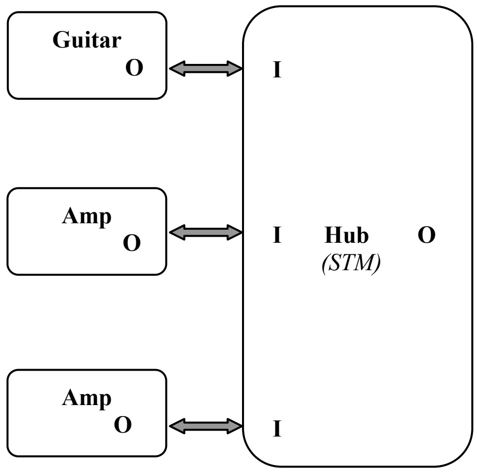

Figure 7-4: Establishing the STM with a Hub using Rules 1 and 2

This final example depicts a relatively complex MaGIC network. The application of Rules 1 and 3 in the same way shown above reveals the Mixer as the unambiguous network STM.

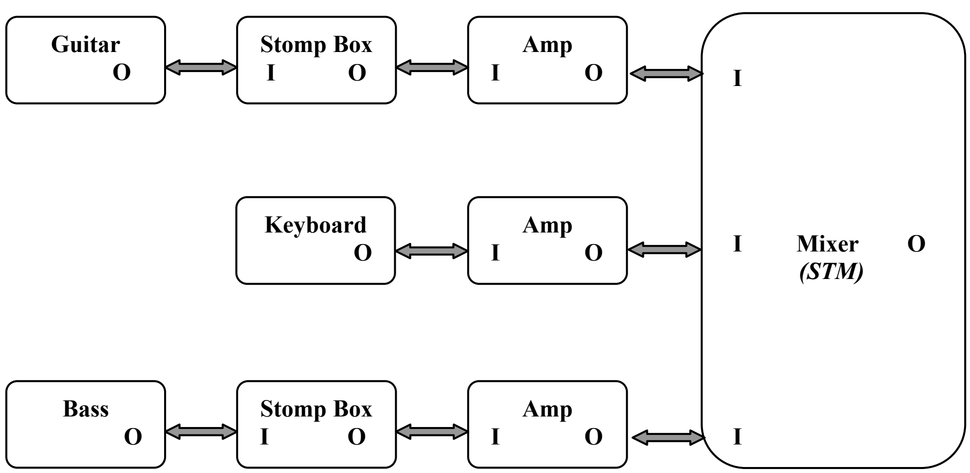

Figure 7-5: Establishing the STM with a Mixer (Hub) using Rules 1 and 3

As the examples above illustrate, all devices must be capable of assuming the role of STM except those with no IN port.

7.3 Synchronizing a Non-STM Device

If a device joins a network with an established STM, it must resynchronize itself and all devices connected to its IN ports with the network base frame rate. This requires locking the internal Phase Lock Loop (PLL) timing circuitry and may take several hundred milliseconds per device.
During this period of resynchronization, a device must not generate any signals or messages on the network or on its application interfaces to prevent against degrade performance or causing equipment damage through signal spikes and glitches.

Either of the following two conditions causes a device to slave itself to existing network STM:

- OUT port is connected
- Received `Change of STM` control message

If either of the above condition is true, the device must:

- Broadcast `Change of STM` control message on all IN ports (Daisy Chain Broadcast) with 1 millisecond intervals until resynchronization is complete
- Lock internal PLL to the network frame rate on OUT port
- An audio device must mute all audio outputs until resynchronization is complete

7.4 Assigning the Unit Address

7.4.1 Overview

Each device selects a 16-bit address number to uniquely identify itself on the network. Addresses 0xF000 – 0xFFFF, 0x0 (unless it is the STM), or other addresses assigned to other devices must not be used.

The address is assigned in two stages:

1. Device assigns itself a tentative address and advertises it on the network using the `Address Advertisement` broadcast approximately every 5ms. If an `Address Conflict` message is received the device restarts this process, otherwise it moves to stage 2 after approximately 500 ms.

2. Device assigns the temporary address chosen on stage 1 as its network unit address and invokes user applications so they may start their advertisement on the network. If at this stage an `Address Conflict` message is received, the device must abandon this address, notify the applications, and restart at stage 1. The device must notify the applications about the address change.

7.4.2 Tentative Address Value Generation

A device can choose as its tentative address any 16-bit binary value from the range 0x1 to 0xEFFF excluding those that are explicitly known as being used by other devices. For example, it must not use address values that have been rejected during previous attempts or values being advertised by other devices on the network.

The following approach is recommended to select the first tentative address value:

- Use a value from the previous session on the network. Not only does this simplify the initial selection by it also enables easier recovery from connector's failures.

- Use a 16-bit address value that is generated based on the device MAC address. This approach should guarantee rare conflicts since all devices must have unique MAC addresses.

If an address value was rejected then a device must generate another address value using a pseudo-random sequence generator. The implementation of the generator must ensure a value repetition period not less than (2^{15}-1).

7.5 Connecting and disconnecting Ports

Connecting or disconnecting two physical MaGIC ports is in effect merging or splitting two networks.

Connecting ports resynchronizes the all devices starting from the new STM by:

1. Lock timing circuitries
2. Reassign addresses
3. Restart applications

This process propagates through the network as each device in the chain locks its timing circuitry to the network frame rate.

Address reassignment should rarely result in new values since their choice depends on unique device parameters. This process should also provide for graceful application restarts on the newly merged network.

Disconnection is similar to connection except that the root of the disconnected chain becomes the STM. The network continuing with the same STM must not go through the resynchronization process. Other devices must elegantly and appropriately react to the disappearance of control and media application(s) that were physically disconnected.

Manufacturers must insure against signal spikes or glitches that may damage connected equipment or affect the application operation quality.

7.6 Neighbor Advertisement

Once a device has assigned itself a tentative address, it must advertise itself to its neighbors. This allows applications to quickly scan the network and collect relevant topology information.

This is done by sending the “Neighbor Advertisement” control message with the destination address value 0xFFFB (“Neighbor”) to all neighbors every 200 milliseconds. A device receives the message and stores the following information as an attribute of the port through which it received the information:

- Source MAC address of sender port
- Source Unit Address (tentative or permanent)
- Sender programmable symbolic name (limited to 32 octets)

Every device is required to continue advertising to all neighbors throughout the duration of operation.

7.7 Incompatible Devices

If a device connects to a network operating at an unsupported sample rate, it must conveniently notify the user and not transmit data.

8. Control Links

8.1 Overview

Control links are virtual bi-directional communication pipes between control applications on two or more MaGIC devices created by recording the following parameters:

- Full 32-bit component address (16 bits unit address and 16 bits component address)
- Communication parameters (master/slave relationship, communication protocol, etc.)

Multiple components may be linked to allow multiple sources to send control data simultaneously to multiple destinations. In this case, the component link table must be capable of storing multiple records, one record per peer component.

As a simple example, consider a knob (rotary encoder) on a device, and a volume control on another device. A control link is the logical mapping that allows the knob to regulate the remotely located volume through the MaGIC network.

While control applications are capable of communicating without previously established control links, this mechanism simplifies device implementation by enabling a single application with sufficient resources on the network to centrally manage the task of linking. Imagine a computer with a sophisticated GUI that supported remote control link assignment.

Such an application would act as a network supervisor that would manage other applications, define media routing, and establish control links. A network could possibly have multiple supervisors located on different devices across the network. The MaGIC Application Layer chapter addresses network supervisors in details.

In simpler cases, control links may be pre-programmed into devices by manufacturers or automatically established based on predetermined algorithms.

This chapter describes standard control messages used for establishing control links. Devices may also establish control links using proprietary mechanisms as long as they are compliant with this specification.

8.2 Writing a Control Link Record

A device modifies the content of component control link table by sending an `Add/Remove Link Record` message to a component of another device. The message format is discussed in section 6.4 and the payload is defined in the following table:

Field	Size
Link-To Unit Address	**2 octets**
Link-To Component Address	**2 octets**
Requested Link Parameters	**2 octets**
Optional Link Parameters	**0 to 4090 octets**

Table 8-1: Add/Remove Link Record Message Format

The Link-To unit and component address fields together uniquely identify the component whose link table is to be modified.

The 16-bit Requested Link Parameters field is defined in the following table:

Bit	Name	Description
16	Add/Remove Command	1 requires the recipient to add the record with specified parameters. 0 requires the recipient to remove the record specified with Link-To address fields Note. All other fields must be ignored if this bit = 0
15-14	Master/Slave Relationship Or Remove All	0x – Unspecified master/slave relationship 10 – the recipient must become slave 11- the recipient must become master
13-8	-	Reserved for future use. Must be transmitted 0 and ignored by the recipient.
7-0	Control Link Protocol	This field specifies a control protocol for the established link.

Table 8-2: Requested Link Parameters field format

Optional Link Parameters may be sent immediately following the Requested Link Parameters field.

As with all other control messages, if the total message size exceeds 32 it must be fragmented and sent in multiple frames. Message length is limited to 4096 octets, which limits the maximum size of Optional Link Parameters field to 4090.

The recipient must report back to the requesting device with operation completion status.

8.3 Establishing a Control Link on the Supervisor's Request

The `Establish/Drop Control Link` control message allows a network supervisor to request any component on the network to establish or drop a Control Link with any other component.

The message control data format is identical to `Add/Remove Link Record` message in addition of the following:

- Link-To address fields specify the assigned peer for the recipient
- Requested Link Parameters specify the recipient side of the master/slave relationship
- The recipient may ignore any part of Optional Link Parameters if they are inapplicable or unsupported.

The recipient must report back to the requesting device with operation completion status.

8.4 Reading or Clearing a Control Link Table

A `Read/Clear Link Table` message allows a device to:

- Read a list of linked component addresses, or,
- Erase the content of a component control link table

This message requires one parameter in the first control data octet (frame octet 186). The parameter is a command to report the list of linked components when zero. Otherwise, it is a command to clear/erase the contents of the control link table.

The recipient must report back to the sender with operation completion status sending either the `Operation Completion Status` or the list of linked components.

The list of linked components must be reported using the `List of Linked Components` message in the following format:

Field	Size in Octets
Link-To Unit Address 0	**2**
Link-To Component Address 0	**2**
Link-To Unit Address 1	**2**
Link-To Component Address 1	**2**
So on…	

Table 8-3: List of Linked Components Message Format

If its link table contains no records, the component must return the `List of Linked Components` message with an empty payload and a zero message length field as described in chapter 6.4.1.4.

8.5 Reading Control Link Parameters

The `Read Link Parameters` message allows a device to read link parameters of a remote component. The message has two parameters as shown in the following table:

Field	Size in Octets
Link-To Unit Address	2
Link-To Component Address	2

Table 8-4: Read Link Parameters Message Format

For existing links, the recipient must reply with the List of Link Parameters in a format similar to `Add/Remove Link Record` message specified above in table 8-1.

If the requested link does not exist the recipient must notify the requesting device using the `Operation Completion Status` message.

9. Media Data Routing

9.1 Overview

MaGIC devices use 32-bit data slots for transmitting real-time audio and video data on the network. Data slots are the smallest transport units that devices can assign to particular virtual media pipes.

For flexible routing of virtual media pipes, every multi-port device must incorporate an internal router that forwards the payload of these data slots from input to output ports in real time based on the routing table each output port is required to have.

This table must contain the same number of records as data slots the port outputs. Each record must uniquely identify the source of the associated data slot.
The media router assembles the output frame media payload, sequentially for each slot of each port, and repeats this process cyclically and synchronously with the network clock.

A network supervisor may establish media routes on the network by modifying routing tables of connected ports. This can be accomplished using control messages defined in the subsequent sections.

9.2 Routing table format

Each MaGIC device is required to have at least one but no more than 32767 network ports. An OUT port if present is always assigned the address 0. Each IN port is assigned an address using consecutive numbers starting from 1 even if the OUT port is absent.

A network port 32767 has a special NULL function. If media data is routed to this port then it must be discarded.

Likewise, each device may have between 0 and 32768 application ports that must be assigned consecutive numbers from 0 to 32767.

Routing tables for both network and application ports must have the same format. Each table size must be set according to the maximum number of data slots each output port is capable of processing at the lowest network base rate. This number must not exceed 65536.

A 32-bit routing record must consist of:

- 16-bit port number
- 16-bit slot number

The most significant bit of the port number defines the port type: 1 indicates a network port and 0 an application port.

The 16-bit slot number is logically divided into a reserved for future use 11-bit cable number and 5-bit slot position. The slot position is represented in low bits of the slot number.

100-Mbit physical layer based devices must transmit the cable number bits set to zero.

9.3 Setting the Routing Table

The `Set Routine Table` control message allows defining up to 1023 routing records at a time. The format of the control message payload is as follows:

Field	Size in octets
Output Port	2
Table Offset	2
Input Port 0	2
Input Slot 0	2
Input Port 1	2
Input Slot 1	2
Input Port 2	2
So on…	

Table 9-1: Set Routing Table Message Payload Format

The message payload consists of the output port/routing table number followed by the Table Offset value and a list of routing records that must be consecutively loaded into the table starting from the specified offset.

If message size exceeds 32 octets it must be transmitted in multiple control frames.

9.4 Reading the Routing Table

The `Read Routine Table` control message allows for reading the routing information from a device. The format of the control message payload is as follows:

Field	Size in octets
Output Port	2
Table Offset	2
Number of Records	2

Table 9-2: Read Routing Table Message Payload Format

The recipient device must respond with the `Routing Table Data` message whose format is identical to `Set Routing Table`. The returned number of records must match the requested value.

9.5 Muting a device

The `Mute` allows the transmission of a sequence of 32-bit masks to another device to enable or disable particular data slots. A mask value of 1 indicates a disabled slot that must be set to zero.

Field	Size in Octets
Output Port	**2**
Table Offset	**2**
Mask 0	**4**
Mask 1	**4**
So on…	

Table 9-3: Mute Message Payload Format

As shown in the table above, the message payload specifies the output port whose table is to be modified along with a list of masks that are to be applied to consecutive 32-slot groups—one 32-bit mask per logical cable.

10. Device Attributes

10.1 Overview

A device must store descriptive parameters or attributes such as a symbolic name or a number of ports to allow other devices to recognize it on a network.

These attributes can be static, such as a MAC address or pseudo-static such as device unit address that remains constant through a network session or possibly even between sessions.

The MaGIC network layer provides a unified interface to such unformatted attributes and allows them to be grouped in tree-like structures. Each attribute has a unique address that can be described as a sequence of 32-bit values. Attributes with addresses that end with a zero contain a descriptor for other attributes in the sub-tree. An attribute with address zero is the root descriptor that defines all attributes-trees with addresses 1 to 65535. For example, an attribute with address 3.5.0 contains a description for all implemented attributes with addresses from 3.5.1 to 3.5.65535.

10.2 Descriptor format

The descriptor is a consecutive list of records. Each record contains the following fields:

- 16-bit sub-address
- 16-bit attribute type

Records must be stored in the order of increasing sub-addresses. 16-bit attribute type describes attribute stored with the listed sub-address.
The attribute itself has the following fields:

- 1-bit value/sub-tree field (0-value, 1-subtree)
- 3-bit value type filed
- 12-bit length field

The first indicates whether the attribute is a value or another sub-tree of values or nested sub-trees. The second defines the value type as described the table below. The third defines the value size in octets.

Value type	Name	Description
0	Undefined	Must not be used
1	ASCII	The value is ASCII string (up to 4096 octets)
2	Unicode	The value is 16-bit Unicode string (Up to 2048 symbols).
3	Undefined	Must not be used
4	Integer	The value is 32-bit signed integer.
5	Floating Point	The value is a floating point value
6-7	Undefined	Reserved for future use

Table 10-1: Attribute value type definition

10.3 Reading an Attribute

The message payload format is as follows.

Field	Size in Octets
Root sub-address	**2**
Sub-address1	**2**
Sub-address2	**2**
So on…	

Table 10-2: Read Attribute Control Messages

The nested depth of sub-addresses is limited to 16 to allow the control message to be sent in the control data payload of a single frame.

The recipient device must return the attribute value using the `Attribute Value` control message. The value itself must be sent in the control data payload of one or more frames, as needed.

10.4 Required Attributes

See Appendix B for a list of required attributes that must be defined by all MaGIC devices. .

11. Network Layer Control Messages

11.1 Network Layer Control Messages at-a-glance

CMC	Name	Description
0x01	Operation Completion Status	Used for error reporting
0x03	Change of STM	Forces device resynchronization
0x05	Address Advertisement	Used for device address auto-configuration. Tentative address broadcast
0x07	Address Conflict	Reports an address conflict between two or more devices.
0x09	Neighbor Advertisement	Reports device symbolic name to neighbor devices
0x11	Add/Remove Link Record	Adds or removes a record to/from the control link table of a device component.
0x13	Establish/Drop Control Link	Establishes or disconnects a control link between two remote components.
0x15	Read/Clear Link Table	Reads or erases a control link table of a device component.
0x17	List of Linked Components	Provides list of addresses for linked components.
0x19	Read Link Parameters	Read parameters of a particular control link.
0x1B	List of Link Parameters	Provides information about a control link.
0x31	Set routing table	Programs port routing table.
0x33	Read routing table	Accesses port routing table data.
0x35	Routing table data	Reports content of port routing table.
0x41	Mute	Transmits a list of data slot enable/disable masks.
0x51	Read Attribute	Requests an attribute value
0x53	Attribute Value	Transmits the requested attribute value.

Table 11-1: Network Control Messages

11.2 Operation Completion Status

CMC = 0x01

Parameters

- Completion Status/Error Code (1 octets)
- Reference message (12 octets of header and first 16 octets of control data)

Format

Frame Octets	Bits 0-7	
174	0	-
175	0x1	
176	Message Length	0
177	Message Length	
178–179	Destination Unit Address	
180–181	Source Unit Address	
182–183	Destination Component Address	
184–185	Source Component Address	
186	Completion Status Code	
187–189	Reserved = 0 (3 octets)	
190–201	Reference Message Header (12 octets)	
202-217	Reference Message Control Data (16 octets)	

Table 11-2: Operation Completion Status Message Format

Value	Description
0	Success
0x01	Parameter Does Not Exist.
0x02	Insufficient Resources To Process Request
0x3-0xFE	Reserved Error Codes
0xFF	Unknown Error

Table 11-3: Completion Status Code value definition

Description

This message must be sent in order to report a completion status of requested operation or to report an error.

11.3 Change of STM

CMC = 0x03

Parameters
None

Format

Frame Octets	Bits 0-7	
174	0	-
175	0x03	
176	0	0
177	0	
178–179	Destination Unit Address	
180–181	Source Unit Address	
182–183	0	
184–185	0	
186-217	0	

Table 11-4: Change of STM Message Format

Description

The recipient must resynchronize its PLL due to change of STM. All audio devices must mute their audio outputs until the completion of resynchronization.

11.4 Address advertisement

CMC = 0x05

Parameters

- Source Unit Address = Tentative Unit Address

Format

Frame Octets	Bits 0-7	
174	0	-
175	0x05	
176	0	0
177	0	
178–179	0xFFFF	
180–181	Tentative Unit Address	
182–183	0	
184–185	0	
186-217	0	

Table 11-5: Address Advertisement Message Format

Description

During auto-configuration, a device must send this message 100 times with 5-millisecond interval.

11.5 Address Conflict

CMC = 0x07

Parameters
None

Format

Frame Octets	Bits 0-7	
174	0	-
175	0x7	
176	0	0
177	0	
178–179	Destination Unit Address	
180–181	Source Unit Address	
182–183	0	
184–185	0	
186-217	0	

Table 11-6: Address Conflict Message Format

Description

This message must be sent to report an address conflict between two or more devices on network.

The message may use one of two allowed configurations:

- Destination Unit Address = Source Unit Address (default)
- Destination Unit Address = 0xFFFF

11.6 Neighbor Advertisement

CMC = 0x09

Parameters

- Symbolic name of device (string of octets)

Format

Frame Octets	Bits 0-7	
174	0	-
175	0x9	
176	Message Length	0
177	Message Length	
178–179	0xFFFB	
180–181	Source Unit Address	
182–183	0	
184–185	0	
186-217	Device Symbolic Name	

Table 11-7: Neighbor Advertisement Message Format

Description

Every device must send this message to all connected ports at 200 ms intervals to allow interested devices to retain updated information about network topology and configuration.

11.7 Add/Remove Link Record

CMC = 0x11

Parameters

- Link-To unit and component address
- Requested link parameters
- Optional Link parameters

Format

Frame Octets	Bits 0-7	
174	**0**	**-**
175	**0x11**	
176	**Message Length**	**0**
177	**Message Length**	
178–179	**Destination Unit Address**	
180–181	**Source Unit Address**	
182–183	**Destination Component Address**	
184–185	**Source Component Address**	
186-187	**Link-To Unit Address (2 octets)**	
188–189	**Link-To Component Address (2 octets)**	
190–191	**Requested Link Parameters (2 octets)**	
192…	**Optional Link Parameters (Up to 4090 octets)**	

Table 11-8: Add/Remove Link Record Message Format

Description

See section 8.2.

11.8 Establish/Drop Control Link

CMC = 0x13

Parameters

- Link-To unit and component address
- Requested link parameters
- Optional Link parameters

Format

Frame Octets	Bits 0-7	
174	0	-
175	0x13	
176	Message Length	0
177	Message Length	
178–179	Destination Unit Address	
180–181	Source Unit Address	
182–183	Destination Component Address	
184–185	Source Component Address	
186-187	Link-To Unit Address (2 octets)	
188–189	Link-To Component Address (2 octets)	
190–191	Requested Link Parameters (2 octets)	
192…	Optional Link Parameters (Up to 4090 octets)	

Table 11-9: Establish/Drop Control Link Message Format

Description

See section 8.3.

11.9 Read/Clear Link Table

CMC = 0x15

Parameters

- Clear Command (1 – clear, 0 - read)

Format

Frame Octets	Bits 0-7	
174	**0**	**-**
175	**0x15**	
176	**0**	**0**
177	**1**	
178–179	**Destination Unit Address**	
180–181	**Source Unit Address**	
182–183	**Destination Component Address**	
184–185	**Source Component Address**	
186	**Clear Command**	
187–217	**0**	

Table 11-10: Read/Clear Link Table Message Format

Description

See section 8.4.

11.10 List of Linked Components

CMC = 0x17

Parameters Link-To unit and component address for all components

Format

Frame Octets	Bits 0-7	
174	0	-
175	0x17	
176	Message Length	0
177	Message Length	
178–179	Destination Unit Address	
180–181	Source Unit Address	
182–183	Destination Component Address	
184–185	Source Component Address	
186-187	Link-To Unit Address 0	
188–189	Link-To Component Address 0	
190–191	Link-To Unit Address 1	
192–193	Link-To Component Address 1	
194…	So on…	

Table 11-11: List of Linked Components Message Format

Description

See section 8.4.

11.11 Read Link Parameters

CMC = 0x19

Parameters

- Link-To unit and component address

Format

Frame Octets	Bits 0-7	
174	**0**	**-**
175	**0x19**	
176	**0**	**0**
177	**4**	
178–179	**Destination Unit Address**	
180–181	**Source Unit Address**	
182–183	**Destination Component Address**	
184–185	**Source Component Address**	
186-187	**Link-To Unit Address**	
188–189	**Link-To Component Address**	
190–217	**0**	

Table 11-12: Read Link Parameters Message Format

Description

See section 8.5.

11.12 List of Link Parameters

CMC = 0x1B

Parameters

- Link-To unit and component address
- Requested link parameters
- Optional Link parameters

Format

Frame Octets	Bits 0-7	
174	**0**	**-**
175	**0x1B**	
176	**Message Length**	**0**
177	**Message Length**	
178–179	**Destination Unit Address**	
180–181	**Source Unit Address**	
182–183	**Destination Component Address**	
184–185	**Source Component Address**	
186-187	**Link-To Unit Address (2 octets)**	
188–189	**Link-To Component Address (2 octets)**	
190–191	**Requested Link Parameters (2 octets)**	
192…	**Optional Link Parameters (Up to 4090 octets)**	

Table 11-13: List of Link Parameters Message Format

Description

See section 8.5.

11.13 Set Routing Table

CMC = 0x31

Parameters

- Output port number (defines the affected routing table)
- Table Offset (points to the first record to be loaded)
- List of routing records consisting of pairs Input Port Number/Input Slot Number

Format

Frame Octets	Bits 0-7	
174	**0**	**-**
175	**0x31**	
176	**Message Length**	**0**
177	**Message Length**	
178–179	**Destination Unit Address**	
180–181	**Source Unit Address**	
182–183	**0**	
184–185	**0**	
186-187	**Output Port (2 octets)**	
188–189	**Table Offset (2 octets)**	
190–191	**Input Port 0 (2 octets)**	
192-193	**Input Slot 0 (2 octets)**	
194–195	**Input Port 1 (2 octets)**	
196-197	**Input Slot 1 (2 octets)**	
198–199	**Input Port 2 (2 octets)**	
200…	**So on…**	

Table 11-14: Set Routing Table Message Format

Description

See section 9.3.

11.14 Read Routing Table

CMC = 0x33

See section

- Output port number (defines the affected routing table)
- Table Offset (defines the starting record)
- Number of Records (defines the number of records to read)

Format

Frame Octets	Bits 0-7	
174	**0**	**-**
175	**0x31**	
176	**0**	**0**
177	**4**	
178–179	**Destination Unit Address**	
180–181	**Source Unit Address**	
182–183	**0**	
184–185	**0**	
186-187	**Output Port (2 octets)**	
188–189	**Table Offset (2 octets)**	
190–191	**Number of Records (2 octets)**	
192–217	**0**	

Table 11-15: Read Routing Table Message Format

See section 9.4.

11.15 Routing Table Data

CMC = 0x35

Parameters

- Output port number (defines the routing table)
- Table Offset (defines the starting record position)
- List of routing records consisting of pairs Input Port Number/Input Slot Number

Format

Frame Octets	Bits 0-7	
174	**0**	**-**
175	**0x35**	
176	**Message Length**	**0**
177	**Message Length**	
178–179	**Destination Unit Address**	
180–181	**Source Unit Address**	
182–183	**0**	
184–185	**0**	
186-187	**Output Port (2 octets)**	
188–189	**Table Offset (2 octets)**	
190–191	**Input Port 0 (2 octets)**	
192-193	**Input Slot 0 (2 octets)**	
194–195	**Input Port 1 (2 octets)**	
196-197	**Input Slot 1 (2 octets)**	
198–199	**Input Port 2 (2 octets)**	
200…	**So on…**	

Table 11-16: Routing Table Data Message Format

Description

See section 9.4.

11.16 Mute

CMC = 0x41

Parameters

- Output port number (defines the routing table)
- Table Offset (defines the starting records position)
- List of 32-bit masks

Format

Frame Octets	Bits 0-7	
174	**0**	**-**
175	**0x41**	
176	**Message Length**	**0**
177	**Message Length**	
178–179	**Destination Unit Address**	
180–181	**Source Unit Address**	
182–183	**0**	
184–185	**0**	
186-187	**Output Port (2 octets)**	
188–189	**Table Offset (2 octets)**	
190–193	**Mask 0 (4 octets)**	
194-197	**Mask 1 (4 octets)**	
198…	**So on…**	

Table 11-17: Mute Message Format

Description

See section 9.5.

11.17 Read Attribute

CMC = 0x51

Parameters

- Attribute address

Format

Frame Octets	Bits 0-7	
174	0	-
175	0x51	
176	Message Length	0
177	Message Length	
178–179	Destination Unit Address	
180–181	Source Unit Address	
182–183	0	
184–185	0	
186-187	Root sub-address (2 octets)	
188–189	Sub-address1 (2 octets)	
190–191	Sub-address20 (2 octets)	
192…	So on…	

Table 11-18: Read Attribute Message Format

Description

See section 10.3.

11.18 Attribute Value

CMC = 0x53

Parameters

- Attribute Value

Format

Frame Octets	Bits 0-7	
174	**0**	**-**
175	**0x53**	
176	**Message Length**	**0**
177	**Message Length**	
178–179	**Destination Unit Address**	
180–181	**Source Unit Address**	
182–183	**0**	
184–185	**0**	
186…	**Attribute Value**	

Table 11-19: Attribute Value Message Format

Description

See section 10.3.

Appendix A: Cyclic Redundancy Check

The following is an example of a CRC-32 generation function written in C:

```
/*
 * crc32h.c -- package to compute 32-bit CRC one byte at a time using
 *             the Big Endian (highest bit first) bit convention.
 *
 * Synopsis:
 *   void gen_crc_table (void):
 *      Generates a 256-word table containing all CRC remainders for
 *      every possible 8-bit byte. It must be executed (once) before
 *      any CRC updates.
 *
 *   unsigned update_crc (unsigned long crc_accum, char *data_blk_ptr,
 *                        int data_blk_size):
 *      Returns the updated value of the CRC accumulator after
 *      processing each byte in the addressed block of data.
 *
 * It is assumed that an unsigned long is at least 32 bits wide and
 * a char occupies one 8-bit byte of storage.
 *
 * The generator polynomial used for this version of the package is
 * x^32+x^26+x^23+x^22+x^16+x^12+x^11+x^10+x^8+x^7+x^5+x^4+x^2+x^1+x^0
 * as specified in the Autodin/Ethernet/ADCCP protocol standards.
 * Other degree 32 polynomials may be substituted by re-defining the
 * symbol POLYNOMIAL below. Lower degree polynomials must first be
 * multiplied by an appropriate power of x. The representation used
 * is that the coefficient of x^0 is stored in the LSB of the 32-bit
 * word and the coefficient of x^31 is stored in the most significant
 * bit. The CRC is to be appended to the data most significant byte
 * first. For those protocols in which bytes are transmitted MSB
 * first and in the same order as they are encountered in the block
 * this convention results in the CRC remainder being transmitted wit
 * the coefficient of x^31 first and with that of x^0 last (just as
 * would be done by a hardware shift register mechanization).
 *
 * The table lookup technique was adapted from the algorithm described
 * in Byte-wise CRC Calculations, Avram Perez, IEEE Micro 3, 4(1983).
 */

#define POLYNOMIAL 0x04c11db7L

static unsigned long crc_table[256];

void gen_crc_table()
  /*
   * Generate the table of CRC remainders for all possible bytes:
   */
{
        register int i, j;
        register unsigned long crc_accum;

        for (i = 0; i < 256; i++)
        {
```

```
          crc_accum = ( (unsigned long) i << 24 );
          for (j = 0; j < 8; j++)
          {
            if (crc_accum & 0x80000000L)
                crc_accum = ( crc_accum << 1 ) ^ POLYNOMIAL;
            else
                crc_accum = ( crc_accum << 1 );
          }

          crc_table[i] = crc_accum;
        }

        return;
}


unsigned long update_crc(unsigned long crc_accum, char *data_blk_ptr,
                         int data_blk_size)
  /*
   * Update the CRC on the data block one byte at a time
   */

{
        register int i, j;

        for (j = 0; j < data_blk_size; j++)
        {
          i = ( (int) ( crc_accum >> 24) ^ *data_blk_ptr++ ) & 0xff;
          crc_accum = ( crc_accum << 8 ) ^ crc_table[i];
        }

        return crc_accum;
}
```

Appendix B: Required Device Attributes

Root level attributes:

Address	Attribute	Type
0	Root Descriptor	Descriptor
1	Product/Device ID	Integer
2	Product/Device Name	Unicode string (16 symbols or less)
16	Vendor ID	Integer (uses only 24 bits)
17	Vendor Name	Unicode String (16 symbols or less)
32	Reserved for application specific device description (supported protocols)	Subtree
64	Device Status (Address)	Subtree
80	Network Ports	Subtree
84	Media Ports	Subtree
88	Components	Subtree
92	Media Slot Router	Subtree

Table 11-20: Required Root Level Attributes

Device Status:

Address	Attribute	Type
64.1	Unit Address	Integer (uses 16 bits)

Table 11-21: Required Device Status Attributes

Network Ports:

Address	Attribute	Type
80.1	MaGIC port 0 (OUT)	Subtree
80.2	MaGIC port 1 (IN0)	Subtree
80.3	MaGIC port 2 (IN1)	Subtree
80.4	So on	

Table 11-22: Required Network Ports Attributes

Network ports, Media Ports, Components, Media Slot Router:

To be defined.

Appendix C: References

1. IEEE 802.3 – 2002, Part 3: Carrier-sense multiple-access with collision detection (CSMA/CD) access method and physical layer specifications.

2. IEEE 802.2 – 1998, Part 2: Logical Link Control.

3. Copyright Law of the United States of America. 1992. http://www.loc.gov/copyright/title17/92chap10.html

4. AES Recommended practice for digital audio engineering – Serial transmission format for two-channel linearly represented audio data, AES3-1992 (r1997).

5. Byte-wise CRC Calculations, Avram Perez, IEEE Micro 3, 4 (1983).