Email This Letter

09 May 2007

Chuck Adams
IBM
North Castle Drive
Armonk, NY 10504
wcadams@us.ibm.com

Re: P1801 - Standard for Design and Verification of Low Power Integrated Circuits

Dear Chuck:

I am pleased to inform you that on 07 May 2007 the IEEE-SA Standards Board approved the above referenced project until 31 December 2011. A copy of the file can be found on our website at http://standards.ieee.org/board/nes/projects/1801.pdf.

Now that your project has been approved, please forward a roster of participants involved in the development of this project. This request is in accordance with the IEEE-SA Operations Manual, Clause 5.1.2i under Duties of the Sponsor which states:

"Submit annually to the IEEE Standards Department an electronic roster of individuals participating on standards projects"

For your convenience, an Excel spreadsheet for your use has been posted on our website at http://standards.ieee.org/guides/par/roster.xls. Please forward this list to me via e-mail at s.hampton@ieee.org no later than 05 August 2007.

Please visit our website, IEEE Standards Development Online (http://standards.ieee.org/resources/development/index.html), for tools, forms and training to assist you in the standards development process. Specifically for entity projects, please be aware that baseline entity sponsor procedures (http://standards.ieee.org/corpforum/cag/sponsor.html) and entity working group procedures (http://standards.ieee.org/corpforum/cag/wgproc.html) are available for your use. Guides to the policies and procedures of entity standardization can be found at http://standards.ieee.org/corpforum/participation/corpstdspandp.html.

You should also be aware that anyone who wishes to earn and maintain voting rights in an entity working group must pay an annual entity project participation fee. An initial roster of contacts who have

indicated an interest in becoming a voting member of the working group and who therefore should be invoiced for this fee shall be submitted to Lauren Suppa – Administrator, Business Development via email at l.suppa@ieee.org no later than two weeks from the date of this letter.

If you have any questions about the rules of entity project development, please contact Mary Lynne Nielsen at m.nielsen@ieee.org.

Also, we strongly recommend that a copy of your draft be sent to this office for review prior to the final vote by the working group to allow for a quick review by editorial staff before sponsor balloting begins.

If you should have any further questions, please contact me at +1 732 562 6003 or by email at s.hampton@ieee.org.

Sincerely,

Sherry Hampton
Administrator, Governance
Standards Activities
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CC: victorb@improvsys.com, stephen_bailey@mentor.com BCC: s.hampton@ieee.org, t.t.lee@ieee.org, m.kipness@ieee.org

PAR Request Date: 05 March 2007

PAR Approval Date: 07 May 2007

PAR Signature Page on File: Yes

Type of PAR: New IEEE Standard

Status: PAR for a New IEEE Standard

Root Project:

1.1 Project No.: **1801**

1.2 Type of Document: Standard

1.3 Life Cycle: Full-Use

1.4 Is this document in ballot now? No

2.1 Title
Standard for Design and Verification of Low Power Integrated Circuits

3.1 Working Group Name	UPF: Standard for Design and Verification of Low Power Integrated Circuits
Working Group Chair	Bailey, Stephen A Phone: 303-775-1655 Email: stephen_bailey@mentor.com
Working Group Vice Chair	Delp, Gary Phone: 1 507 289 7276 Email: gary.delp@gmail.com
3.2 Sponsor	IEEE-SA Board of Governors Corporate Advisory Group (BOG/CAG)
Sponsor Chair	Adams, Chuck Phone: 914-765-4382 Email: wcadams@us.ibm.com
Name of Standards Liaison Representative (if applicable)	
3.3 Joint Sponsor	IEEE Computer Society Design Automation (C/DA) Berman, Victor Phone: 978 927 0555 x 27 Email: victorb@improvsys.com

4.1 Type of Ballot: Entity

4.2 Expected Date of Submission for Initial Sponsor Ballot: August 2007

4.3 Projected Completion Date for Submittal to RevCom: February 2008

5.1 Approximate number of people expected to work on this project: 10

5.2 Scope: This standard establishes a format used to define the low power design intent for electronic systems and electronic intellectual property. The format provides the ability to specify the supply network, switches, isolation, retention and other aspects relevant to power management of an electronic system. The standard defines the relationship between the low power design specification and the logic design specification captured via other formats (e.g., standard hardware description languages).

5.3 Is the completion of this document contingent upon the completion of another document? No

5.4 Purpose: The standard provides portability of low power design specifications that can be used with a variety of commercial products throughout an electronic system design, analysis, verification and implementation flow.

5.5 Need for the Project: As electronics manufacturing process technology has advanced, power management has become a dominant factor in electronic system optimization. The industry has employed new design techniques to reduce static and dynamic energy consumption. These techniques are not possible to capture in existing standard hardware description languages such as SystemVerilog (IEEE Std-1800), Verilog (IEEE Std-1364) and VHDL (IEC/IEEE Std-61691-1-1) which support logic design specification but not the specification of low power design intent. The standard format replaces non-portable proprietary formats and eliminates the need for specifying the same information multiple times in non-standard formats -- a common source for errors in the design flow. The standard allows the electronics industry to design chips and systems that consume less power and generate less heat accruing economic and ecological benefits.

5.6 Stakeholders for the Standard: Electronics systems designers of systems-on-chips (e.g., networking and mobile communications), processor providers (e.g., servers and laptops), silicon vendors and manufacturers, providers of intellectual property and vendors of electronic design automation software all have a vested interest in an industry standard for low power design specification.

6.1.a. Has the IEEE-SA policy on intellectual property been presented to those responsible for preparing/submitting this PAR prior to the PAR submittal to the IEEE-SA Standards Board? Yes **Presented Date:** 2007-02-26
If no, please explain:

6.1.b. Is the Sponsor aware of any copyright permissions needed for this project? Yes
If yes, please explain: There are two low power formats that have been developed – Common Power Format (CPF) and Unified Power Format (UPF). Requests to assign copyright to the IEEE for the purpose of creating a single standard format have been made by the study group to the relevant organizations. The working group will create a single standard based on the technical contributions provided to the working group.

6.1.c. Is the Sponsor aware of possible registration activity related to this project? No
If yes, please explain:

7.1 Are there other standards or projects with a similar scope? No
If yes, please explain:

Sponsor Organization:
Project/Standard Number:
Project/Standard Date: 0000-00-00
Project/Standard Title:

7.2 Is there potential for this standard (in part or in whole) to be adopted by another national, regional, or international organization? ? Yes
Technical Committee Name and Number: IEC TC93 WG2
Contact person: Dennis B Brophy
Contact person Phone Number: 503-685-0893
Contact person Email Address: dennisb@model.com

7.3 Will this project result in any health, safety, security, or environmental guidance that affects or applies to human health or safety? No

7.4 Additional Explanatory Notes:

8.1 Sponsor Information:
Is the Scope of this project within the approved scope/definition of the Sponsor's Charter? Yes
If no, please explain: