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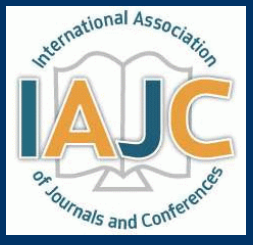

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The TECHNOLOGY INTERFACE INTERNATIONAL JOURNAL (TIIJ) is an independent, not-for-profit publication, which aims to provide the engineering technology community with a resource and forum for scholarly expression and reflection.

TIIJ is published twice annually (Fall/Winter and Spring/Summer issues) and includes peer-reviewed articles that contribute to our understanding of the issues, problems, and research associated with engineering technology and related fields. The journal encourages the submission of manuscripts from private, public, and academic sectors. The views expressed are those of the authors and do not necessarily reflect the opinions of TIIJ or its editors.

EDITORIAL OFFICE:

Philip Weinsier, Ed.D.
Editor-in-Chief
Office: (419) 372-0628
Email: philipw@bgsu.edu
Department of Applied Sciences
Bowling Green State University-Firelands
One University Dr.
Huron, OH 44839

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EDITOR'S NOTE:
THE TECHNOLOGY INTERFACE
INTERNATIONAL JOURNAL JOINS IAJC

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TIIJ is the Newest Member of the IAJC-owned Journals

After many successful years of service to engineering technology, and special thanks to former editor Jeff Beasley, the Technology Interface Journal sports a new name and joins the International Association of Journals and Conferences (IAJC). For the first published issue of the *Technology Interface International Journal* (TIIJ) since joining IAJC, the acceptance rate was just under 50%. We expect that future rates will continue to be in a range similar to what they had been over the journal's previous years, roughly 50%. Information about TIIJ can be accessed via the IAJC web site (www.iajc.org) or directly at www.tiij.org. TIIJ, like the other IAJC journals, is published both online and in print.

IAJC also Welcomes Three New Affiliate Journals

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IAJC would also like to welcome the following to its growing list of affiliate journals: The *International Journal of Engineering* (IJE), the *International Journal of Industrial Engineering Computations* (IJIEC) and the *International Transaction Journal of Engineering, Management, & Applied Sciences & Technologies* (ITJEMAST). With a total of 13 journals, authors now have a venue for publishing work across a broad range of topics.

IAJC-ASEE 2011 Joint International Conference

The editors and staff at IAJC would like to thank you, our readers, for your continued support and look forward to seeing you at the upcoming IAJC conference. For this third biennial IAJC conference, we will be partnering with the American Society for Engineering Education (ASEE). This event will be held at the University of Hartford, CT, April 29-30, 2011, and is sponsored by IAJC, ASEE and IEEE (the Institute of Electrical and Electronic Engineers).

The IAJC-ASEE Conference Committee is pleased to invite faculty, students, researchers, engineers, and practitioners to present their latest accomplishments and innovations in all areas of engineering, engineering technology, math, science and related technologies. Presentation papers selected from the conference will be considered for publication in one of the three IAJC journals or other affiliate journals. Oftentimes, these papers, along with manuscripts submitted at-large, are reviewed and published in less than half the time of other journals. Please refer to the publishing details at the back of this journal, or visit us at www.iajc.org, where you can also read any of our previously published journal issues, as well as obtain information on chapters, membership and benefits, and journals.

International Review Board

TIIJ is steered by IAJC's distinguished Board of Directors and is supported by an international review board consisting of prominent individuals representing many well-known universities, colleges, and corporations in the United States and abroad. To maintain this high-quality journal, manuscripts that appear in the *Articles* section have been subjected to a rigorous review process. This includes blind reviews by three or more members of the international editorial review board—with expertise in a directly related field—followed by a detailed review by the journal editors.

THE EVOLUTION OF VIRTUAL REALITY ENVIRONMENTS AND IMPLEMENTATION OF NEW TECHNOLOGIES: AN OVERVIEW OF THE CURRENT STATE OF RESEARCH

Kimberly James Nankivell, Purdue University Calumet

Abstract

The evolution and use of virtual reality environments (VREs) have coincided with the advancement in software and hardware technologies. These advancements in technologies have provided academia, business, and government new avenues for expansion with less expensive and more enhanced forms of VREs. This study sought to compile a review of available literature with respect to the implementation and usability of VREs, examining how the advances in these technologies have affected these environments. This review considers how these environments are being used and the nature of the institutions exploiting them. Further outlined is the newest research and the potentials this research is discovering. Subsequently, this study considered the legal, social, and political questions that the participants in VREs must address and concluded with what possible new technologies are being examined and opportunities for future research in these virtual reality environments.

Introduction

The use of virtual reality environments (VREs) in education, business, research, and government has increased substantially since the early introduction of the technology. Within the last decade the cost of the technologies to create VREs has become reasonable for many organizations and institutions. Prior to the advancement of these technologies, only those organizations and institutions which could afford the high-priced mainframe computers required to create these environments could implement them [1]. The original implementations of VREs were for simulations, engineering, and entertainment. The explosion in computer hardware and software technology over the past few decades brought with it an evolution in the functionality and availability of VREs.

The definition of VRE has matured with the evolution of the technologies such that a VRE is now defined as a computer-generated three-dimensional (3D) location, created by a virtual environment software package that can provide an interactive experience influenced by a user [2]. The user experience provided is one of interaction, immersion, and imagination combining simulation, multimedia functionality and artificial intelligence, experiences which are delivered over network technologies. The navigational systems within these VREs can be classified into two types. The first type employs immersive VREs that require various types of devices such as head-mounted displays, projection-based setting (CAVE), stereoscopic headsets, etc. The desktop virtual navigation system is the alternative and is the least expensive VRE approach that employs the display screen of the system to engage the user [3].

The introduction of Web 2.0 has seen an increase in deploying these environments. Virtual Reality Modeling Language (VRML) is currently the open source standard of choice for creating internet based virtual environments [3]. Interactive environments such as Second Life, Cyworld, and Entropia Universe are increasing in their popularity and usability as social platforms on the World Wide Web. These interactive worlds employ avatars, which are digital representations of the user, to provide the virtual presence to interact with other participants.

The current research into the implementations of VREs is on many fronts. The evolution of virtual environments coincides with research into the devices and technologies to increase the functionality of these VREs. Motion-capture systems, projection systems, and headset displays are just some of the fields of research. These types of technologies will enhance the interactivity and usability of such environments to customize VREs for such endeavors as training and social interaction [4].

The next section will detail the methodology used to examine the validity of the articles reviewed, including the rationale for including those articles reviewed for this study. The following section provides an overview of the types of VREs being employed and the various institutions and organizations which use these technologies. A review of the quantitative and qualitative research being conducted is presented, along with results and discussion on the literature review and conclusions drawn from this review.

Research Methodology

An empirical methodology was carried out for this overview in order to examine the current research on the topic. This review was designed to assist in identifying the issues, uses and solutions research has undertaken to better understand virtual reality environments (VREs) and provide the best methodologies to increase and improve the use of these environments.

One of the core purposes of this review was to create a valid and robust reference list to add to the credibility of the research. Each reference was evaluated using the following criteria: (a) the integrity of the author(s) and/or institution(s) where the research was performed along with a robustness and methodology that conforms to best practices, (b) whether the article was subjected to a peer-review process, (c) timeliness and relevance of the article, and (d) the diversity of the subject matter to current academic research was also considered carefully. Some anecdotal articles were also included as a means of providing richness to the content of the article.

Virtual Reality Environments

Historical Perspective

Virtual reality environments were once considered to be available only to those institutions and organizations that had access to large sums of money and mainframe computers. The environments were rudimentary in nature, with limited modeling technologies available for creating realistic environments and characters. The initial implementations of these VREs were for simulation, training and educational endeavors. The cost of these technologies was considered prohibitive for all but a few institutions. It was estimated that a quarter of a million dollars ($250,000 US) would be required to create a very limited set of networked virtual worlds Beyond the initial cost of the system to create a VRE, the usability of such systems was far from what would be required to facilitate the multiple methods of interaction required. The networking technologies inhibited the distribution of these VREs and limited the size and scope as well. The modeling software also was a hindrance to usability, providing only simple systems with counts under 10,000 polygons [5].

The research in the early 1990s recognized the need for advancements in technologies to overcome the impediments that hindered the use of VREs. It was suggested that lightweight, dynamic software programming would need to be developed to allow for fluid interaction of environments including advancements in collision detection, command structure and the user interface. It was also suggested that this dynamic software be developed specifically for VRE creation and implementation. Along with software improvements, devices needed to be developed to allow for more functional participation in immersive environments such as head-mounted displays, hand-held devices and motion-capture tracking devices [5], [6]. These initial implementations and recommendations provided the needed foundations for the research and advancements that has progressed to today.

Current VRE Implementation

These technologies have improved to the point where current VRE implementations can provide a wide variety of interactions, environments and characters, thus providing greater diversity in uses. Currently, VREs are far less expensive to implement than they were fifteen years ago. Current research indicates that a well-conceived VRE can be deployed on a high-end desktop computer or created over the internet using reasonably priced server technology [6]. This availability of affordable VREs has spawned growing implementation and research into evolving the medium.

The business community is realizing the benefits that virtual environments can provide through their implementations in production, marketing and communication. The use of a virtual production line at Deere & Company provides an example of the advantages that virtualization can provide. The company used a 3D computer model to recreate a parts production line, which then enabled investigation into how modifications to the production line would translate into enhanced parts production. This VRE, named VRFactory, proved that creating an immersive virtual production line allows for “the exploration of design changes and their effects on the simulation” [2].

The VRFactory as defined by Rehn et al. [2] was developed by modifying off-the-shelf software and hardware technologies. The final product referred to as Assembly Line Solution Set (ALiSS) incorporated four components, which created the functionality that was essential for the requirements outlined by Deere & Company. These components included a Graphics module that provided the means of displaying the 3D objects in the VRE, including the production line and parts. It also generated the user interface. The second component was a Data Processing module that handled the interpretation of the results of the simulations. A third component, the Logical module, was incorporated into ALiSS to establish and monitor the behavior of the virtual objects in the simulations. The final Interaction module was employed to provide the controls of ALiSS functionality [2]. The system was then deployed using a six-screen projection system to provide for full immersion for its users.

Prior to this implementation, the manufacturing industry was quite hesitant to employ these types of simulations or virtual production processes due to (a) time constraints for simulation development, (b) the cost of deploying effective simulation models, and (c) a lack of accessible real-time data of current production. These limitations were overcome by the development of the ALiSS system with its realized goals of (a) reduction in development time of the model, (b) the ability for non-specialists in simulations to perform investigations, (c) the transfer of results from simulation to actual production, and (d) the consistency of design of the final production line. The system was extensively tested and found to be extremely useful in evaluating prototype design and production-line processes [1]. This VRE allows a designer to run through a wide range of designs virtually and provides the stakeholders the opportunity to collaborate on the most appropriate direction to explore.

The increasing successful use of VREs within the business community has also expanded into the realm of online virtual worlds. The introduction of Second Life in 2003 by Linden Research, Inc. [7] marked the emergence of one of the most successful online virtual communities. Second Life, along with many other virtual communities (Entropia Universe, Cyworld, Active Worlds etc.), can be defined as virtual worlds (VW) or metaverses, which allow for a user to view alternate worlds via a computer screen or specialized goggles. The interaction within these alternate worlds is achieved by means of a digital representation in the form of an avatar [8]. These virtual worlds are a collaborative environment where one is able to experience the feeling of being physically connected with other individuals [9]. Along with the feeling of a physical presence, one is able to experience all forms of reality as diverse as eighteenth century London to a galaxy far into the future.

The avatar is the digital representation of the user and can have a distinct look and wardrobe, own its own property and make friends and associates. The communication can be by text and voice along with non-verbal gestures and expressions. The avatar (user) can, in many virtual worlds, create virtual business which can earn virtual money and the user can actually make a real-life living in the VW. The virtual money in many instances can be converted into real currency. The VW phenomenon not only has opportunities for individuals, but corporations, academic institutions, governments and researchers as well.

The Second Life Experience

The research community has taken a close look at Second Life (SL), which presently asserts a membership of over 13 million distinctive membership accounts with an in-world presence of over 680,000 in April of 2008 [8]. It has been reported that Second Life has claimed to have the first virtual millionaire with a convertible currency called the Linden dollar allowing for actual exchange of currency through the LindeX virtual stock exchange [10]. The SL community provides a foundation for making possible communication, entertainment and education, which has provided businesses and academia opportunities to provide virtual facilities and services that users are accustomed to in the real world.

Businesses have begun opening store fronts to provide virtual goods and services in a manner similar to real-world endeavors. Banks (Wells Fargo, for example) have established a presence in SL. Meta Bank is a totally virtual bank providing the same services that a real bank provides, such as loans for purchasing virtual property and saving accounts for accruing interest. The entertainment industry has also established a presence in SL with MTV building its own space or "island" called MTV's Virtual Laguna Beach. (Islands are virtual spaces that individuals or entities can purchase for development.) Advertisers are also moving into SL to take advantage of the media-rich environment of the VW [10]. These business activities have evolved to where many businesses are creating virtual space for training.

The nature of SL provides for free-form user-created content that can be manipulated to suit the needs of the creator. British Petroleum has embraced this functionality by recreating a gasoline storage and piping system representative of a typical gas station. This virtual gas station allows trainees to visually inspect the underground components of the station and observe the operation of the safety devices. This provides a unique perspective of an extremely complex system that could not be achieved in real life [9].

Galagan [9] also reports on IBM's incorporation of SL into its corporate structure with a variety of experimental ways of providing new experiences and training for its employees. It is reported that over 6,000 IBM employees log into SL each week to experience a wide variety of activities. These activities include training, conversations with customers and the holding of meetings worldwide. A unique aspect of using SL is the opening up of the IBM Island to retired IBM employees to chat and stay in contact with one another and current IBM employees. Advanced 3D voice capability has been incorporated into the IBM implementation to allow for a more natural and realistic means of communicating.

Customer feedback is another avenue that has been employed by businesses to better design and market its products, as suggested by Galagan [9]. Starwood Hotels prototyped versions of its new high-tech loft-like hotels, referred to as Aloft. As part of the design process, the company created various prototypes of the proposed hotel and requested feedback on the most desirable designs. The auto-

maker Pontiac has a space in SL where its engineers can chat with customers on design and engineering concerns. Many other institutions such as Cisco, the National Oceanic and Atmospheric Administration (NOAA), NASA and the Tech Museum of Innovation have incorporated SL into their organizational culture to further enrich and enhance the goals of their respective institutions.

Medical research and information technologists have embraced SL as an avenue for research, dissemination of knowledge and training. Delarge [8] researched a variety of opportunities available in the VW environment. He concluded that "the most compelling and unique applications were in the areas of education & training and research" [8]. Play2Train, Second Health London and Ann Myers Medical Center provided the best examples of virtual applications that mimic real-world environments within the medical community. Ann Myers Medical Center is a virtual medical center for experimentation in virtual training for First Life Medical and Nursing students in diagnostics and bedside manner. The National Health Service London has created Second Health Life as a means of distributing health-care information and medical-practice information in an efficient and innovative manner. It is suggested by Delarge [8] that these and other types of medical endeavors are ideally suited for the VW environments.

Educational institutions have established a presence in SL as extensions of their physical classrooms. Harvard Law School provides a portion of its CyberOne course on Second Life's Berkman Island. A combined political science and business course is offered by Emery University housed at SIMsim Island [10]. These universities, along with many others, are recognizing the value that a VW such as Second Life (SL) can provide in the educational process. Many institutions in fact have gone one step further and have provided facilities for researchers and staff to create their own virtual reality environments (VREs).

Institutionally-owned VREs

Young [11] examines several universities' innovative implementations of VREs as supplements to their traditional educational activities. Cornell University has created a virtual science museum called SciCenter where the laws of physics do not apply. This, as suggested by one its creators, Ms. Corbit, provides for an educational 3D world that acts like a video game and creates a rich environment for education. The University of North Carolina at Wilmington has begun using VREs as sites for virtual classrooms. The instructors using this technology have been impressed with the level of communication provided by the environments and the interactivity demonstrated by the learners. These virtual classrooms are housed in an expansive virtual three-story building which boasts an atrium and balconies for students to gather and relax. Assistant Professor of Education Gill observed that the students did remain in close proximity to one another, but when their avatars got too close or collided, the students demonstrated a sense of being offended for trespassing into their virtual space. The overall experience was extremely positive with the students attending the virtual classes more regularly than was experienced in previous physical classroom attendance.

The VREs have always been an integral component of the modern military establishment. The traditional use of VREs, and their related simulations as discussed by Stackpole [1], has been for battle-plan strategies, pilot training and weapons training. These traditional VREs are now included in even more realistic training for increasing the effectiveness and efficiencies in deploying and designing the ever-increasing complex military systems. The basic motivator for the increased use of these VRE technologies is to reduce cost and increase safety [11].

Virtual Reality Research

Virtual environments have been employed in the form of virtual laboratories for many years. The Virtual Laboratory (VL) has been used as an alternative to physical labs due to the lack of funds, physical space, and the threat of physical harm to the student [12], along with the lack of physical proximity of the student to the physical lab. These VLs have taken on many degrees of complexity from a simple simulation presented on a CD to a network-based VL providing remote access to a complete learning environment with user set-ups [13].

Virtual Laboratory

Some of the more notable projects using VL technologies are being done at Te´ le´ universite´ in Toronto, Canada, and Drexel University in Philadelphia, PA. VPLab is the name given to the Te' le' universite' project that provides a student with a virtual lab that is instinctive, enjoyable, and an interface that is interactive. This VPLab was designed to provide the learner with an appearance of a serious lab environment and not a video game. The interface offers eight sets of generic tools that can perform twelve physics experiments.

Once the prototype of the VPLab was finalized, the virtual lab was presented to 13 students to determine the perceptions and integrity of the system. The evaluation involved the collection of data in three phases: (a) a questionnaire gathering demographic information on the students familiarity with simulations and computer software; (b) a series

of lab exercises were required that were indicative of what a novice user would perform; and, (c) an exit interview with each learn to better comprehend the effectiveness of the VPLab.

The overall reaction by the students was quite favorable with many valuable elements mentioned. Though one of the many objectives of the project was to stay away from the appearance of the VPLab as a video game, many of the students stated otherwise. The positive reactions towards the VPLab outstripped the negative reactions. The availability of on-demand video clips of an actual experiment being performed was quite beneficial. The visual cues on the functionality of each virtual object were extremely helpful in conducting the experiments and added to the realism. The students emphasized the feeling of freedom and control within the VPLab [13]. Overall, the VPLab was considered a success with further refinements being proposed by the researchers.

A second deployment of a virtual laboratory was performed at Drexel University and the results of the deployment and research were reported by Leitner and Cane [14]. This virtual network lab (VNL) was conceived to provide online learners with the experience of an actual IT laboratory. The VNL was created to allow online learners the ability to carry out multiple IT experiments, including the configuration of a virtual network. The researcher augmented the VNL by employing the Blackboard system as a course management tool.

The VNL designers' approach was an open system which allowed the students to work within the environment and have input into the construction of the virtual network connections for access to the lab [14]. This approach allowed the students to choose the appropriate elements to build the laboratory environment from which to carry out the experiments. This open-format construction was closely watched by the instructor to coordinate the level of competency of each student, generating a greater degree of learning. The software packages chosen for the VNL were typical of real-world IT labs.

The VNL as reported by Leitner and Cane [14] was deployed on an existing server and was designed so that each course instructor could set up the components reflective of the course and experimental outcomes. This allowed for elements to be either open (those elements that the student could modify) or closed (those elements that the student had no control over). Once these components were established by the instructor, the student was instructed to perform the assignment. The addition of the Blackboard course management system provided the instructor with the capability of maintaining course control. The designers also incorporated a management system named DameWare, which enables the instructor to log in to the VNL systems and monitor the students' behavior.

The VNL system has been implemented and is in the early stages of its deployment but has not been evaluated with respect to learning outcomes. Leitner and Cane [14] are still working on more appropriate means of integrating the VNL into the IT curriculum. They are also contemplating utilizing this system in the classroom in addition to online learning.

Usability Research

Actual research into VREs has been somewhat sporadic, but the past few years have shown an increase which has stimulated the growth of these environments [6]. The usability of VREs is one area where research has had some impact, as demonstrated by the research performed by Schroeder, Heldal, and Tromp [15]. Their research article "The Usability of Collaborative Virtual Environments and Methods for the Analysis of Interaction" examined two methods of analyzing interaction within VREs. They suggest that problems do exist within these environments and these VREs are limited due to the available field of view, the interaction of objects, and the awkward tools for navigation and avatar gesturing.

Research in usability has been limited, as suggested by the Schroeder et al. [15] and is due to the immaturity and lack of VREs available for research. Thus, usability is one of the main issues directed at VREs and why many are reluctant to use them. To this end, the authors of "The Usability of Collaborative Virtual Environments and Methods for the Analysis of Interaction" took a comprehensive look at usability issues. The nature of this digital medium allowed for the capture of the interactions of the users, which provided for more reliable results. The major obstacles that were addressed in the research were (a) how to generalize the results to other VRE settings, (b) discovering patterns of the interaction that are common and unique, and (c) developing the proper method for analyzing and capturing the interaction [15]. The underlying goal of the research was to improve the usability of VREs. This was accomplished by focusing on the techniques for analyzing interaction within these environments.

Evaluating Sequence of Behavior

Categories of behavior. The research employed two methods for analyzing the interaction of participants within VREs. The first method was quantitative in nature, evaluating sequences of behavior within a group environment. The VREs were presented via the desktop technology. The first step in this approach was to establish a set of categories for

scoring the observed behaviors. Initially, twenty six categories were established that were reviewed by a panel of experts.

The review refined the categories to eight distinct variables to be analyzed. These eight categories were: (a) external events outside the VRE, (b) communication, (c) avatar gestures, (d) manipulation of the avatar, (e) navigation of the avatar, (f) positioning of the avatar, (g) viewing the environment, and (h) verify to activity. Within these categories there were between two and fifteen subcategories to better quantify the activities [15]. These categories were designed to focus the research on the behavior within a VRE during the acts of collaboration.

Analysis of interaction. This method analyzed a series of video recordings of participants interacting as they performed various tasks. The researchers then scored the interactions observed, based on the eight categories identified. This method permitted the researcher to follow a series of interactions in a very detailed manner. This, then, provided the opportunity to breakdown the types of actions that are performed during the interaction. An example of the data that this method generated was presented by the authors. The example detailed four trials involving three to nine participants and lasting a total of thirty two minutes. These observations generated 705 individual acts to be analyzed and categorized.

Conclusion on usability. Through this process a number of conclusions about how individuals interact within a VRE where developed. It was discovered that almost half (48.1%) of all acts were in the form of communication, with general communication accounting for 20.4 % and the balance, verifying the functionality of the VRE with fellow users. It was also determined that newer users communicate more often than experts and that experts scanned or viewed the environment more often. It was also observed that as a user navigates within the environment, there is less likelihood that he/she will communicate, as the focus is on navigation and not communication. The research was able to establish the time requirements for various acts performed within the VRE.

The actions that require the most time were communication, when they were done via text input. Navigation typically took between 1 and 2 seconds, except when the avatar was moving backwards and most other acts on average took about 1 second. Reaction times in communication were another area that demonstrated some interesting results. General, unfocused communication usually required about 5 seconds for a response. When the communication was a part of collaboration, the response time was much faster, within a range of 1 to 2 seconds.

Recommendations on usability. The results of the observed interactions produced a number of recommendations as advocated by Schroeder et al. [15]. The first of these recommendations was to fully or partially automate a regularly occurring task. A second recommendation was to develop a better instrument for providing feedback to other users and, finally, there needed to be an easier way to navigate to a particular position.

Benefits of method. The main benefit of this method is to provide other researchers a means of uniformly analyzing interactions within a VRE. The advantages of the methodology are (a) sequences can be categorized and inspected in detail, (b) correlation between activities can be identified and aligned, (c) length of specific activities can be established, and (d) the frequency of various activities can be established. There are, however, three main disadvantages that researchers must take into account when using this method of analysis. The time required to perform this type of analysis is quite extensive and should be considered when designing the research. There is also the problem of generalizability and whether the results from one VRE can be generalized to another. Finally, the qualitative elements of the users' experience are lost by reducing the data to its basic quantitative form. This loss of richness of the qualitative data can be problematic when the data is being reviewed by persons other than the ones that scored the activities.

Definition of collaboration. The second method explored in the research [15] expanded the model developed by Heldal in 2004, which attempted to identify those elements that support or disrupt the acts of collaboration by users. The elements that disrupt collaboration were identified as the lack of awareness of what others are doing, inadequate feedback from others on one's own actions, and the difficulty in seeing what others are actually seeing. The research was performed in an immersive projection environment (CAVE) and involved two sets of trials. The trials were distinct in that one paired strangers and the other paired friends to determine whether the disparate pairs would act differently in given collaborative situations.

Results of qualitative approach. The second method employed a qualitative approach to reviewing the actions of the paired participants. The research used video and audio recordings, questionnaires, interviews and real-time observation, which was quite similar to the first method. The results provided some insights into the collaborative nature of the paired participants along with observations related to those elements that disrupt collaboration. Perceptual issues were discovered when users were attempting to navigate within an environment where the horizon was indistinguishable. The user had difficulty recognizing various locations due to the bland horizon and often got lost. Interaction among the par-

ticipants was also quite revealing in that when collaborating the users respected each other's virtual space, but while navigating there tended to be a disregard for one another's space and at times participants would actually walk through the other's avatar.

The appearance of the avatars was only a concern when the participants were not actively involved in a specific task. The discussion about one another's appearance typically occurred early in a session or after a task had been completed. During the collaborative process, the focus was on the task with little concern about each other's avatar appearance. The treatment of the avatar was sometimes perceived as real, versus times when the avatar was ignored or was similar to the way objects were perceived. Depending on the objective of the task, participants would sometimes walk through an object as if it did not exist, while other times the object presented an obstacle to be dealt with.

The two methods were quite similar in their approach to analyzing the interactions of participants. The first method observed the actions of individuals as they navigated a VRE, while the second method focused on pairs of participants and how the pairs collaborated within a VRE. The research focused more on the methods employed, striving to established validity in this type of research. The research did generate a few recommendations for better usability within a virtual environment. The researchers provide additional suggestions for researchers as they investigate usability within a VRE. Schroeder et al. [15] suggest that one (a) think about what to study from the beginning, (b) plan the iterations of design, test, redesign and test considering the methods outlined in this current study, (c) focus on the specific aspects of behavior that are of interest, (d) use appropriate combinations of methods, and (e) evaluate the results to achieve logical suggestions for redesign [15].

Authoring Tools

The lack of virtual environments can be attributed to a combination of cost and the ability to program the interactivity into the environments. The cost for development of these environments has declined as the technology has increased, thus reducing one of the obstacles in creating VREs. The technical skills required to create a VRE are still one of the pervasive reasons why more VREs are not being developed [6]. The research conducted by Hendricks et al. [6] considers the conceptual creation of an authoring tool that will provide the novice with the ability to create and implement a VRE, which includes extensive interactivity. The proposed tool would expand on the Virtual Reality Meta Language (VRML), which is considered the 3D version of HTML. The authoring tool would provide "both novice and advanced users a single system on which to develop, with the opportunity for novice users to smoothly migrate to creating more complex applications" [6]. The research defines the framework for such an authoring tool.

Implementing VREs. The behavior and interaction of VREs can be implemented in one of two general ways. The first is behavior-based where the interactions of the objects are considered attributes of the objects. For example, an avatar runs according to the way the object is programmed and is programmed to know what to do in response to other objects. The second way is event-based where the interactions occur in the environment. These events are produced by the users' activity or are produced by a change in the state of the objects. Currently, the main development tools use one or a combination of both of these methods but do not provide the user support required for the novice to work with them effectively.

Prototype authoring tool. The ideal authoring tool, as prescribed by Hendricks et al. [6], would be useful not only for the advanced programmer but the novice as well. The system would (a) allow for a smooth transition of user support so that users with various levels of skills are able to work with the system, (b) the system should be able to produce, regardless of the expertise of the user, as complex a VRE as required, (c) the system should be able to produce a viable VRE in a short period of time, similar to the time is takes to produce a GUI application, and (d) the system should allow for deployment on any hardware or software platform including new technologies [6].

Their system would have three main features or modules interacting with one another in varying ways. The first module would be a Graphics module consisting of a world component and an objects component that are stored in the database. The world component controls the rendering of the objects in the database. The second module would comprise a Scripting interface for implementation of the scripting language of choice rather than relying on one specific scripting language. The final Events module would be responsible for coordinating the interactions within the environment. It houses the structures for attribute variables, actions and conditions.

The proposed generic authoring tool allows both the novice and advanced user the ability to create interactivity by specifying pre-defined event-action pairs provided by the system. The support system will allow the novice user to migrate to more complex actions as his/her expertise increases. The development time will be greatly reduced as the use of scripting languages will reduce the time spent on compiling and employing API code. Since the system is modular, various implementations of a module can be used. The scripting module, for example, could simultaneously run

both a portion of Python and JavaScript. The authors conclude that VRE authoring tools have increased in number and usability, but few have targeted the novice developer. The implementation of their meta-authoring system would assist in overcoming this problem and rapidly generate more VREs with richer content.

Implications for the Future

The development and implementation has been an ongoing process in the area of virtual reality environments. The term "Virtual Reality Environments" has evolved to represent a computer-generated 3D collaborative environment, where the user can interact and manipulate the environment. These environments are limited only by one's imagination where physics and the natural world can be modified. The potential for VREs is unlimited, providing distinct advantages over existing communication and interactive technologies. These 3D virtual environments, as suggested by Pekkola [16], have these distinct advantages: (a) a mutual understanding and sense of space, (b) a mutual perception of the presence of others through their avatars, (c) a commonality of the sense of time, (d) the ability to negotiate and communicate with others, and (e) a means of sharing models and objects in virtual space and collectively achieve understanding of activities [16].

The recent exponential growth of virtual worlds (VWs) such as Second Life demonstrates the realization by individuals, the private sector, academia and government sectors of the power of VREs. Individuals have embraced the entertainment and collaborative nature of these environments to the point where some are now making a living in these VWs. The private sector is expanding its operations into these worlds as well, establishing store fronts, meeting areas, research endeavors and marketing campaigns to take advantage of these new opportunities. Academia has also moved into these new environments to take advantage of the inexpensive virtual space available and the ability to communicate, educate and research within these environments.

As these VWs evolve, new issues arise that must be addressed. The ability of users to create and own objects has spawned the existence of virtual businesses. This rise in business activities has prompted governments to take a look at avenues for taxing these types of activities. Along with business activities, the very nature of owning property has created new questions that must be addressed legally. There are increasing concerns about such concepts as the legal definitions of intellectual property as created within these VWs [17]. The owners of these VWs also have to consider how they word their "terms of service" as a recent court case ruled against Second Life and its restrictive "terms of service" (ToS). In that case, a federal district court found that the Second Life's ToS was illegal in its strict ownership and participation requirements and awarded a substantial settlement to the plaintiff [18]. Virtual governments are now being created by the citizens of the VWs to establish laws by which the residence must abide.

Research in VREs has increased as the cost of creating, and expertise to develop, them has decreased. This research is delving into many arenas within the VREs, especially into the navigation, field of view, gesturing and mechanics of motion. There has been extensive research into the software applications that create these environments with an emphasis on ease of development. There has been widespread research into the hardware used in simulating, navigating and observing these environments.

Conclusion

There has been an ever-increasing amount of research into the VREs and the various ways that they can be used and exploited. The research efforts have mainly focused on the architecture, navigation and delivery of the VRE technology with minimal research into the social and legal aspects of these environments. Many institutions have become actively engaged in these VREs and many are exploring alternative uses for them. The potential of VREs has been recognized as a new source of research opportunities, which has prompted continued development in this area. There are justifiable arguments both for and against to the viability of these technologies, though it is imperative that research into the merits as a social, business, entertainment and educational tool be continued.

The continued growth in the software and hardware will also have a dramatic impact on the growth and acceptability of VREs in the future. As suggested by Bray and Konsynski [10], there are several interesting questions for researchers that include business theory, political systems and social interaction that provide a wealth of research opportunities. These new environments have demonstrated their current effectiveness, showing great promise, and should be explored with great vigor.

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Biographies

KIMBERLY JAMES NANKIVELL received his B.S. degree in Marketing from the University of Arizona, Tucson, Arizona, in 1974, a Masters degree in Information Technology from American Intercontinental University, Hoffman Estates, Illinois, in 2003 and a Ph.D. degree in Information Technology from Capella University, Minneapolis, Minnesota, in 2011. Currently he is an assistant Professor of Computer Graphics Technology. He can be reached at nankivel@purduecal.edu.

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DESIGN AND DEVELOPMENT OF A DURABILITY TESTING MACHINE

Bhargav Shah, Arizona State University; Sangram Redkar, Arizona State University

Abstract

This work presents the process of design and development of a durability testing machine, development of a statistical testing methodology and subsequent reliability testing results of surge brake assemblies used in commercial trailers. The surge brake assembly is a critical component of the trailer braking system that is actuated by the relative deceleration of the towing vehicle and trailer. The durability-testing machine used to test surge brake assemblies was designed and developed using state–of-the-art analysis and design software—Autodesk Inventor for CAD, MSC-ADAMS for dynamic analysis and MSC-NASTRAN for Finite Element Analysis (FEA). This durability testing machine can be used for accelerated life testing where, due to high speeds of operation, dynamic effects play a significant role. This machine was designed in such a way that it can withstand the alternating inertial loadings and continue to perform optimally and consistently over a useful operating life. This paper presents the mechanical and electrical design methodology, development and commissioning of this machine. It also outlines the statistical testing procedure for surge brake assembly and reliability testing results. The durability testing results for the surge brake assemblies can be used for reliability analysis, vendor comparison and component selection. It can also be used to identify the probable causes of failure of surge brake assemblies in the field.

Introduction

Durability is an ability to sustain and endure. Product or component durability means that the products or components should perform their intended function for the designed lifespan without failure. Durability is a critical parameter in the design process. It is also important to validate the product durability and specifications provided by the Original Equipment Manufacturer (OEM) through standardized testing procedures before the component is put into use. Depending upon the application, intended use, environment and expected reliability, there are various standards for durability testing such as DO 160E, MIL 810E and SAE J1153 [1], to mention a few.

The objectives and original contributions of this work are:
1. Design and develop a durability testing machine to test surge brake assemblies used in trailers. Using a practical design methodology, the specifications for surge brake testing were derived. The design parameters and constraints were finalized using preliminary testing. Various design alternatives were evaluated and the most appropriate design was finalized. This design was used to size various subcomponents using machine design principles [2], [3]. It should be noted that a twofold design approach was used: a) a strength-based design where the component is strong enough to withstand the load, and b) a deformation-based design where the component does not undergo deformation (either in static or dynamic conditions) that would affect the operation or performance of the machine. Finally, the durability testing machine was built and commissioned. Thus, the theoretical design was put into practice, refined and tested.

2. Establish a data analysis and test procedure for vendor comparison. The authors proposed a Weibull analysis for reliability studies and comparison. This provided a systematic practical approach to quantify and compare surge brake reliability.

The results of the durability testing can be used to conduct Failure Mode Effect Analysis (FMEA), reliability analysis, design validation, life-cycle analysis, and to study effects of varying operating conditions on the component performance [4]. The durability machine designed and developed in this work is versatile and can be used to test a variety of products/components such as trailer surge brakes, trailer suspension systems, hitch-ball and hitch-receiver assemblies.

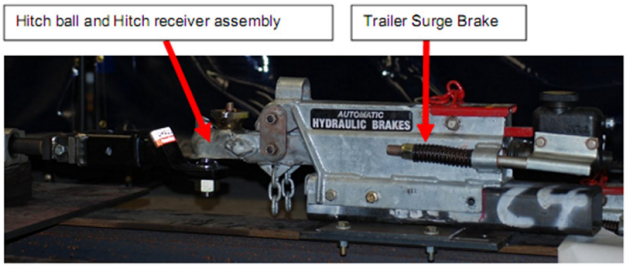

Figure 1. The surge brake

The surge brake (as shown in Figure 1) is a critical component of the trailer braking system that is actuated by the relative deceleration of the towing vehicle and trailer. The Society of Automotive Engineers (SAE) sets standards for all components in automobiles. SAE J1153 is the standard used for master cylinders in the braking system [1]. All of the surge brake OEMs are required to adhere to this stan-

dard. The SAE J1153 has parameters set for durability testing of master cylinders in the trailer braking system. These standards are set for cold-temperature and high-temperature durability.

A durability testing machine was designed to test the surge brakes. This machine has the following anticipated benefits/uses.

1. The durability testing will help analyze the quality of production parts. Products supplied by different suppliers can be easily accessed and compared with this test.
2. The machine can complete 500,000 cycles within 10 days. Data collected from this test will help in making future design changes to the products.
3. The machine uses a simple mechanical cam and cam follower mechanism for actuation. It is very flexible and can be used for durability testing of other products such as suspension springs, hitch-ball and hitch-receiver assemblies.
4. This durability test simulates forces experienced in real time and, hence, the data obtained will be very useful to simulate field failures.

Various types of computer software were used in this project. Autodesk Inventor was used to create 3D models. Microsoft Excel and Minitab were used to tabulate and analyze the data. The MSC ADAMS software was used to create a simulation model of the automatic surge brake system. In order to minimize the cost of the machine, commercial standard parts and in-stock components were used. The machinery handbook [2] was used as a standard guide for all of the part selections. Few specialized parts such as the cam shaft and cam were machined locally.

This paper presents the design of the machine, implementation and testing results, and is organized as follows: Section 2 presents the detailed design and development of the durability testing machine. Section 3 discusses the reliability analysis and vendor comparison case study. Finally, section 4 presents the conclusion.

Design of a Durability Testing Machine

The design and development of the durability testing machine involved various stages like developing preliminary specifications of the machine, conceptual design, mechanism design, dynamic analysis, machine component design, assembly, construction and testing. A conceptual mechanism initially proposed to actuate a surge brake is shown in Figure 2. This mechanism is a simple cam and roller follower. The surge is actuated with the forces generated by the follower. The cam is powered with an electric motor. The cam-follower returns back to its initial position with the help of return springs in the surge actuator. The efficient cycling of the surge brake depends greatly on the performance of the return springs. If the return spring does not return to its initial position, the cam follower will not be in positive contact with the cam and will damage the cam and cam follower over a period of time. The surge brake is linked to a hydraulic drum brake and the brake lines are filled completely with the brake fluid. The pressure maintained within the system should be within the OEM design specifications.

The surge action does not follow a straight line. The path followed by the surge action is an arc. As a result of this curved path, the mechanism needs to be designed such that path variations are allowed, thus a hinge is incorporated between the hitch receiver assembly and the cam follower. This hinge sustains significant vertical loads and protects the linear motion bearing from overload and wear. In order to actuate and test multiple surge brakes simultaneously and maintain dynamic stability, a symmetric actuation mechanism is desirable.

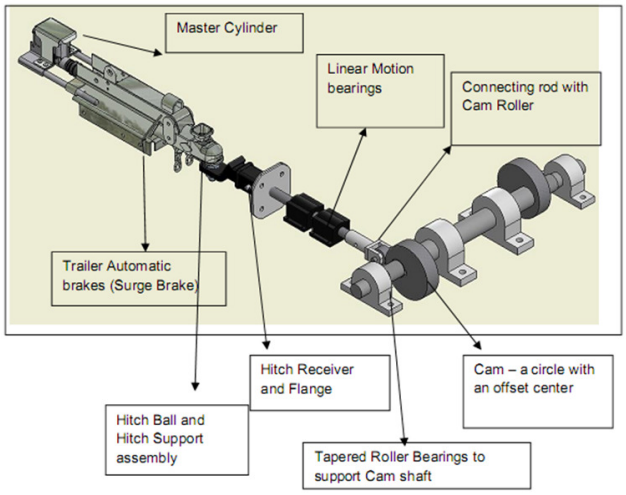

Figure 2. Conceptual design

Dynamic Analysis

In order to get the loads and toque requirements, a dynamic analysis was carried out. For dynamic analysis, a simple free-body diagram of the surge brake was drawn as shown in Figure 3. The simulation model was created in MSC-ADAMS based on this free-body diagram. All of the components except emergency springs were included in the simulation model.

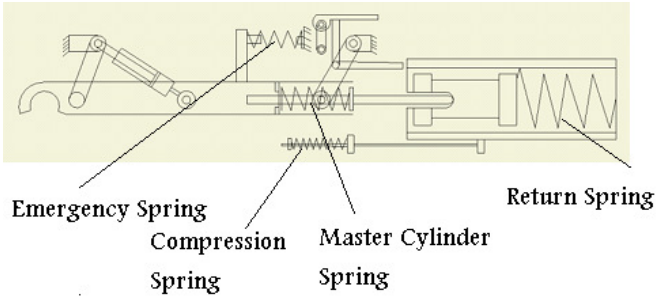

Figure 3. Free-body diagram

The surge brake actuates when there is an inward force. The surge returns back to its initial position with the help of return springs. The surge brake also has safety features to stop the trailer in case of disconnection from the towing vehicle. These emergency brakes are a set of compressed springs which are released when the emergency brakes are pulled. These compressed springs provide the energy to actuate the master cylinder and generate brake pressure. It should be noted that these springs are activated only in case of emergency and, hence, not included in the MSC ADAMS model.

The MSC ADAMS simulation model is shown in Figure 4. The purpose of this simulation was to get a better understanding of the dynamics of the surge brake action and compute forces and power required. These forces can be used for finite element analysis of the machine components.

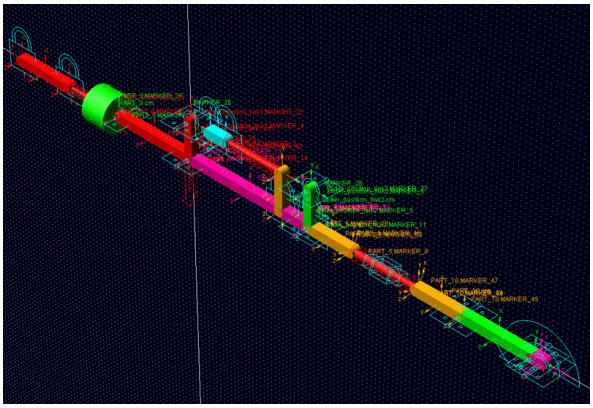

Figure 4. MSC ADAMS simulation model

The simulation model was comprised of the following springs:

- Compression spring
- Return spring
- Master cylinder spring

The sample simulation results are shown in Figures 5 and 6. The time step for simulation was 0.01 seconds. However, the results are plotted for 10-second intervals. Figure 5 shows the spring deformations corresponding to the compression spring (Spring 1), return spring (Spring 2) and the master cylinder spring (Spring 3). It should also be noted that spring displacements corresponded well with the data provided by manufacturer.

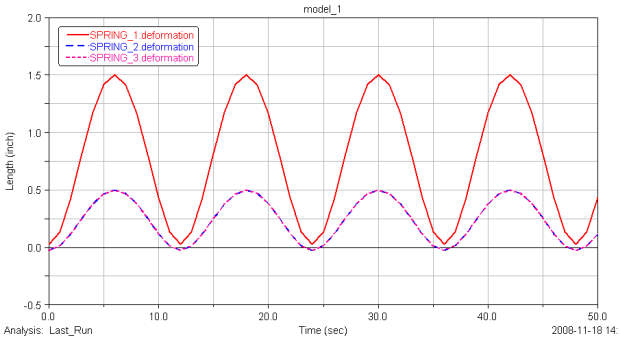

Figure 5. Spring deformation

The torque required to drive the surge brake assembly is shown in Figure 6. Here, MSC ADAMS simulations were carried out to get torque requirements for different types of surge brake assemblies with different springs and inertial properties at different operating speeds. This analysis helped to determine the maximum power required to operate the machine and motor selection.

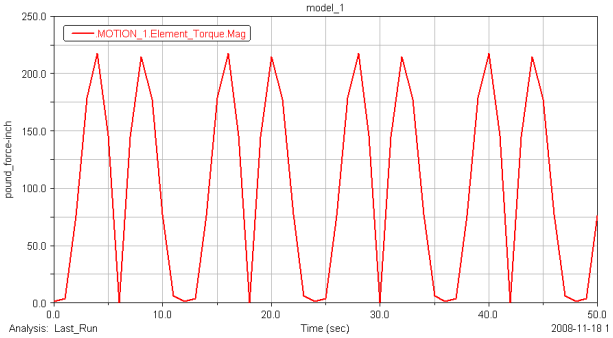

Figure 6. Torque requirements

A torque analysis was carried out for 1 surge brake assembly. In the initial design, the machine was anticipated to operate a minimum of 4 surge brakes at a time; hence, the total torque requirement would be 4 times (about 1000 lb.in).

Components of the Machine

Based on the requirement, cost and benefit analyses, the following components were selected for the machine.

NORD DRIVE SYSTEM:

A 5-horse-power Nord motor was selected to power this machine. The motor was coupled with a gear box with a double-sided solid-shaft output. The maximum output torque generated for this power plant was 9000in-lb at 35 rpm. Even though the maximum torque required was 1000lb-in, this drive system was selected as it was available in-stock and using this existing drive system would have lowered the cost of machine significantly. It was also envisioned that in case the durability machine were expanded to test more surge brakes at the same time, this power plant would be able to support the additional capacity.

YASKAWA VARIABLE FREQUENCY DRIVE:

A variable-frequency drive was used to control the speed of the motor. The variable-frequency drive controls the frequency of the alternating current. This, in turn, controls the output speed of the motor.

LINEAR MOTION BEARINGS:

Linear motion bearings were used to constrain the motion of the connecting rod to only one translation axis. These linear motion bearings were fixed into a fully enclosed and sealed pillow block to support them. They have recirculating roller bearings to improve the life of the bearings.

JAW COUPLING:

A jaw coupling was used to couple the output shaft of the motor with the camshaft assembly. This jaw coupling has two hubs with protruding jaws. These jaws overlap axially and interlock torsionally through a compliant insert of rubber or soft metal material. The clearances allow some axial, angular and parallel misalignment, but can also allow some undesirable backlash.

TAPERED ROLLER BEARINGS:

Tapered roller bearings are used to support the drive shaft. These bearings experience an alternating force of 1500lbs. The input force on the surge brakes is equivalent to the forces on these bearings. Tapered rollers bearings were chosen as they are capable of taking higher axial loads. These bearings have a longer life and are generally used in very high load applications. In this machine, each shaft was supported by two tapered roller bearings on either side of the cam.

LOAD RUNNER PLAIN YOKE STYLE:

A load runner rolls smoothly over the circumference of the CAM with minimum friction. The load runner can accept very high forces. The load runner was sandwiched between two metal pieces. It was held in position with a long shank bolt. The load runner has tapered roller bearings that can withstand radial forces.

The following components were specially designed for the machine.

1. Driveshaft and CAM assembly
2. Cam follower assembly
3. Cycle testing supporting structure

The driveshaft of the durability testing machine was one of the crucial components. It was subjected to high torques and bending forces. The output torque of the motor was 9000in-lb and shear force of 1500lbs. The shaft was attached to the cam. This cam generated the displacement to cycle-test the surge brakes. The cam was made of steel and had a diameter of 7.5 inches. The shaft was coupled to a 5hp motor. The shaft was coupled at one end with the output shaft of the motors gearbox. The shaft was held in position with the help of two heavy duty roller bearings with pillow blocks. The cam was placed between two pillow blocks. The heavy duty bearings gave good support to the shaft to reduce the deflection.

The design of the shaft was made based on the Machine Design Reference [3]; some of the crucial design factors were the diameter of the shaft, the dimensions and type of keyways used in the shaft. The calculations were based on the following procedures [3].

1. Shaft design for steady torsion and fully reversed bending
2. Shaft design for repeated torsion and repeated bending
3. Designing a stepped shaft to minimize deflection

The material selected for shaft design was steel 4340. It is a high-quality steel used generally for aerospace applications. The hardness level of the shaft was 40-45 Rockwell hardness on the ‘C’ scale. The driveshaft was designed to have very tight tolerances. The shaft drawing is shown in Figure 7.

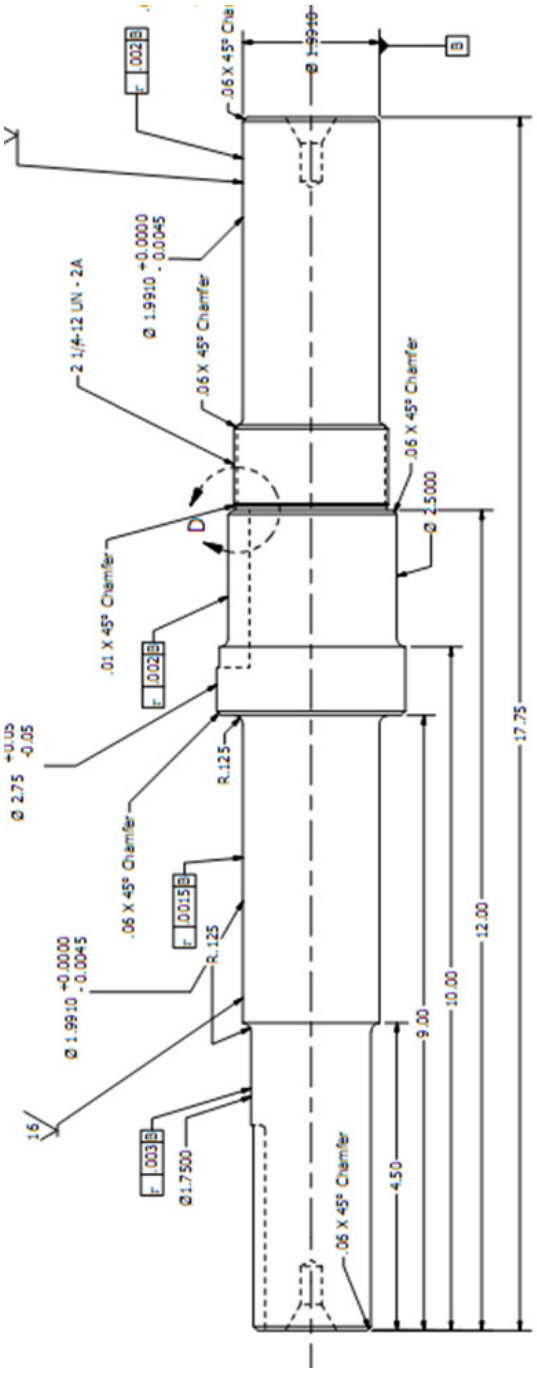

Figure 7. Driveshaft drawing

The cam designed was circular with an offset center. The final displacement achieved by the cam was equal to twice the offset. The cam was made using SAE HR 8617 Steel. The cam drawing is shown in Figure 8.

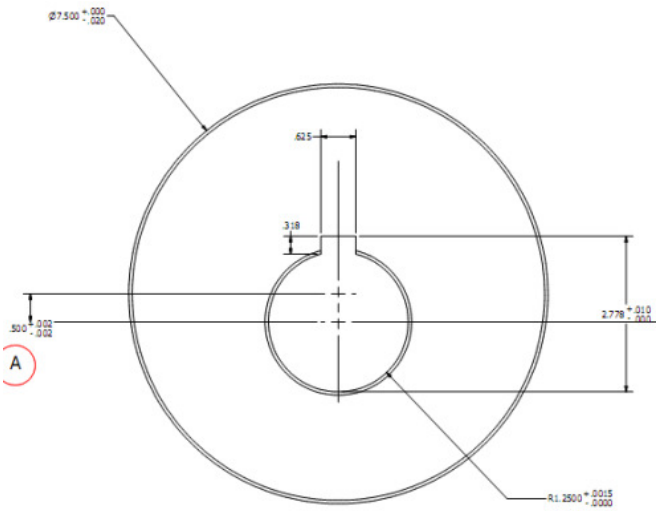

Figure 8: Cam drawing

The final assembly of the durability testing machine is shown in Figures 9 and 10.

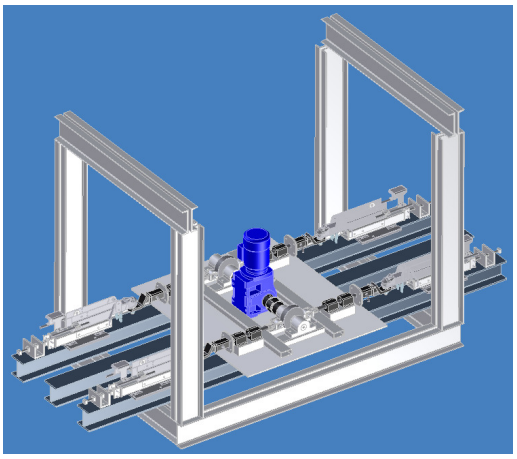

Figure 9. Durability testing machine model

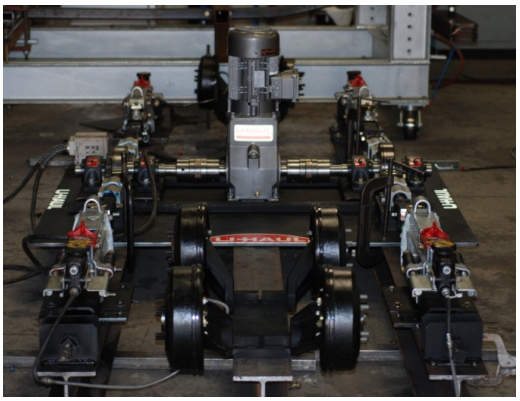

Figure 10. Durability testing machine assembly

Reliability Analysis

The purpose of the machine was to test the performance and durability of surge brakes. These surge brakes were supplied by several suppliers. In this section, a method for vendor comparison and selection is proposed. For durability or fatigue testing, one way to analyze the data is by plotting reliability curves [5]. Reliability can be calculated by plotting Weibull graphs [4, 6]. The Weibull distribution has been used extensively in reliability engineering as a model of time to failure for electrical and mechanical components and systems [6]. The Weibull method is also used for electronic devices such as memory elements and mechanical components such as bearings, structural elements in aircrafts and automobiles. Today most statistical packages offer simple ways to create the Weibull distribution and plot reliability graphs [7]. The two software packages used in this study are Minitab and Microsoft Excel.

The method for plotting a reliability curve in Excel is explained with a case study. Consider two suppliers for the surge brake assemblies. The company has to choose the supplier based on the quality of the surge brakes. Each supplier supplies ten complete surge brake assemblies. Ten surge brakes are cyclically tested in the durability testing machine where insufficient brake pressure is developed in the master cylinder at full stroke due to a variety of reasons (SR: Sluggish Response, SF: Spring Failure, SL: Seal Leakage, AJ: Assembly Jammed, OT: Other) as given in Table 1. Table 1 presents the Surge Brake Number, Cycles To Fail (CTF) and Primary Failure Cause (PFC).

Table 1. Surge brake test data

Surge Brake Number	Supplier A CTF	Supplier A PFC	Supplier B CTF	Supplier B PFC
1	400,000	AJ	280,000	SL
2	415,000	SF	320,000	AJ
3	500,000	AJ	375,000	SR
4	385,000	SF	390,000	OT
5	427,000	SL	410,000	SF
6	398,000	OT	435,000	SR
7	287,000	SL	485,000	SF
8	157,000	SL	490,000	AJ
9	293,000	OT	330,000	SR
10	370,000	SR	161,000	SL

It can be seen that, based on the data collected, it is difficult to predict the reliability directly. The data can be interpreted in a better way using the reliability graph. The Weibull analysis can be carried out using the procedure described by Dorner [8]. The Weibull reliability function [6] is given in equation (1).

$$R(t) = e^{-\left(\frac{t}{\alpha}\right)\beta} \tag{1}$$

Beta (β) is referred to as the shape parameter. If β is less than one, the failure rate is decreasing over time. If β is greater than one, the failure rate is increasing over time. If β is equal to one, the failure rate is constant over time. Alpha (α) is called the characteristic life. This is the value at which, when t = α, 63.2% of all Weibull failures occur regardless of the shape parameter.

The method of least squares was used to fit a straight line to a set of points in order to determine the estimates of the parameters of the two-parameter Weibull distribution [9]. A measure of how well a linear model fits the data was found using the correlation coefficient, denoted by ρ. It is a measure of the correlation between the median ranks and the data. Median ranks are values used to estimate the cumulative distribution function (CDF) for each failure (e.g., Bernards approximation MR = (j-0.3)/(N+0.4) where j is the rank failure position and N is the total number of failures observed).

The correlation coefficient, σ , was calculated using equation (2)

$$\rho = \frac{\sigma_{xy}}{\sigma_x \sigma_y} \tag{2}$$

where,

σ_{xy} is the covariance of x and y

σ_x is the standard deviation of x

σ_y is the standard deviation of y

The range of ρ is $-1 \leq \rho \leq +1$. Values of $\rho \geq 0.75$ are desirable. However, values of $\rho \geq 0.90$ are more desirable. A value of +1 is a perfect fit with a positive slope, while -1 is a perfect fit with a negative slope. When the value is closer to ±1, the paired values (x_i, y_i) lie on a straight line.

The reliability curves for suppliers A and B are computed via a Weibull analysis and are shown in Figure 11. ρ values for suppliers A and B are 0.86 and 0.82, respectively. For a detailed computation, one can refer to Shah [10]. Figure 11 shows the reliability comparison of suppliers A and B, where the number of cycles to failure are plotted against the percentage of population. The reliability curves for both the suppliers are parallel to each other. They have similar lower and upper reliability values but, in the intermediate section, supplier A has a higher reliability. Thus, it can be seen that supplier A is more reliable than supplier B.

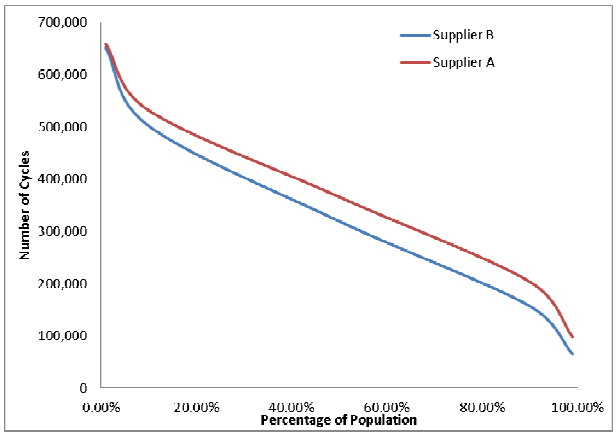

Figure 11. Reliability plot for suppliers A and B

Conclusion

In this work, design and development of a durability testing machine for surge brake was presented. This machine would be useful in analyzing the quality of the products supplied by the suppliers. This machine can not only be used to test surge brakes, master cylinders, leaf springs and other components which are part of the trailer suspension. In future work, the ADAMS simulation model will be refined so that performance of the assembly can be predicted in the simulation software and can be compared with experimental results.

Also presented here is a practical statistical approach to compare surge brake reliability based on a Weibull analysis. A case study was also presented that shows the vendor comparison procedure and its application. Using this statistical procedure, the suppliers can be compared more efficiently and in a cost-effective way. The data collected from testing can be used to analyze future master cylinder designs. The machine is now in operation and has completed over 700,000 cycles.

Acknowledgements

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Biographies

BHARGAV SHAH received his MS in Technology from Arizona State University in 2009. He may be reached at blshah@asu.edu

SANGRAM REDKAR is an assistant professor at Department of Engineering Technology at Arizona State University. He may be reached at sredkar@asu.edu.

DESIGN PROJECT BASED MODULES TO PROMOTE ENGINEERING LEARNING AND RETENTION

Shaobiao Cai, Penn State University; Yongli Zhao, St. Cloud State University

Abstract

Increasing retention among first year engineering students is one of the major goals in engineering education. There is evidence showing that learning experiences directly impact freshman retention. Among the many factors in engineering learning and retention, on which the educators may have influences, are student engagement, interest, academic success and, in particular, math performance. This study looked at the influences of implementing a fundamental active design project into a first-year engineering course on various learning indicators among engineering students, and identifying methodologies to make improvements. The implementation procedures are presented here. Evaluation of the results using faculty perception, student perception, and the design assessment rubrics are also discussed. It was found that the project enhanced and added a new dimension to this first engineering experience course. The students showed great interest, active participation, and developed positive aptitude in engineering learning through the project. It was observed that the students gained a better understanding of engineering ethics and concepts, and were more willing to acquire new knowledge independently. Students further exhibited a significant increase in confidence in learning engineering subjects.

Introduction

Learning and retention are among the major common issues in engineering education. Effective learning modules will help to promote retention. The retention addressed in this study was defined as the percent of students continuing in engineering from their freshman year to sophomore year. First-year freshman retention rates between 30% and 45% are typical for many universities, though it varies for specific programs. Increasing retention among first-year engineering students is one of the major issues in engineering education. For example, the statistical data among the commonwealth campuses at Penn State University shows that there are more than six hundred freshman students who declare engineering as their preferred major every year throughout the university's history. However, only about one-third remain in engineering, one-third pursue other STEM majors, and the last third drop out after two years [1]. The factors affecting the retention of engineering students vary. According to Penn State University's college of engineering, poor math performance is one of the major eliminating factors. Only about 61% of freshman students can pass the pre-calculus courses with a grade of C or better, which is required for engineering majors. Among underrepresented (African American, Native or Hispanic) freshman students who declare engineering as a major, only about 13% remain in STEM fields. Studies of this issue have been conducted by many educators and researchers on high-school academics performance and SAT scores [2-5], gender, ethnicity, citizenship status [6], and freshman year academic performance, especially grades in math and science courses [7], [8]. Good test scores and academic standing in high school and college are commonly used as indicators of success in engineering. However, engineering students may leave the field of study due to perception differences of the institutional culture and career aspects instead of academic performance [9]. Self-efficacy and physical fitness are also reported as positive predictors of freshman retention. Inability to handle stress, mismatch between personal expectations and college reality, and lack of personal commitment to a college education are also given as reasons for freshman attrition [10]. However, those studies are more focused on statistical data analysis.

In this current study, the authors present the implementation of strategies to actively change or impact students' attitudes and behaviors (which are believed to be important influence factors for promoting learning and freshman engineering student retention) regardless of their background. The active design learning modules were implemented at Penn State Hazleton, and evaluation rubrics were collaboratively developed at both Penn State Hazleton and St. Cloud State University. The learning modules were designed to engage students in science, mathematics, teamwork and communication skills in a fun, non-threatening environment. A first-year engineering design experience course was chosen as the medium, and toys were chosen as the "catalyst". Procedures were designed, evaluation techniques developed, various indicators implemented, and the results and observations were obtained and evaluated.

Project Implementation

Observations showed that a freshman student who is comfortable in learning engineering topics and actively participates in learning activities is not likely to leave the field of study after the first year. First-year engineering student retention can be affected by various complicated internal or external factors. Based on the experiences and observations

obtained, it is believed that among the "controllable" factors, student engagement, learning interest, confidence in studying, knowledge and understanding of engineering topics (for convenience, these are represented as the "Four-Element" indicators hereafter) will have a significant impact on learning engineering concepts and retaining first-year engineering students. A mechanism which can enhance these Four-Element indicators was expected to produce positive gains in retention. The following sections present the design, implementation and the effects of active design learning modulus in an introductory engineering course.

Course Identification

An introductory engineering course, EDSGN100, was used as the medium for studying the effectiveness of the learning modulus in enhancing student engagement, interest, confidence and knowledge and understanding. The reason for choosing this course was that it was required for all engineering students at Penn State Hazleton. This course provides students with experience in practicing fundamental engineering design processes, data processing skills and ethics through hands-on creative team work. The objectives of this course are: 1) Conceptually design a system, component, product, service, or process to meet desired needs, and understand solutions and designs in the context of overall systems; 2) Apply knowledge of basic science and mathematics to engineering; 3) Design and conduct basic experiments, as well as analyze and interpret data; 4) Participate effectively in small teams; 5) Identify, formulate, and solve engineering problems; 6) Communicate effectively using written and graphical forms and oral presentations; 7) Demonstrate professional and ethical responsibility; 8) Use software tools relevant to engineering practice. This course influences all aspects of the Four-Element indicators discussed in the previous section. Toys were identified as catalysts to bring a "FUN" component to the learning environment. The design project was implemented on a team basis and spanned the entire semester.

Project Design Learning Modules

The project was designed to meet the course educational objectives and enhance the Four-Element indicators. In order to meet these goals, the major activities and learning modules were carefully designed, as shown in Table 1. The concept of learning in a "FUN" environment was integrated into the identified course. The students were guided to complete the project and meet the goals, while having fun following the procedure shown below. The learning modules were integrated into the activities.

1) Assign the design project to the class.
2) Form small groups (2 to 4 persons each) in the class.
3) Determine a toy of interest under a given budget (each group was free to choose their toy).
4) Discuss decision-making strategies with the instructor to finalize the project idea.
5) Purchase product and tools needed for each team.

Table 1. Learning modules and objectives

	Objective Items	Learning Modules (Team Based)						
		Toy product examination (dissection, measurement, assembly…), new design concepts and solutions	Drawings and CAD modeling	Product fabrication (follow design processes)	Data processing	Design Documentation	Presentation	Report writing
Course objectives	1)	■		■		■		
	2)	■		■	■			
	3)	■			■			
	4)	■	■	■	■	■	■	■
	5)	■		■	■			
	6)					■	■	■
	7)	■	■	■	■	■	■	■
	8)		■		■	■	■	■
Four-Element Indicators	I_1	■	■	■	■	■	■	■
	I_2	■	■	■			■	
	I_3	■	■	■			■	
	I_4	■	■	■	■	■	■	■

(Note: In Table 1, course objectives 1 through 8 are those presented in the course identification section, where I_1 is Student Engagement, I_2 is Learning Interest, I_3 is Confidence, I_4 is Knowledge & Understanding.)

6) Test and examine the product and its functions. Document work done and relevant findings.
7) Dissect the product with tools, study how different parts are assembled, and how various functions are performed.
8) Conduct measurements with calipers and make working drawings.
9) Brainstorming for improvement and new product designs, document ideas with word expression and drawings, propose next stage work.
10) Give a presentation about their teamwork, product studying and proposal for next stage work in making improvement and fabrication.
11) Create CAD models (parts, assembly, and drawings) for the product to be done.

12) Fabrication and documentation of activities.
13) Test the new product, collect, analyze and interpret data.
14) Write a final report describing the whole design process, the effort, the work done above including product benchmarking, marketing and financial justification).
15) New product demonstration and final presentation.
16) Survey and peer evaluation.

When assigning the design project to the class, each team has the freedom to choose their own product and the option to redesign the product. All teams are required to follow the guidelines and document their activities throughout the entire project period (semester long). For instance, one team decided to work on a toy car. While they were working on the product, they came up with an idea to design a concept solar toy car (based on their interest). Figure 1 shows the three learning modules involved in the project: new product design (Figure 1a), computer modeling (Figure 1b), and professional presentation (Figure 1c).

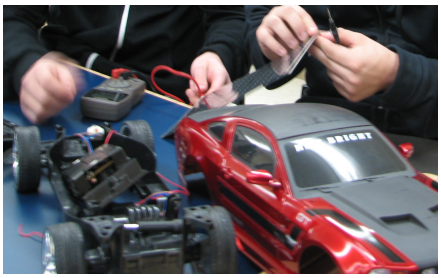

Figure 1a. Solar toy car development

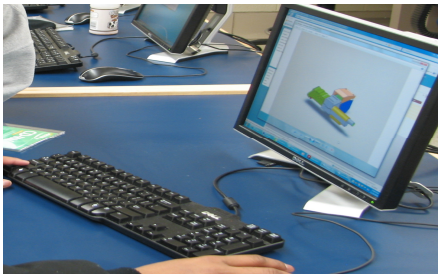

Figure 1b. 3D solid modeling with CAD software

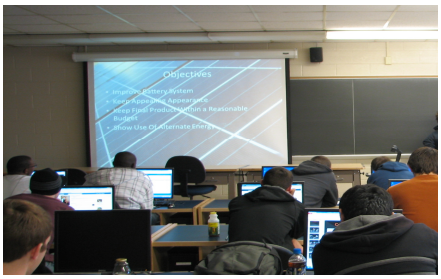

Figure 1c. Professional presentation

It is worth mentioning that during the project period, the students were guided to solve the problems they encountered, and no direct answers were given. For the example mentioned above, typical problems such as how the right type of solar panel could be identified, how the existing power system could be replaced, how the solar panel could be installed, and what should be done to solve the issue of a solar panel not directly running the motor, need to be solved in order to complete the project. It should also be noted that the answers to the questions involved an active learning process. The students were encouraged to conduct testing and data analysis, to use references and internet resources, and to consult engineering professionals other than the instructor to find out the answers. New supplies were provided based on their justified needs.

Evaluation and Assessment

In order to evaluate the effectiveness in the enhancement of student engagement, learning interest, confidence built and knowledge and understanding gained, three assessment techniques (namely, faculty perception, student perception and rubrics for quality work) and their relevant indicators were designed to make sure each outcome item could be evaluated sufficiently, and that all four items could be evaluated by each of the chosen three techniques to guarantee the effectiveness. The evaluation techniques and indicators are shown in Table 2.

Table 2. Evaluation techniques and their relevant indicators

Evaluation Techniques		Indicators used in Evaluation
1	Faculty perception	Attendance
		Answer and ask question
		Teamwork
		Attitude
		Working skills
		Independent study
2	Student perception	Self evaluation/survey
		Peer evaluation on teamwork and contributions
3	Assessment Rubrics (for quality work)	Report
		Presentation

The rubrics for evaluating the written report and oral presentation were also used. In the report evaluation rubric, visual quality, delivery of the report, content/correctness, and completeness were considered. In the oral presentation evaluation rubric, the items such as format and organization, content, PPT slide quality, and presentation skills were used to judge them.

Results and Discussion

The project was implemented in the EDSGN100 class beginning in Spring 2009 and ending in Fall 2010, a span of three semesters.

Table 3. Results and observations (I indicates evaluation techniques, and II represents indicators).

I	II	Results/Observations
Faculty perception	Attendance	Overall class attendance was about 92% to 95% during the project period, 85% in the other class time.
	Answer and ask question	The students were observed actively asking and answering questions. When answering questions, they exhibited confidence about the knowledge learned. Students could use equations and drawings to express the idea in addition to oral expression.
	Teamwork	The students collaborated well and efficiently. Seldom heard complains. They worked together with responsibility and respect, and actively engaged in completing a quality project. Good time management and communication skills were also observed. The students believed they could work in a team environment effectively by the end.
	Attitude	Teamwork, peer pressure, strict standards led to attitude change significantly. The students were able to do a objective self evaluation, were willing to take advices and suggestions from the others, and showed the willingness to learn.
	Working skills	The students understood and could follow the design procedures and requirements well. They could design methods to conduct testing, collecting data and perform analysis.
	Independent study	The students were required to obtain their own solution(s) or answer(s) for each task or a technical problem met before asking. They showed good independent study ability.
Student perception	Self evaluation /survey	Average 92% of the students expressed that the project was interesting. They believed that it made the engineering design concepts easy to understand, and helped them to develop skills in teamwork, report writing and presentation, helped them to gain first engineering experiences and to better understand the field of study, helped in building confidence in studying. 95% students indicated that they will continue in the field of study and plan to get the degree in engineering.
	Peer evaluation on teamwork and contributions	Peer evaluation was given to students to evaluate the contribution and performance of the others in the group for the project. The evaluations were all positive (students who dropped the class for various reasons were not included).
Assessment Rubrics	Report	It is observed that the students could follow the requirements and do quality work. The reports were scored between 85% and 95% using the rubric.
	Presentation	Rubric was applied. The students could follow and meet the requirements, and more than 80% can do better than what are required. Students could make PPT slides with good quality, show good presentation skills, demonstrate knowledge learned, discuss and answer questions confidently.

The implementation of the active design learning modules lead to a significant increase in student engagement, learning interest, confidence, and knowledge and understanding of basic engineering principles. The first-year engineering freshman retention rates in 2009 and 2010 were all at 98%. Though many factors may have contributed to these achievements, the positive impact of the project was observed.

Conclusion

Active design learning modules were incorporated into an existing first engineering design experience course. The design components introduced students to engineering ethics, design process and prototyping through products that everyone uses, such as toys. The students explored the design process through dissection and design or redesign, using drawing techniques and CAD tools, prototyping of a new design, field-testing, teamwork, writing a technical report, and giving presentations. The project enhanced and added a new dimension to this first engineering design experience course. The students showed high interest, active participation, and developed positive engineering aptitude in learning and doing their work. It was observed that the students gained a better understanding of engineering ethics, engineering design process, and gained necessary skills in technical report writing and oral presentation. It was shown that the students had increased understanding in the field of study, and increased confidence in learning engineering topics. Good retention rates were achieved. It is believed that this is partially due to the contribution of the project. It is believed that a freshman student with interest, confidence, good participation, performance in learning, and good understanding in the field of study is likely to remain in the field of choice for the second year.

Acknowledgement

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Biographies

SHAOBIAO CAI is an assistant professor in Mechanical Engineering and General Engineering in Alternative Energy and Power Generation at Penn State University Hazleton campus. Dr. Cai may be reached at quc13@psu.edu

YONGLI ZHAO is an assistant professor in Mechanical and Manufacturing Engineering at St. Cloud State University. Dr. Zhao may be reached at yzhao@stcloudstate.edu

FINDING THE EXACT MAXIMUM IMPEDANCE RESONANT FREQUENCY OF A PRACTICAL PARALLEL RESONANT CIRCUIT WITHOUT CALCULUS

Kenneth V. Cartwright, College of The Bahamas; Elton Joseph, College of The Bahamas; Edit J. Kaminsky, University of New Orleans

Abstract

A practical parallel resonant circuit has a resistor in series with an inductor, and that combination is in parallel with a capacitor. For such a circuit, it is well known that there are two possible definitions for the resonant frequency: (i) the resonant frequency f_p, which is the frequency at which the phase of the total impedance is zero, and (ii) the resonant frequency f_m, which is the frequency that achieves maximum magnitude of the total impedance. To find the latter traditionally requires calculus. However, in this paper, the authors show how f_m can be found exactly without using calculus. By modifying a formula that is given as an approximation to f_m in a popular technology textbook, an improvement in the accuracy of the approximation was achieved. Furthermore, a novel expression for the exact maximum impedance, as a function of $Q = \sqrt{L/C}/R$. was derived. This has been approximated by previous authors as RQ^2 for $Q \geq 10$. However, in this report, the authors show that this approximation has a percentage error less than -2% for $Q \geq 5$, and less than -10% for $Q \geq 2$. Furthermore, it can be shown that the maximum impedance is also accurately approximated by $R\sqrt{Q^2\left(1+Q^2\right)}$, which has an excellent percentage error performance, even for $Q = 1$, with a percentage error of only -4% for this value, and less than -0.6% for $Q \geq 1.5$. Finally, the authors used PSpice simulations to verify their results.

Introduction

The parallel resonant circuit of Figure 1 is used in many technology texts. However, the parallel resonant circuit of Figure 2 is of more concern in practice. This is because it is virtually impossible to build a coil without resistance, which is represented by the resistor R in Figure 2. Hence, Figure 2 represents a practical parallel resonant circuit, whereas Figure 1 depicts the ideal case.

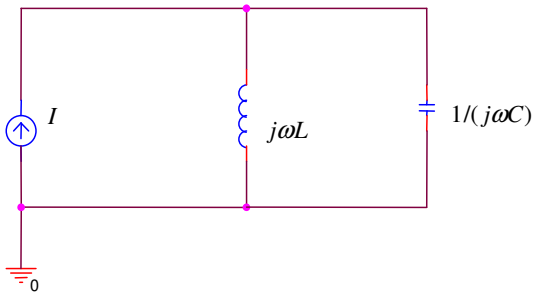

Figure 1. An ideal parallel resonant circuit

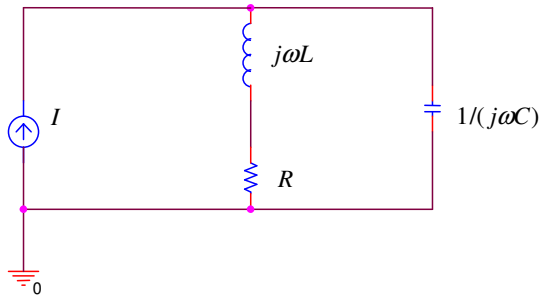

Figure 2. A practical parallel resonant circuit

Boylestad [1] is one technology author who considers Figure 2 in detail. He identifies two possible definitions for the resonant frequency:

(i) the resonant frequency f_p, which is the frequency at which the phase of the impedance of Figure 2 is zero, and

(ii) the resonant frequency f_m, which is the frequency for which the magnitude of the impedance is a maximum.

For completeness, $f_p = f_o\sqrt{1-\frac{1}{Q^2}}$, where $f_o = \frac{1}{2\pi\sqrt{LC}}$ was used in this report. Also, the derivation of f_p does not require calculus and is the same as that used by Boylestad [1]. On the other hand, the conventional method of finding f_m requires calculus [2]. However, the purpose of this paper is to show how this can be done without calculus. Interestingly, the authors found no engineering technology author who provided an exact equation for f_m. Boylestad [1] uses

$f_m = f_o\sqrt{1-\frac{1}{4Q^2}}$. However, as shown here, this equation is actually an approximation to the exact maximum impedance resonant frequency, f_m, which is derived here.

Furthermore, using the equation for the maximum impedance resonant frequency, a novel expression for the exact maximum impedance magnitude, as a function of Q can be derived. This has been previously approximated by other authors as RQ^2 for $Q \geq 10$. However, the authors show that this approximation is useable for smaller Q values: indeed, the aforementioned approximation has a percentage error less than -2% for $Q \geq 5$, and less than -10% for $Q \geq 2$. Additionally, it can be demonstrated that the maximum impedance is better approximated by $R\sqrt{Q^2\left(1+Q^2\right)}$. In fact, this approximation has an excellent percentage error performance: for $Q \geq 1.5$ it is less than -0.6% and for $Q = 1$ the percentage error is only -4%. Furthermore, the authors used PSpice simulations to confirm their results.

In the discussion above, the observant reader would realize that the definition of Q was neglected, which is the quality factor of the coil. In this paper, in order to get results consistent with Walton's [2], $Q = \sqrt{L/C}\,/\,R.$ was used. However, it should be noted that other authors might use $Q_p = 2\pi f_p L/R.$ Hence, the reader needs to exercise caution when reading the literature. Fortunately, using $f_p = f_o\sqrt{1-\frac{1}{Q^2}}$, it is easy to show that there is a simple relationship between the two, i.e., $Q = \sqrt{Q_p^2+1}.$ Clearly, for large values of $Q_p, Q \approx Q_p.$

The authors would also like to point out that for most practical situations in electrical engineering or engineering technology, such as communication systems, $Q \geq 10,$ as pointed out by Beasley and Miller [3]. Also, electrical engineering technology textbooks generally analyze the circuit of Figure 2 quite well for $Q \geq 10.$ However, there are practical systems in electrical engineering technology for which $Q < 10.$ For example, the ultra wideband FM demodulator [4] requires a practical parallel resonant circuit with $Q = 2.5.$ Also, traffic detection loops have the equivalent circuit of Figure 2, where Q values can be as low as 5, according to Klein et al. [5]. Hence, it might be important that electrical engineering technologists understand the circuit of Figure 2 for low values of Q as well. In this paper, the authors show how the practical parallel resonant circuit of Figure 2 can be analyzed, even by the electrical engineering technology student who has not yet had the opportunity to study calculus.

Impedance of the Practical Parallel Resonant Circuit

In this section, an expression for the impedance of the circuit in Figure 2 is derived. In order to do this, many authors, including Boylestad [1], first convert Figure 2 to an equivalent parallel *RLC* circuit. However, in this paper, the authors follow Walton [2] and work directly with Figure 2. Indeed, the impedance of this circuit is given by

$$\begin{aligned} Z &= \frac{\left(R+j\omega L\right)\frac{1}{j\omega C}}{R+j\omega L+\frac{1}{j\omega C}} = \frac{R+j\omega L}{j\omega RC + j^2\omega^2 LC + 1} \\ &= \frac{R+j\omega L}{j\omega RC - \omega^2 LC + 1}. \end{aligned} \tag{1}$$

From equation (1), the magnitude of the impedance is easily found to be

$$|Z| = \sqrt{\frac{R^2+(\omega L)^2}{\left(\omega RC\right)^2+\left(1-LC\omega^2\right)^2}}. \tag{2}$$

In principle, it is possible to find the maximum impedance resonant frequency f_m from equation (2) using calculus. However, the math is less tedious if f_m is found from the square of equation (2), i.e., from

$$|Z|^2 = \frac{R^2+(\omega L)^2}{\left(\omega RC\right)^2+\left(1-LC\omega^2\right)^2}. \tag{3}$$

Furthermore, as with Walton [2], it will be convenient to write equation (3) in terms of the square of the normalized frequency x, which is defined to be

$$x = \left(\frac{\omega}{\omega_0}\right)^2 = \left(\frac{\omega}{\frac{1}{\sqrt{LC}}}\right)^2 = LC\omega^2. \tag{4}$$

Substituting equation (4), $\omega^2 = x/LC,$ into equation (3) yields

$$|Z|^2 = \frac{R^2 + \frac{Lx}{C}}{\frac{R^2Cx}{L} + (1-x)^2} = \frac{R^2\left(1 + \frac{Lx}{R^2C}\right)}{\frac{R^2Cx}{L} + (1-x)^2}. \quad (5)$$

Recall that the quality factor of the coil is (by definition) $Q = \frac{\omega_0 L}{R} = \frac{1}{R}\sqrt{\frac{L}{C}}$. Hence,

$$Q^2 = \left(\frac{\omega_0 L}{R}\right)^2 = \frac{L}{R^2C}. \quad (6)$$

Substituting equation (6) into equation (5) gives

$$|Z|^2 = \frac{R^2(1 + Q^2x)}{\frac{x}{Q^2} + (1-x)^2}. \quad (7)$$

Multiplying both the numerator and denominator of equation (7) by Q^2 results in

$$|Z|^2 = \frac{R^2Q^2(1 + Q^2x)}{x + Q^2(1-x)^2}. \quad (8)$$

Finally, dividing both sides of equation (8) by R^2 gives

$$\begin{aligned} \frac{|Z|^2}{R^2} = S &= \frac{Q^2(1+Q^2x)}{x + Q^2(1-x)^2} \\ &= \frac{Q^2(1+Q^2x)}{Q^2x^2 - (2Q^2 - 1)x + Q^2} \\ &= \frac{Q^2x + 1}{x^2 - (2 - 1/Q^2)x + 1}. \end{aligned} \quad (9)$$

Note that in equation (9), S is defined as $\frac{|Z|^2}{R^2} = \left|\frac{Z}{R}\right|^2$, i.e., the square of the magnitude of the normalized impedance.

Maximum Impedance Resonant Frequency

Now that it has been established how the magnitude of the impedance of the practical parallel circuit is changing with frequency, one is in a position to find the frequency at which the maximum impedance magnitude occurs. The conventional way of doing this is with calculus; however, as stated earlier, the purpose of this paper is to show how this can be done without calculus, which will now be addressed in this section.

In order to find the maximum of equation (9) without calculus, by using the authors' method, equation (9) will have to be manipulated into the form $S = \frac{Ay}{By^2 + Cy + D}$, where A, B, C, D are constants, i.e., do not depend upon the square of the normalized frequency, x, whereas y is indeed a function of x.

To do this, let $y = x + \frac{1}{Q^2}$. Hence, equation (9) becomes

$$\begin{aligned} S &= \frac{Q^2\left(y - \frac{1}{Q^2}\right) + 1}{\left(y - \frac{1}{Q^2}\right)^2 - \left(2 - \frac{1}{Q^2}\right)\left(y - \frac{1}{Q^2}\right) + 1} \\ &= \frac{Q^2y}{y^2 - \frac{2}{Q^2}y + \frac{1}{Q^4} - \left(2y - \frac{1}{Q^2}y - \frac{2}{Q^2} + \frac{1}{Q^4}\right) + 1} \\ &= \frac{Q^2y}{y^2 - \left(2 + \frac{1}{Q^2}\right)y + 1 + \frac{2}{Q^2}}. \end{aligned} \quad (10)$$

Note that equation (10) is now in the required form, from which the maximum value of equation (10) is easily found without calculus, as will now be shown.

Equation (10) must first be rewritten as

$$\begin{aligned} S &= \frac{Q^2}{y + \frac{1 + \frac{2}{Q^2}}{y} - \left(2 + \frac{1}{Q^2}\right)} \\ &= \frac{Q^2}{\left(\sqrt{y} - \frac{\sqrt{1 + \frac{2}{Q^2}}}{\sqrt{y}}\right)^2 + 2\sqrt{1 + \frac{2}{Q^2}} - \left(2 + \frac{1}{Q^2}\right)}. \end{aligned} \quad (11)$$

However, equation (11) can be written as

$$S = \frac{a}{b + c}, \quad (12)$$

where,

$$a = Q^2, b = \left(\sqrt{y} - \frac{\sqrt{1+\frac{2}{Q^2}}}{\sqrt{y}} \right)^2 \text{ and } c = 2\sqrt{1+\frac{2}{Q^2}} - \left(2+\frac{1}{Q^2}\right).$$

For equation (12), please note the following:

(i) a is a positive number that is not a function of frequency,

(ii) c is a positive number for $Q > 1/2$ (please see Appendix A for a proof of this) that is not a function of frequency, and

(iii) b is a non-negative number, i.e., $b \geq 0$, and is a function of frequency.

Hence, to maximize equation (12) with respect to frequency only requires that b is properly chosen (a and c are independent of frequency). In fact, to maximize equation (12) with respect to frequency requires that the denominator of equation (12) be minimized, and in order to do the latter requires that $b = 0$ as c is a positive number. However,

$$b = \left(\sqrt{y} - \frac{\sqrt{1+\frac{2}{Q^2}}}{\sqrt{y}} \right)^2 = 0 \text{ requires that } y = \sqrt{1+\frac{2}{Q^2}} \text{ or } x = \sqrt{1+\frac{2}{Q^2}} - \frac{1}{Q^2}.$$

Therefore,

$$\left(\frac{\omega_m}{\omega_0}\right)^2 = \left(\frac{f_m}{f_0}\right)^2 = \frac{-1}{Q^2} + \sqrt{\frac{2}{Q^2}+1}. \quad (13)$$

Solving equation (13) gives the maximum impedance resonant frequency as

$$f_m = f_o \sqrt{\frac{-1}{Q^2} + \sqrt{\frac{2}{Q^2}+1}}. \quad (14)$$

Fortunately, equation (14) is the same expression that is derived with calculus as given by Walton [2].

Furthermore, in order for equation (14) to be valid, one must have $\frac{-1}{Q^2} + \sqrt{\frac{2}{Q^2}+1} \geq 0$. Hence, $Q \geq \sqrt{\sqrt{2}-1} = .6436$, as shown in Appendix B. This is fortunate because in deriving equation (14) without calculus earlier, it was assumed that $Q > 0.5$. Therefore, this assumption has not imposed any limitation on the derivation. (By the way, for $Q \leq .6436$, $f_m = 0$, as can be easily verified by plotting equation (9)).

Approximations to the Maximum Impedance Resonant Frequency

A. Approximations to the Maximum Impedance Resonant Frequency, Equation (14)

For large values of Q, it is possible to simplify equation (14) because $\frac{2}{Q^2}$ is quite a bit smaller than 1 and

$$\sqrt{1+\frac{2}{Q^2}} \approx 1 + \frac{1}{Q^2} - \frac{1}{2Q^4}. \quad (15)$$

Equation (15) follows from the well-known fact that $\sqrt{1+a} \approx 1 + \frac{a}{2} - \frac{a^2}{8}$, if a is small. Indeed, the smaller a is, the more accurate the approximation becomes. Likewise, the larger Q is, the more accurate equation (15) becomes.

Substituting equation (15) into equation (13) gives an excellent approximation to the square of the maximum impedance resonant frequency, i.e.,

$$\left(\frac{\omega_m}{\omega_0}\right)^2 = 1 - \frac{1}{2Q^4}. \quad (16)$$

Hence, from equation (16), the maximum impedance resonant frequency is well approximated by

$$f_m = f_o \sqrt{1 - \frac{1}{2Q^4}}. \quad (17)$$

It is interesting that Boylestad [1], in his equation (20.32), equation (20.44), and Table 20.1, gives the maximum impedance resonant frequency as

$$f_m = f_o \sqrt{1 - \frac{1}{4Q^2}}. \quad (18)$$

It is not known how this equation was derived, as no derivation for this is given in his text; however, it is clearly an approximation to the exact value equation (14). It might be that this is simply a typographical error, with $4Q^2$ inadvertently being used in place of $2Q^4$.

In the subsection below, the authors show that equation (17) is a substantially more accurate approximation to equation (14) than equation (18) is for Q values that are normally of interest.

B. Accuracy of the Approximations to the Maximum Impedance Resonant Frequency

Now that two approximations to the maximum impedance resonant frequency have been established, the natural question is how accurate is each approximation. To answer this question, the percentage error of equations (17) and (18), plotted in Figure 3, is defined by

$$P_{error} = \left(\frac{\text{Approximation Equation (17) or Equation (18)}}{\text{Exact Equation (14)}} \text{-1} \right) 100\%. \tag{19}$$

From Figure 3, it is clear that the percentage error for equation (17) is substantially smaller than that of equation (18) for Q values that are normally of interest. Indeed, the higher the Q, the more accurate is the approximation for equations (17) and (18) for $Q \geq 1.41$.

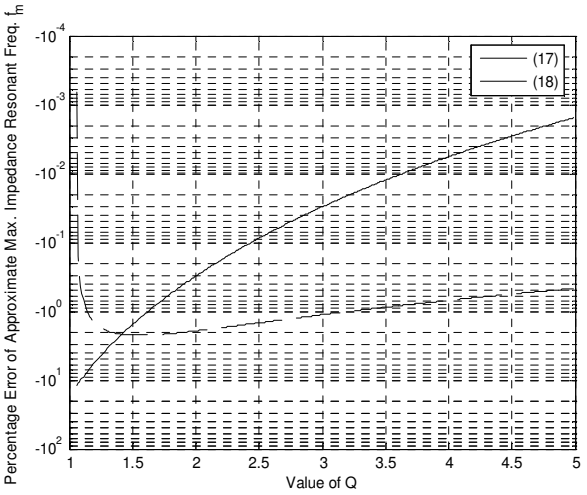

Figure 3. Percentage error of the approximations for equations (17) and (18) to the true maximum impedance resonant frequency given by equation (14)

Interestingly, equation (18) is more accurate than equation (17) for a limited range and actually improves as Q is lowered over that range, which is upper bounded by $Q = 1.41$. The percentage error of equation (18) is actually zero when equation (14) equals equation (18), or $Q = \frac{3}{2\sqrt{2}} \approx 1.0607$.

Finding the Impedance Magnitude at the Three Resonant Frequencies

Now that equations for the three resonant frequencies f_p, f_m and f_o have been established, they can be used along with equation (9) to find the actual impedance magnitudes at these frequencies. Note that f_o is being referred to as a resonant frequency, as it is the resonant frequency of Figure 2 when $R = 0$; indeed, for this case, $f_p = f_m = f_o$.

A. Impedance Magnitude at $\omega_o = \frac{1}{\sqrt{LC}}$.

When the frequency of the source is $\omega = \omega_o = 1/\sqrt{LC}$, $x = 1$; hence, from equation (9), the magnitude of the impedance is given by

$$|Z|_o = R\sqrt{Q^2\left(1+Q^2\right)}. \tag{20}$$

For large $Q, 1+Q^2 \approx Q^2$. Hence, equation (20) becomes

$$|Z|_o \approx RQ^2. \tag{21}$$

B. Impedance Magnitude at the Zero-Phase Resonant Frequency, $\omega_p = \omega_o\sqrt{1-\frac{1}{Q^2}}$.

When the source frequency is the zero-phase resonant frequency, i.e., $\omega_p = \omega_o\sqrt{1-\frac{1}{Q^2}}$, $x = 1-1/Q^2$, and the magnitude of the impedance is again found from Equation (9) to be

$$\begin{aligned} |Z|_p &= R\sqrt{\frac{Q^2\left(1+Q^2\left(1-\frac{1}{Q^2}\right)\right)}{1-\frac{1}{Q^2}+Q^2\left(1-\left(1-\frac{1}{Q^2}\right)\right)^2}} \\ &= R\sqrt{\frac{Q^4}{1-\frac{1}{Q^2}+Q^2\frac{1}{Q^4}}} \\ &= RQ^2. \end{aligned} \tag{22}$$

Comparing equation (22) to equation (20) shows that the magnitude of the impedance at the zero-phase resonant frequency is always smaller than that at ω_o, i.e., $|Z|_p < |Z|_o$. However, for large values of Q, these are very close in val-

ue, i.e., $|Z|_p \approx |Z|_o$.

It should also be noted that many authors, including Boylestad [1], use equation (22) as the approximation for the maximum impedance magnitude when $Q \geq 10$. However, equation (20) is bigger than equation (22) for all values of Q. Hence, equation (20) might be a better approximation to the exact maximum impedance magnitude, especially for low Q values. Indeed, this is the case as verified below.

C. Maximum Impedance Magnitude, $|Z|_{\max}$: Impedance at the Maximum Impedance Resonant Frequency, $\omega_m = \omega_o \sqrt{-\frac{1}{Q^2} + \sqrt{1 + \frac{2}{Q^2}}}$

From equation (12), the maximum impedance magnitude, $S_{\max}$, occurs for $b = 0$; hence,

$$S_{\max} = \frac{a}{c} = \frac{Q^2}{2\sqrt{1+\frac{2}{Q^2}} - 2 - \frac{1}{Q^2}} = \frac{Q^2}{2\frac{1}{Q}\sqrt{Q^2+2} - 2 - \frac{1}{Q^2}} = \frac{Q^4}{2Q\sqrt{Q^2+2} - 2Q^2 - 1}. \quad (23)$$

Using $S_{\max} = |Z|^2_{\max} / R^2$, equation (23) becomes

$$|Z|_{\max} = RQ^2 \sqrt{\frac{1}{2Q\sqrt{Q^2+2} - 2Q^2 - 1}}. \quad (24)$$

To the authors' knowledge, the expression in equation (24) has never appeared in the open literature before. Interestingly, for large values of Q, $\sqrt{Q^2+2} = Q\sqrt{1+\frac{2}{Q^2}} \approx Q\left(1+\frac{1}{Q^2}\right)$, and so the denominator under the square root sign of equation (24) becomes unity. Thus, for large values of Q, $|Z|_{\max} \approx RQ^2$; hence, $|Z|_p \approx |Z|_o \approx |Z|_{\max}$.

D. Accuracy of the Approximations to the Maximum Impedance Magnitude

Now that the approximations of equations (20) and (22) have been established to the exact maximum impedance, given by equation (24), the accuracy of each should be tested. This can be done by computing the percentage error, given by

$$P_{error} = \left(\frac{\text{Approximation Equation (20) or Equation (22)}}{\text{Exact Equation (24)}} - 1 \right) 100\%. \quad (25)$$

These percentage errors are plotted in Figure 4.

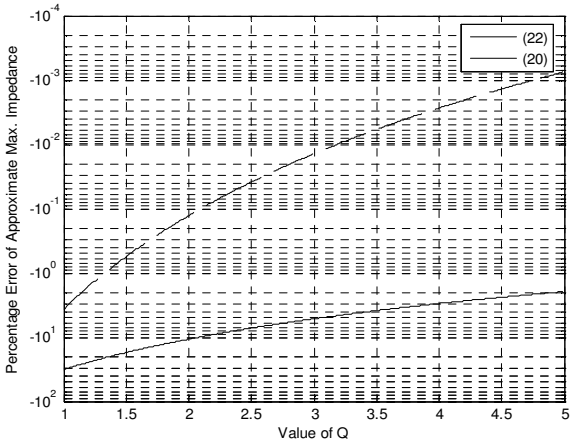

Figure 4. Percentage error of the maximum impedance magnitude estimates. Clearly, equations (20) and (22) always underestimate the true maximum impedance magnitude. Furthermore, equation (20) is a better approximation than equation (22) for all Q values of interest

As mentioned earlier, equation (22) is used to approximate the maximum magnitude of the impedance for $Q \geq 10$. However, Figure 4 shows that equation (22) has a percentage error of less than -2% for $Q \geq 5$, and less than -10% for $Q \geq 2$. Hence, equation (22) can be used for very small Q values with a tolerable percentage error. Furthermore, equation (22) has the advantage of being the simplest approximation.

On the other hand, equation (20) has excellent percentage error performance, even for $Q = 1$, with a percentage error of only -4%, whereas for $Q \geq 1.5$, the percentage error is less than -0.6%.

Verification through PSpice Simulations

In this section, PSpice is used to verify the authors' derived equations. For all simulations, the authors used $C = 10\mu\text{F}$ and $L = 25.33\mu\text{H}$; (see Figure 2); hence, $f_o = 10k\text{Hz}$. Due to space limitations, $R = 2\pi f_o L/Q = \sqrt{L/C}/Q$, was chosen for only two Q values, as listed in Table 1.

Table 1. *R* values needed to achieve desired *Q* values for the circuit of Figure 2

Desired *Q* Value	Corresponding *R* Value (Ω)
1.5	1.06103
3	0.53051

For all of the simulation plots of this section, the amplitude of the voltage across the practical parallel circuit is plotted, i.e., the voltage across the capacitor, divided by the magnitude of the current source, which is 1A, the magnitude of the impedance seen by the current source.

Furthermore, the PSpice simulation data was exported to Matlab for actual plotting; it was found that this would allow for more readable graphs. Another advantage is that Matlab can then be used to search for the maximum impedance point, with great precision. In fact, this is how the PSpice simulated values given in Tables 2(a) to 3(b), were found.

A. Results for *Q*=1.5

Figure 5 shows a PSpice simulation plot of the magnitude of the impedance of the practical parallel circuit for *Q*=1.5.

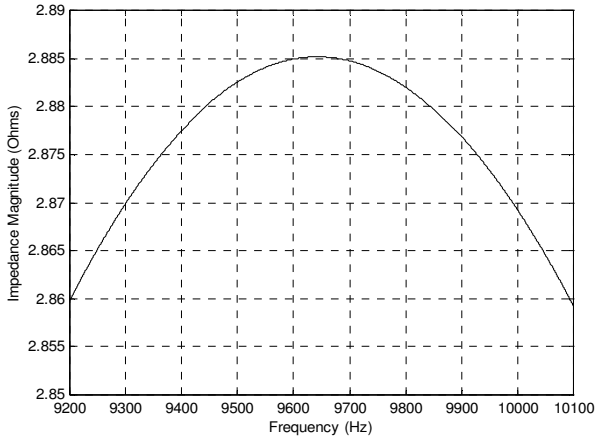

Figure 5. Magnitude of the impedance of the practical parallel circuit of Figure 2 for *Q*=1.5

For convenience, the simulated results are presented and compared to the theoretical results in Tables 2(a) and 2(b).

Table 2(a). Simulated results compared with theoretical results for the maximum impedance resonant frequency when *Q*=1.5

Maximum Impedance Resonant Frequency	Value	Percentage error compared with exact theoretical Equation (14)
PSpice simulated value	9643.4 Hz	0.00104%
Theoretical value from Equation (14)	9643.3 Hz	NA
Approximate value with Equation (18)	9428.1 Hz	−2.232%
Approximate value with Equation (17)	9493.3 Hz	−1.555%

Table 2(b). Simulated results compared with theoretical results for the maximum impedance magnitude when *Q*=1.5

Maximum Impedance Magnitude	Value	Percentage error compared with exact theoretical Equation (24)
PSpice simulated value	2.8852 Ω	0%
Theoretical value from Equation (24)	2.8852 Ω	NA
Approximate value with Equation (22)	2.3873 Ω	−17.26%
Approximate value with Equation (20)	2.8692 Ω	−.5546%

B. Results for *Q*=3

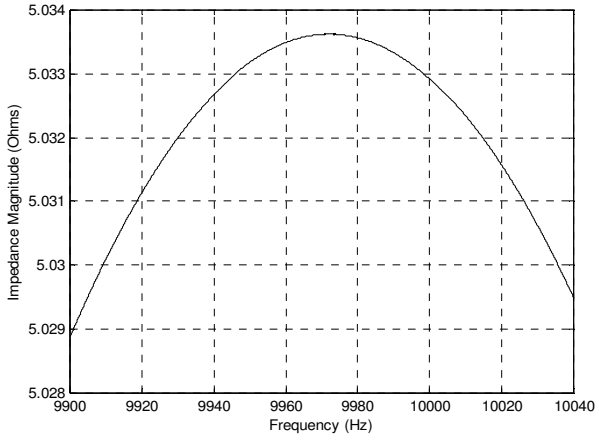

Figure 6. Magnitude of the impedance of the practical parallel circuit of Figure 2 for *Q* = 3

Table 3(a). Simulated results compared with theoretical results for the maximum impedance resonant frequency when Q=3

Maximum Impedance Resonant Frequency	Value	Percentage error compared with exact theoretical Equation (14)
PSpice simulated value	9972.1 Hz	0 %
Theoretical value from Equation (14)	9972.1 Hz	NA
Approximate valuewith Equation (18)	9860.1 Hz	−1.123%
Approximate value with Equation (17)	9969.1 Hz	−0.030%

Table 3(b). Simulated results compared with theoretical results for the maximum impedance magnitude when Q=3

Maximum Impedance Magnitude	Value	Percentage error compared with exact theoretical Equation (24)
PSpice simulated value	5.0336 Ω	0%
Theoretical value from Equation (24)	5.0336 Ω	NA
Approximate value with Equation (22)	4.7746 Ω	−5.145%
Approximate value with Equation (20)	5.0329 Ω	−0.0139%

Figure 6 shows a PSpice simulation plot of the magnitude of the impedance of the practical parallel circuit for Q=3. Again, the simulated results are presented and compared to the theoretical results in Tables 3(a) and 3(b).

C. Discussion

Based upon the tables above and other simulations not reported here due to space limitations, the following observations can be made concerning the maximum impedance frequency:

1. The theoretical value given by equation (14) and the PSpice simulations show excellent agreement.
2. The approximate theoretical value given by equation (17) is more accurate than the value from equation (18) for $Q \geq 1.41$. Both of these approximations improve with increasing Q values.

Furthermore, the following observations can be made concerning the maximum impedance:

1. The theoretical value given by equation (24) and the PSpice simulations show excellent agreement.
2. It is quite apparent that the maximum impedance magnitude is in fact well approximated by the impedance magnitude given by equation (20), which of course is the impedance magnitude at the resonant frequency, f_o. Additionally, this approximation improves with increasing Q values.

Conclusion

In this paper, the maximum impedance resonant frequency was derived without calculus. In so doing, the authors also modified a formula that is given for this in a popular technology textbook, thereby increasing its accuracy. Furthermore, the authors also found a novel expression for the exact maximum impedance. This has been approximated by previous authors as RQ^2 for $Q \geq 10$. However, it was shown here that this approximation has a percentage error less than -2% for $Q \geq 5$, and less than -10% for $Q \geq 2$. It was further shown that the maximum impedance is also well approximated by $R\sqrt{Q^2\left(1+Q^2\right)}$, which has excellent percentage error performance, even for $Q = 1$, with a percentage error of only -4% for this value, and less than -0.6% for $Q \geq 1.5$. Finally, the authors used PSpice simulations to verify their results.

Appendix A

In this appendix, the authors show that

$$2\sqrt{1+\frac{2}{Q^2}} - \left(2+\frac{1}{Q^2}\right) > 0. \qquad \text{(A1)}$$

Rearranging equation (A1) produces

$$2\sqrt{1+\frac{2}{Q^2}} > 2+\frac{1}{Q^2} \;\Rightarrow\; \sqrt{1+\frac{2}{Q^2}} > 1+\frac{1}{2Q^2}. \qquad \text{(A2)}$$

Further rearrangement of equation (A2) gives

$$\begin{aligned} &1+\frac{2}{Q^2} > \left(1+\frac{1}{2Q^2}\right)^2 \Rightarrow 1+\frac{2}{Q^2} > 1+\frac{1}{Q^2}+\frac{1}{4Q^4} \\ &\Rightarrow \frac{1}{Q^2} > \frac{1}{4Q^4} \Rightarrow 1 > \frac{1}{4Q^2} \\ &\Rightarrow Q^2 > \frac{1}{4} \Rightarrow Q > \frac{1}{2}. \end{aligned} \qquad \text{(A3)}$$

Appendix B

In this appendix, the authors show that

$$\frac{-1}{Q^2}+\sqrt{\frac{2}{Q^2}+1}\geq 0 \text{ for } Q\geq\sqrt{\sqrt{2}-1}=.6436.$$

Beginning with

$$\sqrt{\frac{2}{Q^2}+1}\geq\frac{1}{Q^2}\Rightarrow\frac{2}{Q^2}+1\geq\frac{1}{Q^4} \quad \text{(B1)}$$
$$\Rightarrow 2Q^2+Q^4\geq 1\Rightarrow Q^4+2Q^2-1\geq 0.$$

Solving equation (B1) gives

$$Q^2\geq -1\pm\frac{\sqrt{4+4}}{2}=-1\pm\frac{2\sqrt{2}}{2}. \quad \text{(B2)}$$

However, Q^2 must be non-negative, so $Q^2\geq -1+\sqrt{2}$.

Hence, $Q\geq\sqrt{\sqrt{2}-1}=.6436,$ as stated previously.

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Biographies

KENNETH V. CARTWRIGHT received a B.E.Sc. degree in Electrical Engineering from the University of Western Ontario, London, Ontario, Canada, in 1978; a M.S. degree in Electrical Engineering from Tulane University, New Orleans, Louisiana, in 1987; and a Ph.D. degree in Electrical Engineering from Tulane University, New Orleans, Louisiana, in 1990. Currently, he is a Professor of Electrical Engineering at the College of The Bahamas. His teaching and research areas include analog electronics, control systems, and analog and digital communication systems. He has authored/co-authored many papers, which are listed on his website http://sites.google.com/site/kvcartwright/. Dr. Cartwright may be reached at kvcartwright@yahoo.com.

ELTON JOSEPH received a B.S.E.T. degree in Electrical Engineering Technology from the College of The Bahamas (COB), Nassau, Bahamas in 2009. The research for this paper was done while he was a student at COB. He has worked for the Marine and Environment Science Institute located at the College. Currently, he works on environmental projects around The Bahamas. His interests include designing ways to make coastal developments more environmentally friendly and sustainable. Mr. Joseph may be reached at eltonevey@gmail.com.

EDIT J. KAMINSKY received her B.S. degree in Electrical Engineering, summa cum laude, from the Universidad Autónoma de Centro América, Costa Rica, in 1986 and her M.S. and Ph.D degrees in Electrical Engineering from Tulane University, New Orleans, Louisiana, in 1987 and 1991, respectively. Professor Kaminsky is currently the Department Chair of Electrical Engineering at the University of New Orleans**.** Her current research interests are in the areas of digital communications, and sonar and signal processing. Her publications are listed on her website at http://fs.uno.edu/ejbourge. Dr. Kaminsky may be reached at ejbourge@uno.edu.

EVALUATION OF FATIGUE CRITERIA FOR ASPHALT PAVEMENTS

Mena I. Souliman, Arizona State University; Kamil E. Kaloush, Arizona State University

Abstract

Load-associated fatigue cracking is one of the major distress types occurring in flexible pavement systems. Bending flexural beam fatigue testing has been used for several decades and is considered to be an integral part of the new Superpave advanced characterization procedure. However, there is a great need to assess and develop a fatigue criterion based on initial and failure stiffness of the mixture under consideration.

A laboratory testing program was performed on a Reference, Asphalt Rubber (AR), and Polymer modified-gap graded mixtures. Strain-controlled fatigue tests were conducted according to American Association of State Highway and Transportation Officials (AASHTO) procedures on all of the three mixtures at one temperature.

Using a COANOVA statistical analysis approach, the Arizona State University (ASU) method, which is independent on the mode of loading, temperature, frequency, or mixture formulation, was concluded to be the most accurate method to analyze beam fatigue results. This method has the potential for unifying current fatigue analyses using a rational energy-based approach and it has a well-defined fatigue failure point when compared with other proposed methods. It was also concluded that the AR mixture showed higher fatigue life than the Polymer and the Reference mixtures.

Introduction

The flexural fatigue test is used to characterize the fatigue life of Hot Mix Asphalt (HMA) at intermediate pavement operating temperatures. This characterization is useful because it provides estimates of HMA pavement layer fatigue life under repeated traffic loading. In a well-designed pavement, strains in the pavement are low enough so that fatigue is not a problem. However, when pavements are underdesigned, strains are sufficiently high to cause fatigue failures under repeated loads. These failures ultimately result in fatigue cracking which will cause disintegration of the pavement if not maintained.

The basic flexural fatigue test subjects a HMA beam to repeated flexural bending in a controlled atmosphere. In order to relate laboratory results to normally observed field performance, a shift factor of 10 to 20 is typically needed. Due to the complexity of the testing equipment and long testing times, the flexural fatigue test is primarily a research test and is not a standard test in Superpave mix design or quality assurance testing.

The standard beam fatigue procedure is found in AASHTO T 321: Determining the Fatigue Life of Compacted Hot-Mix Asphalt (HMA) Subjected to Repeated Flexural Bending [1]. The flexural fatigue test has been used by various researchers to evaluate the fatigue performance of pavements [2-5].

Study Objective

The primary objective of this study was to present different fatigue analysis criteria including the traditional way of determining the failure criteria at specific stiffness reduction from the initial stiffness and the recent mechanistic dissipated energy methods. Subsequently, a comparison was made between all of the fatigue analysis results to asses which method is the most reliable, accurate, and simplest to be implemented as the major method for fatigue analysis. To accomplish this objective, a laboratory testing program was performed on a project which included three types of mixes: Reference, Polymer modified and Asphalt Rubber (AR) modified-gap graded mixtures. The fatigue parameters at each temperature were determined and the general fatigue model parameters for one of the mixtures (the polymer mix) were calculated.

Background

In HMA pavements, fatigue cracking occurs when repeated traffic loads ultimately cause sufficient damage in a flexible pavement to result in fatigue cracking. A number of factors can influence a pavement's ability to withstand fatigue, including pavement structure (thin pavements or those that do not have strong underlying layers are more likely to show fatigue cracking than thicker pavements or those with a strong support structure), age of the pavement, and the materials used in construction. The flexural fatigue test is used to investigate fatigue as it relates to HMA construction materials.

The most common model form used to predict the number of load repetitions to fatigue cracking is a function of the tensile strain and mixture stiffness (modulus). The basic

structure for almost every fatigue model developed and presented in the literature for fatigue characterization is of the following form [1]:

$$N_f = K_1\left(\frac{1}{\varepsilon_t}\right)^{k_2}\left(\frac{1}{E}\right)^{k_3} \quad (1)$$

where:

N_f = number of repetitions to fatigue cracking

ε_t = tensile strain at the critical location

E = stiffness of the material

K_1, K_2, K_3 = laboratory calibration parameters

In the laboratory, two types of controlled loading are generally applied for fatigue characterization: constant stress and constant strain. In constant stress testing, the applied stress during the fatigue testing remains constant. As the repetitive load causes damage in the test specimen, the strain increases resulting in a lower stiffness with time. For the constant strain test, the strain remains constant with the number of repetitions. Because of the damage due to repetitive loading, the stress must be reduced resulting in a reduced stiffness as a function of repetitions. The constant stress type of loading is considered applicable to thicker pavement layers, usually more than 8 inches. For AC thicknesses between these extremes, fatigue behavior is governed by a mixed mode of loading, mathematically expressed as some model yielding intermediate fatigue prediction to the constant strain and stress conditions.

A. Testing Equipment

Flexural fatigue tests are performed according to the AASHTO T321-03 [1]. The device is typically placed inside an environmental chamber to control the temperature during the test. The cradle mechanism allows for free translation and rotation of the clamps and provides loading at three points. Pneumatic actuators at the ends of the beam center it laterally and clamp it. Servomotor driven-clamps secure the beam at four points with a pre-determined clamping force. Haversine or sinusoidal loading may be applied to the beam via the built-in digital servo-controlled pneumatic actuator. The innovative "floating" on-specimen transducer measures and controls the true beam deflection irrespective of loading-frame compliance. The test is run under either controlled-strain or controlled-stress loading.

In the constant stress mode, the stress remains constant but the strain increases with the number of load repetitions. In the constant strain test, the strain is kept constant and the stress decreases with the number of load repetitions. In either case, the initial deflection level is adjusted so that the specimen will undergo a minimum of 10,000 load cycles before its stiffness is reduced to 50 percent or less of the initial stiffness. In this study, all tests were conducted in the control strain type of loading.

B. Dissipated Energy Concept

(1)

When applying load to a material, the material will exhibit some stain induced by the acting stress. The area under the stress-strain curve represents the energy being inputted into the material. When the load is removed from the material, the stress is removed and the strain is recovered, as shown in Figure 1. If the loading and unloading curves coincide, of all the energy put into the material is recovered after the load is removed. If the two curves do not coincide, there is energy lost in the material. This energy can be altered through mechanical work, heat generation, or damage in the material in a manner that it could not be used to return the material to its original shape. This energy difference is the dissipated energy of the material caused by the load cycle. So, dissipated energy can be defined as the damping energy or the energy loss per load cycle in any repeated or dynamic test.

Many researchers have studied dissipated energy [2], [6-12]. The equation for calculating dissipated energy per cycle in a linear viscoelastic material in the flexural fatigue test is given by the following equation:

$$\omega_i = \pi\sigma_i\varepsilon_i \sin\phi_i \quad (2)$$

where:

ω_i = dissipated energy at load cycle, i;

σ_I = stress at the load cycle, i;

ε_I = strain at the load cycle, i;

ϕ_I = phase angle between stress and strain at the load cycle, i

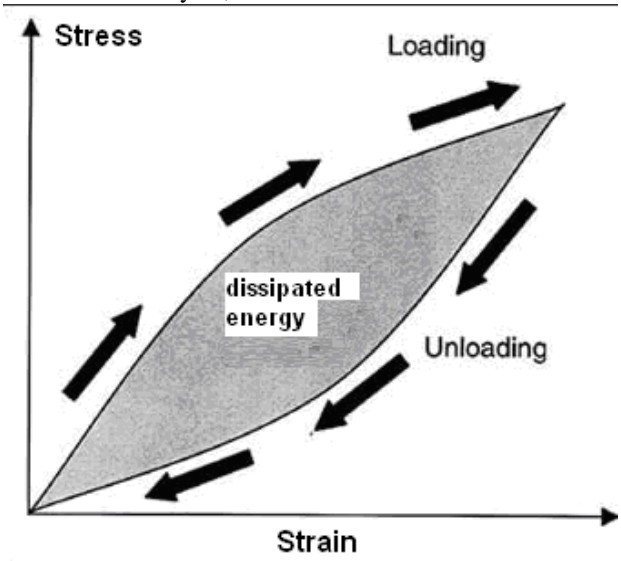

Figure 1. Stress-strain curve for viscoelastic solid

C. Pronks' Method

One of the most accurate dissipated energy methods is Pronks' method [13]. In 1997, Pronk suggested a different expression of energy ratio for the constant strain test to define failure as the ratio of the cumulative dissipated energy up to cycle n to the dissipated energy for cycle n (W_n/w_n). Under constant strain, plotting the energy ratio for different cycles versus the number of load cycles for each specimen, the fatigue life was defined as the number of load cycles when the energy ratio deviates from a straight line, as shown in Figure 2.

D. Stiffness Degradation Ratio versus Number of Repetitions (ASU-Approach)

A new rational fatigue failure criterion was developed [5] in recent study based on Rowe and Bouldins' failure definition. By normalizing Rowe and Bouldins' ratio (N_iS_i) by dividing it by the initial stiffness (S_o), a new stiffness ratio was developed at ASU as (N_i*S_i/S_o), where Ni is the cycle number, Si is the stiffness at cycle i, and S_o is the initial stiffness taken at cycle number 50. By plotting the stiffness degradation ratio value (N_i*S_i/S_o) versus the load cycles, a peak value can be obtained. Failure is then defined as the number of load repetitions at the peak value of that curve for both controlled-strain and controlled-stress modes as shown in Figure 3.

The results also show that there is no significant difference between the two curves for controlled-stress and controlled–strain modes. It was noted that the curves from constant strain testing and constant stress testing have almost the same trend. Again, a very high R^2 value of 0.991 was obtained as an average for all mixes used in the study. It was concluded that the stiffness degradation ratio at failure, as defined in this new method, represents a basic material behavior at which damage accumulation in the mixture has produced an inability of the mixture to resist further damage independent of the mode of loading.

The final conclusion for the final damage ratio was around 0.5 of the initial stiffness. The results of this study verify that 50 percent of the initial stiffness is the best value for the failure fatigue criterion.

Test Results and Analysis

A. Mixtures Characteristics

In 2008, a first cooperative effort between ASU and the Swedish Road Administration (SRA) took place in testing Reference and Asphalt rubber-gap-graded mixtures placed on Malmo E6 External Ring Road in Sweden. In 2009, SRA and ASU undertook another joint effort to test three types of gap-graded mixtures: Reference, Polymer-modified and Rubber-modified mixes, placed on highway E18 between the interchanges Järva Krog and Bergshamra in the Stockholm area of Sweden.

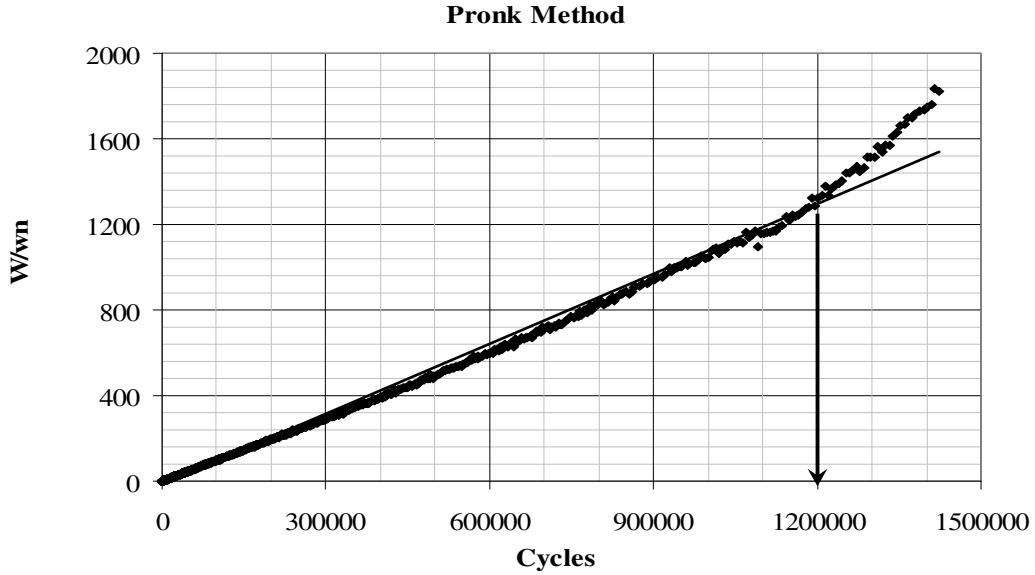

Figure 2. N_f Determination for the AR sample using Pronk's method

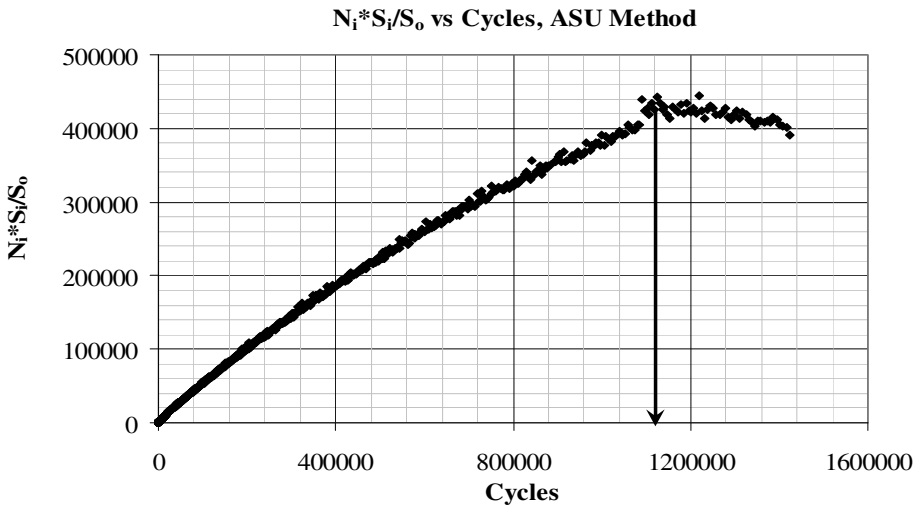

Figure 3. N_f Determination for the AR sample using the ASU method

Rice specific gravities for the mixtures were determined. Beam specimens were prepared according to the Strategic Highway Research Program (SHRP) and the American Association of State Highway and Transportation Officials (AASHTO): SHRP M-009 and AASHTO T321-03 (2003). Air voids, thickness and bulk specific gravities were measured for each test specimen and the samples were stored in plastic bags in preparation for the testing program.

The designated road section within the construction project had three asphalt mixtures: a Reference gap-graded mixture (designation: ABS 16 70/100) used as a control, a Polymer-modified mixture (designation: ABS 16 Nypol 50/100-75), and a Rubber-modified mixture (designation: GAP 16) that contained approximately 20 percent ground tire rubber (crumb rubber). Figure 4 shows the road in the Stockholm area where the three mixtures were placed.

Figure 4. Test Sections in fast lanes on highway E18 between the Järva-Krog & Bergshamra interchanges

The Swedish Road Administration provided information stating that the field compaction / air voids for the three mixtures was around 3.0%. The original mix designs were done using the Marshall Mix design method. Table 1 shows the reported average aggregate gradations for each mixture. The in-situ mixture properties of the Stockholm pavement test sections are reported in Table 2, which includes % binder content by mass of the mix, Marshall Percent void content by volume of the mix, and maximum theoretical specific gravity of the mixes estimated at ASU laboratories. The base bitumen used was Pen 70/100. The polymer bitumen was designated Nypol 50/100-75 and rubber was called GAP 16.

Table 1. Average aggregate gradations, Stockholm highway

Gradation (% Passing by mass of each sieve)	Sieve Size (mm)	Reference	Polymer	Rubber
	22.4	100	100	100
	16	98	98	98
	11.2	65	65	68
	8	38	38	44
	4	23	23	24
	2	21	21	22
	0.063	10.5	10.5	7.5

Table 2. Mixture characteristics, Stockholm highway

Mix	Binder Content (%)	Air Voids (%)	G_{mm}
Reference ABS 16 70/100	5.9	2.6	2.4642
Polymer ABS 16 Nypol 50/100-75	5.9	2.6	2.4558
Rubber GAP 16	8.7	2.4	2.3588

B. Determination of K_1 and K_2 Coefficients at each Temperature

It has been accepted for many years that the fatigue behavior of the asphalt-aggregate mixes can be characterized by a relationship of the form:

$$N_f = K_1\left(1/\varepsilon_o\right)^{K_2} \quad (3)$$

where,

ε_o = initial tensile strain

K_1, K_2 = experimentally determined coefficients

The above relationship is applicable to a given asphalt mix. Moreover, the fatigue relationships (flexural strain versus the number of loading cycles) for each mixture are shown in Figures 5 through 7. The relationships obtained have good measures of model accuracy as indicated by the coefficient of determination (R^2). Comparing fatigue curves for different mixes is not straightforward because of the different mixes' modules. A look at the fatigue models' coefficients may provide some guidance. Therefore, the below comparisons are made in general terms.

A summary of the regression equations is shown in table 3. The R^2 values are an indication of good to very good model accuracy. The relationships obtained are rational in that lower fatigue life (number of repetitions) is obtained as the temperature decreases.

Figures 5 through 7 illustrate how to determine the K_1 and K_2 values for all three mixes using five different approaches.

1. Initial stiffness after 50 cycles and Nf at 50% of the initial stiffness
2. Initial stiffness after 50 cycles and Nf at 40% of the initial stiffness
3. Initial stiffness after 50 cycles and Nf at 30% of the initial stiffness
4. Dissipated energy method, Pronk Method
5. Dissipated energy method, ASU Method

Table 3. Summary of regression coefficients for the fatigue relationships for 21°C using different approaches to find N_f

Reference mix	K_1	5.00E-10	5.00E-12	7.00E-12	1.00E-12	2.00E-11
	K_2	4.17	4.88	4.9	5.03	4.79
	R^2	0.9468	0.9693	0.9845	0.9858	0.9879
AR mix	K_1*	1.00E-09	2.00E-12	4.00E-12	2.00E-11	1.00E-11
	K_2*	4.17	5.4	5.39	5.09	5.25
	R^2	0.9842	0.9169	0.8803	0.8469	0.8723
Polymer mix	K_1	2.00E-09	1.00E-08	2.00E-07	0.0002	1.00E-06
	K_2	4.16	4.07	3.71	2.41	3.5
	R^2	0.9612	0.9252	0.9454	0.7618	0.9433

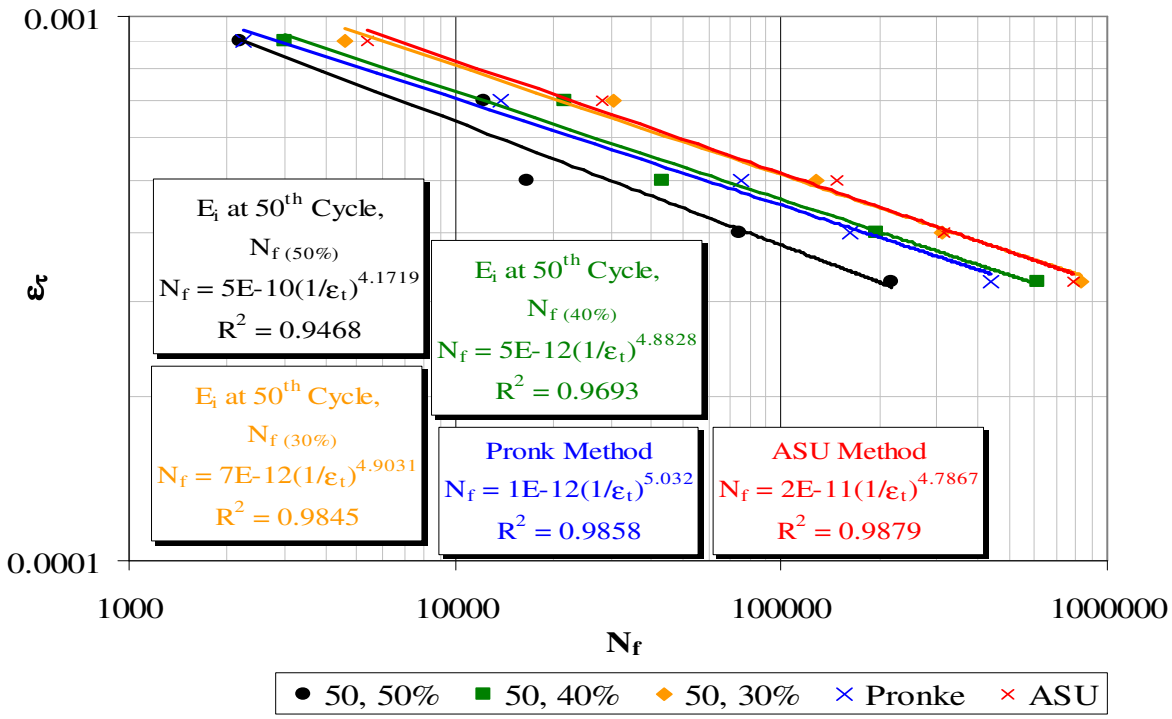

Figure 5. N_f versus strain using different N_f determination approaches, Reference mixture (21°C)

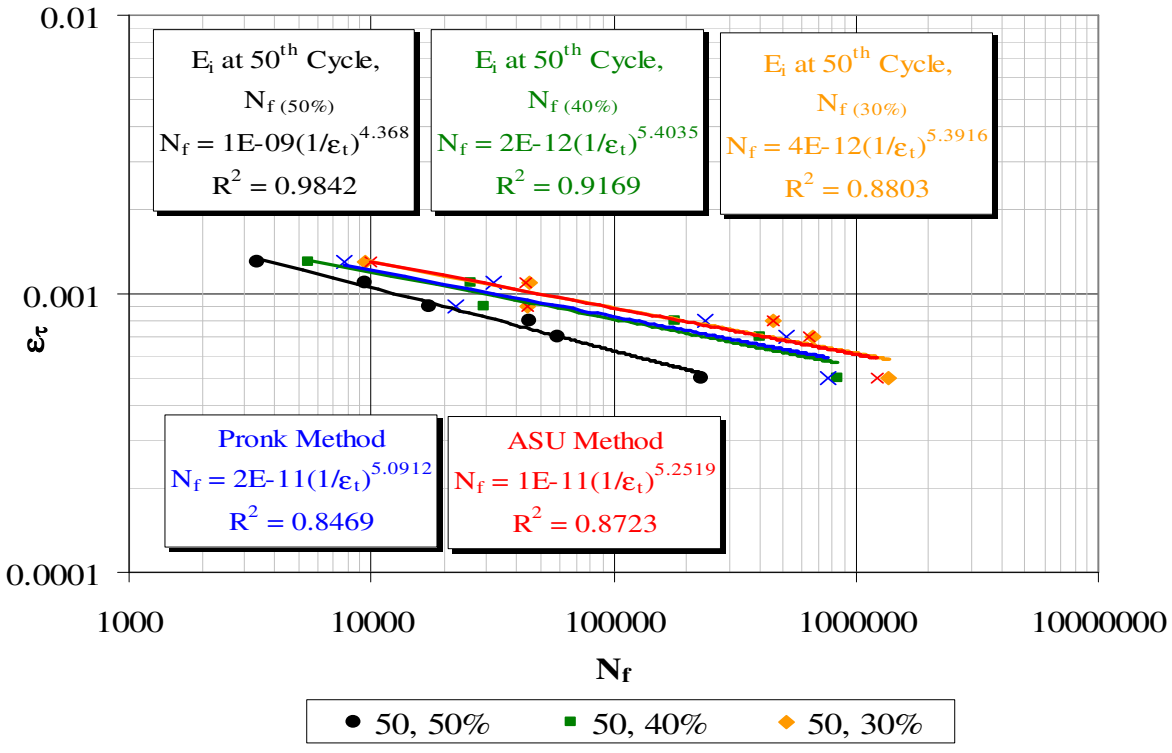

Figure 6. N_f versus strain using different N_f determination approaches, AR mixture (21°C)

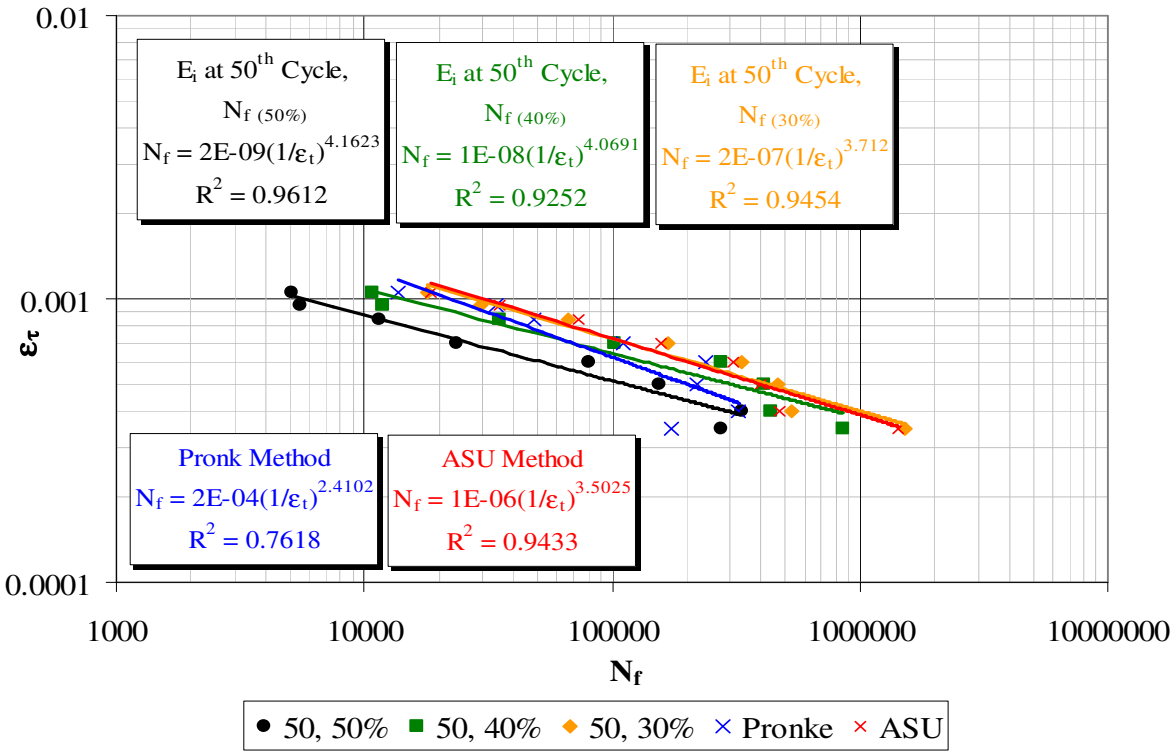

Figure 7. N_f versus strain using different N_f determination approaches, Polymer mixture (21°C)

C. COANOVA Statistical Analysis of the Equality of Fatigue Analysis Methods

In order to determine if two fatigue analysis methods are different, the COANOVA statistical approach introduced by Neter, et al. [14] and Motulsky et al. [15] can be used. The detailed procedure is explained as follows:

1. Hypothesis: Ho: the two method results are the same. Ha: the two method results are different.
2. Fit the full or unrestricted model to get the error sum of squares SSE(F)=SSE1 + SSE2, where SSE1 is the error sum of squares for regression method 1, and SSE2 is the error sum of squares for regression method 2; the total degrees of freedom df(F)=df1+df2.
3. Fit the reduced or restricted model (combine each data set into one big data set) under the Ho hypothesis that all method results are the same, and obtain the error sum of squares SSE(R) and degrees of freedom df(R) for the reduced model.
4. Calculate the F* statistic using the equation:

$$F^* = \frac{SSE(R) - SSE(F)}{df(R) - df(F)} \div \frac{SSE(F)}{df(F)} \qquad (4)$$

5. Obtain the p-value by using excel internal function of F probability distribution for the two data sets (FDIST):

$$p - value = FDIST\left(F^*, df_a, df_b\right) \qquad (5)$$

where: dfa=df(R)-df(F), and dfb=df(F).

6. Reject Ho if p-value <= α to conclude the two method results are different. Otherwise, Ho hypothesis that the two methods are the same is to be accepted.

The p-value is the level of significance, which is defined as the probability of obtaining a value of the test statistic that is as likely or more likely to reject Ho as the actual observed value of the test statistic. This probability is computed assuming that the null hypothesis is true. Thus, if the level of significance (p-value) is a small value, then the sample data fail to support Ho and our decision is to reject Ho (Neter et al., 1990). To determine the rejection region, the value of a type I error, α, should be pre-set based on the research requirement and sample size. A traditional α-value of 0.05 can be used when the sample size is not very large.

In this case, two Strain Level-Nf lines that arrive from two different fatigue analyses methods were used. For example,

in Table 4, the comparison between the ASU method and a 30% reduction of the initial stiffness method, SSE (F), was calculated by summing SSE1 and SSE2, as follows: SSE1 + SSE2 = 0.0485+0.0360 = 0.0845. For the combined regression curve from both mixtures, SSE(R) = 0.0862. The calculated F* = 0.1594 with dfa = 1 and dfb= 8. Therefore, p-value = FDIST (0.312, 2, 5) = 0.700. Because the p-value was greater than α=0.05, we failed to reject the Ho hypothesis and concluded that the two methods were statistically the same. They can be pooled into one line with R-square of 0.99, suggesting that the relationship of Strain Level-Nf can be independent of mixture properties. The other methods (50% reduction of initial stiffness, 40% reduction of initial stiffness , and Pronk Methods) seem to introduce different results as compared to the ASU method. Table 4 demonstrates the complete comparison between the different methods of analysis.

D. COANOVA Statistical Comparison between All Swedish Mixtures

The same COANOVA statistical approach mentioned above was utilized to assess if modifying the reference mixture by adding Rubber or Polymer made an improvement in the fatigue life performance or not. Table 5 and Figures 8 through 11 show that there is a significant difference in the fatigue life performance between the Reference and both AR and Polymer-modified mixes.

Table 4. Comparison between ASU Method and other fatigue analysis methods

Comparison	ASU vs 30%	ASU vs 40%	ASU vs 50%	ASU vs Pronk
SEE(F)	0.0845	0.1328	0.1613	0.0826
SEE(R)	0.0862	0.2839	1.0211	0.3191
df(F)	8	8	8	8
df(R)	9	9	9	9
F*	0.159	9.101	42.654	22.921
df(a)	1	1	1	1
df(b)	8	8	8	8
P-value	0.7001	0.0166	0.0002	0.0014
Fcrit @ a=0.05	5.32	5.32	5.32	5.32
Decision	Same	Different	Different	Different

Table 5. Comparison between all of the Swedish mixtures

Comparison	Reference vs. polymer	Reference vs. AR	Polymer vs. AR
SEE(F)	0.1943	0.4723	0.5946
SEE(R)	1.3147	3.1729	1.3613
df(F)	11	9	12
df(R)	12	10	13
F*	63.444	51.465	15.472
df(a)	1	1	1
df(b)	11	9	12
P-value	0	0.0001	0.002
Fcrit @ a=0.05	4.84	5.12	4.75
Decision	Different	Different	Different

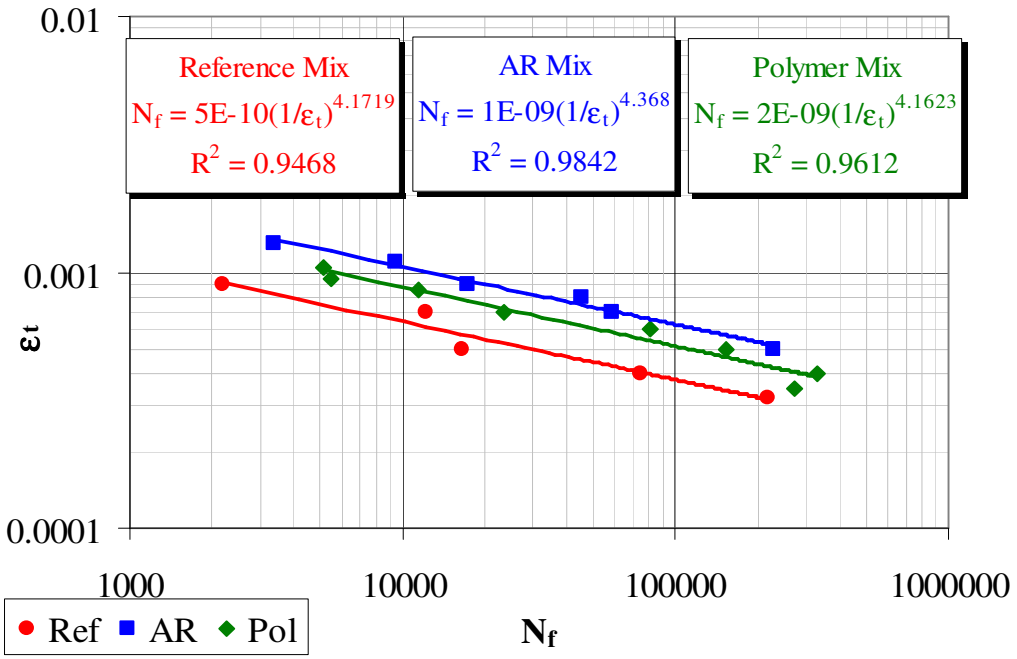

Figure 8. Comparison between all Swedish mixes at 21°C using N_f at 50% of the initial stiffness

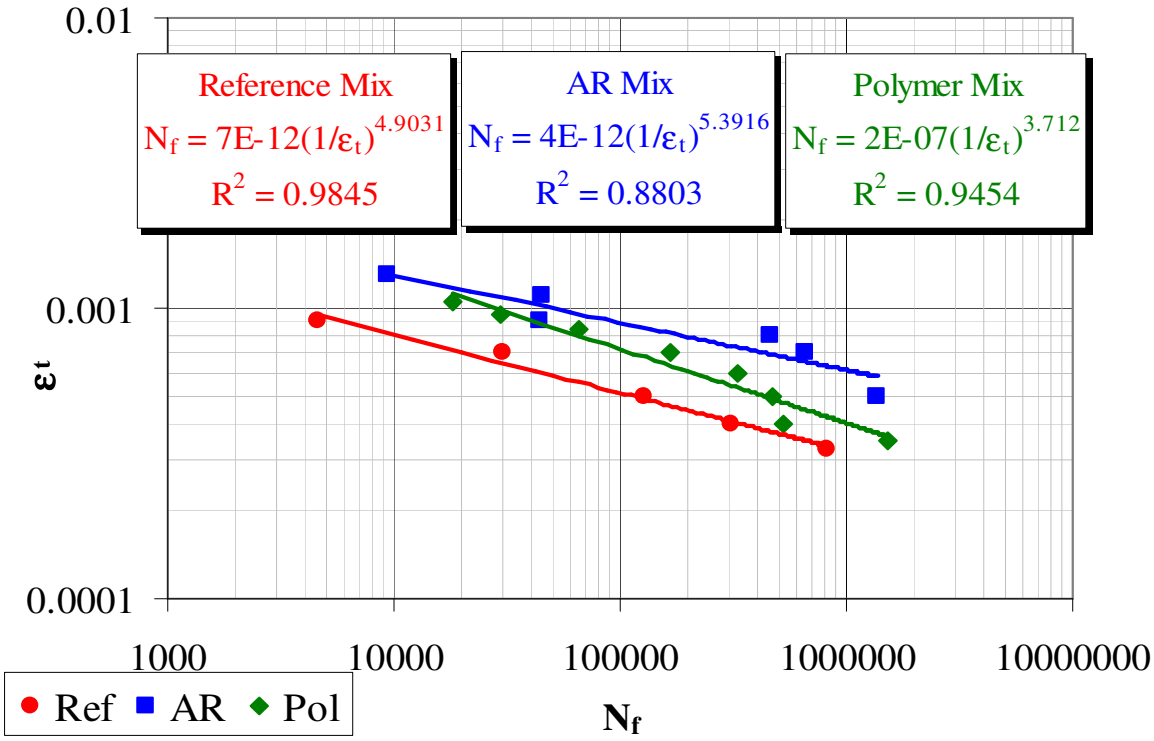

Figure 9. Comparison between all Swedish mixes at 21°C using N_f at 30% of the initial stiffness

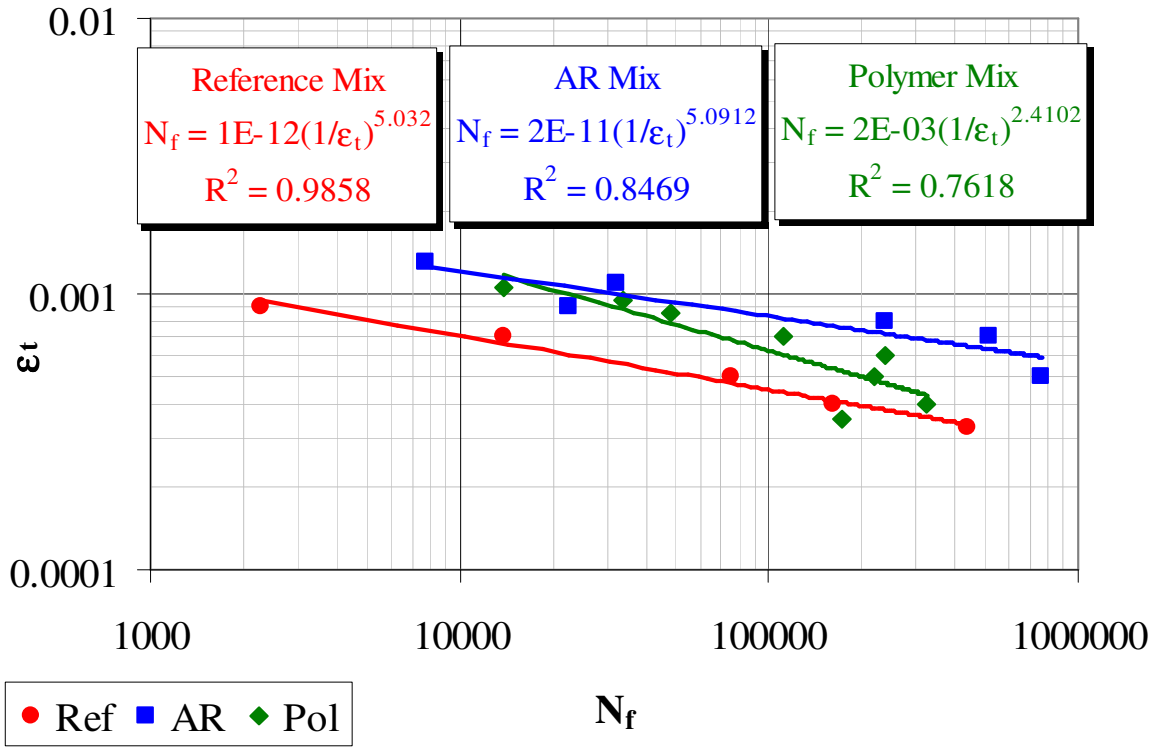

Figure 10. Comparison between all Swedish mixes at 21°C using Pronk's method

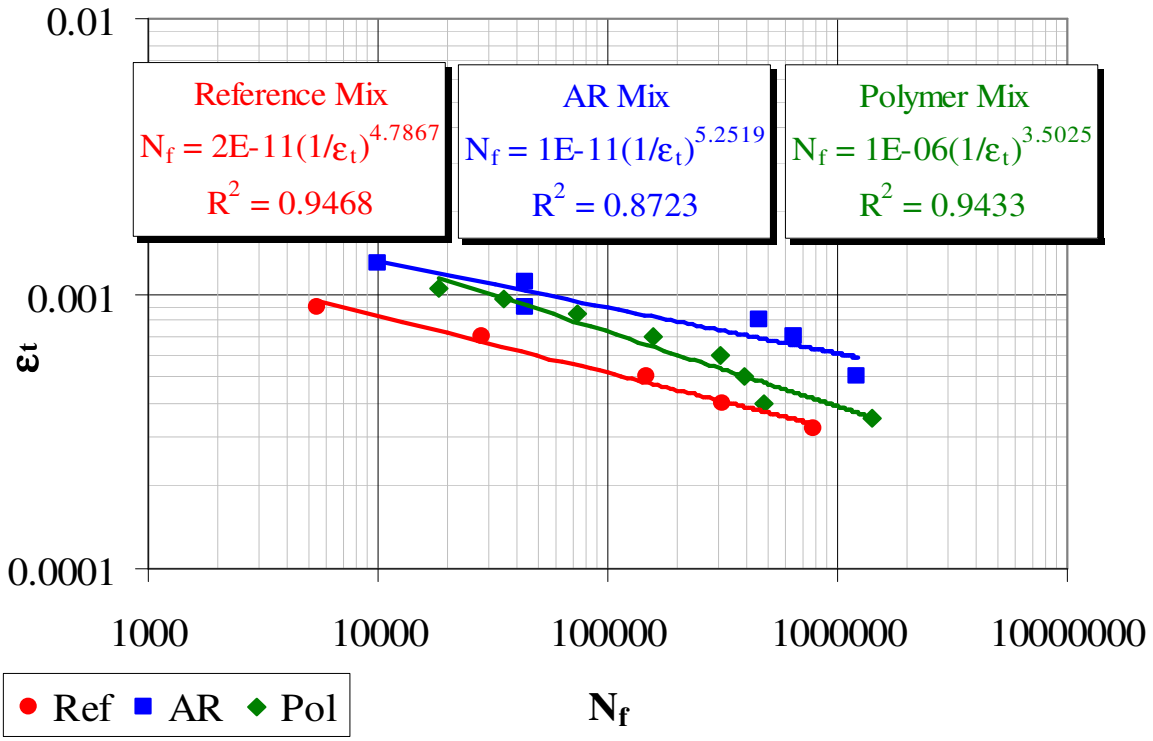

Figure 11. Comparison between all Swedish mixes at 21°C using the ASU method

Summary and Conclusions

Constant strain Flexural tests were performed according to the AASHTO T321-2003 and SHRP M-009 procedures to evaluate the fatigue performance of the Reference, Polymer, and AR Swedish mixtures.

The fatigue models developed for the mixtures in this study had excellent measures of accuracy and were rational in that lower fatigue life was obtained as the test temperature decreased. Moreover, dissipated energy concepts like the Pronk and ASU methods were applied to determine N_f.

Using a COANOVA statistical analysis approach, the AR mixture showed higher fatigue life than the other two mixes, the Polymer and the Reference mixes. The comparison was done at 21°C. The fatigue life of the AR mixture was approximately 27 times greater than the Polymer mix. On the other hand, the fatigue life of the AR mixture was about 91 times greater than the Reference mix. By adding rubber to the conventional mix, the HMA mixture was more flexible. As a result, it will last longer until it reaches failure.

The same COANOVA statistical technique was utilized to conclude that the conventional 30% reduction of the initial stiffness approach had the closest results as compared with the ASU method. Also, the ASU method provided very accurate results when compared with the conventional analysis methods. Moreover, by plotting the stiffness degradation ratio value (Ni*Si/So) versus the load cycles, a peak value could be obtained. Failure is then defined as the number of load repetitions at the peak value of that curve for both controlled-strain and controlled-stress modes. Other dissipated approaches have blurred criteria to define N_f.

Recommendations

Using a COANOVA statistical analysis approach, the Arizona State University (ASU) method which is independent on the mode of loading, temperature, frequency, or mixture formulation was concluded to be the most accurate method to analyze beam fatigue results. This method has the potential for unifying current fatigue analyses using a rational energy-based approach and it has a well-defined fatigue failure point compared to other proposed methods.

The recommended fatigue analysis approach is the ASU dissipated-energy method for the following reasons:

- It is a very accurate and reliable method; it was recommended from a previous national NCHRP 9-19 project [5].
- It is very convenient to define the failure point compared to other dissipated-energy approaches.
- It produces the same results that come from the current conventional 30% of the initial stiffness method.

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Biographies

MENA I. SOULIMAN is a PhD student who works as a graduate research associate of the Department of Civil, Environmental, and Sustainable Engineering at Arizona State University. He obtained his Masters Degree on Civil and Environmental Engineering from Arizona State University at 2009. His research interest is pavement analysis and design, pavement maintenance and rehabilitation, highway materials. Mena Souliman may be reached at mena.souliman@asu.edu

DEVELOPING A DIGITAL LOGIC DESIGN CURRICULUM IN ELECTRICAL ENGINEERING TECHNOLOGY: BRIDGING THE GAP BETWEEN INDUSTRY AND ACADEMIA

Nasser Alaraje, Michigan Technological University; Aleksandr Sergeyev, Michigan Technological University

Abstract

Hardware Description Language (HDL) and Field Programmable Gate Arrays (FPGA) have revolutionized the way Digital Logic Design is taught and implemented. Traditional ways of teaching logic design using discrete components, Transistor-Transistor Logic (TTL) and Complementary Metal Oxide Semiconductor (CMOS) have been replaced by programmable logic devices (Complex Programmable Logic Devices, CPLD, and FPGAs). Today, a more standard development process is widely used in industry. The process uses hardware description languages as a design-entry tool to describe the digital systems. The two most widely used hardware description languages in industry are Very High-speed Integrated Circuit Hardware Description Language (VHDL) and Verifying Logic (Verilog). This study aimed to reshape the way digital logic design is taught in electrical engineering technology programs. Instead of teaching topics and skills that are quickly becoming out-of-date and less important to employers, curriculum revisions were developed to match the current industry expectation of skills in hardware description languages and FPGA design. The new curriculum revision will provide students with a hands-on educational experience that is well-respected by industry.

Introduction

Although most traditional electrical and computer engineering programs have updated their curricula to include topics in hardware description language and programmable logic designs such as Field Programmable Gate Array (FPGA) and Complex Programmable Logic Device (CPLD), only 19.5 percent of four-year and 16.5 percent of two-year electrical and computer engineering technology programs at U.S. academic institutions currently have a curriculum component in hardware description language and programmable logic design [1]. To effectively meet the next generation's workforce needs, the electrical and computer engineering technology curriculum must be current and relevant and teach technology that is widely used in industry. To meet this goal, the School of Technology is stepping up to this challenge by updating the electrical engineering technology (EET) curriculum with two new courses to cover new concepts and skills in logic design; one in digital logic design using Very High Speed Integrated Circuit Hardware Description Language (VHDL) and the second in FPGA design. These curriculum revisions will provide EET undergraduate students the opportunity to learn concepts and hands-on skills in logic design that are highly marketable and address the needs of industry.

In this paper, the authors first describe the contents of the two new courses, one in hardware description languages and the second in programmable logic design. Following this is a discussion of how these courses can build the infrastructure of qualified senior students to conduct System-on-FPGA (SoFPGA) research projects in the School of Technology at Michigan Technological University.

Research Background

Historically, EET programs have included a traditional logic design course that covers topics in combinational logic and sequential logic circuits. The course is usually based on discrete components such as Transistor-Transistor Logic (TTL) and Complementary Metal Oxide Semiconductor (CMOS), and although these topics represent fundamental concepts in logic design and optimization theory, they are far from the most current industry practice in logic design. Topics that have been traditionally taught in logic design courses are less important to current employers. The time spent teaching Boolean algebra and how to minimize Boolean expressions using Boolean algebra or Karnaugh Map (K-Map) can be better spent teaching current and industry-relevant practice in logic design. This line of thought applies to both the design of combinational circuits and to the design of sequential circuits [1]. For the curriculum to adequately meet the current needs of the industry, EET programs must teach digital logic using VHDL and FPGAs [2]. Consequently, students will be equipped with design skills that are current, relevant and widely used in the industry.

Recent research also suggests that the proposed courses are industry-relevant. Furtner and Widmer [1] conducted an employer survey to rank currently taught logic design con-

cepts at Purdue University. The survey included questions about many topics that are heavily explained in logic design courses such as Boolean algebra, design simplifications using K-Map or Quine Mclusky, and design implementation using discrete gates. Each was given a low priority from the employer's perspective. On the other hand, topics that cover designing with a hardware description language such as VHDL or Verifying Logic (Verilog) received high-priority rankings from employers [1].

Unfortunately, curricula have not yet caught up to industry needs. A survey of digital design textbook users by Pearson Press shows that only 19.5 percent of the 52 four-year EET programs that responded to the survey cover topics in logic design using hardware description languages, and only 40 percent are planning to introduce hardware description languages in the near future [1]. According to Nie and Pecan [2], only six universities with programs in EET offer digital logic design courses integrated with VHDL and FPGAs. The research was conducted on 60 universities and colleges that offer EET programs. Of the remaining 54 universities, six have independent-study courses in hardware modeling and FPGA design.

Clearly, engineering technology programs are far behind in teaching the skills that represent current and future industry needs. As a result, the School of Technology is stepping up to this challenge by developing and introducing two new courses, one in hardware description languages and the second in programmable logic design. The major objectives of this curricular shift are to give the students in the EET program the opportunity to learn and experience logic design using FPGAs to meet current industry expectations. This will create a pool of informed electrical engineering technologists from which the industry can draw. This pool of students will also be given the opportunity to conduct undergraduate research in hardware modeling and Field Programmable Logic design.

Why FPGA?

Programmable Logic Devices in general and FPGA-based reprogrammable logic design became more attractive as a design medium during the last decade and, as a result, industrial use of FPGAs in digital logic design is increasing rapidly. As would be expected following changes in industry technology, the need for highly qualified logic designers with FPGA expertise is increasing at a fast rate. According to the U.S. Department of Labor, the job outlook is on the rise and will continue to expand for at least the short- to medium-term future [3]. To respond to industry needs for FPGA design skills, universities are updating their curricula with courses in hardware description languages and programmable logic design. Although most traditional electrical and computer engineering programs have updated their curriculum to include topics in hardware description language and programmable logic design, to date only 19.5 percent [1] of electrical and computer engineering technology four-year programs among U.S. academic institutions have a curriculum component in hardware description language and programmable logic design. Similarly, only 16.5 percent [1] of electrical and computer engineering technology two-year programs have a curriculum component in hardware modeling and programmable logic design.

The applications utilizing FPGAs as a design medium predominate [4]. FPGAs have been used extensively not only in logic emulation but also in custom-computing machines. The reprogrammable nature of Static Random Access Memory (SRAM)-FPGAs makes it the workhorse of many new applications that require reprogrammability. SRAM-FPGAs are the most popular FPGAs and are becoming the tools-of-choice in many reprogrammable applications. The reprogrammability features make them more attractive because they can be completely changed by the same electrical process. A microprocessor can be configured to run different applications and the configuration of SRAM-FPGAs can be changed for bug fixes or upgrades, making them an ideal prototyping medium. FPGAs have evolved from merely a glue logic device to a platform-based design medium. According to the International Technology Roadmap on Semiconductors (ITRS), we are approaching a four-billion-transistor chip by the end of this decade [5]. This will allow building of very complex, high-performance systems using FPGAs [5].

Platform FPGAs will dominate the embedded system design in the near future [5], and the capability to use a single programmable device that includes a processor capable of interfacing with programmable logic makes them the design of choice. As the price of FPGAs comes down, the development cycle shortens, and the time-to-market (TTM) pressure is reduced. As FPGAs become more widely used, the need for highly qualified logic designers with FPGA expertise will continue to increase, perhaps at an even more rapid pace.

Curriculum Revision

Figure 1 shows the current and proposed digital design logic sequence, which incorporates the addition of two new courses that will be added to the current course (Digital Electronics). The EET program will introduce two new courses (Digital Design Using VHDL and Topics in Programmable Logic). The descriptions of the two new courses are provided below. Each of these courses is three credit hours with two hours per week of recitation and three hours of lab. These two new courses were added without impact-

ing the overall degree plan. The current EET program has a shortage of courses in digital logic design; only one course (Digital Electronics) is currently offered. The EET program will still be structured as a 127-credit-hour program with 68 credits of technical courses in Electrical Engineering Technology. This is in line with ABET requirements [6]. As stated in the ABET Criterion 5 Curriculum, **"**Baccalaureate programs must consist of a minimum of 124 semester hours … and the technical content is limited to no more than 2/3 the total credit hours for the program" [6].

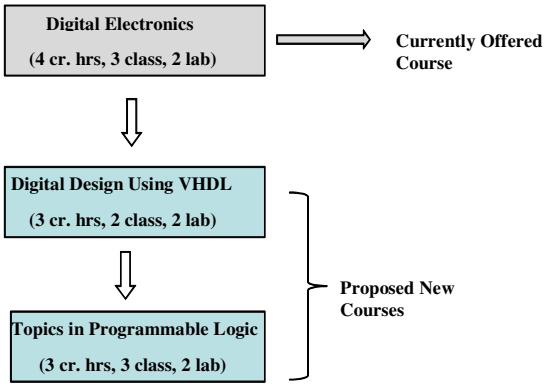

Figure 1. Proposed digital logic design course sequence

New Course 1: Digital Design Using VHDL

Course Objectives: This course places an emphasis on the language concepts of digital systems design using VHDL. The course will focus on good digital design practices and writing test benches for design verification. Low-level gate modeling techniques with varying timing details will be presented as well as a structural level of abstraction for wiring predefined gates and other predefined components. The information gained can be applied to any digital design by using a top-down design approach. Students will gain valuable hands-on experience in writing efficient hardware designs using VHDL and performing high-level HDL simulations.

The academic objectives of the "Digital Design using VHDL" course are to provide students with the skills and experience that they need to be competitive in the job market and as employees with high-value skills in the workplace. The students will learn the design of major components of digital systems, such as arithmetic logic units (ALUs), floating points, memory, and controllers using VHDL. In addition, the students will learn FPGA design flow beginning with HDL design entry and circuit simulation to verify the correctness of the intended design and writing test benches. To accomplish this in a one-semester course, the intent of lectures and labs is to have the students achieve the following:

1. Gain knowledge on programmable logic devices (PLD) and their design methodologies
2. Learn fundamental concepts of hardware description languages
3. Learn how to use HDL for modeling basic building blocks of digital systems
4. Learn about different design entry methods
5. Learn how to model digital circuits in hardware description languages
6. Learn how to use VHDL editors, debug designs and perform logic simulation
7. Learn how to use Altera's Quartus® II development software
8. Learn how to perform timing analysis and verification

Course Structure: The course "Digital Design using VHDL" is three credit hours with two hours per week of recitation and three hours per week in the lab. The course will be open for students with sophomore status or higher and the prerequisites are Circuits I and Programming Languages. The course will integrate Altera's Quartus® II development software, and the lab will use Altera's DE2 FPGA evaluation board.

New Course 2: Topics in Programmable Logic Design

Course Objectives: Due to industry's increased demand for FPGA designers, the intent of this course is to give students real-world experience in FPGA logic design and give them training with design tools widely used in industry. Tools used in the course will include Altera's Quartus® II development software and FPGA design implementation on Altera's DE2 FPGA evaluation board. The long-term objective of this course is to provide a learning opportunity that will result in research activities focused on FPGA design. This research will provide more in-depth training for senior students and will engage undergraduate students in applied research opportunities.

The academic objectives of the FPGA logic design course are to provide students with skills and experience in the FPGA design process. Students will learn FPGA design flow using Quartus® II [7] development software to develop an FPGA circuit simulation, starting from HDL design entry, followed by FPGA Synthesis for Altera FPGA devices, Place and Route and Timing Analysis. To accomplish this in a one-semester course, the intent of lectures and labs is to have the students achieve the following:

1. Learn how to use HDL for modeling basic building blocks of digital systems
2. Learn FPGA technology and the impact of using FPGA in logic design
3. Learn FPGA design flow using Altera's Quartus® II development software
4. Gain FPGA design experience by synthesizing, mapping, and placing and routing a given design on Altera's DE2 FPGA evaluation board
5. Work in groups of two or three to learn how to cooperate in teams
6. Learn to document their results

The designs are carried out using modern computer-aided design (CAD) tools, and the Altera's Quartus® II development software [7]. The final systems will be implemented with state-of-the-art devices such as the Altera FPGA device family and micro-controllers. Altera's DE2 evaluation boards will be used as the target platforms.

Course Structure: The course "Topics in Programmable Logic" is three credit hours with two hours per week of recitation and three hours of lab. The course will be open to senior students and the pre-requisite is "Digital Design using VHDL." The course will integrate Altera's Quartus® II development software. The lab will use Altera's DE2 FPGA evaluation board, which will be used as the target platform for lab experiments. Students will learn how to implement a complete system on the FPGA evaluation boards.

Altera Corporation is a market leader, holding a large market share in programmable logic. Each FPGA vendor development software package is device dependent; for example, Altera's Quartus® II development software only targets Altera's device family. Learning Altera's Quartus® II development software will give students the opportunity to learn FPGA design flow using the most widely used tools for FPGA design. At the same time, these skills are largely transferable to other design tools, so students will learn valuable skills useful across industrial platforms.

Undergraduate Research Opportunities: System-on-FPGA (SoFPGA) Research Project

New System-on-a-Chip (SoC) design techniques are necessary to address the communication requirements for future SoCs. The currently used bus-centered approach has become an inappropriate choice because of its limitation as a shared medium that restricts the scalability of the communication architecture. Also, long bus wires result in performance degradation due to the increased capacitive load. The long wires also consume more power to drive all of the Intellectual Property Cores (IP Cores) on the bus. A research project examining new communication architecture, the NoFPGA (Network-on-FPGA), for future System-on-FPGA (SoFPGA) [8] is currently under investigation by the primary author. The long-term objective of this project is to provide a learning opportunity at the School of Technology which will result in research activities focused on SoFPGA and hardware design modeling. This research experience will provide more in-depth training for undergraduate senior students.

SoFPGA Router Architecture: The SoFPGA model is based on IP router architecture as the basic building block of low-overhead-cost SoFPGAs. This router will be implemented as a VHDL model for Mesh and Torus topologies. Since an FPGA is a 2-D device, Mesh and Torus are the best topologies to interconnect IP cores on a reconfigurable SoFPGA.

SoFPGA Mesh Topology Router Architecture: The IP router is responsible for switching incoming packets on any of the five input ports (named North, East, South, West, and IP) to any of the five output ports based on header routing information. Figure 2 shows a block diagram of the Mesh topology IP router architecture; it shows the 5 input/output ports: North, East, South, West, and local IP.

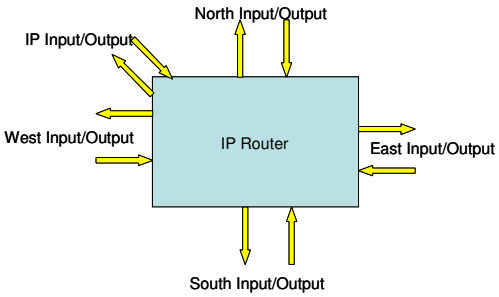

Figure 2. Block Diagram of Mesh SoFPGA IP router

The functionality of an IP router can be viewed as multiplexing and de-multiplexing five different data flows: the North, East, South, West, and IP directions. Each direction has a FIFO buffer. The IP interface to the SoFPGA translates the interface signals of the functional IP core to the NoFPGA packet format. All IP cores are implemented as independent IP cores.

The IP router is composed of a node controller and five port modules, one in each direction. The IP node controller is responsible for multiplexing the incoming five data flows on the outgoing five output ports; it also generates the handshaking signals for flow control. Figure 3 shows the block level diagram of the Mesh IP router; it shows the node controller as well as the five port modules.

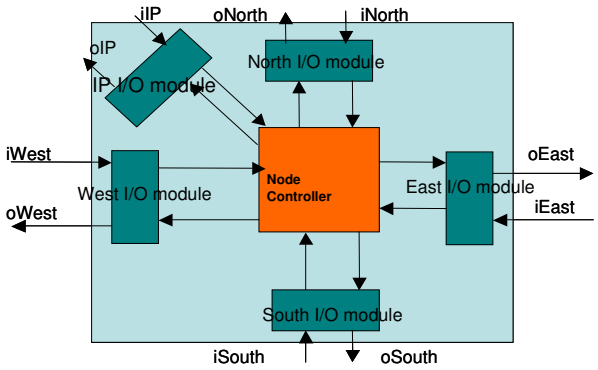

Figure 3. Mesh IP Router block diagram

The five I/O port modules connect the IP core to its five neighboring nodes: East, South, West, North, and the local IP core. The links are bi-directional and data flows in both directions. The X-Y routing algorithm is used with a directional flag bit to define whether data is moved in the positive–X direction or negative–X direction, as well as the positive–Y direction or negative–Y direction.

SoFPGA Torus Topology Router Architecture: In 2-D Mesh topology, the IP Router routes packets in all directions: North, East, South, and West. To simplify the routing logic, we will implement a simpler routing topology: the Torus. Torus is simply a 2-D Mesh folded along both vertical and horizontal directions. Packets will be routed in only two directions (East-West and North-South) in addition to the local IP direction. Figure 4 shows a block diagram of the Torus topology IP router architecture; it shows the two input/output ports, X (East-West) and Y (North-South), and local IP.

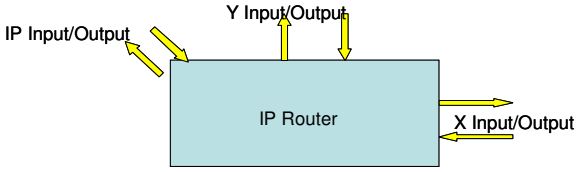

Figure 4. Block Diagram of SoFPGA Torus IP Router

The Torus IP router is composed of a node controller and three port modules (one in the X direction, one in the Y direction and one in the IP direction). The IP node controller is responsible for multiplexing incoming three-data flow on the outgoing three output ports; it also generates the handshaking signals for flow control. Figure 5 shows the block-level diagram of the Torus IP router; it shows the node controller as well as the three port modules.

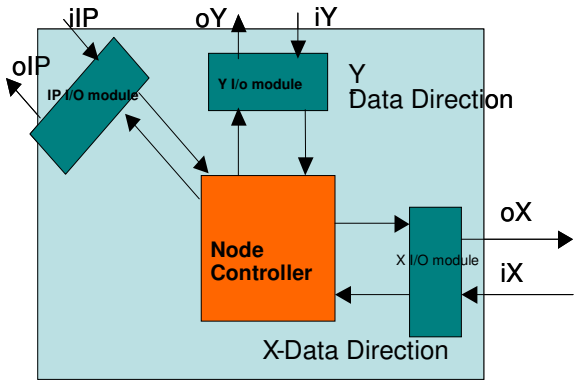

Figure 5. Torus IP Router block diagram

The three I/O port modules connect the IP core to its four neighboring nodes (East, South, West, North) and the local IP core by daisy-chaining the X-port module to form a horizontal circular ring and Y-port module to form a vertical ring. The same routing algorithm used for the Mesh topology IP router will be used with the Torus IP router (X-Y routing) but only along two directions, East and South, which in turn will reduce the complexity of the IP router.

The SoFPGA model is based on router architecture as the basic building block of low-overhead-cost SoFPGAs. Both Mesh and Torus IP routers will be modeled in HDL; senior students with skills gained from the FPGA design course will represent a good pool of research staff to implement this design. For the students, this will represent a real-world experience and will be beneficial for them when they start making career decisions. This router will be implemented as an HDL model for Mesh and Torus topologies.

Conclusion

With the demand of skilled FPGA designers on the rise, the objective of this paper was to present two new courses, one in hardware description languages and the second in programmable logic design, which will be a new addition to the EET program in the School of Technology at Michigan Technological University. Also, the authors proposed a reconfigurable SoFPGA (System-on-FPGA) architecture, which is a real-world experience for students to participate in and gain knowledge from. The research project offers the students the opportunity to work on a state-of-the-art current research problem. The goals of this curriculum revision are to give students a real-world experience with FPGA logic design and give them the necessary training with design tools used industry-wide. EET undergraduates will not only gain highly marketable skills and knowledge, but also will work with faculty advisors on applied research projects in

hardware modeling and programmable logic design. Such an approach to the education of engineering technology students meets the expectations of ABET accreditation standards by connecting students to the solutions of real problems.

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Biographies

NASSER ALARAJE is currently the Electrical Engineering Technology program chair as well as a faculty member at Michigan Technological University, he taught and developed courses in Computer Engineering technology area at University of Cincinnati, and Michigan Technological University. Dr. Alaraje's research interests focuses on processor architecture, System-on-Chip design methodology, Field-Programmable Logic Array (FPGA) architecture and design methodology, Engineering Technology Education, and hardware description language modeling. Dr. Alaraje is a Fulbright scholar; he is a member of American Society for Engineering Education (ASEE), a member of ASEE Electrical and Computer Engineering Division, a member of ASEE Engineering Technology Division, a member of Institute of Electrical & Electronic Engineers (IEEE), and a member of Electrical and Computer Engineering Technology Department Heads Association (ECETDHA). Dr. Alaraje may be reached at alaraje@mtu.edu.

ALEKSANDR SERGEYEV earned his bachelor degree in electrical engineering in Moscow University of Electronics and Automation in 1995. He obtained the Master degree in Physics from Michigan Technological University in 2004 and the PhD degree in Electrical Engineering from Michigan Technological University in 2007. Dr. Sergeyev is currently an Assistant Professor in the Electrical Engineering Technology program in the School of Technology at Michigan Technological University. Dr. Sergeyev research interests include high energy lasers propagation through the turbulent atmosphere, developing advanced control algorithms for wavefront sensing and mitigating effects of the turbulent atmosphere, digital inline holography, digital signal processing, and laser spectroscopy. He is also involved in developing new eye-tracking experimental techniques for extracting 3-D shape of the object from the movement of human eyes. Dr. Sergeyev is he is a member of American Society for Engineering Education (ASEE) and actively involved in promoting engineering education. Dr. Sergeyev may be reached at avsergue@mtu.edu.

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USING AN INDUSTRIAL ADVISORY COUNCIL FOR STUDENT OUTCOMES ASSESSMENT: A WORK IN PROGRESS

Thomas A. Seybert, Pennsylvania State University Wilkes-Barre Campus

Abstract

The Pennsylvania State University Surveying Program offers a two-year degree in Surveying Technology (TAC-ABET accredited) and a four-year degree in Surveying Engineering (EAC-ABET accredited). The program's Industrial Advisory Council (IAC) has been an active and effective partner in curriculum design, course review, and accreditation efforts. The council is chosen from members of professional surveying societies in Pennsylvania and surrounding states. This paper presents experiences with the IAC that have been helpful in supporting program missions and objectives. Particularly, the IAC has helped in assessing the achievement of student outcomes for TAC and EAC accreditation efforts.

Introduction

ABET requires engineering technology programs to form and utilize an advisory committee, board, or council from industry and the profession. The ABET Technology Accreditation Commission (TAC) explains the advisory committee as follows [1]:

> An advisory committee representing the organizations that employ graduates must be utilized to advise the program in establishing, achieving, and assessing its goals. The committee must periodically review program curricula and provide advisement on current and future needs of the technical fields in which graduates are employed.

Interestingly, the ABET Engineering Accreditation Commission (EAC) does not require engineering programs to establish an advisory committee [2]. However, most accredited engineering programs have advisory committees in order to keep their programs current in meeting the needs of industry and the profession.

As a result of a literature review and interviews with advisory board directors and members, Genheimer and Shehab [3] proposed eight primary purposes or objectives of advisory boards. They are:

- To advise the program on curriculum content to meet industry needs
- To provide input and feedback to help meet ABET accreditation criteria
- To provide input on program health and development opportunities
- To serve as an advocate for the program with administration, community, industry, alumni, etc.
- To assist with seminars, design projects, graduate placement, mentoring, etc.
- To help promote and coordinate research opportunities with industry
- To raise funds for school use from board member personal resources
- To use board member contacts and influence to raise funds from other sources

At Penn State, all engineering and engineering technology programs have an Industrial Advisory Council (IAC) which is expected to [4]:

- Act as an advisory group to each department (program) on specific academic and research issues
- Act as a link between the department (program) and its industrial and professional partners, providing an opportunity for communication of current and future industry and professional needs to the department (program)
- Identify actions that the College of Engineering should take to meet special departmental (program) needs
- Provide recommendations on initiatives that the department (program) or college should undertake to continuously improve educational and research efforts to meet the needs of the world and the profession

These two lists represent viewpoints from academia and advisory committees, and there is overlap between the two. Interestingly, academia does not specifically identify fund raising as an expectation. However, the advisory board directors and members are aware of this important activity.

This paper summarizes the activities of the industrial advisory council (IAC) of the Surveying Program at Penn State Wilkes-Barre, and explains efforts to directly include the IAC in student outcomes assessment.

The Surveying Program IAC

Penn State Wilkes-Barre is one of 24 campuses in the Penn State University system. It is small in size with an em-

phasis on teaching. In partnership with the College of Engineering, the Wilkes-Barre campus offers two academic tracks of study in surveying: the Associate of Engineering Technology in Surveying Technology (TAC accredited) and the Bachelor of Science in Surveying Engineering (EAC accredited). Since the programs are housed at a campus location with limited research opportunities or initiatives, the Surveying Program IAC focuses on curriculum issues, marketing, funding, and professional guidance. The council meets twice per year and consists of 10 to 14 professional land surveyors practicing in Pennsylvania, New Jersey, New York, and Maryland. The committee has been very active in evaluating the progress and effectiveness of the program in meeting the needs of the profession. Many changes in curriculum have been implemented based upon IAC recommendations.

Activities of the IAC

The Surveying Program IAC is involved in many activities which are typical of most councils. Over the past several years the IAC has addressed the following issues.

ABET Preparation

During the preparation for ABET 2000 accreditation visits (TAC and EAC) that included implementation of student outcomes assessment and continuous quality improvement, the IAC reviewed drafts of the program's vision and mission statements. They also reviewed drafts of program objectives and student outcomes, making suggestions for clarifying each and making sure the objectives met the needs of the surveying profession.

Before every ABET visitation (TAC and EAC), the IAC reviews a draft of the self-study report for the program. Particular attention is paid to the specific ABET criteria of students, program objectives, student outcomes, continuous improvement, curriculum, faculty, facilities and support. Suggestions are often provided by the IAC for ways to strengthen the report, and sometimes areas are identified that need further explanation. Suggested changes are discussed with the faculty, and the final adjustments are made to the self-study report before submission to ABET.

ABET Visits

When the program is visited for accreditation review by an ABET team, the fall IAC meeting is scheduled during the ABET visitation period. The ABET luncheon is attended by the program faculty, staff, students, campus administration, and IAC members. This provides the ABET team with direct access to the IAC for an entire day. This scheme has proven beneficial in the past, and is typically appreciated by the ABET review team.

ABET Review

After each ABET visit, the preliminary report provided by the ABET review team is shared with the IAC during the following spring meeting. Specific comments on each of the ABET criteria are reviewed in detail. The council members have the opportunity to provide input (with respect to the comments) and make suggestions for action to correct any concerns or weaknesses identified by ABET. In some cases, when the program faculty disagree with the ABET report, the IAC will assist in providing clarifying words for the formal response.

Marketing and Recruitment

The IAC is always asked to spread the word that there are plenty of job opportunities for graduates of the surveying program. The IAC members typically use high school visitations, company open houses, national surveyor's week events, and other activities to provide visibility for the program. Recruiting materials provided by the Pennsylvania Land Surveyors Foundation and Penn State Wilkes-Barre are used in these visits to assist IAC members in delivering an effective presentation. Some members are involved in the TrigStar [5] program, which is a national exam given to high school students interested in mathematics and computing. By design, this program exposes high school students to the mathematics of surveying and the surveying profession. Additionally, the IAC makes suggestions for university marketing and recruiting to increase and maintain enrollment in the program.

Curriculum Review

Periodically, the IAC splits into two subcommittees to review the Surveying Engineering and the Surveying Technology curricula. Outcomes are re-evaluated and course outlines with associated course outcomes are reviewed. These are checked to make sure that the sum of all courses supports the achievement of the program objectives and student outcomes.

Instruction Issues

The IAC often reviews the mathematics courses and assesses the quality of math instruction through interviews with students in the program. The quality of mathematics instruction is critical to success in the surveying program

curriculum. On a few occasions, issues in instruction have been identified, and the support of the IAC was helpful when approaching the administration about necessary changes.

Articulation

To increase enrollment and graduation numbers in the programs, the IAC suggested a joint meeting of surveying program administrators in Pennsylvania (Penn State Wilkes-Barre and Penn College of Technology) to examine the academic content and objectives of the two programs. The goal was to look for ways to increase enrollments in the baccalaureate program. This suggestion led to the successful development of a student articulation plan allowing for transfer from the Penn College of Technology surveying technology associate degree program to Penn State Wilkes-Barre's baccalaureate Surveying Engineering program. Since this arrangement, similar student articulation plans have been established for Gloucester County College in New Jersey and Paul Smith's College in New York.

Library Holdings

Periodically, a pair of IAC members is asked to visit the campus library to review library holdings related to surveying. Recommendations are made for the removal of outdated materials and the addition of new text and reference books to update existing holdings, or for the addition of new material in support of new technologies.

Laboratory Equipment

The IAC periodically inspects the surveying laboratory equipment room and assesses the equipment's appropriateness to meet the needs of the profession. Recommendations are made and used by the faculty leverage for securing university funds to purchase new equipment. The IAC also helps the program faculty to develop and maintain a 10-year equipment maintenance and upgrade plan to assist the campus administration in budgetary planning.

Student Surveying Society

Every year the president of the Penn State Surveying Society, a student organization, makes a report of student activities to the IAC. The IAC in return makes suggestions for new service activities to the profession, campus, and community. The IAC often suggests or finds funding sources that enable students to attend state and national professional conferences. Every year, typically 12 to 15 students attend the Pennsylvania state conference, and one to two students attend a national surveying conference using these funds.

Student Outcomes Assessment

At some point during the past 20 years, the Surveying Program chair suggested that the IAC consider meeting with graduating students of the Surveying Technology program to provide an informal exit interview. This was prior to the existence of the Bachelor of Science program, which graduated its first students in 1996. At that time, the program was administering paper exit surveys to the graduates. However, some problems identified through the paper surveys lacked detailed information to further explain the cause of the problem. Exit interviews were proposed as a method for gaining detailed information about specific problems. The IAC members agreed to administer exit interviews every semester through a face-to-face meeting with the graduating students.

The format of the exit interview meeting is a luncheon for the IAC and graduating students on the day of the regularly scheduled IAC meetings. Faculty and administration are not present at this session, so the students can speak freely without being identified. The interviews have a flexible structure that allows the council to take questioning in a direction that might provide more detailed and useful information to improve the program.

The IAC questions the students on a variety of issues such as curriculum, faculty, equipment, administration, and campus life. The interview structure is similar to the paper exit survey, so that it provides similar information, with additional details obtained via questioning. The format is very useful and helps faculty pinpoint specific causes of certain problems. This often leads to a quicker and more comprehensive solution to the problems.

With the advent of outcomes-based assessment of program success, the program chair suggested that the IAC ask the graduates about their perception, as a group, of their abilities with respect to each student outcome. The council agreed that this could be beneficial to the program, so during the spring 2007 exit interviews, the graduating students were separated into two groups, consisting of the associate degree students and the baccalaureate degree students, since each program has different accreditations (Seybert [6]). Each group was specifically asked about their perceived successful achievement of each student outcome. When a particular outcome is determined by the IAC to be unacceptable, the IAC members probe further to determine the cause of underachievement. This interview procedure yields very detailed information about why a student outcome is not being met, and allows a quick response to correct the problem.

The expanded role of the IAC in administering exit interviews was instituted prior to the incorporation of outcomes assessment in the ABET accreditation requirements. Thus,

outcomes assessment was added to the exit interview process as a bonus feature for data collection in student outcomes assessment. The IAC is still active in traditional assessment activities such as evaluation of student work in the senior seminar course. IAC assessment also complements the efforts of the faculty in documenting continuous program improvement through coursework or other student activities. The exit interview assessment practice is not used as a substitute for the accepted practices of assessment rubrics, course-to-outcomes mapping, performance criteria data collection, data analysis, and other common assessment activities performed by the program faculty.

Lessons Learned on Effective Implementation

During the first implementation of this exit interview format, three student outcomes were identified as unacceptable. A sample of the summary of findings is as follows.

Outcome 8: An ability to collect field data for map production

Mapping skills were adequate, but the surveying engineering students wanted exposure to more difficult mapping problems, including sight obstructions and inter-visibility problems. This was not an issue with the surveying technology students, since they take a required technology course in practical field problems that addresses the more difficult aspects of mapping. As a result of this finding, advanced elements of mapping were incorporated into some upper level surveying engineering laboratory exercises.

Outcome 10: An ability to apply the principles of metric photogrammetry with single and stereo pair aerial photographs

It was almost unanimous that this outcome was not being met in both programs. The students clearly articulated that the problem was a technical instruction issue in the student computer laboratory. The student lab was on a network that was causing data acquisition problems which were not discovered until the class was performing exercises. Labs were not effective. This observation was presented to the instructor of the lab, and measures were taken in the next course offering to correct this issue. These specific details were not discovered through the paper exit survey.

Outcome 14: A commitment to quality, timeliness, and continuous improvement

Some students commented that two or three faculty in the program would not penalize students for late work, even when the course outline clearly stated a penalty for late work. They felt that this was a measure of timeliness that was not being enforced. This problem was easily addressed the following semester.

Unfortunately, during the first implementation of this exit interview, the program chair did not convey the importance of recording a perceived level of achievement on all outcomes. The council recorded details only for outcomes that were perceived as unacceptable. Therefore, only three student outcomes were assigned a specific level of achievement. The other student outcomes could only be identified as achieved at an acceptable level, without any further definition of achievement level. Additionally, the paper exit surveys were not collected prior to the IAC exit interview. This information, if summarized and made available during the exit interview, would be very helpful to the IAC in terms of quickly identifying unsatisfactory outcomes, thus allowing the council to spend more time on those outcomes that needed attention. Furthermore, the IAC was not given a rubric for the assessment process, making the consistency of their evaluation methods somewhat uncertain.

During the following two years (2007 to 2009), implementation of the exit interviews met with both success and failure. Administrative snags caused some interviews to provide limited or no results. In one case, an inadvertent oversight of the administration caused a very late call for the IAC meeting, and only two IAC members and one student attended the exit interview. For reasons of confidentiality, the interview was cancelled. In another case, the verbal instructions to the council for administration of the interview were not clear, causing some confusion. Some results were obtained, but the student groups were not separated properly, so the results could not be applied consistently to the correct program (associate degree versus baccalaureate degree), thus making some of the results invalid for either degree. Another semester, the program chair was new to the position and did not understand the process used in the past. Instructions were either lost or given incorrectly.

Proposed Exit Interview Procedures

To avoid problems of process, it will be proposed to the IAC and the program chair that exit interviews beginning spring 2011 will follow a set of written procedures approved by the IAC and program faculty. The proposed exit interview procedure is as follows.

The IAC chairperson will appoint two council members who agree to be exit interview chairpersons: one for the sur-

veying technology program and one for the surveying engineering program. The remaining number of council members will be divided to complete the two exit interview teams.

Prior to the IAC semester meeting:

1. The program chair will administer and compile results of the exit survey to graduating students. The survey will be administered using SurveyMonkey™ and the compiled analysis will be shared with the exit interview chairpersons.

2. Student outcomes assessment worksheets specific to the program will be sent to the exit interview chairpersons. Assessment worksheets will include a set of skill/knowledge descriptions to be used by the interview chairperson during questioning.

3. A rubric for assessing level of achievement of each skill/knowledge supporting each student outcome will be provided to the exit interview teams. The rubric provides guidance for consistent assessment of level of achievement. See the example worksheet in Appendix A which was created based upon an example assessment-planning matrix proposed by Rogers [7].

During the exit interview:

4. The interviewer will pose questions one by one to the student group, which will be directly related to the skills/knowledge listed in the individual outcomes worksheet. Three levels of achievement (2 = exceeds, 1 = meets, 0 = does not meet) will be provided. As questions are posed to the graduating student group, the interview chairperson will mark the perceived level of achievement on the worksheet for each skill/knowledge description. Using the results of this questioning, the interviewer will record a summary (average) score (between 2 and 0) for the student outcome.

5. If the summary score for the outcome varies significantly from the score obtained from the graduate exit survey (Survey Monkey™), a reason for the difference will be pursued and recorded if possible.

6. If the outcome is marked with a level less than 1.0, the interview team will question the group further to explore reasons why a satisfactory rating was not achieved.

7. Reasons for lack of achievement will be verbally summarized and repeated back to the graduating students to make sure that what was heard matches what was recorded. Once both interviewer and interviewees agree on correctness and the response is recorded on the worksheet, the interview chairperson will proceed to the next outcomes assessment worksheet.

8. At the completion of the student outcomes assessment questioning, the exit survey will move to other topics related to the academic experiences of the graduating students such as campus environment, classroom facilities, laboratory equipment, computing facilities, faculty, and other program and campus quality issues.

Immediately after the exit interview:

9. The overall results will be summarized immediately after the exit interview by the recording team secretary. Results will be shared with the faculty and administration on the same day as the exit interviews.

10. During the feedback session, the complete exit interview worksheets on student outcomes will be given to the program chair. These worksheets will become part of the program's continuous quality improvement documentation for the next ABET review.

It is believed that the consistent implementation of these instructions will improve the quality of information obtained through the exit interviews. As the instructions are reviewed, approved, and implemented, the results of successive exit interviews will be reviewed. Improvements to the instructions and process will be made and re-evaluated annually.

Conclusions

The Penn State Wilkes-Barre Surveying Program utilizes its Industrial Advisory Council (IAC) to administer exit interviews to graduating students. Part of the interview is direct questioning of the graduates on their perceived level of achievement of each student outcome. The IAC summarizes the general response by the group on each outcome. If the general response is below a specified level, the IAC members question the students to determine the finer details of the problem(s) behind the lack of achievement. The summary exit survey acts as a form of assessment used by the program to support ABET accreditation documentation. Additionally, the finer details, which typically cannot be extracted from paper or Web-based surveys, are very helpful in identifying changes to the program that will increase the level of achievement in the student outcomes. Although the outcomes assessment process has experienced problems with

implementation, improved future exit surveys should provide an excellent resource for documenting outcomes achievement.

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Biography

THOMAS SEYBERT is an Associate Professor of Engineering at Penn State Wilkes-Barre. He instructs undergraduate students in surveying technology and surveying engineering. He is the Director of Engineering Technology and Commonwealth Engineering for the Penn State campuses offering College of Engineering programs. His academic specialty is land development and storm water management. He is the author of *Storm water Management for Land Development* [2006], published by Wiley. Dr. Seybert can be reached at tseybert@psu.edu.

APPENDIX A: Example IAC Worksheet Date: _____ Recorder: _____

SUR E Student Outcome 4: Students will demonstrate the ability to work effectively in multi-specialty teams.

Skill/knowledge	Supporting Courses	2 Exceeds	1 Meets	0 Does not meet	Rating
1. Produces research information for the team	EDSGN 100, SUR 241, SUR 372W, SUR 482	Provides comprehensive and relevant information in a timely fashion to support the team project completion	Provides satisfactory information necessary to complete the team project on time	Does not provide satisfactory information to complete the project, either in quality or timeliness	
2. Demonstrates an understanding of team role when assigned	EDSGN 100, SUR 241, SUR 372W, SUR 482	Accepts team role and completes duties in a timely and professional manner to complete the team project	Accepts team role and adequately completes duties to complete the team project on time	Does not accept team role, or does not complete duties in a timely manner for project completion	
3. Shares in the work of the team	EDSGN 100, SUR 241, SUR 372W, SUR 482	Completes assigned and other work as needed to complete the project in a timely and professional manner	Completes assigned work as needed to complete the team project on time	Does not complete assigned work necessary for project completion	

Exit Survey estimated level of achievement: _____

Exit Interview estimated level of achievement: _____

Reason for disparity in evaluations:_____

_____

Student reasons for poor outcome: _____

_____

_____

Student/IAC suggestions for improvement: _____

_____

_____

MEETING STUDENT AND INDUSTRY NEEDS THROUGH EXPERIENTIAL LEARNING AND SOFT SKILLS STUDY IN COMPUTER GRAPHICS

Jana Whittington, Purdue University Calumet; Kim J. Nankivell, Purdue University Calumet;
Joy L. Colwell, J.D., Purdue University Calumet

Abstract

Students in a Computer Graphics (CG) degree program need a variety of real-world portfolio projects and experiences before graduation in order to prepare them for their careers. One way to incorporate real-world experiences is to use experiential learning (EL) components in the CG curriculum. Faculty within a CG degree program would benefit from an understanding of the experiential learning instructional methodologies to pedagogically develop curricula for an EL course in computer graphics.

Generally, employers who hire CG graduates want proof of real-world experience and often ask for a minimum of three years of experience in the field. Real-world experience, to employers, often includes not only the technical skills but also the soft skills of teamwork, appreciation for diversity, and communication. Traditional classroom learning, as well as traditional classroom simulations of real-world portfolio projects, may not always fully prepare the learner for the CG work environment. Conversely, immersing a student in the real-world CG work environment may not always provide the needed pedagogical structure that will fulfill EL requirements or standard course and program requirements. Incorporating soft skills classes into a CG plan of study can help provide the other component of real-world skills that employers seek.

In this study, the authors addressed how EL can be implemented into a CG course or program structure, which will provide a significant transfer of learning through involvement with real-world projects.

Introduction

Students in a Computer Graphics (CG) degree program need a variety of real-world portfolio projects and experience before graduation to prepare them for their careers. One way to incorporate real-world experiences is to use experiential learning (EL) components in the CG curriculum. Generally, employers who hire CG graduates want proof of real-world experience and often ask for a minimum of three years of experience in the field. Real-world experience, to employers, often includes not only the technical skills but also the soft skills of teamwork, appreciation for diversity, and communication. Soft skills are distinguished from hard science and technical skills or subject matter skills, and are generally understood to include the non-technical requirements of such accrediting bodies as the Technology Accreditation Commission, (TAC) [1] of the Accreditation Board for Engineering Technology (ABET) [2] or the Association for Technology, Management, and Applied Engineering (ATMAE) [3], or those skills which make students work-ready. Traditional classroom learning, as well as traditional classroom simulations of real-world portfolio projects, may not always fully prepare the learner for the CG work environment. Conversely, immersing a student in the real-world CG work environment may not always provide the needed pedagogical structure that will fulfill EL requirements or standard course and program requirements. Incorporating soft skills classes into a CG plan of study can help provide the other component of real-world skills that employers seek. Faculty in CG disciplines need to be conversant in EL to help structure their courses in ways that will give their students real-world learning. CG departments and programs would be well-served to make their faculty aware of current thinking in EL. Experiential learning needs to be clearly understood and easily assessed by faculty to make it possible to incorporate EL components into their courses.

The lens of this experiential learning paper is based on constructivist theory, examination of experiential learning theory, empirical data and evidence from actual experience [4]. The constructivist learning environment is authentic, case-based, problem-based, flexible, and assists the learner from introductory knowledge acquisition to expertise in knowledge acquisition [5]. Flexible constructivist learning practice has facilitated the growth of experiential leaning practice. An empirical case exemplifies the results of students who have given input as to the results of their experience. For example a student recently presented his experience (along with two faculty) at the ACM SIGGRAPH 2008 conference and in an experiential learning workshop held at Purdue Calumet about his experience [6]. The results of the experience reveal a gradual introduction to experiential projects over a three-year period in the undergraduate graphics program. Portfolio examples presented by speaker Jeff Noy at the ACM SIGGRAPH 2008 conference, described how the new authentic knowledge related to the

graphics field and soft skills were enhanced from the experience. "This experience is like no other at the college level. What I learned could not be more relevant or important to building knowledge and career through experience" [6]. He further stated that the authentic problem-solving experience proved to be more than any group project or class project. The results of the compilation of different authentic experiential experiences resulted in a full-time position within a graphics company, expansion of the business, and opened up doors for up-and-coming experiential learners.

Other student comments include those by Richard Smosna, who completed a project while working with Allied Electrical: "Whether you want to freelance or work for a big company, you have to find a way to get your foot in the door" [7]. Having been through the experience with his senior design project, "I'm not scared to go out and talk to companies. They were very welcoming to me" [7]. Student Charles Kellar stated: "School will teach you all the theories of doing the work, and give you the tools," notes Kellar, who put together a Web site for a family business, Gene Kellar Productions. "But until you actually do it, you don't understand how you'll work under pressure, how much time it will take" [7]. Christopher Nawracaj interned with Deep River Water Park in Hobart, Indiana, and as a senior design project redesigned the entertainment center's Web site. "It looks a lot better showing you've done something for a corporation or had an internship, rather than just your class work, stated Chris Nawracaj" [7]. In 2010, Chris completed a social networking research project and a master's degree, which was an extension of the undergraduate EL experience.

As stated by Beard and Wilson [8], an appropriate identification of EL methodologies and criteria needs to be accessible to faculty as well as assessment methods for evaluating the EL course. EL requirements go beyond the mere inclusion of real-world experiences in a course. Learning occurs when students participate in an activity, reflect upon the activity, use analytical skills to derive useful insights from the experience, and then incorporate this into a new understanding to apply in their daily lives [9]. Experiential learning captures the interest and involvement of the participants, but most importantly it contributes significantly to the transfer of learning. Therefore, EL requires not just the experiences, but the act of understanding the significance of the experience. In conclusion, there must be the component of reflection and an understanding of what this means for the students' professional development [6].

While experiential education is not a new concept, the extension of experiential education components in a structured manner throughout an undergraduate CG degree curriculum is a new development, supported by renewed interest in experiential education. Incorporating EL in a structured manner throughout a curriculum requires the ongoing support of administration and faculty, and presents some issues beyond those generally experienced by a single faculty member incorporating EL in a single class under his or her control. In this study, the authors explored some of the multi-level issues experienced in incorporating EL across a program, requiring the understanding and cooperation of multiple faculty members in the discipline.

Instructional Intervention

To implement EL in a degree program, faculty need to be made aware of the experiential criteria so they can design an appropriate and effective EL course. Faculty at Purdue University Calumet gain insight about EL through workshops and information provided by the National Society for Experiential Education [10], [11]. Once the National Society for Experiential Education standards of practice for EL have been defined within the course, faculty in the CG program can share pedagogies for best practices through the syllabus and introductory materials. This pedagogical communication among faculty will help to elicit best practices and program assessment methods for an EL course and program objectives.

Benefits of Experiential Learning

The real-world experience will be reflected in the learner EL portfolio. The EL portfolio goes beyond the traditional classroom assignments reflected in a student portfolio and provides an insight for potential employers about the student's real-world experience. This EL portfolio tells the potential employer that the learner has practiced specific CG technical and soft skills on the job. This EL course opportunity also permits the EL learners to apply teamwork, appreciation for diversity, communication and CG copyright law considerations to real-world CG on-the-job experience. This insight into student experience will make the students and graduates more desirable candidates in the job market, since employers will know that the students are work-ready and will not need the same level of training in professional skills as those who do not have demonstrated experience. By implementing EL in various courses at various levels, students will develop an extensive EL portfolio, and an effective program-wide assessment method can be established. This gives faculty the opportunity to learn and implement the EL standards both in coursework and throughout the program.

If Need Is Not Addressed

If the learning need is not addressed, students will not have a defined or recorded EL experience course within the degree program. They also will not have, or are less likely to

have, a working knowledge of the legal and ethical situations related to the computer graphics profession, nor will they have quality real-world exposure by the time of graduation. Graduates are, therefore, less desirable to employers who will have to invest some time in filling in the gap between technical skills and soft skills and their application in the workplace. Those graduates will be slower in reaching full productivity than those who have already mastered these skills.

Communication Benefits

The students benefit from the multifaceted learning experience, and are strengthened by peer-to-peer interaction, employer-to-learner interaction, and teacher-to-learner interaction. These multiple levels of communication can enhance the students' communication skills. The teacher-to-learner interaction in EL takes place in scheduled face-to-face meetings and through weekly logs submitted by the learner. The instructor has the opportunity to respond to logs for more clarification. The learner, through log submissions, has the opportunity to synthesize each workweek and reflect on his or her EL experiences. EL work-related problems could be discussed with the instructor on a weekly basis to help the student address any on-the-job issues which might arise. The learner is required, through logs and final portfolio reflections, to reflect on work-related problems and successes.

The classroom peer-to-peer interaction takes place through weekly blogs where students share experiences with one another within a course setting. Students within a course setting may be working on different types of EL projects but share the requirement to reflect on those various experiences. By sharing the experience, learners have the opportunity to learn from one another about similar and different work experiences. These reflections go beyond the classroom-learned experience and provide experiential reflections to aid in the educational experience. Peer-to-peer interaction also takes place when students work together on an EL project as a group. The makeup and organization of the learner group as well as the experience of working with real-world clients goes beyond the classroom group project simulation. Client involvement adds to the dynamics of communication within the work place. Working well with others is a common job requirement, and the triangulation of group communication and client-group communication is a valued soft skill needed for CG graduates. Blogs are used by learners to a) define their roles within the EL project, and b) report weekly progress within the EL group project. Each group member is still required to submit a weekly log to the instructor as well as meet with the instructor to reflect on and discuss experiences. This gives the instructor an insight into the individual student's progress. Another benefit to the peer-to-peer group interaction is the opportunity to learn and update CG knowledge, since technology is ever-changing. Instructors and learners have the opportunity to address complex issues and suggest alternatives. The EL learner then has the opportunity to synthesize information from multiple sources as well as contribute to the resolution of an issue. Many course management systems can help an instructor provide convenient blogs, journals, etc. for their EL students.

Soft Skills

Soft skills are commonly understood to include those skills which professionals must possess in addition to their technical skills in order to be effective in the workplace. Those skills variously include effective oral and written communication, interpersonal skills, ability to work effectively on a team, time management and planning, conflict resolution, ethical decision-making, continuing self-education, and leadership [12].

The importance of soft skills can be seen in the Technology Accreditation Criteria for the Accreditation Board for Engineering and Technology [2]. TAC/ABET Criterion 2 lists the eleven areas of expertise a graduate must possess upon program completion, known as the "a-k" criterion [1], [2]. Under this standard, an engineering technology program must demonstrate that graduates have:

a) an appropriate mastery of the knowledge, techniques, skills and modern tools of their disciplines;
b) an ability to apply current knowledge and adapt to emerging applications of mathematics, science, engineering and technology;
c) an ability to conduct, analyze and interpret experiments and apply experimental results to improve processes;
d) an ability to apply creativity in the design of systems, components or processes appropriate to program objectives;
e) an ability to function effectively on teams;
f) an ability to identify, analyze and solve technical problems;
g) an ability to communicate effectively;
h) a recognition of the need for, and an ability to engage in lifelong learning;
i) an ability to understand professional, ethical and social responsibilities;
j) a respect for diversity and a knowledge of contemporary professional, societal and global issues; and,
k) a commitment to quality, timeliness, and continuous improvement.

Less than half of the eleven criteria apply to technical areas. All others cover soft skills (i.e., communication, teamwork, problem-solving and appreciation for diversity), and as a technology program these standards have relevance

for computer graphics technology. The purpose of the EL process is to allow students to combine their technical skills with the soft skills important to a technical profession. EL requires the students to go beyond the 'safe' environment of the classroom and practice their soft skills in a realistic setting.

The Association of Technology, Management and Applied Engineering [13] also considers non-technical skills. In its standards for baccalaureate accreditation, industrial work experience is considered. In the 2009 Accreditation Handbook, Section 6.3.10 covers Industrial Experience. "Each program of study shall include appropriate industrial experience such as industrial tours, work-study options/cooperative education, and/or senior seminars focusing on problem-solving activities related to industry. Industrial experiences shall be designed to provide an understanding of the industrial environment and what industry expects of students upon employment " [3].

Both of these major accrediting bodies recognize the importance of students' preparation for the work world, a need that EL can help programs meet.

EL Integration within a CG Program

Faculty interested in teaching EL within a CG program have defined capstone EL courses at various levels of instruction. Courses defined at the 100, 200 and 300 levels have an EL component within the course. This means that the course has a client-based project after specified classroom materials are delivered and assessed. This gives the learner the opportunity to apply newly learned knowledge in a real-world application. With this stair-step approach, students also have the benefit of classroom instruction in conjunction with an introduction to work-force situations at the entry level. By implementing EL in a smaller project at earlier levels of instruction, students are able to build EL knowledge and are better prepared for an immersive EL experience in the upper program course levels. The EL 400-level courses consist of the full EL experience, where students work individually for employers or participate in individual and group-client-defined projects outside of the traditional classroom setting. An online course management system, as described above, is used to aid in the pedagogical delivery of the fully developed EL course. Course sites can house log submission, blogs and discussion boards, and can provide a central location for various EL students to share reflective observations.

Process: Implementing an EL Course

The following are key questions which CG faculty and programs can consider as a guide to analyzing the prospect of offering EL courses.

a) What are the learning objectives and perceived outcomes of the experiential course, and how are they accomplished?
b) How can the learning objectives be experienced through reflection?
c) Where will the skills, practices and experiences occur outside of the university setting?
d) What professional groups, businesses or non-profits are accessible to the instructor and student?
e) How will the site objectives correspond to the course objectives?
f) How will the course objectives relate to the program objectives?
g) When and how should the sites be identified and contacted?
h) What is the course enrollment, and how many students should be enrolled in one experiential course?
i) What pre-site activities are required to prompt, organize and enhance the experiential learning objectives?
j) How will students be assigned to an experiential course to receive credit?
k) How will a site contract be prepared?
l) What reflection activities will best develop student learning from experience?
m) How will reflection be evaluated and assessed?
n) How will the experiential course be validated within the university?

Key Methods

If a CG program finds it desirable to implement an EL course or series of courses, the following points can be used as a guide to aid the program with the implementation.

a) The program should disseminate information about experiential learning initiatives through surveys to gain feedback and assess the interest in or need for EL in the program.
b) Faculty interested in teaching an EL course should attend workshops where EL experts will speak about their experiences and disseminate materials to aid in creating a successful EL course. The National Society for Experiential Education [10] mentioned above is an excellent resource to help faculty get started with the principles and standards of experiential education.
c) The program should poll faculty to identify those who might be interested in teaching EL courses.
d) The CG program should collect information from potential EL site employers to gain an insight into the

feasibility of an EL course incorporating employer projects or work experiences. A campus career development or placement office may be of assistance with this part of the process.

e) The faculty should identify courses that might have an existing EL emphasis or component within the degree program.
f) The faculty should identify components within the course where learners will need to have prior knowledge before engaging in an experiential project.

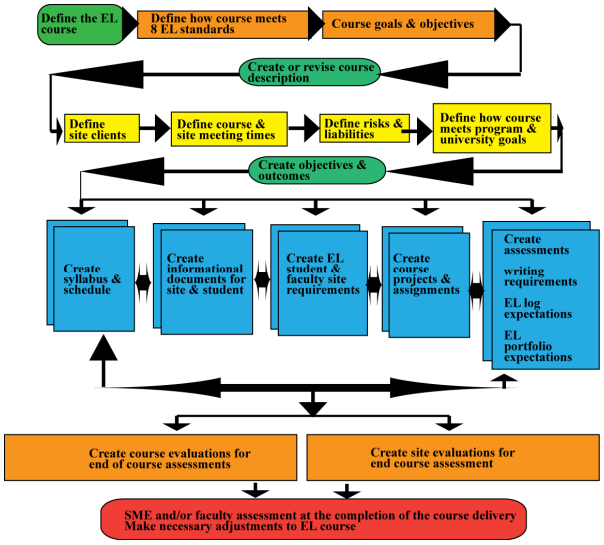

Figure 1. Flowchart for faculty to implement EL courses within a degree program

Conclusion

In the authors' implementation of this concept, several discoveries were made. The following discovery points have led to the recommendations listed below.

Discoveries

a) There are faculty who are interested in developing and teaching courses that meet the EL standards.
b) EL is a valuable complement to formal classroom instruction. It can enhance learning through the transformation of experience [4].
c) Six courses were identified as potential EL courses which could be offered within the CG degree program.
d) EL education is both philosophy and pedagogy [9].
e) Faculty within the CG program will be able to help students transform experience into knowledge through EL.
f) Through EL courses, faculty will be able to assist students in obtaining valuable real-world experience and relevant portfolio projects, including soft skills experience.

The following recommendations are the result of the planning and assessment process for developing program-wide EL, and faculty experiences in attempting to implement EL on a program-wide basis.

Recommendations

a) The CG degree program needs to define and implement a plan to develop EL into each experiential course.
b) The faculty within the CG program need to define the pedagogical standards for each course as it relates to the degree program.
c) Pedagogical standards for each course can be defined using the National Society for Experiential Education standards [10].
d) An assessment method needs to be established for EL courses.
e) Curriculum documents need to be generated for designated EL courses so that they are easily identified in the course catalog. This is especially important where campuses have EL requirements for students in order to graduate.
f) Course load for faculty teaching an EL course needs to be established. EL courses can be time-intensive for faculty, especially if the faculty members are recruiting client projects or employers to participate in the EL course.
g) Potential EL sites need to be identified.
h) Faculty who wish to develop and teach an EL course need to attend EL workshops to gain a better understanding of the EL standards and practice as well as an understanding of how to avoid risks and liabilities associated with an EL site.
i) University strategies need to be developed to avoid or mitigate risks and possible liabilities for any areas of concern.

Although program-wide implementation of EL courses can be a daunting task, the benefits for students are undeniable. The resultant growth in technical and soft skills will yield better-qualified graduates. The online environment has provided an opportunity for offsite communication for both peer-to-peer and instructor-to-peer situations. Many students work within the labs on campus and share their EL experiences with newer students. This helps to build and enrich the learning environment. Students have the opportunity to participate in a professional experience, while the teacher becomes the coach and guide to aid in learning. The benefits of the real-life portfolio have already proven to be instrumental for students in gaining employment after education. Many students gain employment while in school via the EL experience. The official implementation for the EL initiative began in Fall 2008 for the University as a whole. Companies

in the area see it as a benefit and have been cooperative in helping to build the opportunities. The CG program has already partnered with local companies. One such local company has expanded its business based on the CG interns who were hired near or after graduation.

Future Study

This study focused on the issues involved in the implementation of EL throughout the CG program. Areas for future study include assessment after implementation of the EL initiative in the CG program at both the course level and the program level. Assessments will include the courses with EL components, collecting data from students with EL experiences, and surveying employers/clients who have provided EL experiences for students in the program.

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Biographies

Dr. JANA WHITTINGTON has a Ph.D. in Education with a Specialization in Instructional Design and Online Learning from Capella University, Minneapolis, Minnesota, US, 2010. Additionally Dr. Whittington has a MA in Studio Art and Humanities from California State University, Dominguez Hills, CA, US, 2000; a BFA in Studio Painting from Northern Arizona University, US, 1996 and; AA in Graphic Design from Yavapai, College, Prescott, AZ, US, 1993. She has taught a variety of courses for 15+ years in fine art, graphics, multimedia, video, web design, and research methods at the graduate, undergraduate levels. Course delivery methods include online, hybrid and traditional delivery and she has been a faculty mentor for distance education. In addition to current tenure teaching assignments, Dr. Whittington has created e-learning materials for parole and probation officers to be delivered internationally. Dr. Whittington has an active publication and a grant record. Dr. Whittington may be reached at whitting@purduecal.edu.

Dr. KIMBERLY JAMES NANKIVELL received his Ph.D. degree in Information Technology from Capella University, Minneapolis, Minnesota, in 2011; a Master's degree in Information Technology from American Intercontinental University, Hoffman Estates, Illinois, in 2003 and; B.S. degree in Marketing from the University of Arizona, Tucson, Arizona, in 1974. Dr. Nankivell is currently an assistant Professor of Computer Graphics Technology at Purdue University Calumet. Dr. Nankivell has an active publication record. Dr. Nankivell can be reached at nankivel@purduecal.edu.

JOY L. COLWELL, J.D., received her Doctor of Jurisprudence degree *cum laude* from Indiana University in Bloomington, Indiana, in 1984. She holds the rank of Associate Professor of Organizational Leadership and Supervision at Purdue University Calumet, and is currently Director of Graduate Studies for the campus. Her publications include work in distance education, graduate education, and professional skills in technology fields. She regularly teaches in the areas of leadership and ethics, conflict resolution, and personnel law. Professor Colwell may be reached at colwell@purduecal.edu.

CASE STUDY: APPLYING QFD IN A GRADUATE CURRICULUM DESIGN FOR AN INDUSTRIAL ENGINEERING TECHNOLOGY PROGRAM

Joseph C. Chen, Bradley University; Julie Z. Zhang, University of Northern Iowa

Abstract

This paper presents a case study where the Quality Function Deployment (QFD) method was applied in curriculum design/revision for a graduate Industrial Technology program. With the advancement and development of new technologies, increasing demands for graduates' technical and social skills make the curricular design of Industrial Technology programs very difficult. This paper introduces Quality Function Deployment (QFD) as a systematic method to ensure that educational curricula meet the demands of students and industry. More specifically, this case study shows how the QFD model can help students systematically sort customer issues or concerns—hereafter referred to as "voices"—and create prioritized suggestions, with a final goal of improving curricula design for the Industrial Technology field.

Introduction

Given recent innovations in industry, more and more academic institutions are facing three major challenges. First, due to the rise of the knowledge economy, and some negative perceptions about manufacturing such as low wages, manufacturing layoffs, international outsourcing, and severe international competition, younger generations are discouraged to purse careers in manufacturing [1]. In a worldwide context, American students are unwilling to pursue engineering degrees compared to students from China, Singapore, Japan, and other Asian countries [2].

Secondly, American manufacturing industries are facing a shortage of adequately educated employees with specific knowledge and skills, because baby boomers are nearing retirement age. According to the Iowa Advanced Manufacturing Road Map [3], the lack of an adequately trained workforce will be the biggest challenge facing midwest advanced manufacturing firms in the next ten years.

The third challenge is that knowledge-based enterprise drives business leaders to incorporate knowledge from various sources into strategic business development plans. These sources include customer requirements, market expectations, understanding competitors, financial conditions, etc. Of those factors, the most important one involves human resources; that is, what knowledge employees should possess in order to make the business grow steadily and healthily. Facing these challenges, it is necessary and critical for educators and researchers in engineering or technology areas to create new strategies to update the traditional curriculum to be more attractive, effective, and competitive.

Quality Function Deployment (QFD)

Quality Function Deployment (QFD) is a structured process that provides a means for identifying and carrying the voice of the customer through each stage of product or service development and implementation [4], [5]. This concept was first developed and systemized in Japan in the 1960s and 1970s. Later, Professor Yoji Akao introduced it to the U.S. [4]. The purpose for using QFD is to incorporate customer requirements early in the planning stage to help design products or improve the quality of services. QFD provides a systematic approach that can be followed during all stages of product development in order to document and record data that will be used to make decisions.

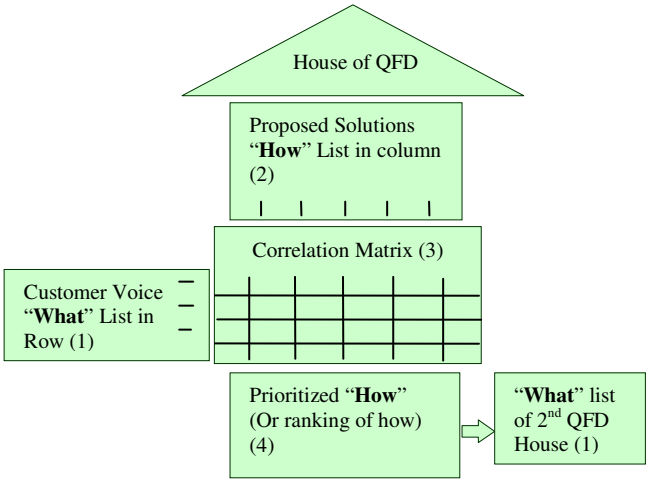

Figure 1. Structure of the QFD model

The graph in Figure 1 provides a clear view of the structure of the QFD model. It can be seen that the QFD model contains four primary stages. The first stage involves collecting information. At this stage, information is collected in terms of what defines quality, such as customer needs or

requirements, engineering measures, and product features. The QFD model regards the voice of the customer, a list of customer requirements or desires, as the substantive component, referred to as the "what".

The second stage specifies the applicable procedures or actions for carrying out the design of the product based on customer desires obtained from the "what" stage. The QFD model regards this function as the "how". This stage involves achieving the goals defined in the previous stage, consisting of the implementation of processes, facilities, and methods. In this step, the emphasis shifts from identifying the problem to solving the problem. Normally, actions in the "how" list are generated by the process of brainstorming.

The third stage involves establishing a relevance matrix between the "what" and "how" that is shown in Figure 1. The QFD process is a means of capturing the voice of the customer and conveying this voice into a new product design or making improvements. Each of the elements of stage one ("what") are listed in the rows and ranked, and their importance scale becomes a multiplication factor. Each of the elements of stage two ("how") are listed in the columns. The relationship matrix shows how stage one and stage two correlate with each other. The matrix is then used to analyze how each "how" will help fulfill each "what". When a relationship exists between a "how" and a "what", the "how" will satisfy a particular customer requirement or solve a problem. The correlation of "what" and "how" was filled into the matrix by using a scale of 1 to 5, with 5 being most important and 1 being least important. If a "how" is a strong measure of compliance with a "what", then the "how" is a very important strategy to implement "what" and 5 will be the scale. However, if a "how" provides no indication as to whether the product complies with the "what", then there is likely no relationship and the correlation scale will be empty (treated as zero). Filling in and analyzing this matrix will likely take a large portion of the time in QFD meetings.

The fourth and final stage involves ranking the possible solutions. Ranking is determined by the weighted sum of the correlations, with the weight defined by the customer ranking scale. Therefore, the possible solutions can be prioritized and listed in the bottom of the "house" shown in Figure 1. Depending upon the specific product requirements in the development process, the QFD method can be implemented in order to construct one, two, or even three houses, consecutively, to make the proposed improvements more specific and more applicable.

Some of the measurable benefits of using the QFD models include reduced costs (product, design, and manufacturing), improved quality, more satisfied customers, shorter development time, and more appealing final products. Originally, being a tool for quality improvement in industry incorporating customer voice into product design, QFD has also been employed in educational research, such as curriculum design and development [6] and enhancement of educational program effectiveness [7]**.** A QFD study performed at the National University of Singapore's Business School indicated that the QFD methodology can be applied equally well to a service environment like higher education [8]. Specifically, QFD has been used for identifying the gap between industry expectations regarding employee skill/knowledge and current engineering program curriculum limitations [9].

Next, a case study is presented relating to how the QFD model was used to transfer customer voices into prioritized recommendations and possible remedies for an existing Industrial Technology graduate program curriculum.

Background

This case study is based on a project conducted by a group of graduate students from the Industrial Technology and Education program at a leading research university. The background for the project was the Department of Industrial Technology and Education (ITEC), which was in the middle of revising the curriculum, due to the merger of the College of Agriculture and the College of Education within the university. The Department of Industrial Technology and Education used to belong to the College of Education. The merger, along with technology development and industrial globalization and competition, brought new challenges to the curriculum revision committee. The college and the department researched their current program curricula and then utilized the QFD method to suggest improvements to the graduate curriculum for the future.

Application of QFD for an Industrial Engineering Technology Graduate Program

The goal of the QFD case study conducted by the graduate students was to recommend changes to the existing I TEC graduate program curriculum for improvement. After discussion, the group members set up the project objective that the suggested recommendations should be made to enhance the current graduate program, efficiently use the current university resources, meet the needs of graduate students in terms of educational and professional development, and make the graduate department more attractive to future students.

Throughout the project, the student group initialized an outline following the QFD procedures to construct the House of Quality matrix shown in Figure 1. The main feature of their project is that by implementing the QFD method they constructed a House of Quality matrix to extract the customers' (students') needs and obtain the prioritized sug-

gestions regarding curricular change. The outline of the case study is shown below:

- Identify the product and customer
- Customer voice (the "what")
- Specific actions/methods to make improvements (the "how")
- Define the matrix
- Prioritize suggestions
- Recommendations

Following the project outline, the first step was the identification of product and customer. Since the major purpose of the project was to help revise the curriculum for the Industrial Technology graduate program, in general, the product in the QFD model should be the education that prepares students for the industrial technology field. The graduate student group performed in-depth research on the current graduate program curriculum from the university catalog and program mission statements. The product in their project is further specified as the preparation of graduate students' technical/academic skills and professional readiness that would provide students enrolled both in the Masters and Ph.D. programs for potential employment opportunities.

The next step after product identification was the identification of the customer voices (the "what") from both internal and external customers. For this particular case study, the internal customers were the graduate students, and the external customers were related industries or academic institutions which may have served as potential employers for the graduates. Due to time constraints, only the voices of internal customers were considered for input.

During data collection, there were two primary data sources for customer voices: survey and interview results. The first data source was a graduate follow-up survey conducted in 2003 by sending the instruments to graduates of the past ten years from 1993 to 2003. The survey produced 54 responses from the alumni and was used for further analysis. Meanwhile, an interview was conducted to gather information from current graduate students for a second data source of customer voices. The participants in this interview were the six group members in this project. The core question that was asked in the survey and interview was "What improvements are most needed in the I TEC graduate program at the university?"

The group members analyzed the survey responses and determined eight major points for suggested improvement. This was done by looking at the various suggestions from all of the responses, and then grouping all of the suggestions relevant to the objectives into more general points. These points, and the percentages based on frequency of mention in the surveys, are shown in Table 1.

- 25% of the responses suggest that I TEC graduate students require more knowledge or skill related to research and statistics
- 21% of the responses suggest adding more computer and technology-related courses
- 18% of the responses suggest improving the facilities and equipment
- 13% of the responses suggest that the funding and financial support opportunities are insufficient
- 8% of the responses suggest improving publication writing skills
- 5% of the responses suggest broadening internship opportunities, adding business and management courses, and revising the core requirements, respectively.

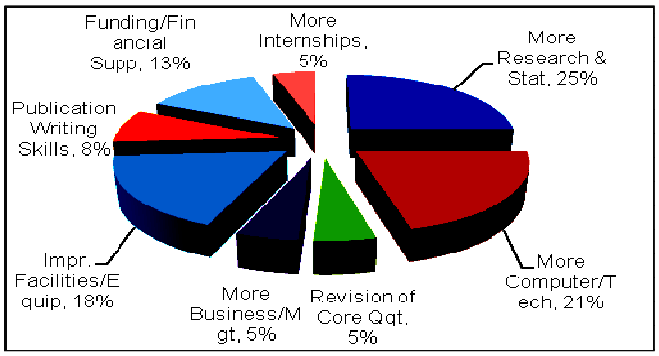

Figure 2. Survey and Interview Response

Ratings serve both as weighting factors and multipliers for other numbers in the matrix. The group members individually ranked each of the customer voice items on a scale of 1 to 5, with 1 being least significant and 5 being most significant, and then an average of the group was used for the importance rating. These rankings do not necessarily reflect the percentage of frequency of the items in the survey, as the group looked at all of the items together and decided which were more important in the overall picture. Table 2 displays the items of customer voice in order of weight and their corresponding importance ratings.

Table 1. Customer Voice Table

#	Customer Voice	Weight
1	More computer/technology related courses	4.8
2	More flexibility in course selection	4.3
3	Funding/financial support	4.2
4	Publication writing skill training	3.8
5	Improvement on facility and equipment	3.5
6	More internship for graduate students	3.3
7	More courses focused on research	3.0
8	More business and management courses	2.0

The graduate group brainstormed ideas and each individual member came up with a list of possible "how's" based on the customer voice/requirements. After brainstorming, the

next step was to determine which of the ideas in the comprehensive list were most frequent within the group. This involved discussing each other's ideas and agreeing on a shorter list which encompassed the most prevalent ideas in the group.

The final list of "how's" are:

- Hire more faculty
- Give faculty more research time
- Give faculty more research funding
- Add new equipment, computer hardware and software
- Invite speakers from industry for I TEC 615 (graduate seminar class)
- Reduce course requirements by 6-9 credits
- Require a real-world, industry-related project
- Provide more exposure to other advanced technologies
- Advise students to get internships and funding
- Advise students to find appropriate university-wide courses
- Ensure that a permanent staff/faculty member is in charge of equipment maintenance

Once "what" and "how" were specified and listed in row and column formats, respectively, the graduates constructed the matrix using an approach as presented above (see Figure 1). The correlation of "what" and "how" was filled in the matrix, again by using 1 - 5 scale, with 5 being most important and 1 being least important. The correlation scale shown in Table 2 is the average value from the six group members. The bottom of the matrix has the absolute and relative scores. The absolute score is the sum of the weighted relationship values for each ("how" and "what"). This is basically the sum of each relationship score multiplied by the associated ("what") importance ranking for each column. The relative score is the ranked or prioritized value for the absolute scores, as shown in Table 2.

The group then reviewed the entire relationship matrix and developed some recommendations based on the "how" ranking order. In this way, the group was able to identify the prioritized improvement needs and possible solutions. Upon completion of the QFD house, the graduate group used some other criteria such as financial availability and realistic assumptions to make general recommendations with an overall goal of benefiting the department and increasing ITEC program recognition. The recommendations from the graduate group are summarized as:

Table2. QFD Matrix

	Importance scale 1-5	Hire more faculty	Faculty should be given more time on research	Faculty should get more research funding	Add new equipment, computer hardware and software	Invite speaks from industry for ITEC615	Reduce 6-9 credits from course requirement	Real world industry related project	More exposure to other advanced technology	Advise students get internship and finance assistance	Advise students find appropriate university-wide course	Permanent staff/faculty in charge of equipment
More computer/technology related course	4.8	3.5	1.2	0.2	3.2	0.5	0.5	1.0	4.3	0.8	2.5	0.5
Courses focused on research and statistics	3	2.2	2.0	0.8	0.7	2.2	1.2	0.7	0.5	0.2	2.3	
More internship for graduate student	3.3	0.2	0.3	0.5	0.8	1.2	0.3	3.8	3.2	4.3		
Funding/Financial support	4.2	3.3	4.0	4.3	1.8	0.2		1.2	1.0	3.2		1.2
Publication writing skills	3.8	0.8	0.8	0.5		0.5	0.5	0.3		0.2	2.2	
Improvement on facility and equipment	3.5	1.0	1.3	2.5	5.0	0.8	0.3	1.0	1.3	0.3		4.7
Add more business and management courses	2	2.5	0.5	0.3	0.2	0.2	1.7	0.2			1.8	0.2
Revision of core course requirement	4.3	0.5	0.7		0.7		4.7		0.7		1.5	0.2
	Absolute	51.7	41.2	34.5	48.4	18.6	33.5	29.5	44.5	33.9	37.4	24.7
	Relative	**1**	**4**	**6**	**2**	**11**	**8**	**9**	**3**	**7**	**5**	**10**

- Increase the flexibility of electives for graduate students by increasing the partnership, communication, and collaboration between professors and departments within the university campus.
- Benchmark other ITEC or related programs at other universities for ideas and strategies.
- Develop partnerships with industry for sources of:
    - Funding
    - Internship opportunities
    - Projects
    - Equipment
- Investigate "instructor only" positions to help:
    - Reduce the load on current faculty
    - Increase funding grant submission
    - Increase publications
- Ultimately lead to increased program recognition
    - At the university level
    - Nationwide
    - Internationally

Conclusion

This case study implemented QFD methods on the design of the educational program curriculum. By employing the House of Quality matrix, the customer voices could be systematically lined up by scaling factors. This is an efficient information collecting and sorting mechanism. Once the technical attributes and all other input information together with the customer voice were identified, they were entered into the correlation matrix. Finally, the output or the product features, which in this case study were suggestions to the curriculum design, were produced by certain engineering measures. Therefore, it can be seen that using the QFD model could focus the process of incorporating customer desires/wants/needs into technical specifications. The matrices capture, organize and display the information. More specifically, the QFD approach allowed the students to understand the design process from beginning to end, including what resources would be needed.

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Biographies

JOSEPHY C. CHEN is a professor in the Industrial & Manufacturing Engineering & Technology Department at Bradley University. He teaches lean manufacturing, Six Sigma, quality function deployment, design for manufacturability, manufacturing economics, facility planning both at the undergraduate and graduate levels. He also performs research in adaptive control for automated machines, online lean assessment via RFID technique, and Curriculum Development to enhance education of lean manufacturing system design and methodologies. Dr. Chen can be contact at jchen@bumail.bradley.edu

JULIE Z. ZHANG is an assistant professor in the Industrial Technology Department at the University of Northern Iowa. She teaches courses related to manufacturing processes, manufacturing automation, statistical quality control, total quality management and CAD/CAM/CNC applications. Her research includes green manufacturing and evaluation of bio-based cutting fluids, real-time cutting tool condition monitoring, and adaptive control for automated machines.

ANALYSIS OF METALLURGICAL AND MECHANICAL FAILURE OF A CENTRIFUGAL COMPRESSOR

N. Rezamahdi, MAPNA Group; M. Tofighi Naeem, MAPNA Turbine Engineering & Manufacturing Co. (TUGA);
S.A. Jazayeri, K.N. Toosi University of Technology

Abstract

The present paper reports the investigation of a sudden failure of a two stage centrifugal compressor that was used in the oil industry. This study is composed of two sections: metallurgical and mechanical. The first section was carried out in the laboratory, and in the second one the impeller was modeled by Mechanical Desktop (MDT) and analyzed by Ansys Workbench software. Then, the results of both sections were compared and validated.

The impeller was subjected to a series of examinations, including visual inspection, photographic documentation, non destructive testing (NDT), optical microscopy, scanning electron microscopy (SEM), and quantometer. Samples from the longitudinal and transverse sections of the disc were prepared for metallography. The morphology of the fracture surfaces and fatigue striations are shown through the use of SEM.

On the fracture surface there are curved lines called Chevron markings which seem to converge near mid-thickness of the fracture surface. Investigation shows that because of very long period of operation and cyclic loads, the impeller was subjected to fatigue damage. Fatigue cracks grew to a critical size and caused the catastrophic failure of the impeller; also, creep mechanisms accelerated this phenomenon. A visual inspection and photographic documentation of the 2nd stage impeller has revealed the presence of many cracks of different lengths at different regions of damaged impeller, on both disc and cover.

In the software analysis, pressure, thermal and stress distributions under operating conditions were identified, and critical points were found.

Introduction

Apparently the most common mode of failure in metallic parts is fatigue. Determination of a maintenance policy after the occurrence of a fatigue failure in service is based on finding the number of loading cycles which caused the failure [1]. The compression of gas within a plant is integral to the oil industry, too. It is thus of utmost importance that premature failure of these pieces of equipment be avoided [2]. The rupture of metal parts is a complex phenomenon that depends on the nature of the material (composition, structure and morphology), temperature, the deformation or excitation mode (traction, flexure, fatigue…), and the rate at which strain is applied [3, 4]. An examination of the fracture surfaces can provide information as to the origin and the cause of the fracture; these causes may include the apparent heterogeneity, the ductility and sometimes, the grain size. When a metal piece breaks, two major questions are to be answered: what are the modes and speed of rupture, and what is the origin of the damage (metallurgical failure, manufacturing defects, …) [3].

Damage tolerant fatigue design methods for critical rotating components such as discs and shafts in gas turbine engines are well established. These address crack propagation through the application of fracture mechanics, assuming defects are present in the material. The prediction methods have limitations, but at lower temperatures, these are conservative. It is not clear, however, that similar conservatism is valid at higher temperatures where additional failure modes due to creep and environment interact with those arising from fatigue [5].

In this study we focus on a two stage centrifugal compressor that failed during the operation. Failure analysis is carried out to delineate the cause of failure. This compressor is made of low alloy steel by quenched and tempered treatment. The rotor is composed of two impellers, one of them for the first and the other for the second stage. The impellers have been constructed by welding the blades to the cover and all of these parts were made by forging.

Visual Inspections

After the compressor disassembling and the rotor removal, it was evident that the 2nd stage impeller was catastrophically broken. A visual inspection of the 2nd stage impeller has revealed the presence of many cracks, on both disc and cover (Figures 1, 2).

Fortunately, the crack often leaves a series of fracture markings in its wake that may indicate the relative direction of crack motion. For example, the curved lines (called "chevron" markings) which seem to converge near mid-thickness of the fracture surface shown in figure 3 have been shown to point back toward the crack origin. It is believed that within the material localized separations ahead of the crack grow

back to meet the advancing crack front and form these curved tear lines. All one needs to do is follow the "chevron" arrow. When a crack initiates in a large component, it sometimes branches out in several directions as it runs through the structure. Although the "chevron" markings along each branch will point in different directions relative to the component geometry, it is important to recognize that the different sets of "chevron" markings all point in the same relative direction-back toward the origin. "Chevron" markings grow out radially from an internally located origin [6].

The assembly of the compressor was dismantled. Dye penetrant inspection (DPI) and magnetic particles tests were carried out to detect the defects on the impeller (figure 4). Since cracks and failures were so clear, even without using these tests all of them were noticeable.

Figure 1. Fracture on Cover

Figure 2. Fracture on Disc

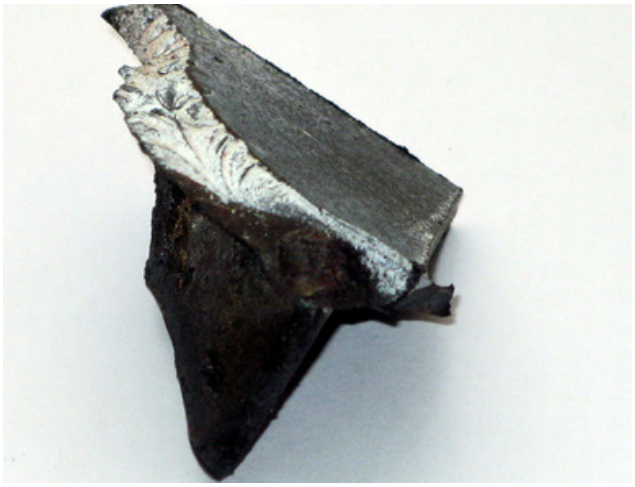

Figure 3. One Sample of Impeller and Chevron Markings on its Fracture Surface

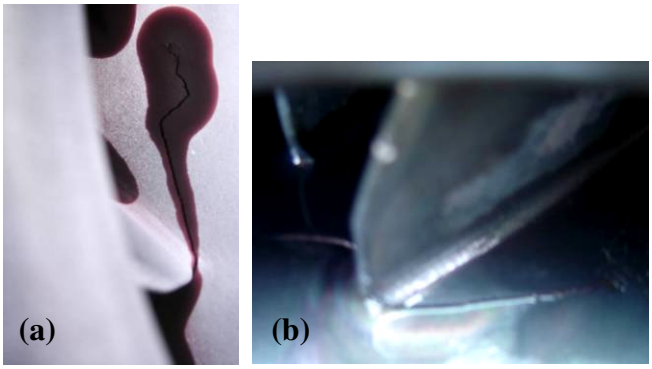

Figure 4. Crack around the Blade
Figure 4(a) DPI, Figure 4(b) Magnetic Particles

Chemistry

The chemical composition analysis of the failed impeller using the quantometer, shows that it is similar to ASTM A514 Steel, grade F as shown in Table 1. Also, the composition and mole fraction of the inlet gas to the compressor are illustrated in Table 2.

Metallography

Samples from the longitudinal and transverse sections of the disc were prepared for metallography. Polished samples were immersion etched in the nital's reagent (5% nitric acid + alcohol) until grain boundaries appeared. In structural review, by considering the comparison of longitudinal and transverse sections, the morphology of grains shows that they are coaxial and have the same dimensions in different directions, therefore, mechanical strength of this part is nearly equal in different directions.

Table 1. Chemical Composition of the Impeller

composition	impeller	ASTM A514 Steel, grade F
Fe	96.3	97
C	0.0887	0.1-0.2
Si	0.214	0.25
Mn	0.820	0.8
P	0.0114	
S	0.0243	
Cr	0.527	0.48
Mo	0.487	
Ni	0.968	0.85
Al	0.0461	
Co	0.0139	
Cu	0.305	0.33
Nb	0.002	
Ti	0.0354	
V	0.0594	0.06
W	0.0150	
Pb	0.0250	
Sn	0.0020	
B	0.0026	0.0030
Ca	0.0010	
Zr	0.0020	
As	0.0050	

Table 2. Chemical Composition of Inlet Gas

composition	Mole fraction%	Molecular weight
CH_4	87.3	16
C_2H_6	5.74	30.1
C_3H_8	2.42	44.1
n-C_4H_{10}	0.8	55.1
I-C_4H_{10}	0.41	58.1
C_5H_{12}	0.52	72.2
C_6H_{14}	0.14	86.2
H_2S	0.07	34.1
CO_2	2.51	44
N_2	0.09	28

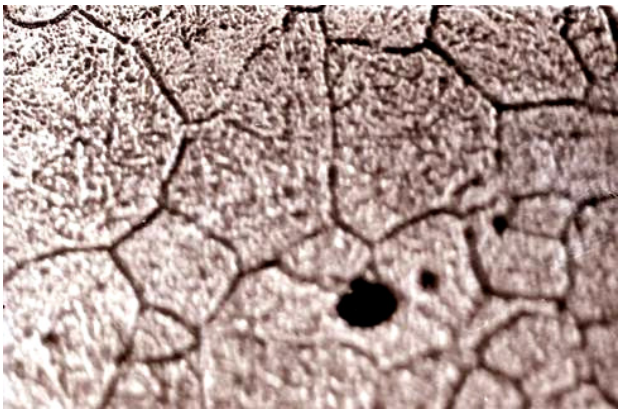

Figure 5. Macrocracks Have Formed on Grain Boundaries (200X)

Also, as can be seen in figure 5, there are macro cracks on grain boundaries. They are the resultant of creep mechanisms. First, isolated cavities are formed on boundaries, then the quantity of them increases, and oriented cavities are made. Then these cavities join together and form micro cracks and macro cracks, respectively.

Fractography

The fatigue fracture surface of the impeller was cut to be observed by SEM. As can be seen in figure 6, the fracture surface created by the fatigue crack is smooth, but the initial crack looks coarse [7]. Figure 7 shows a part of cover coating that was removed due to fatigue. Figure 8 displays cracks on fracture surface. Figure 9 shows fatigue striations and in figure10 detachment of grains due to the creep mechanism is clear.

Microscopic striations on fatigue fracture surfaces were first observed by Zapffe and Worden [8] in 1950 using optical microscopy. Forsyth and Ryder [9] subsequently showed that each striation was produced by one cycle of stress by examining fracture surfaces of specimens subjected to simple program loading. These observations showed that striations often have a saw tooth profile [10].

Mechanical Section

In this section, we modeled the impeller and flow of gas with mechanical desktop (MDT) modeling software.

Element of fluid (flow of gas) is called core, here. Figures 11, 12 show the mechanical model of the impeller and its core, respectively.

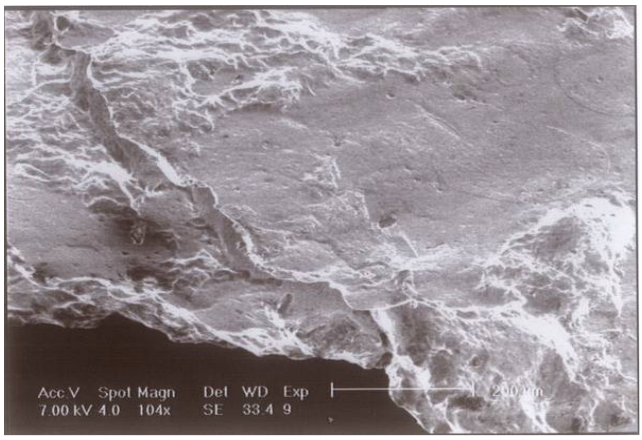

Figure 6. Fatigue Fracture Surface

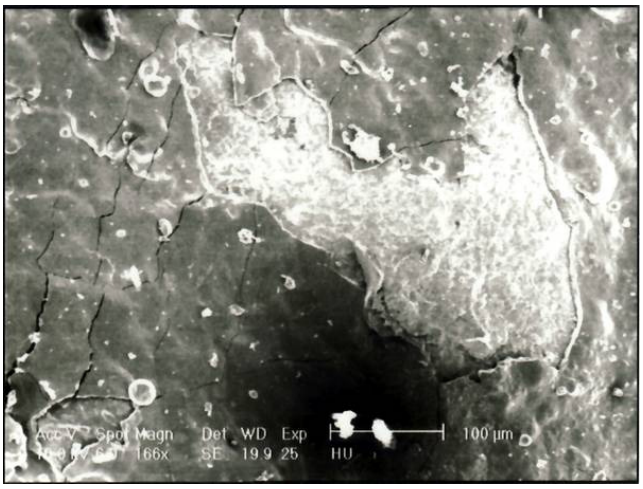

Figure 7. Fatigue Cracks on Cover Coating

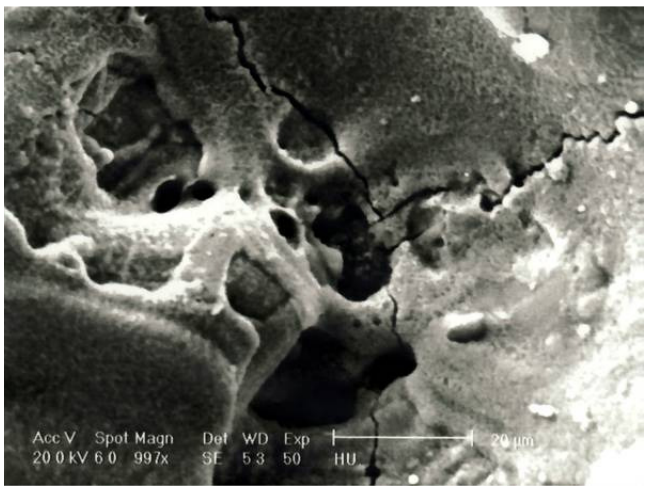

Figure 8. Cracks on Fracture Surface

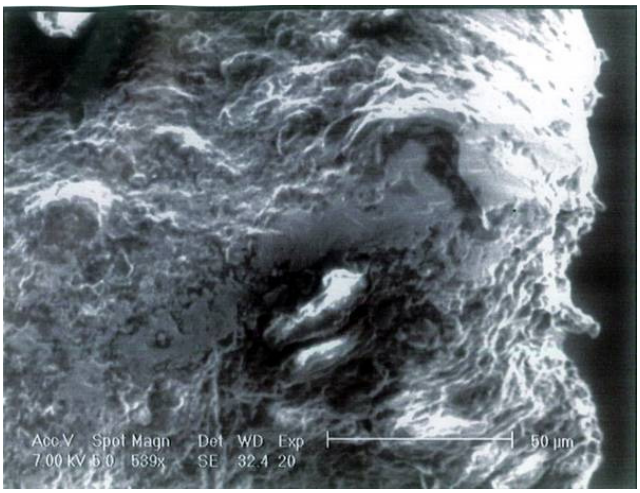

Figure 9. Fatigue Striations

Figure 10. Detachment of Grains due to Creep Mechanisms

As can be seen from the series of figures below, pressure and temperature distributions, streamlines and velocity vectors of flow were analyzed by using advanced CFD (figures 13-17).

From figure 13, it is clear that pressure values vary from 134 bars at inlet to 140 bars at outlet. These changes were made layer by layer in gas flow. Temperature variations are similar to pressure, too. Temperature magnitude has changed from 326 to 328.5 K (figure 14).

Apparently, velocity values change from 90 m/s at inlet to 137 m/s at outlet. In figures 15, 16 velocity streamlines are observed.

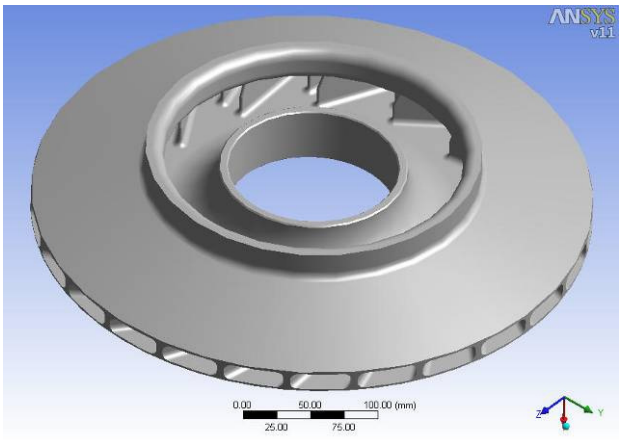

Figure 11. Mechanical Model of the Impeller

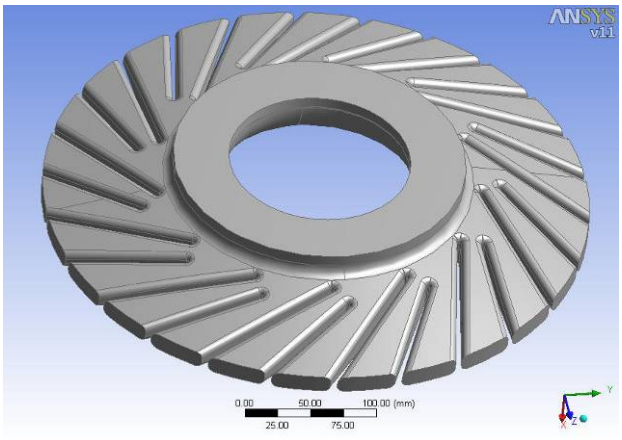

Figure 12. Mechanical Model of the Core

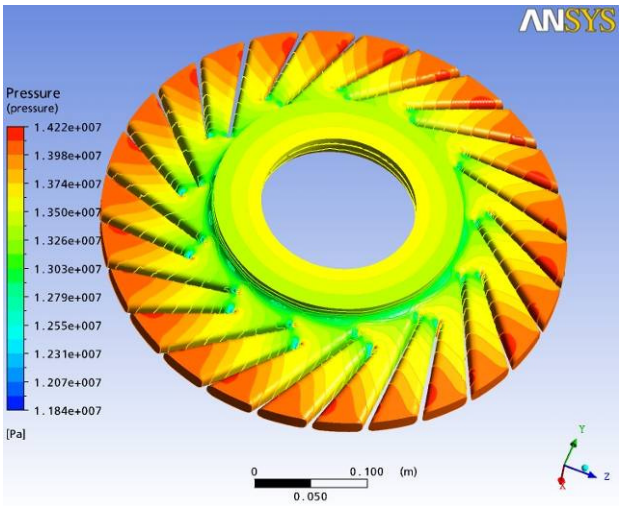

Figure 13. Flow Pressure Contour

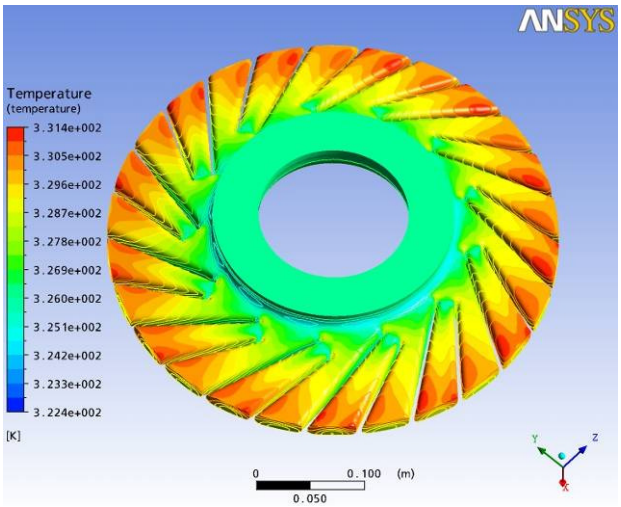

Figure 14. Flow Temperature Contour

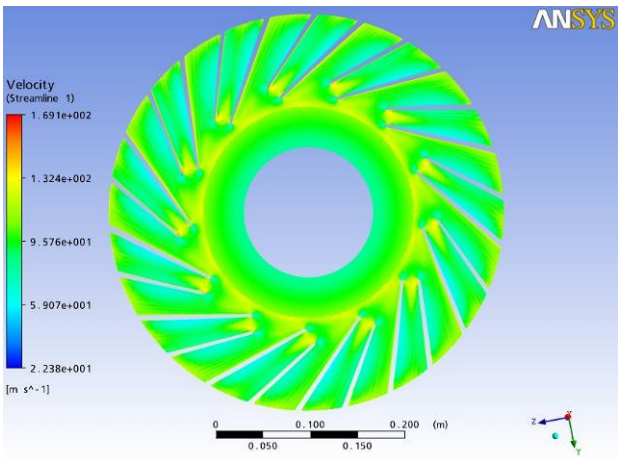

Figure 15. Velocity Streamline (Top View)

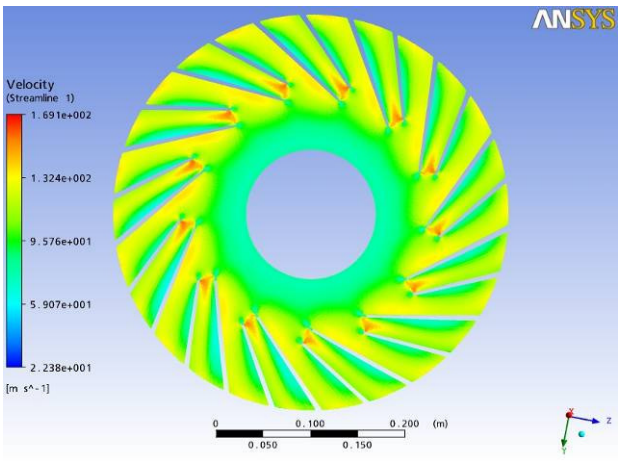

Figure 16. Velocity Streamline (Bottom View)

By making a comparison between figures 16, 18, 19 we found that there is a good agreement between practical and analytical results. In practice, it was observed that critical

points were put at the junction of disc and blade. On the other hand, we analyzed the impeller using software and the resultant was similar. Because of the high flow velocity (approximately 169 m/s) at these points and mechanical design (vertical connection) between blade and disc, the result is a zone of stress concentration. The stress contour is shown in figure 19 and the position of maximum stress is clear in figure 20. By considering pressure and temperature contributions we understand that these parameters increase along the flow path. Also, observing velocity magnitude shows us that its magnitude increases at outlet. These results have a good agreement with real conditions.

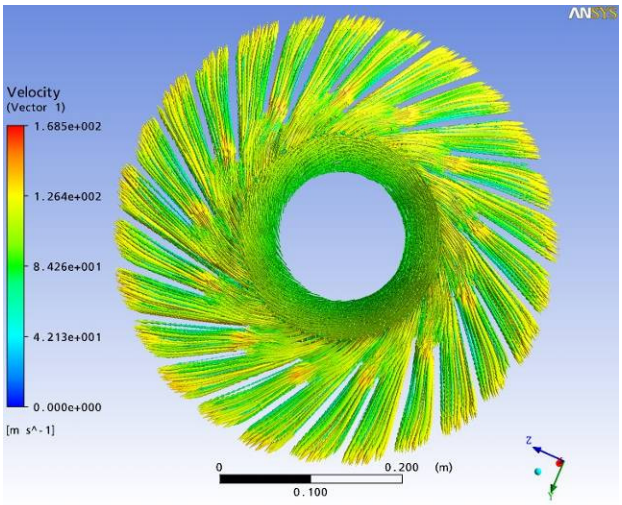

Figure 17. Velocity Vector

Figure 18. Crack at the Junction of Blade and Disc

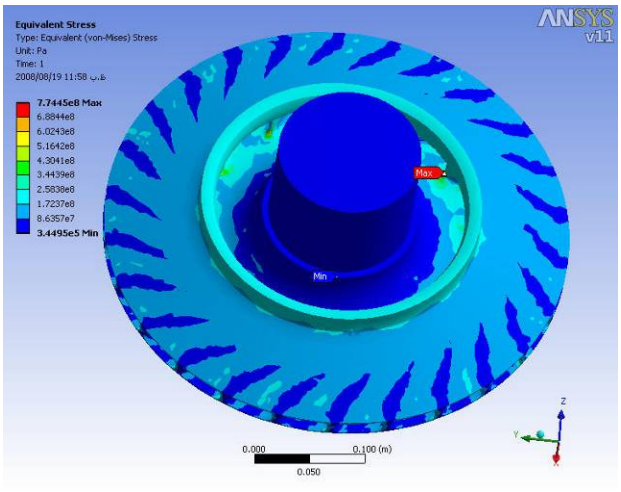

Figure 19. Stress Distribution

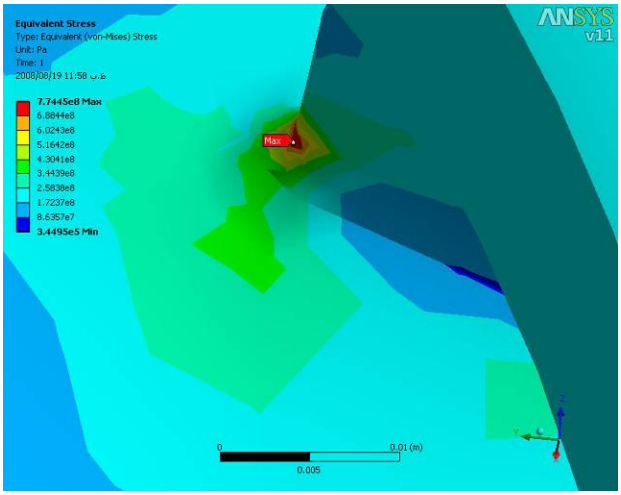

Figure 20. Stress Concentration

Conclusion

The failure analysis of the second stage impeller of a two stage centrifugal compressor after 81000 hours of operation period is carried out. Visual examination, photographic documentation and non destructive testing (NDT) revealed the presence of many cracks on both disc and cover and different sets of chevron markings.

After microstructural investigation by optical microscopy it is found that there were some macro cracks on grain boundaries which were the resultant of creep mechanism. Also, fractography by SEM showed fatigue striations. Also, some fatigue cracks were found on fracture surfaces.

It is assumed that the accident happened from a fatigue crack through continued operation and changes in operational conditions.

Also, these observations were confirmed by mechanical analysis that carried out with ANSYS Workbench. Therefore, there is a good agreement between practical and analytical results. These observations illustrate that the failure of this impeller has occurred on the basis of a creep-fatigue mechanism.

Acknowledgments

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Biographies

N. REZAMAHDI received the B.S. degree in Mechanical Engineering from the University of Guilan, Rasht, Guilan, in 2005, the M.S. degree in Mechanical Engineering from the K.N.T University of Technology, Tehran, Iran, in 2008. Currently, She is an engineer of MAPNA Group in Tehran. Her working and research areas include Turbomachinery and Fractography. N. Rezamahdimay be reached at Rezamehdi_N@mapna.com

M. TOFIGHI NAEEM received the B.S. degree in Mechanical Engineering from the University of Guilan, Rasht, Guilan, in 2005, the M.S. degree in Mechanical Engineering from the K.N.T University of Technology, Tehran, Iran, in 2008. Currently, He is an engineer of MAPNA Turbine Engineering & Manufacturing Co. (TUGA) in Karaj. His working and research areas include Turbomachinery and Fractography. M. Tofighi Naeem be reached at Tofighi.Mehdi@mapnaturbine.com & M.Tofighinaeem@gmail.com

S.A. JAZAYERI received the B.S. degree in Mechanical Engineering (Lon), the M.S. degree in Mechanical Engineering (Bath), and the Ph.D. degree in Mechanical Engineering (UVic). Currently, He is an assistant Professor of Mechanical Engineering at K.N.Toosi University of Technology, Tehran, Iran. His teaching and research areas include fluid mechanics, automobile especially diesel engines and combustion. S.A. Jazayeri may be reached at jazayeri@kntu.ac.ir & sajazayeri@hotmail.com

BUILT-IN-SELF-TEST (BIST) FOR SYSTEM-ON-A-CHIP USING OUTPUT VOLTAGE DIFFERENCE BETWEEN FAULT-FREE AND FAULTY DEVICES

Graham Thomas, Texas Southern University

Abstract

System-on-a-chip (SoC), also referred to as system-level integration (SLI), has become very popular over the last decade. The popularity of this technology is driven mostly by the need for manufacturers to utilize the millions of unused gates on the wafer. System–on-a-chip development came about because of the "design gap" between the multi-million gate capacity of modern-day process technology and the slow pace of designers to find ways to utilize the millions of gates on the wafer. As knowledge and system implementations improve, more semiconductor manufacturers and vendors look to SoC's to better utilize the vast silicon area available on the wafer. SoC testing is in its infancy phase as engineers and designers try to figure out the best approach to design and test circuits. SoC's seem to be the next revolution in very-large-scale-integration (VLSI) circuit design. Finding a good built-in-self-test (BIST) method that is reliable is one of the issues which system designers need to address. The purpose of this study was to develop a BIST method that could make comparisons between the output voltages of fault-free devices and faulty devices. The primary goal was to highlight the importance of having a good test method for testing SoC devices and to present a reliable and accurate BIST method for testing an SoC.

Introduction

System-on-a-chip (SoC) seems to be the next revolution in very-large-scale-integrated (VLSI) circuit design. This revolution creates a new set of design and functional challenges for designers. Finding a good built-in-self-test (BIST) method that is reliable is one of the issues which system designers need to address. This study identifies the problem of having a good test method for testing SoC devices as one of the challenges being faced by designers. The approach taken in this study was to find a testing method for an SoC that would be reliable and accurate.

A review of the current literature on SoC testing indicated that no attempts have been made to develop a BIST method for SoC's that makes comparisons between the output voltage values of fault-free devices with faulty devices. The foundation of this study was based on the assumption that a faulty device has an output voltage that is quite different from that of a fault-free device. This difference in output voltage between the two devices could, therefore, be used to determine whether the devices are faulty and the type of fault affecting the device. The intention of this study was to exploit this feature of voltage difference among devices to develop a programmable BIST method to determine if the assumption made could be validated.

SoC, also referred to as system-level-integration (SLI), has become very popular over the last decade. The popularity of this technology is driven mostly by the need of manufacturers to utilize the millions of unused gates on the wafer. The lack of better design tools and methodologies to use these unused gates or transistors has resulted in the development of multiple systems on the same chip. SoC, very-large-scale-integrated circuits (VLSI), has been discussed throughout the literature. Many meanings have been applied to SoC's; the most compelling is a design which has components at a level above what is presently being used [1]. In the past, this design was a heterogeneous design which simultaneously included either analog with digital and non-transistor structures or simply different kinds of digital circuitry (e.g. dedicated logic with programmable core) [2].

While all of these have design challenges beyond that necessary for a single circuit type, it is the possible inclusion of all the above (analog, non-transistor, various types of digital) which rises to the level of a true SoC. This represents the integration of all the functions that were previously interconnected on a PC board, resulting in the attainment of a more sophisticated design level [2], [3]. Such high levels of integration are required in applications that are cost, power and size sensitive. The clearest examples of such products are systems which support wireless communications in portable devices. These can range from cell phones to portable multimedia terminals. Demonstrations of these systems are now beginning to appear.

Designers have integrated both the analog and digital functions as well as passive elements that are compatible with CMOS (complementary metal oxide semiconductor) technology [4]. The various types of digital computation required further complicate these prototypical SoC implementations, ranging from control processing for protocols

and user interface, up to the highest speed-dedicated digital circuitry for early stages of link demodulation. The demand for the most efficient integrated solution requires a simultaneous optimization of the passive devices, analog circuits as well as the computational structures used to implement the digital processing. The choice of the latter is particularly important as the various approaches can range over many orders of magnitude in size and energy efficiency [1].

SoC development came about because of the design gap between the multi-million-gate capacity of modern-day process technology and the slow pace of designers to find ways to utilize the millions of gates on the wafer [2]. As knowledge and system implementations improve more semiconductor manufacturers and vendors look to SoC's to better utilize the vast silicon area available on the wafer [5].

Why SoC?

The driving force behind SoC's is the large number of transistors that are available from the deep sub-micron technology process. These large numbers of gates are at the designer's disposal. So the capacity is there. However, the space on a wafer system board is expensive for smaller devices as numerous transistors are left unused. Through SoC's, substantial power savings may be obtained and reduction in packaging may also be a benefit. Embedding analog cores in the SoC could help increase noise immunity. By embedding processor cores using software and hardware rather than hardware only, designers can be more flexible in their designs. Embedding cores together in a single piece of silicon increases bandwidth of a system bus and, thus, increases overall system performance. Signals do not have to travel through I/O buffers and board interconnects, which helps signal integrity. The speed of the central processing unit (CPU) has been increasing by 60% per year, while the speed of dynamic random access memory (DRAM) has only increased by 7% per year. Providing on-chip DRAM increases the bandwidth by shortening the distance between memory and processor and provides a wider bus architecture that would be expensive at the board-level. This change from board-level to on-chip could help with the speed disparity between processor and DRAM [6].

SoC Architecture

In SoC designs, pre-designed cores are the essential components. A system chip may contain combinations of cores for on-chip functions such as large memory arrays, audio and video controllers, microprocessors, modems, digital-signal-processor (DSP) functions, internet tuners, and 2D and 3D graphics. These cores are generally available in either high level descriptive language (HDL) or transistor-level layout. The flexibility in the use of cores depends on the form in which they are available. Cores are available in three distinct forms: 1) soft cores, 2) firm cores, and 3) hard cores. They are defined as follows:

Soft cores: reusable blocks in the form of a synthesizable register-transfer-logic (RTL) description or a net list of generic library elements. The user of the soft core is responsible for implementation and layout [2], [7].

Firm cores: reusable blocks that have been structurally and topologically optimized for performance and area through floor planning and placement, perhaps using a range of process technologies. These exist as synthesized code or as a net list of generic library elements [7].

Hard cores: reusable blocks that have been optimized for performance, power and size, and are mapped to a specific process technology [7]. These exist as a fully placed and routed net list and as a fixed layout. Figure 1 gives a general block diagram representation of the structure of an SoC.

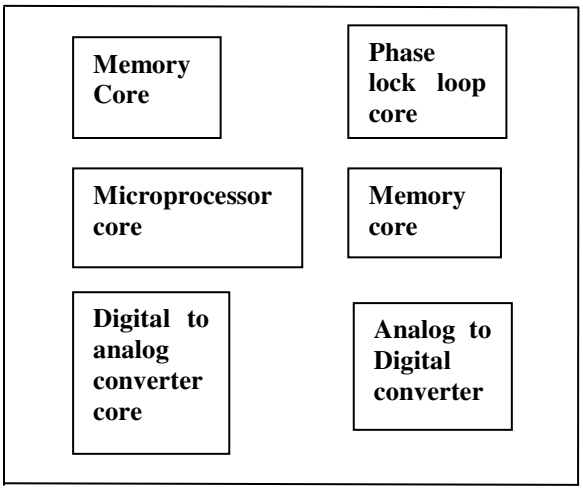

Figure 1. Block diagram of an SoC

The trade-offs among hard, firm and soft cores is in terms of parameters such as reusability, flexibility, optimized performance, cost and time-to-market. Some examples of core-based SoC's are media processors, global-positioning-system (GPS) controllers, single-chip cellular phones, global system for mobile communications (GSM) phones, smart pager ASIC and PC-on-a-chip.

SoC Performance

Improvement in the semiconductor industry doubles every eighteen months. The rate of increase is fuelled by semicon-

ductor miniaturization technology. The miniaturization of the semiconductor has caused a revolution in the development of high-performance components using semiconductors. The 1999 International Technology Roadmap for Semiconductor (ITRS) suggests that, "innovation in the techniques used in circuit and system design will be essential to maintain the historical trends in performance improvements" [6]. Achieving this technological advancement in circuit and system design is increasingly becoming dependent on integration of multiple silicon technologies on the same chip [6]. The devices that result from this integration are referred to as system-on-a-chip (SoC) devices.

Good design is paramount to the performance of these SoC devices. Therefore, manufacturers will have to combine knowledgeable design techniques with accurate and thorough testing of components to deliver a state-of-the-art product to the consumer. This would suggest that the design process is additionally important for SoC devices due to increasing system complexity. Design of SoC devices will progressively get more difficult as the devices will become increasingly more complex. It may be concluded that performance of SoC devices is strongly correlated with good design.

SoC Testing and Evaluation

Another challenge in producing quality SoC devices is ensuring the testability of an integrated-circuit design. This is a difficult task to accomplish since the testability of multiple systems on a chip is not a well-defined area of integrated-circuit design. Testing of integrated circuits has been more or less developed for single-chip systems. Physical testing of the SoC individual circuits can be done at the wafer level before the circuits are made into individual chip sets.

Difficulties may arise in the implementation of test methodologies when testing SoC's as a whole. Some of the difficulties which may arise in testing an SoC are given below [2]:

- Timing verification
- Getting embedded pins
- Combing differing test methodologies from different IP providers
- At-speed testing
- Test pattern reliability for hard cores
- Access
- Controllability
- Observability
- Reuse of test
- Reuse of DFT
- Mixed signal test
- Synchronization

The keys to designing testable circuits are:

1. Controllability: the ability to set and reset the inputs and every node internal to the circuit.
2. Observability: the ability to observe either directly or indirectly the state of any node in the circuit, which also includes the output and input pins.

SoC Advantages versus Disadvantages

The downscaling of CMOS transistors has enabled large numbers of transistors to be integrated on a single chip. These large numbers of transistors are not necessarily used in the design process; this has laid the foundation for the development of an SoC. Circuits that in the past would be placed on a printed circuit board may now be integrated on a single chip [5]. Table 1 compares some advantages and disadvantages of SoC's.

Table 1. Advantages versus disadvantages of SoC's

Advantages	Disadvantages
Lower power consumption	Turnaround times are major obstacles
Cost reduction	No simple testing methodology
Help in noise reduction	
Flexibility of design	
Reduction in packaging	
Miniaturization of various systems	
IP reusability of existing macros	

Purpose/Motivation

The continuous progress in silicon-related technology has fueled the development of new and exciting products that are finally available to consumers at an affordable cost. Because of the progress made and the demand by consumers for high-quality affordable products, performance in silicon technology has doubled every eighteen months, which is in line with Moore's law. As a result of the performance increase (mainly in speed and size), millions of transistors go unused on the wafer.

Because of the current leakage that results from small sizes of transistors, electronic designers are particularly concerned about the ever-shrinking size of transistors. This reduction in the size of transistors has provided an opportunity for designers to miniaturize consumer products, simplifying

them to such an extent that they become more affordable to consumers. The result of this change to smaller sizes has contributed to the relatively new phenomenon called system-on-a-chip.

SoC can mean different things to different people. When SoC is mentioned in this research study, it refers to taking the individual electronic devices called "chips" and placing them on a single wafer. These electronic devices (chips) include but are not limited to microprocessors, phase-locked loop, analog-to-digital converters, digital-to-analog converters, memory devices, transceivers, and amplifiers.

The development of SoC's resulted in a new challenge for engineers; the challenge of testing the SoC device as a single unit. Devices that have been tested as separate units may behave quite differently when tested as an integrated unit. Some characteristics that may show different behaviors include power consumption, timing analysis and synchronization. The effects resulting from the differences in characteristics may be quite different for a single unit than for multiple-unit system. For testing purposes, many researchers have proposed different test methodologies. Some researchers have made modifications to existing tests for single integrated circuits on a chip, while others have developed new methods for testing integrated circuits. Some of the methods proposed are complicated and are very expensive to implement. Based on the results of this literature review on testing methodologies, this study was primarily focused on finding a test for SoC devices that is simple, yet robust, and that is viable and easy to implement. The proposed method presented here is an integrated test methodology, such as a built-in-self-test (BIST) method, but will be user/designer/test-engineer activated. The approach is a programmable test method. Programmable test methods are testing methods in which the user/designer/test engineer is able to select which device on the SoC should be tested at any point in time.

Methodology

The methodology in this study was an integrated test method for testing systems that are placed on a single chip; referred to as system-on-a-chip (SoC). Testing SoC devices is a difficult task. Because of the difficulty involved, testing has mainly been done after the system has been designed and fabricated [2]. New and novel works are now being put forward to tackle the problem of integrating the testing circuitry on-chip during the design process [3]. Some of the challenges facing designers are how to manage undesirable features such as increased area on the die, cost, and power consumption, which may result from the addition of test circuitry [2].

The test method proposed for this research study was based on the assumption that a faulty device has an output voltage that is different from the voltage of a fault-free device. In this study, this assumed difference in voltage was used in order to determine the type of device; that is, whether the device was a faulty or fault-free device. To evaluate the assumption made in this study, six (6) different circuits were designed and simulations were conducted on each of these circuits. The circuits designed included phase-locked loop, analog-to-digital converter, digital-to-analog converter, operational transconductance amplifier, differential amplifier, and operational amplifier. A test circuit was also designed using comparator circuitry with the output buffer section of the circuit missing. The test circuit selects the circuit to be tested, isolates the circuit from all other circuits, and provides the input voltage for the circuit. In this study, the only circuit which was considered was the digital phase-locked loop (DPLL, see Figure 2) with its different components.

To be able to determine if a device is faulty or not, the normal operating voltages of a fault-free device had to be known a priori. Therefore, the first step in the simulation on each circuit was to establish the normal operating output voltage for each circuit; the fault-free devices were simulated to obtain their normal operating output voltages. Once the normal operating output voltage was observed and recorded for each of the six circuits, faults of different types were inserted into the circuits. The operating output voltage for each circuit with the inserted fault was observed and recorded. The operating output voltages for faulty and fault-free circuits were tabulated so that comparisons could be made. Comparisons of the operating output voltages for each circuit before and after the insertion of faults were made.

To determine the type of fault affecting the faulty circuits, operating output voltages were observed and recorded for each faulty circuit. To accomplish this, short-circuit and open-circuit faults were inserted into each test circuit. Short-circuit and open-circuit faults were used in this study since these are the most common fault types occurring in integrated circuits [2], [8]. The output voltage for each faulty circuit was observed and recorded. Comparisons of the operating output voltages obtained for all of the faulty circuits were made.

The tool used in the design and simulation of the circuits was the computer-aided-design (CAD) tool called TopSpice. CAD tool facilitates the drawing of circuit schematics at the transistor level and performs simulations to check the design specifications of the circuits to ensure that the circuits meet the design specifications. Because the project does not involve fabrication of a physical chip (mainly due to extremely

high fabrication costs) this CAD tool was used to conduct testing.

A programmable feature was incorporated into the system design using multiplexers. The multiplexers were used to select the circuits to be tested. Binary numbers inputted into the multiplexers were used as the codes for selection of the circuit for testing. For example, the binary code 001, when inputted, would allow the multiplexer to select circuit one for testing.

Each circuit was tested individually on the chip. This eliminated the problems associated with testing interconnected circuits. This was important for this study as it increased the efficiency and reliability of the test results. Also, since circuits were selected by the programmable feature used, the isolation of the circuit for test from all of the other interconnected circuits ensured that only the selected circuit was being tested.

Circuit Description and Function

The description and function of the circuits used for this research study are discussed here. Block diagrams of the circuits are also provided.

Digital phase-locked loop (DPLL)

The digital phase-locked loop circuit (DPLL) is an integrated circuit used in modern communication systems. A DPLL circuit is necessary in a communication system because of the data that needs to be processed and shifted to the transmitter output driver. Shifting that data requires a clock signal. Hence, the DPLL performs the function of generating a clock signal which is locked, or in synchronization, with the incoming signal. The generated clock signal is used in the receiver to clock the shift register and, thus, receive the data. This application of a DPLL is referred to as a clock recovery circuit or bit synchronization circuit. Below is a block diagram of a DPLL.

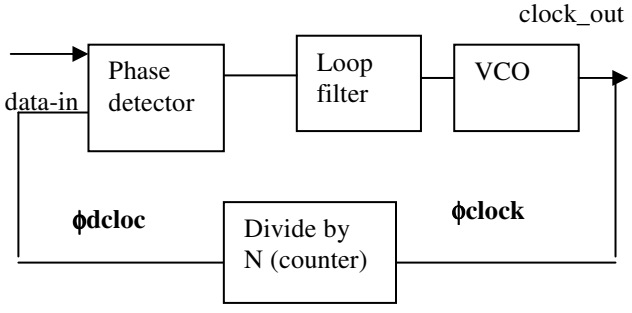

Figure 2. Block diagram of a DPLL circuit

Phase Detector

From the block diagram of the DPLL above, the phase detector (PD) is the first circuit in the loop. There are two types of phase detectors. Each phase detector has its own characteristics. The two types of phase detectors are the exclusive OR gate (XOR) and the phase frequency detector (PFD). For this research study the XOR PD was used.

The XOR PD was chosen for this study because the output voltage is fairly well known. For example, when the input data stream is a string of zeros, the filtered output of the PD is VDD/2, provided the RC constant of the low-pass filter is much greater than the clock signal [9]. Below is a diagram of the phase detector with the loop filter.

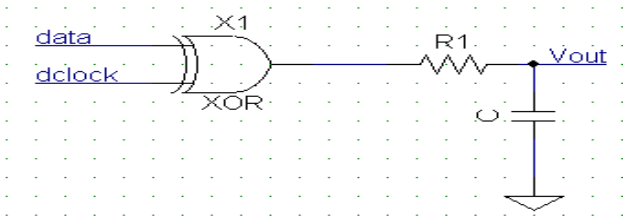

Figure 3. Diagram of the XOR phase detector and low-pass loop filter

Characterizing the Phase Detector

To characterize the PD, consideration is given to the rising edge of the data clock (dclock) and the data. The differences between times for the rising edges were defined as Δt. The phase difference between them was defined as $\Delta\phi$. With the phase for the data as ϕdata and the phase for the data clock as ϕclock, the difference is shown by equation (1) [9].

$$\Delta\phi = \phi\text{data} - \phi\text{clock} = \Delta t * 2\pi/\text{Tdclock} \quad (1)$$

where Tdclock is the period of the data clock.

The DPLL outputs a phase difference which is given by equation (2):

$$\Delta\phi = \Delta t * 2\pi/2\text{Tclock} \quad (2)$$

This phase difference is adjusted by the loop until the phase difference between the DPLL signal and the data is zero. The DPLL is said to be in the lock position. When the loop (DPLL) is in lock state the clock rising edge is centered on the data. Therefore, the time difference, Δt, equals Tclock/2 or Tdclock/4. This makes the phase difference, $\Delta\phi$, equal to $\pi/2$. The average voltage out of the PD, then, is

$$VPDout = VDD * \Delta\phi\pi = (VDD/\pi) * \Delta\phi \qquad (3)$$

The Voltage-controlled Oscillator

The voltage-controlled-oscillator (VCO) circuit oscillates based on the input voltage. The output from the VCO is an oscillating waveform whose frequency is directly related to the input voltage (i.e. fosc α Vvcoin). The gain of the VCO is written as

$$Kvco = (f\ \max - f\ \min)/(V\ \max - V\ \min)(Hz/V) \qquad (4)$$

Because the XOR phase detector was used in the DPLL circuit, consideration was given to VCO designs and the constraint associated with designing the VCO. The constraint relates to the operating frequency range of the VCO; the VCO operating frequency range should be limited to frequencies less than twice the clock frequency but greater than half the clock frequency. The output frequency, fclock, of the VCO is related to the input voltage by:

$$fclock = Kvco * Vvcoin + fo \qquad (5)$$

where fo is a constant.

A seven-stage current-starved VCO was designed for use in this study. A diagram of the seven-stage current-starved VCO is shown in Figure 4.

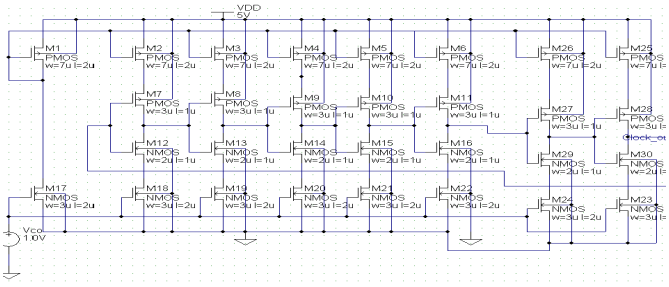

Figure 4. Transistor-level diagram of VCO circuit

To determine the design equation of the VCO, a single stage of the VCO was designed. The stage was repeated N times (N=7); N represents the number of stages.

To design the current-starved VCO to operate at the required frequencies, the time to charge and discharge the total parasitic capacitance was calculated. As shown in the simplified single-stage VCO diagram of Figure 5, the total parasitic capacitance is labeled Ctot. This is the sum of the input and output parasitic capacitance of the transistors making up the circuit. The following calculations show the derivation of Ctot.

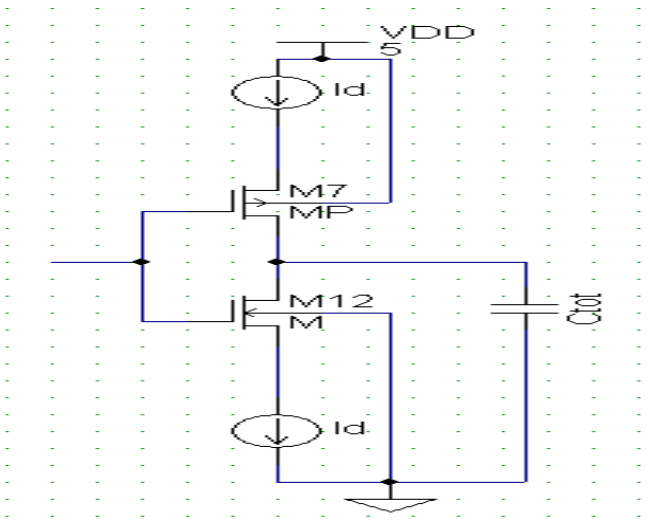

Figure 5. Single stage of VCO for analysis

$$Ctot = Cin + Cout \qquad (6)$$
$$Cin = \tfrac{3}{2} C'ox(WpLp + WnLn)$$
$$Cout = C'ox(WpLp) + WnLn$$

where:

C´ox – is the capacitance of the silicon oxide thickness
Wp - is the width of the pmos-transistor gate
Lp – is the length of the pmos-transistor gate
Wn - is the width of the nmos-transistor gate
Ln – is the length of the nmos-transistor gate

Adding the terms for Cin and Cout yields

$$Ctot = \tfrac{3}{2} C'ox(WpLp + WnLn) + C'ox(WpLp + WnLn) \qquad (7)$$
$$Ctot = C'ox\left[\left(\tfrac{3}{2} WpLp + WnLn\right) + (WpLp + WnLn)\right]$$
$$Ctot = C'ox\left[\left(\tfrac{3}{2} WpLp + WpLp\right) + \left(\tfrac{3}{2} WnLn + WnLn\right)\right]$$

Simplifying and factoring the terms, we get

$$Ctot = C'ox\left[\tfrac{5}{2} WpLp + \tfrac{5}{2} WnLn\right] \qquad (8)$$
$$Ctot = \tfrac{5}{2} C'ox[WpLp + WnLm]$$

Let t1 be the time it takes to charge Ctot from zero to the switching point voltage Vsp of the inverter and t2 be the time to discharge Ctot from VDD to Vsp. Hence:

$$t1 = Ctot * Vsp / Idx \qquad (9)$$
$$t2 = Ctot * (VDD - Vsp) / Idx$$

The oscillating frequency of the current-starved VCO for N-stages (N is an odd number greater than or equal to 5) is given by:

$$fosc = 1/N*(t1+t2) = Idcenter/(N*Ctot*VDD) \quad (10)$$

By setting all of the drain currents, Id, of the transistors equal to Idcenter when Vvcoin = VDD/2, the sum of $t1+t2 = Ctot*VDD/Idcenter$.

Table 2. Inputs and outputs from a fault-free VCO

VCO IN-PUT (V)	PE-RIOD	FREQ. (MHZ)	OUTPUT LOW VOL-TAGE (V)	OUTPUT HIGH VOL-TAGE (V)
0.3	0.685ms	0.0015	0	5
0.4	140us	0.00714	0	5
0.5	24us	0.0417	0	5
1	46ns	21.74	0	5
1.5	12.4ns	80.65	0	5
2	4.5ns	222.22	0	5
2.5	3.6ns	277.78	0	5
3	3.3ns	303.03	0	5
3.5	2.7ns	370.37	0	5
4	2.6ns	384.62	0	5
4.5	2.5ns	400	0	5
5	2.3ns	434.78	0	5

The oscillating frequency, fosc, of the VCO will be equal to the center frequency of the VCO at VDD/2 and the bias current, Id, is equal to Idcenter. The maximum oscillating frequency of the VCO is achieved when the maximum input voltage of the VCO is equal to VDD.

Loop filter

The loop filter is a simple resistor-capacitor low-pass filter with its RC time constant much greater than the period of the clock signal (i.e. RC>>Tclock).

Divide-by-N counter

The divide-by-N counter was not considered in this work since the VCO output voltage was of primary importance and the DPLL locking onto any input signal was not an area of concern.

Digital Phase-locked Loop (DPLL) testing

Testing the DPLL required finding the range of voltages at which the VCO would oscillate. This also provided the range of oscillating frequencies of the VCO. From Table 2, the input voltage range from 0.3V to 5V and the frequency range was from 1.5KHz to 434.78MHz. The design of the VCO also allowed the DPLL (at least theoretically) to oscillate at a low frequency of 1.5KHz. Table 2 also shows the high- and low-voltage outputs for a fault-free VCO.

The DPLL was tested for two types of faults, short- and open-circuit faults (these are the most common faults found in semiconductors), and the high- and low-voltage outputs and frequencies were recorded.

Table 3. Results for short at 1st inverter in the seven-stage oscillator of the VCO

Input voltage (V)	High output voltage (V)	Low output Voltage (V)	Output frequency (MHz)
5	5	0.5	476.2
4.5	5	-0.2	400
4	5	0.4	333.33
3.5	5	0.5	250
3	5	0.3	121.95
2.5	5	0.4	0.050
2	5	0.4	0.025
1.5	5	0.5	0.0181
1	5	0.57	0.010

The plots in Figure 6 show the simulation of the DPLL. The first plot shows the oscillation of the VCO when connected to the Phase Detector and the second plot shows the output of the Phase Detector when it is connected to the VCO.

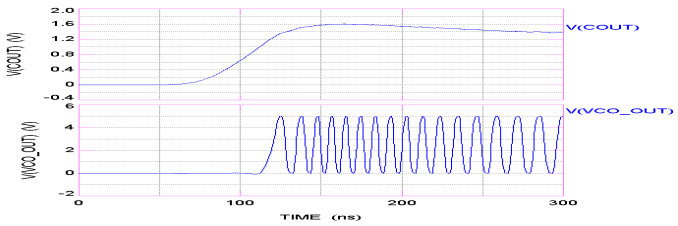

Figure 6. Plots of the DPLL and Phase Detector output voltages

Tables 3 through 8 give the results for faults placed in the VCO circuit. Insertion of faults was made as follows:

Step 1: One short-circuit fault was inserted at a location on the oscillator.

Step 2: Multiple short-circuit faults were inserted at the same time at various locations on the oscillator.

When the faulty circuit was simulated, a low and high voltage and the oscillator frequency were recorded.

Table 4. Results for short at 3rd inverter in the seven-stage oscillator of the VCO

Input voltage (V)	High output voltage (V)	Low output Voltage (V)	Output frequency (MHz)
5	5	-0.21	3.846
4.5	5	0.51	344.8
4	5	0.45	322.5
3.5	5	0.53	232.6
3	5	0.40	117.6
2.5	5	0.46	45.05
2	5	0.32	19.5
1.5	5	0.43	14.7
1	5	0.31	8.26

In Table 5, no oscillation was observed from the VCO; therefore, no low voltages or oscillating frequency were recorded when there were two short-circuit connections on the DPLL's VCO.

Table 5. Results for shorts at 3rd and 7th inverter in the seven-stage oscillator of the VCO

Input voltage (V)	High output voltage (V)	Low output Voltage (V)	Output frequency (MHz)
5	3.75	-	-
4.5	3.75	-	-
4	3.7	-	-
3.5	3.1	-	-
3	2.54	-	-
2.5	2.15	-	-
2	0.75	-	-
1.5	0.49	-	-
1	0.74	-	-

Table 6. Results for open at 7th inverter in the seven-stage oscillator of the VCO

Input voltage (V)	High output voltage (V)	Low output Voltage (V)	Output frequency (MHz)
5	5.52	-0.52	400
4.5	5.35	-0.78	344.8
4	5.3	-0.5	312.5
3.5	5.30	-0.51	270.3
3	5.31	-0.52	204.1
2.5	5.30	0.53	121.95
2	5.21	0.55	94.34
1.5	5.23	0.51	78.74
1	5.0	0.5	48.07

Table 6 gives the results for an open circuit placed at the 7th inverter in the seven-stage VCO. Other open circuit faults placed at different locations caused an error, which prevented the simulator to complete the simulation.

Table 7 shows the no-fault simulation results for the DPLL for the full operating voltage range of the DPLL.

Table 7. Results for the no-fault simulation for the DPLL

Data input voltage (V)	High voltage output (V)	Low voltage output (V)	Phase Detector output (V)	Frequency (MHz)
5	5	0	1.8	111.11
4.5	5	0	1.7	100
4	5	0	1.6	83.33
3.5	5	0	1.63	74.07
3	5	0	1.72	66.67
2.5	5	0	1.65	54.64
2	-	-	-	-
1.5	-	-	-	-
1	-	-	-	-

Table 8 gives the results for introducing a short circuit fault in the DPLL circuit.

Table 8. Results for output of DPLL with a short at the phase detector output

Data input voltage (V)	High voltage output (V)	Low voltage output (V)
5	0.154	-0.64
4.5	0.149	-0.62
4	0.148	-0.61
3.5	0	-0.57
3	0	-0.50
2.5	0	-0.45
2	0	0.40
1.5	0	-0.37
1	0	-0.34

Results from the Digital Phase-locked Loop

Results for the output voltages for a fault-free digital phase-locked loop (DPLL) are given in Table 2. A voltage value called the voltage control oscillator (VCO) input was supplied as input to the oscillatory circuit of the DPLL. This circuit is the VCO and the circuit oscillates based on the magnitude of the input. The higher the voltage input value the faster the oscillation, as seen in Table 2. For the fault-

free circuit, the VCO oscillation goes from rail to rail; the output voltage goes from ground (0V) to the supply voltage value (5V).

Tables 4 and 5 give the results for the short-circuit faults. The short-circuit faults were placed at different locations on the circuit. Each table provides the results for different locations on the VCO circuits. Tables 3 and 4 show that the high-voltage output was not affected but the low-voltage output increased giving voltage values above 0V. These voltage values were similar in magnitude; an indication that the faults were similar.

Testing the DPLL for open circuits was more challenging than testing for short-circuit faults. Table 6 provides the results for the successful simulations performed for an open-circuit fault. Unlike the results for the short circuits where the high output was at the supply voltage, for open-circuit faults the high voltage exceeds the supply voltage and for the low-voltage values, fifty percent of the values were negative and fifty percent of the values were positive.

Generally, the results from this study indicate that types of faults on integrated circuits can be determined by looking at the output voltage of fault-free verses faulty integrated circuits. The results from this study also show that in faulty circuits the output voltages were not within the normal range for output voltage values for fault-free devices. This indicates that identification of faults and type of faults on devices is possible through comparison of output voltages of integrated circuits.

Summary and Analysis

The aim of this study was to explore the possibility of using the output voltage of a faulty SoC device to determine if a built-in-self-test method could be developed to help in determining if a circuit is faulty and the type of fault. The study focused on two of the most common faults found in integrated circuits [2], [8]. These faults are open- and short-circuit faults.

Generally, the results from this study indicate that types of faults on integrated circuits can be determined by looking at the output voltage of fault-free versus faulty integrated circuits. The results from this study indicate that in faulty circuits the output voltages were not within the normal operating range for output voltage values for fault-free devices. This indicates that identification of faults and type of faults on devices is possible through comparison of output voltages of integrated circuits.

The reliability of the results for the circuits studied is evident based on the finding that there was virtually no deviation from one voltage value to the next when the circuits were tested for a particular fault. Generally, the output voltage values had very little difference from each other, irrespective of the location on the circuit where the fault was placed. This was the case no matter what type of fault was used. The results from the study can not pinpoint the exact location of the fault, but can identify the type of fault.

Since each circuit was tested individually on the test circuit setup, this eliminated the problems associated with testing circuits which are interconnected. As a result, test results were obtained faster and were more reliable. Because of the selection circuit used, the circuit under test was isolated from all of the other circuits before testing. This ensured that only one circuit was undergoing testing at a time.

Simulations were also performed to evaluate the extent of error in the circuits used in this study. The results of these simulations identified the magnitude of the error in the circuits as negligible. This provided confirmation as to the reliability of the results. In addition, the results of the simulations performed on the faulty and fault-free circuits to verify that the output values were accurate indicated that the average value and standard deviation of the output voltage values for both the faulty circuit and the fault-free circuit were almost the same; magnitude variations were small. This provides support for the accuracy of the output voltage values obtained and analyzed in this study.

Limitations, Improvements and Expansion

It must be noted that the results should not be used as a one-size-fits-all situation because each circuit has a unique set of characteristics and properties. Therefore, the values obtained should be a guide to testing similar circuits and not as absolute truths. An advantage of this method is that it requires little die space because of the small sizes and numbers of transistors required to build the test-circuit components.

In this study ten pseudo-comparators were used in the test circuit. The number of comparators can be reduced to five. If this test circuitry were implemented on an SoC, this would further lessen the required area on the die and reduce the number of output pins. The downside to that would be more routing of wires, which would be needed to accomplish the connection of each circuit's output to the sole pseudo-comparator. Using more wires for the connections could potentially slow the test circuit and the results obtained. Another improvement would be to upgrade to a more sophis-

ticated software package such as Cadence. This software is more user-friendly and would decrease the time spent going between top-level circuit models and the circuit itself.

In each of the experiments conducted on the circuits in this study, only one type of fault was considered at a time. This way, faults were inserted into the circuits at each setup such that the observations for the effect of each type of fault in each circuit could be recorded. Further work on this topic could include using both types of faults in each circuit. This would expand the study so that the effect of both types of faults on an individual circuit could be studied. In combination, if faults were inserted into each circuit at the same time rather than as separate faults inserted at different times in each circuit, additional information on the effects of a combination of both types of faults on the circuit would be obtained.

Conclusion

The focus of existing literature on SoC testing was on the reduction of the number of input vectors to test integrated circuits and the modification of existing tests for integrated circuits to "fit" the testing of an SoC [2], [10-15]. In this study on SoC testing a new and unique approach was used. The approach used here focuses on the consideration of the output voltage as a factor in the determination of faults in integrated circuits. To determine the effects of the faults and the type of fault within the circuits, a comparison was made between faulty and fault-free circuits and their output voltage values.

The results of this study showed that output voltages can be utilized to determine the characteristic of any circuit; that is, whether the circuit is faulty or fault-free. The results obtained in this study indicated major differences in the output voltage values of faulty circuits and fault-free circuits. In faulty circuits, the output voltage values obtained were much lower than the output voltage values obtained for the fault-free circuits; in fault-free circuits, the output voltage values were generally much higher.

It is evident from the results of this study that the type of fault affected the output voltage values for each circuit. The results showed small variations in the range of output voltage values obtained for short circuits and open circuits where the faults inserted into the circuits were the same class. Much larger variations in the range of output voltage values were obtained for short circuits and open circuits where different classes of faults were inserted into the circuits. In addition, the results showed that the location of the inserted fault did not affect the magnitude of the variations in the range of output voltages obtained for either circuit.

The contribution of this study was to provide a new experimental approach for testing an SoC. This adds value to the existing research on SoC testing by providing an approach that allows for distinguishing between faulty and fault-free circuits as well as in determining the type of fault within the circuits. This adds a unique perspective to and expands the body of research on SoC testing. The body of research on SoC testing now includes not only the reduction of the number of input vectors to test integrated circuits and modification of existing tests for integrated circuits to "fit" the testing of an SoC, but a method (described throughout this study) for distinguishing faulty circuits from fault-free circuits as well as the type of faults within the circuits.

Acknowledgments

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Biographies

DR. G. THOMAS received the B.S. degree in Electrical Engineering from New Mexico State University, Las Cruces, New Mexico, in 1999, the M.S. degree in Electrical Engineering from New Mexico State University, Las Cruces, New Mexico, in 2001 and the Ph.D. degree in Electrical Engineering from New Mexico State University, Las Cruces, New Mexico 2006, respectively. Currently, He is an assistant Professor of Electrical Engineering Texas Southern University. His teaching areas include Digital signal processing, Electronics, DC circuits, and C++ programming.. His research areas include alternative sources of energy, globalization of engineering, integrated circuit design, digital signal processing and application and microprocessor/controller design and use in embedded systems. Dr. Thomas may be reached at thomasg@tsu.edu

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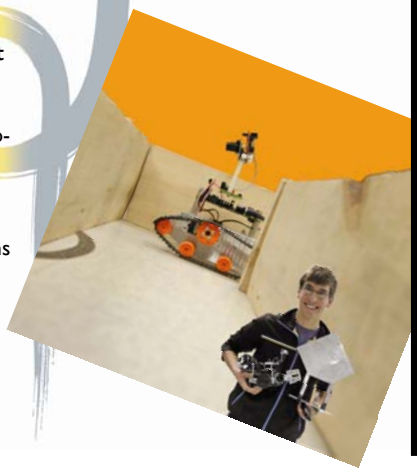

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