Single Event Upset at Ground Level

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Abstract
Ground level upsets have been observed in computer systems containing large amounts of random access memory (RAM). Atmospheric neutrons are most likely the major cause of the upsets based on measured data using the Weapons Neutron Research (WNR) neutron beam.

I. INTRODUCTION

Several years after single event upset (SEU) was discovered in space in 1975, J. Ziegler [1] noted the potential for microelectronics on the ground to be susceptible to SEU from cosmic ray secondaries, primarily neutrons. Ziegler's work was prompted by the work of T. May and M. Woods [2] in uncovering errors in RAM chips due to upsets caused by the alpha particles released by U and Th contaminants within the chip packaging material. The alpha problem was regarded seriously and chip vendors took specific actions to reduce it to tolerable levels, mainly by reducing the alpha particle flux emitted by packaging and processing materials to generally < 0.01 α/cm^2-hr [3].

Unfortunately, the potential for cosmic rays causing SEU on the ground received little attention, and has received almost no public recognition on the part of chip vendors. Very recently, IBM revealed that beginning in 1979, they undertook a very large proprietary effort to understand the phenomenon of upsets at ground level. This 15-year effort involved many different disciplines and activities: field testing of memories, accelerated testing using cyclotron beams, detailed model development on all levels, environmental monitoring and coordination with device designers [4]. In contrast to the lack of recognition of the key role played by cosmic radiation for ground level upsets, the importance of this mechanism was recognized by people dealing with avionics, i.e., electronics in aircraft, relatively early in the open literature. Avionics SEU by the atmospheric neutrons was first predicted in 1984 [5] and later rigorously demonstrated to occur in flight in 1992[6].

II. GROUND LEVEL NEUTRON FLUX

The neutron environment at ground level can be defined in terms of the models for the atmospheric neutron flux at higher altitudes which are mainly based on neutrons in the energy range of 1<E< 10 MeV [7]. A number of studies have shown that the shape of the energy spectrum of the atmospheric neutron flux doesn't change with altitude or latitude, even though its absolute magnitude does vary with location and altitude around the earth [7]. Limited data from a sophisticated ground-based detector system made at 100, 5000 and 10,000 feet above sea level indicate that the 10-100 MeV flux falls off approximately linearly with altitude [8]. Very few measurements of the neutron spectrum at ground level have been made, especially over the entire energy range. One set of the most recent terrestrial spectral measurements, made in Japan [9], was normalized to obtain the neutron spectrum expected in the US, based on scaling airplane spectral measurements made over Japan [9] and the US [10]. These spectra show that the ground spectrum is roughly 1/300 of that at 40000 ft.

III. SINGLE EVENT UPSETS AT GROUND LEVEL

There is considerable evidence of upsets on the ground, but it has been largely kept proprietary or else it has been in the hands of computer systems engineers who do not understand its meaning or implications. In the following paragraphs we will present various examples of this kind of data, including reference to the very recently revealed vast storehouse of data obtained by IBM over a 15-year period via a well-coordinated proprietary effort. In addition, five specific examples will be cited, one from a very large computer system that was taken off line for testing, two from the error log/maintenance history of a collection of large computers, one from a biomedical device utilizing SRAMs that has been implanted in hundreds of patients and one from the system soft error FIT rate (failures in time, i.e., 10^9 device hours) testing performed by RAM vendors.

In addition, we believe that there are extensive collections of other data that provide evidence of these upsets, e.g. in the error and/or maintenance logs of large computer systems. In particular, the error logs of computer systems located in high altitude cities, such as in the Rocky Mountain region, are expected to reveal many such upsets. Although at present such records have not yet been made public, we hope that with the publication of this work, other SEU workers will work cooperatively with computer systems people within their organizations to uncover and reveal the large compilations of errors that exist. These errors have been detected, corrected and logged by the dedicated software and hardware within those computer systems, so the computer systems engineers are satisfied that their systems are well protected. However, in addition, the EDAC (error detection and correction) systems that work so effectively in protecting the large computer systems, can also reveal the mystery of those upsets to SEU researchers who understand the mechanisms causing the errors.

III.A Early IBM Study

An early study showed that when a large number of memories was monitored for single event upset at three locations of varying altitude (5000 feet, sea level and in a mine), the upset rate decreased with decreasing elevation, indicating that atmospheric neutrons are the likely cause [11]. This study has been recently published in a much updated format [12, 13] that carefully separates out the upsets caused by alpha particles emitted by trace elements in the device package from those caused by the atmospheric neutrons. Using the atmospheric upset rate component at three locations within the US, the variation with altitude is the same as the atmospheric neutron flux variation with altitude [12,13]. The very recently issued special edition of the IBM Journal of Research and Development (entirely devoted to the subject of ground level upsets), has a great deal of additional information on the many similar proprietary tests that IBM performed. The results of most of those tests are, however, presented in a relative or normalized format. In those instances in which we can infer absolute error rates, that data will be utilized (see discussion of FIT rates and Table 2 below).

III.B Upset Rate in Fermilab Computer System

The computer system ACPMAPS at Fermilab is a very large system of individual computers, which when joined together, contains about 160 Gbits of DRAM memory [14]. The ACPMAPS is housed in a computer building far removed from the very high energy Fermilab accelerators. It contains 156 Gbits of 4 Mbit fast page-mode DRAM, guarded by parity but not protected by EDAC. In production it consistently experiences single bit errors on an almost daily basis. When the entire system was taken off-line for testing, it routinely gave an upset rate of 2.5 upset/day or 7E-13 upset/bit hr.

It did not appear that these errors were being caused by alphas in the packaging material. First, the rate observed was 5-10 times larger than that which could be inferred from the results of the manufacturers' non-accelerated failure tests, and more than 500 times larger than the FIT rate based on extrapolating from accelerated failure tests with an alpha source. Second, the chip vendor indicated that, based on lab tests with alpha sources, almost all alpha-induced upsets in these DRAMs occur when a "page miss" (a change in the row address) causes 4K bits of data to move from the DRAM cells to a small on-chip SRAM page. The window of vulnerability occurs when the long lines to the DRAM cells are active, so the error rate should be proportional to the rate of page misses (plus refreshes). Contrary to this, Fermilab found that the 2.5 upset/day rate was independent of the rate of page misses, which was varied by over a factor of ten. Finally, as May and Woods showed [2], the alpha induced upset rate is extremely sensitive to critical charge, Q_c, the charge that has to be deposited in a device to "flip" a logic state, e.g., $0 \rightarrow 1$ [1], (factor of > 100 reduction in the rate for a doubling of the Q_c value), whereas with neutrons and the recoils they produce, it is much more gradual. The Fermilab system contains DRAMs from two different manufacturers (and therefore, almost certainly, with different Q_c values) and yet these showed no significant difference in upset rate. Other large computer systems with different DRAMs, including workstation clustered "computer farms" at Fermilab, also exhibit about the same upset/bit-hour rate as observed for ACPMAPS. The observed upset rate in the DRAMs of the ACPMAPS is much more consistent with the SEUs being caused by the atmospheric neutrons rather than packaging material alphas as will be shown below.

III.C Upset Rates in Large Computer Systems

An increasing number of off-the-shelf computers, in the workstation and larger classes, are being designed to incorporate EDAC to protect the RAM from errors. One such model is the Nite Hawk computer. Each Nite Hawk has approximately 1Gbit of DRAM memory, apportioned between global and local memory. Many of these computers have been used in a local systems integration laboratory, where the computer vendor also has the job of performing monthly maintenance on the machines. An informal assessment by the computer maintenance people is that on the average, each machine shows one upset (parity error) per month, with some having two errors and some none. Using the average value of one error per month (defined as 624 hours), this is equivalent to a ground level upset rate of 1.6×10^{-12} upset/bit-hr.

A more accurate measure of the error rate was obtained based on a small number of errors from the error logs, acquired over a few-month period of time. The SYSERR logs of five Nite Hawk 5800 computers were checked; four are simulation computers and the fifth is a development computer. The logs for the four simulation computers covered about 4 months, while that for the developmental computer covered seven months. The four simulation computers experienced 0,1,2 and 3 errors respectively; two of the six errors were in global memory and four in local memory. The amount of total memory available in these four computers varies. All have 64 Mbytes of global memory, two have 160 Mbytes of local memory and two have 256 Mbytes of local memory. Thus two machines have available 1.8 Gbits and two have 2.6 Gbits of memory. At present on average the memory usage on the simulation computers is estimated to be approximately 50%. This leads to an upset rate of 2.5 E-12 upset/bit-hr.

The developmental computer appears to be run on a more consistent basis. Its error log covered a time period of ~30 weeks. This computer has 64 Mbytes in global memory and 64 Mbytes in local memory for a total of 1Gbits. For this machine an 80% usage factor for the total memory was estimated, and over that time period 2 errors (one in global memory and one in local memory) were encountered. The

error rate for the developmental computer is thus 1.7E-12 upset/bit-hr. A more representative error rate was obtained by averaging the error rates of the all five of the Nite Hawk computers and this works out to 2.3E-12 upset/(bit-hr).

A second independent source of upset data is the Cray YMP-8 located about ten miles away from the Nitehawk computers. The main memory of the YMP-8 consists of 32 modules, each with 256 Mbits of SRAM, for a total of ~8.2 Gbits of SRAM. Each module comprises one thousand 256K ×1 SRAMs. The system is protected by a standard EDAC system know as SECDED, single error correct, double error detect. Upsets are found only during the read operation. SECDED is implemented by having Hamming code generated on every write operation. On every read operation the 72 bit word (64 bits comprising the word, 8 extra Hamming code bits) is again checked by the error detection circuit. If a single bit is off, the bit is corrected and the error logged; if a double bit error is found, no correction is attempted, but it is logged and flagged and the entire module is replaced. The new Cray Triton T-94 system , uses double error correct, multiple error detect (DECMED) system employing 12 check bits so that double bit errors can be corrected. It uses 2M×2 SRAMs to comprise the memory in its modules in very compact memory stacks.

We were able to gain access to the system error logs for this Cray YMP-8 covering a period of 22 months (May 1992 - February 1994). Over that time period, 30 out of the 32 modules experienced one or more parity errors. During the first 16 months the parity errors were logged and date stamped, but this changed in August 1993, after which the errors were logged but without a date stamp. To extract individual upset data required careful interpretation of the error logs. This was made easier through the assistance of the systems engineer, but it also required several assumptions to be made in order to interpret the data in a consistent manner. Two examples of errors that were not counted as random errors are illustrative: 1) errors in "flaky" RAM chips (defined as a chip that had the same error at the same location on 2 or more days over the 22 months) and 2) the large number of single bit errors that occurred on Oct. 11, 1992 in four modules during preventative maintenance (PM) because the PM-induced errors were registered in the modules in which the EDAC diagnostic wasn't turned off.

The parity error data was converted into a distribution of parity errors per module. This distribution function is shown in Fig. 1 and is normalized to the errors occurring on an annual basis. Since it is set up as a cumulative distribution, we see that 50% of the modules will have 1.8-2 or more errors per module-year. This is consistent with the mean number of errors which is 2.3 error per module-yr. The figure also shows the theoretical cumulative probability function for a Poisson distribution based on a mean rate of 2.3 error/module-yr. The generally good agreement between the Poisson distribution and the actual upset data indicates that the source of most of the errors is random, such as SEUs produced by the atmospheric neutrons. It also indicates that the high error rates (> 8 error/module-yr) in two of the modules may be due to more than random error.
The distribution also shows that the 10% most error-prone modules will be experiencing at least 6 error/module-yr. The utilization factor of the main memory is about 80% which has to be used to obtain a meaningful bit error rate that can be compared to the rate in other systems. Using the mean upset rate of 2.3 error/module-yr (133 total upsets), this converts to a bit error rate of 1.3E-12 upset/bit-hr.

In addition to the main memory, the Cray also has a secondary bulk storage memory system called the Solid State Device (SSD). The SSD consists of a total of 32 Gbits of DRAM, in this case all in the form of 4M×1 DRAMs, and it too is protected by EDAC. The error logs from the SSD were studied for the same 22-month period of time and it was found that the average number of errors was 2.7/ month for a total of 60 errors. The utilization factor for the SSD is lower than for the main memory, with a value of 20% being a rough estimate. Therefore the 2.7 error/month converts to a bit error rate of 6E-13 upset/bit-hr. The DRAMs also exhibited double bit errors, a total of 17 or ~28% of all the errors. However 10 of the 17 double bit errors occurred during only two of the months. The number of single bit errors for those two months was high but similar to the number of single bit errors during several other months, and the number of errors in the main memory during those two months was about average. Thus, although it is unclear why so many double bit errors occurred during those two months, it appears that the memory usage in the SSD may have been much higher than usual during those periods.

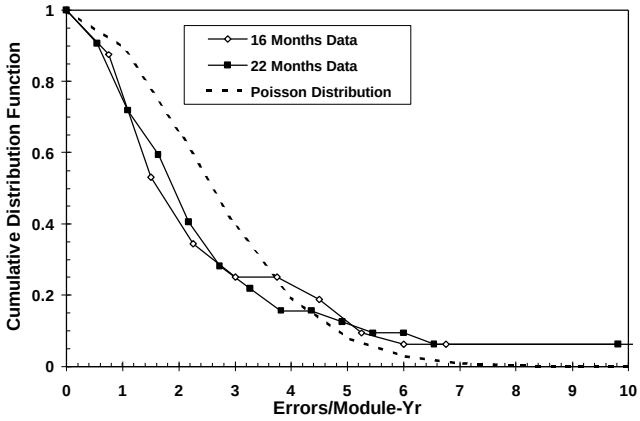

Figure 1 The Cumulative Dsitributiuion Function for Ground Level Errors (Error/Module-Year) in the Main Memory of theCRAY YMP-8

III.D UPSET RATES FROM FIT RATE TESTS BY RAM VENDORS

RAM manufacturers typically perform two types of quality control tests at their facilities in which they record the bit error rate, the rate being given in FIT units: a) system soft

error rate (SSER), by monitoring 1000 parts for 1000 hours, and b) accelerated SER (ASER) obtained by using a radiation source. Historically, RAM vendors have used alpha sources to conduct their accelerated tests. The use of alpha sources for these tests goes back to the early problem of alpha contaminants in the chip packaging causing upsets [2], and it was standardized in terms of a test procedure [16]. However, use of the alpha source does not provide an accurate indication of the ground level upset rate as Lage [17] directly showed by comparing SSER and alpha-source ASER rates. Three other types of ASER testing have been proposed and used: a) proton beams to simulate neutron-induced upset (IBM, [18]), b) the WNR neutron spallation source at Los Alamos (TI [19] and Boeing [20]) and c) a 14 MeV neutron generator (used in conjunction with a calculational method by Boeing [21]).

Examination of SSER FIT rates provides an excellent method of inferring the ground level upset rate. Unfortunately, few such measurements have been published. Those that are available are listed in Table 1 which contains test data conducted by Motorola [16] and by IBM [17]. The upset rates are presented in terms of the FIT rate as well as the per bit rate. All of the Motorola data, which are for various types of Motorola SRAMs, are from SSER tests, and this data has error bars to indicate the poor statistics involved (typically very few errors, e.g., < 5, are measured). The IBM data includes measurements from both SSER (field) and ASER (proton beam) tests on 1M and 4M DRAMs . Two factors are to be noted with the IBM upset data: each of the averaged FIT rates is for a DRAM is from a different vendor, and there are no error bars indicative of the upset statistics.

Table 1 Ground Level Soft Error Rates Measured by RAM Vendors (IBM and Motorola) in a Variety of RAMs

Data By	RAM Size	RAM Type/ Test†	# Diff Devs	Avg. FIT Rate	Range FIT Rates	Average Up/bit-hr
IBM	4M	D/A	5*	3500	53-10,300	8.9E-13
IBM	1M	D/A	2*	3300	2500-4100	3.3E-12
IBM	1M	D/F	2*	325	230-420	3.1E-13
Mot	256K	S/F	3	500	450-560‡	2E-12
Mot	1M	S/F	2	2070	1330-2800‡	2.1E-12
Mot	4M	S/F	4	5750	4500-8900‡	1.5E-12

† D=DRAM, S=SRAM, A indicates accelerated testing using proton beam, F indicates field testing (1000 parts, 1000 hrs)
* In this case each device type was from a different vendor
‡ Each of these individually measured FIT rates had an uncertainty of about a factor of 4 (2-0.5) based on the small number of upsets and the probabilistic treatment of its confidence level

We note a wide variation in the upset rate among the various DRAM devices and significant differences between the SSER and ASER results which is not typical of the measurements in many of their other tests. Nevertheless, taken as a composite, the ground level RAM upset rates listed in Table 1 are relatively consistent, mainly in the range of 1-2 E-12 upset/bit-hr, and are therefore similar to the ground level upset rates measured in the large computer systems discussed above.

IV. ANALYSIS

In summary, five different sources of ground level upset rates in RAM devices have been discussed. These are tabulated in Table 2. The upset rates agree with one another within less than an order of magnitude, and a rate in the range of 1-2 E-12 upset/bit-hr appears to be about average. Thus the simple average value of 1.5 E-12 upset/bit-hr represents the entire range of rates, 0.3-2.3 E-12 upset/bit-hr, for both DRAMs and SRAMs, from the diverse sources of data.

Our hypothesis is that the great majority of these upset are caused by the atmospheric neutrons, i.e., the cosmic ray secondaries at ground level. To demonstrate this, we will tabulate SEU measurements made on both SRAMs and DRAMs that were tested in the WNR neutron beam at the Los Alamos National Laboratory. As we have previously shown [22], the WNR neutron spectrum is essentially identical to that of the atmospheric neutrons. One hour in the WNR beam is equivalent to 2-3 E5 hours (beam intensity varies from year to year) at 40,000 ft, or alternatively, 6-9 E7 hours at ground level (the neutron flux at ground level is taken as 1/300 of that at 40,000 ft.).

Table 3 contains the WNR SEU cross section measurements on three DRAMs and six SRAMs, one of which has been previously published [22]. The WNR SEU response of the six SRAMs on a per bit basis shows a fairly wide variation. However, when the Cypress parts, the only RAMs that exhibited multiple bit upset (a few percent of the single errors), are removed, the variation narrows significantly. It narrows even further if the only 4M SRAM, the MCM6246, which is notably less sensitive, is also removed. Among the three 4M DRAMs, there is also some variation, with the Oki part being notably less sensitive than the other two. None of the nine RAMs exhibited neutron-induced single event latchup, as was to be expected [20].

Column 4 of Table 3 contains the WNR SEU cross section (upsets/fluence > 10 MeV), column 5 the scaled SEU rate at ground level (based on a flux of 19.3 n/cm²-hr on the ground) and column 6 the ground level SEU rate calculated using the burst generation rate (BGR) method [20]. The scaled neutron-induced SEU rates are in the same range of 0.5-2 E-12 upset/bit-hr as those actually measured on the ground as tabulated in Table 2. Thus in making the comparison between the measured bit error rates from computer error logs, field SER data, etc., summarized in Table 2, these error

rates directly correlate with the neutron-induced upset rate from WNR measurements tabulated in Table 3. A direct comparison of the field upset rates and the rates scaled from the WNR measurements is shown in Table 4.

As indicated, use of the WNR beam to measure RAM SEU rates is one of several accelerated SER methods, probably the best one because this neutron beam is so similar to the actual atmospheric neutron spectrum. The IBM method uses a beam of 150 MeV protons to simulate the atmospheric neutrons [18], and they apply an empirically derived factor that ranges between 12 and 17 to convert the measured SEU cross section to the ground level SEU rate (factor varies with type of RAM[18]). This is very similar to the use of the WNR beam, summarized in Table 3, in which the conversion factor is just the hourly neutron flux at ground level > 10 MeV, 19.3 n/cm²-hr, that converts the WNR SEU cross section to the ground level SEU rate. Because of the limited access of the WNR beam [20], we use another method which utilizes heavy ion SEU cross section data via the BGR calculation method [8,31], as an efficient alternative to using the WNR. The effectiveness of this approach has been previously demonstrated [22] for a few RAMs. By comparing columns 4 and 5 of Table 3 we provide further evidence of the effectiveness of the method. Nevertheless, this BGR approach is augmented by measuring the SEU cross section with 14 MeV neutrons to normalize the BGR parameters, before applying them to the atmospheric neutron spectrum.

Having demonstrated that the atmospheric neutrons are primarily responsible for the ground level upsets, there are a number of impacts that this cause-effect relationship has that extend beyond the SEU community. Some of these impacts are summarized in Table 5 and include: a) improving the reliability of large computer systems, b) applying error mitigation techniques to RAMs used in biomedical, commercial and industrial products, c) imposing realistic reliability standards on microelectronics to encourage the development and use of low FIT-rate chips, and d) utilizing the appropriate and available accelerated SER techniques/tests to measure ground level FIT rates.

The diversity of applications in item b) is extremely broad. Biomedical devices tend to be expensive, but due to the urgency of health considerations, additional costs for EDAC or SEU-immune chips can be readily absorbed and passed on. Industrial products might focus on process control applications for which some additional costs might also be warranted to protect against RAM errors. In contrast, commercial products tend to be highly cost competitive, and so the extra costs of error mitigation techniques might be hardest to justify. However, in some instances, such as those related to financial transactions and “smart” cards, or the use of microelectronics-based automobile systems, the vital importance of dealing with such ground level errors, which are to be expected if no mitigation techniques are used, may be much more apparent. Each product may use << 1Mbit of RAM, but because millions of units expected to be sold, the total number of bit-hours in operation may still be large.

V. CONCLUSIONS

Thousands of single event upsets are occurring every year on the ground, yet few in the SEU community are aware of them. These upsets have been recorded mainly in large computer systems equipped with EDAC to detect, correct and log in these errors. We have examined a few such error logs from large computers, as well as other sources of ground level upset data. All of this data is consistent with the atmospheric neutrons being the main cause of the upsets. It is also the same conclusion reached years ago by the IBM team that investigated this topic privately [4]. We demonstrated the correlation by comparison with the neutron-induced SEU rate

Table 2 Tabulation of Ground Level RAM Upsets

System and Location	RAM Type	Total upsets	Ground Upset Rat Up/bit-hr	Basis for Ground Rate
ACPMAPS Compute Network, Fermilab	DRAM	35	7E-13 [15]	System w/ 160 Gbits of DRAM had 2.5 upsets per day
Motorola-APRDL Field SER tests	SRAMs	>30	1.8E-12 [17]	1000 parts for 1000 hours, FIT rates of 500-5000 upset/1E9 hours
IBM Field Tests	DRAMs	?	0.3E-12	Ref. [18]
Cray YMP-8, Seattle, WA	Fujitsu SRAM	133	1.6E-12	Error log record (22 months), reviewed and interpreted
Cray YMP-8, Seattle, WA	DRAMs	60	0.6E-12	Error log record (22 months), reviewed and interpreted
Nite Hawk 5800 Computer Seattle, WA	Toshiba DRAM	8	2.3E-12	Upsets from error logs. Memory utilization from Nitehawk system administrator
Nite Hawk Computers (4800 5800) Seattle, WA	Toshiba DRAM	?	~1.6E-12	Computer maintenance people report ~ 1 upset per month (624 hr.) in each of 58 computers, each w/ 128 MBytes
Simple Average			1.3E-12	

Table 3 RAM SEU Rates at Ground Due to Atmospheric Neutrons Based on Measured SEU Cross Sections in WNR Beam

RAM	Vendor	RAM Size/Type*	Meas'd WNR SEU X-section, cm^2/bit	Gr'nd level SEU Rate, Up/bit-hr, WNR-Scaled	Calculated Gr'nd SEU Rate, Up/bit-hr, BGR Method	Weibull Fit Heavy Ion Parameters Used in BGR Calculation %
TC514400-80	Toshiba	4M/D	1.2E-13	2.3E-12	2.1E-12	4.7E- 7, 0.85, 18.3, 1.13 #
MSM514400-80	Oki	4M/D	2.2E-14	4.3E-13	N/A	N/A
TMS44100[22]	TI	4M/D	9.3E-14	1.8E-12	2.3E-12	3.1E-7 , 0.9, 9.43, 1.24
IDT71256	IDT	256K/S	6.5E-14	1.3E-12	2.3E-12	7.4E-7, 2.66, 16.4, 1.19
HM65656	Matra	256K/S	1.9E-13	3.7E-12	1.2E-12	3.8E-7, 1.98, 11.46, 2.24 ‡
MCM6206	Motorola	256K/S	1.4E-13	2.7E-12	7E-13	2.7E-6, 2.64, 3005, 0.63§
MCM6246	Motorola	4M/S	1.25E-14	2.4E-13	3.4E-13	5.3E-8, 1.1, 5.45, 6.88
CY7C195¶	Cypress	256K/S	5.7E-13	1.1E-11	8.4E-12	2.98E-6, 1.02, 33.7, 1.08 †
CY7C199¶	Cypress	256K/S	5.2E-13	1E-11	"	"
Simple Average for 9 RAMs			1.93E-13	3.72E-12	2.48E-12 (7 unique RAMs)	

*Part Type descriptions: D=DRAM and S=SRAM

% Weibull parameters (see [8]) are in following order: σ_0 (per bit), L_0, W and S; BGR method (see [20]) assumed t=2 μm and C=0.5 in all cases; Weibull parameters are from following related RAMs: # TC514100Z-10, ‡ HM65656 engineering samples [23], § MCM6226, and † CY7C185

¶ These parts exhibited multiple bit upsets during the WNR testing.

based on measurements with the WNR neutron beam. We have not focused on any one specific DRAM or SRAM, but rather on a representative sampling of RAMs to show that the correlation applies to both SRAMs and DRAMs, and applies fairly well regardless of which commercially available RAM is used (however this is not true for those RAMs specifically designed to have a low SEU sensitivity, e.g. the IBM LUNA-C and E DRAMs [26]).

An upset rate in the range of 1-2 E-12 upset/bit-hr was shown to be representative of the rate that most SRAMs and DRAMs in actual field applications are experiencing, although there were a few with lower rates (see Table 2). The upset rate of 1-2 E-12 upset/bit-hr leads to FIT rates of 1000-2000 FITs for a 1Mbit RAM, which is just at the limit of 2000 FITs for soft errors given in the STACK specification for integrated circuits [25]. Thus we would expect that most RAMs of larger memory capacity than 1M (e.g., 4M, 16M, etc) would not meet the STACK limit in actual field applications. RAM tests using an alpha source may yield a rate lower than this limit, but this study, and that by Lage [17], show that this is an erroneous test. The atmospheric neutrons are the cause of most of the upsets on the ground, and the alpha particles do not simulate the neutron interactions with the RAMs, they only simulate alphas emitted from the chip package.

It should be noted that gaining access to error logs may not always be very easy. There is the case of one supercomputer manufacturer who, through a very stringent purchase agreement, precludes any owner of the supercomputer from divulging error information about that computer system. In the case of workstations, which today have on the order of 1Gbit or more of DRAM, EDAC (ECC, error correcting code, in their nomenclature) is still incorporated, but the correctable errors are no longer logged. The exact reason for eliminating the error logging is unclear (100% confidence in the ECC, increased speed, lower cost, etc.), but it will have an impact . On some of the older workstations that had much smaller memory capacities, the errors were in fact logged, but because of the smaller memory size, the errors occurred much less frequently. Systems administrators familiar with these older workstations can recall seeing the occurrence of single bit errors. Based on the data we presented, the 1Gbit workstations should experience 1-2 errors per month, depending on how much of the memory is being used on a daily basis. However, since memory requirements have expanded so dramatically over the last few years and are still continuing to do so, the number of errors are likely to continue to increase at a rapid rate. However, without the error logs, there will be no way to track this expected trend in increasing errors.

It has been suggested that it is the thermal neutron portion (E ~ 0.025 eV) of the atmospheric neutron spectrum, rather than the high energy portion (E> 10 MeV), which is mainly responsible for the upsets [27]. In this case the mechanism is that of the thermal neutrons interacting with the B^{10} fraction of the boron in the borophososilicate glass (BPSG) within the glassivation layer over the die that produces alpha particles. The energy deposition by the alphas leads to the upsets [27]. A very similar mechanism was investigated earlier with respect to the B^{10} content of boron dopants in microelectronics [28]. That analyis found that both the 1.5 MeV alpha and the 0.8 MeV Li recoil produced by thermal neutron interactions with B^{10} can deposit energy leading to

Table 4 Direct Comparison of RAM SEU Rates at Ground Level, From Field Measurements and Scaled from Measured SEU Cross Sections in WNR Neutron Beam

	Observed Upset Rate From Measurements in Field		Upset Rate From WNR SEU Measurements	
RAM	System/SER Upset Data	Gr'nd SEU Rate, Up/bit-hr	Similar RAM tested at WNR	Gr'nd SEU Rate, Up/bit-hr
DRAM	ACPMAPS Computer Network Fermilab, Batavia, IL	7E-13	TC514400-80	2.3E-12
"	IBM Field Tests	3E-13	MSM514400-80	4.3E-13
"	CRAY YMP-8 Computer, Bulk Storage, Seattle, WA	6E-13	TMS44100	1.8E-12
"	Nite Hawk 5800 Computers, Seattle, WA	2.3E-12		
DRAM	Simple Average	1E-12	Simple Average	2E-12
SRAM	Motorola-APRDL Field SER tests, Malaysia	1.8E-12	IDT71256	1.3E-12
"	CRAY YMP-8 Computer, Main Memory, Seattle, WA	1.6E-12	HM65656	3.7E-12
"			MCM6206	2.7E-12
"			MCM6246	2.4E-13
"			CY7C195	1.1E-11
"			CY7C199	1E-11
SRAM	Simple Average	2E-12	Average (6) w/ Cypress	5E-12
			Average (4) w/o Cypress	2E-12

Table 5 Impacts of Identifying Atmospheric Neutrons as Cause of Ground Level Upsets

Impact	Nature of Impact
Improve reliability of large computer systems	Reduce RAM sensitivity through techniques know to SEU community [EDAC, SEU-immune SRAMs, use of other memories less susceptible to SEU (e.g., EEPROMs, flash EEPROMs, etc.)]
Apply error mitigation techniques to RAMs in biomedical, industrial and commercial products	Utilize existing expertise and methods to reduce possibility of RAM upsets at ground level in devices having wide-spread use (thousands-millions of individual products). In commercial products use of low SEU-sensitive RAMs is generally precluded because of increased cost. Example of LUNA-E and C (EDAC) DRAMs developed by IBM to have low SEU rates. However, to be competitive in their THINKPAD laptop computer, IBM uses non-IBM DRAMs [24] because they are cheaper.
Impose realistic reliability standards on microelectronics industry to develop low FIT-rate designs	As RAM devices continue to increase in memory capacity, microelectronics will not be able to meet standards set by its own industry, e.g., 2000 FITs (per device) in STACK Spec 0001, Rev. 12.1 [25]. They meet it now because the same standard provides for only an α source test, and α's are not the real cause of the errors. Once atmospheric neutrons are recognized as main cause of errors, they will not be able to meet the maximum allowed FIT rate for RAMs > 1 Mbit.
Utilize available accelerated SER techniques/tests	Effective SEU testing techniques can be applied to RAMs to quickly determine their ground level sensitivity to upset (FIT rates). These test techniques are a much better and quicker way to provide feedback on the susceptibility of specific new RAM design features than the existing methods (alpha source and SSER tests) that are used.

upsets [28]. In that case, even for the most sensitive RAM tested with thermal neutrons, the upset cross section, in cm^2/bit, was about three orders of magnitude smaller than that from the WNR beam (Table 3). Furthermore, ground level thermal neutron fluxes are greatly influenced by the effects of topography, soil water content and surrounding man-made materials [29]. For a very simple air/material geometry, the thermal neutron flux at the interface varies by a factor of 5 depending on the material [29]. This implies large variations in the thermal flux are possible just due to the material/geometry configuration surrounding a particular computer. In contrast, the measured ground level upset rates in Table 2 show much less variation. Thus for a number of reasons, including complete uncertainty of the BPSG content of commercial SRAMs and DRAMs, large variation of the ground level thermal neutron flux from location to location,

and old measurements showing a much lower upset cross section, we believe that the contribution of thermal neutrons to the ground level upset rate is small.

It has also been suggested that other cosmic ray secondary particles, protons and pions, may also be responsible for the ground level upset rates [30]. These particles may contribute to some portion of the ground level upset rate, but the correlation above, between the measured ground level bit error rate (from error logs, RAM SSER FIT rates, etc.) and the WNR SEU rate measurements, indicate that the atmospheric neutrons are the dominant cause. We expect that additional examinations of other sources of ground level errors will further verify this contention. Such studies might show the effects of latitude and altitude on ground level rates, e.g., similar to the variation of the atmospheric neutron flux with latitude and altitude [8], and of variations in the SEU response of different RAMs, such as that seen in Table 3. Furthermore, such examinations will hopefully lead to expanded cooperation between the SEU community and the designers of microelectronics, computer systems and the diversity of commercial electronic products that use significant quantities of RAM, in terms of accounting for the effects of SEU in those products.

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