TECHNICAL INFORMATION

RELIABILITY MANAGEMENT OF TANTALUM CAPACITORS

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Abstract:

Tantalum capacitors can achieve high reliability in steady state applications. Tantalum capacitors have highly stable capacitance and frequency dependent characteristics. Short circuits are a low level, but not negligible, failure mode. Because of this, reliability management of tantalum chips means the effective control of the S/C failure mode, not least because this mode cannot be designed around by use of redundancy circuits, etc.

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Introduction

Tantalum capacitors are characterized by four performance parameters:

Capacitance (120 Hz)

Dissipation factor (tan δ) (120 Hz) low frequency losses.

ESR —Equivalent Series Resistance (100 kHz) —high frequency losses.

DCL — Direct Current Leakage due to resistive losses through the dielectric.

If any of the above go out of specification (parametric failure), the circuit may still operate, albeit with degraded performance.

Consider what occurs when the degree of parametric shift is increased:

Capacitance shift	larger capacitance shift	
Dissipation factor	large low frequency resistance	open circuit (O.C.)
ESR	large high frequency resistance	open circuit (O.C.)
DCL	increasing leakage current short circuit (S/C)	

Thus two catastrophic failure modes can be generated (O/C and S/C).

Next, consider the relative occurrence of the above failures, taken from one manufacturer's typical life test data, shown in Table 1. (Note that the emergence of a global standard for sizes together with a preferred method of construction [see Figure 1] allows the results given to be considered representative of this technology.)

Table 1

% Fail Per 1000 Hrs.
(7.3m Hrs. Life, Molded Tantalum Chip)

Catastrophic S/C	= 0.015		
		Total	= 0.015
Catastrophic O/C	= 0		
Parametric Cap	= 0.006		
Parametric DF	= 0.016		
		Total	= 0.052
Parametric DCL	= 0.030		
Parametric Impedance	= 0		
		Grand Total	= 0.067

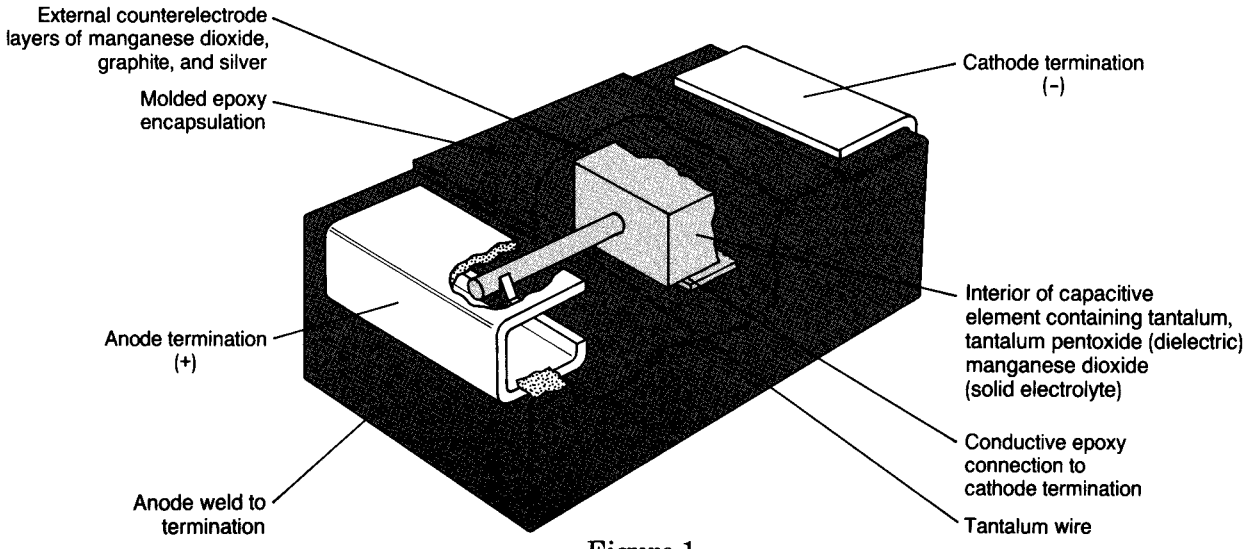


Figure 1.

This table gives the results (expressed in % fail per 1000 hrs.) for 7.3 million component hours of test, across all voltage ranges, at rated volts at 85°C or 2/3 rated volts at 125°C normalized to 3 ohms per volt series resistance.

Three main conclusions can be drawn from these results:

1) Tantalum capacitors can achieve high reliability; in steady state applications standard "level M" parts are capable of exceeding this level by nearly two orders of magnitude with respect to catastrophic failures.

2) Tantalum capacitors have highly stable capacitance and frequency dependent characteristics; in the final limit, the chances of generating an O/C failure is small.

3) Short circuits are a low level, but not negligible, failure mode. S/C failures may be seen to develop from earlier parametric DCL failures. (Note that these initial parametric failures will arise from random points in any given leakage distribution.)

Because of this, reliability management of tantalum chips means the effective control of the S/C failure mode, not least because this mode cannot be designed around by use of redundancy circuits, etc.

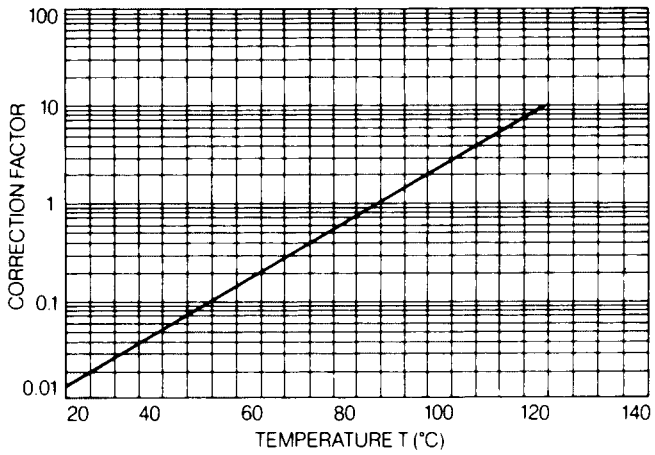
Factors Affecting The Reliability of Tantalum Chips During Operation

Operational reliability is controlled by three variables, whose acceleration factors are well understood:

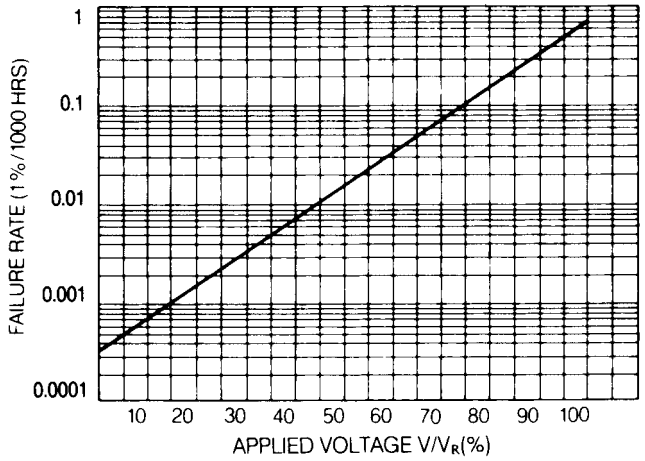
a) Series Resistance
b) Operating Temperature
c) Ratio of Operating Voltage to Rated Voltage (voltage derating)

The acceleration factors for these are shown in Graphs 2a, 2b and 2c.

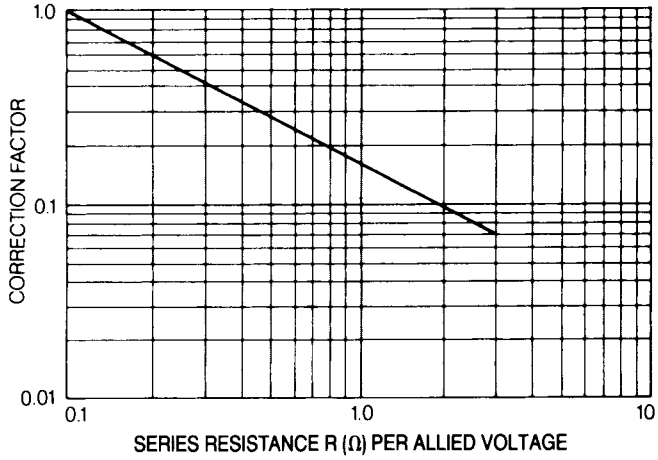
It's worth discussing Series Resistance first (Graph 2a), as it is the most often overlooked. The reason for including a separate resistance into the circuit is to act as protection against voltage spikes and limit current surges to the capacitor. Additionally, in high ripple applications, it acts as an external heat sink and limits thermal stress to the dielectric by sharing the load. In practice, its inclusion may degrade the circuit performance in certain applications, e.g., in power supply o/p filtering. Also, as boards become more densely packed and intercomponent tracks lengths reduced, the capacitors are given greater visibility of any surges or spikes.



Graph 2a: Correction factor to failure rate "F" for series resistance "R" on basic failure rate "F" for typical component.



Graph 2b: Correction factor to failure rate "F" for ambient temperature "T" for typical component.



Graph 2c: Effect of applied voltage on basic failure rate for typical component (60% con. level).

Under these conditions, the self-healing properties of the solid electrolyte cannot be counted on to take effect. (Self-Healing: if a random defect site is generated within the dielectric and forward conduction occurs, local over-heating takes place. With current limiting, the solid

electrolyte surrounding the defect site can decompose to a nonconducting form and isolate the spot, and DCL levels will return to normal. With no current limiting, the dielectric breaks down faster than self healing can take place, and the part will become a catastrophic short.) It should be noted that many applications are "off the graph" i.e., below 0.1 ohms per volt Series Resistance.

Graph 2b shows the temperature dependence of reliability. In high ripple or surge applications, any rise above ambient by the capacitor must be taken into account. It is possible in forced air (or even water cooled) assemblies to achieve better than free-air ratings for power dissipation, but in general such thermal management is costly. If ambient cannot be reduced and the application does generate high ripple, then the thermal rise can be limited by using a lower ESR part. This is not in conflict with Graph 2a, which defines external resistance for surge limiting. For any surge which gets through to the capacitor, a lower internal ESR will dissipate less energy inside the device and produce less thermal shock to localized points in the dielectric.

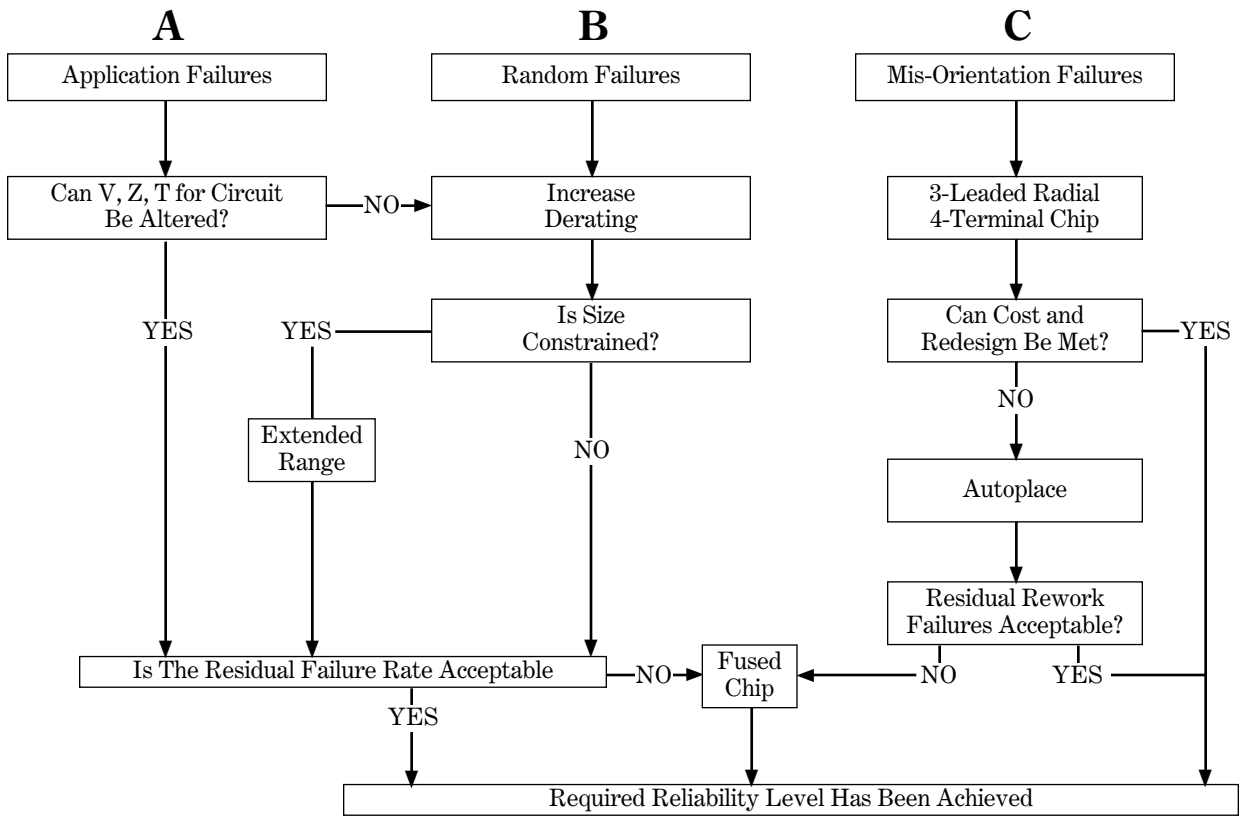
Graph 2c shows the effect of derating on reliability. In general, a 30% derating will produce a tenfold increase in reliability, as ultimately the activation energy required to induce breakdown is a function of the thickness of the dielectric itself.

Until recently, there has been little flexibility possible in component choice to address the above points: Most applications require that densely packaged boards are placed in final assemblies which give little scope for thermal management; no loss in circuit performance due to additional series resistance can be allowed; and once layouts are fixed it is difficult to use a larger case size part with a higher voltage rating.

And yet, as more circuit designs are going to SMT, so the stability of tantalum is being demanded in increasingly aggressive electrical/environmental applications across all industry sectors.

Table 2

Reliability Management for Tantalum Capacitors
Catastrophic S/C Failures



NOTE 1: Fused Chip addresses A, B, C above. Extended Range addresses A, B above. Reversible parts address C only.

NOTE 2: Extended Range *reduces* overall S/C failure rate. Fused Chip *changes existing* S/C failure mode to O/C.

This has lead to the generation of new tantalum products designed to address some or all of the above conditions.

Recent Product Developments Enabling Reliability Control

To counter these problems, three developments in tantalum capacitor design have taken place:

1) The introduction of irreversible tantalum components.

2) Increasing the CV (capacitance/voltage) availability in existing standard sizes.

3) The incorporation of a fuse element into the internal construction converts any S/C failures to O/C.

To put these developments in perspective, consider the "Reliability Control Flow Chart" shown in Table 2.

Three categories of S/C failures are defined:

A) Failures due to misapplication; where voltage, temperature or circuit resistance recommendations are grossly exceeded (or where parts are operated in reverse bias).

B) Residual failure rate due to random mortality.

C) Failures due to wrong insertion giving incorrect polarity in operation.

Categories A and B are related; in standard decoupling applications the residual random failure rate will in general be so low as to be immeasurable. However, as the application becomes more aggressive, the random failure "noise level" will increase in accordance with the acceleration factors given in Graphs 2a, 2b and 2c and failures will become increasingly application driven.

Categories A and B in general are the main source of S/C failures; for auto place operation misorientation (C) will be immeasurably low.

It can be seen that irreversible designs only impact Category C failures and so will be of limited use in auto place operations.

For Category A failures, the option of circuit redesign exists. If this is not practical then the control requirements become identical to those for Category B failures. The key to controlling this category lies in derating (as shown in Graph 2c), and extended range parts enable this without an increase in either case size or footprint.

If the residual failure rate is still unacceptable, then a fused device can be used. In general, the incorporation of an internal fuse will take up space which could alternatively have been used for an extended CV rating. This means that the failure rate itself will not be reduced; rather the S/C mode will be converted to an O/C mode.

Irreversible, Extended CV and Fused Tantalum Capacitors

Irreversible Capacitors

Originally designed to allow safe manual insertion, the construction of the 3-legged radial leaded device is not very different conceptually to that of the standard 2-legged device. Even in automated systems there is still an advantage in using this device if misorientation during rework remains a problem.

However, to manufacture an irreversible SMD is costly in terms of the leadframe design and extensive additional assembly stages.

It should be emphasized that irreversible designs are not equivalent to non-polar designs they merely ensure that the parts are assembled to the PCB in the correct orientation. Any reverse bias application will give reduced reliability. In such cases, two capacitors should be used in series mounted positive-to-positive or negative-to-negative to allow non-polar operation.

Extended Range Capacitors

Two areas of technology have come together to allow the introduction of range extensions in tantalum chips. First of all, the use of higher charge powders (increased CV per gram) has allowed increased ratings for any given pellet size. Secondly, the use of statistical process techniques, taking more effect as production volumes increase, have improved both internal alignment and weld length tolerances so that larger internal elements can be used without compromising minimum molding wall thicknesses.

Table 3a shows the original EIA molded chip ratings and the extended values now available.

As the EIA standard sizes are, to a large extent, governed by the 8mm and 12mm tape dimensions in which they are supplied, the thrust of extended range development is to further increase the CV available while maintaining constant package size.

There is one exception to this, namely the introduction of an E-case design. The current D case has a length limited by the maximum pocket size available on 12mm carrier tape, so there is room for maneuver on H and W dimensions. At one stage, an EIA-J manufacturer did propose an E Case part based on increasing both of these dimensions. However, an EIA-J usage is predominantly A and B Case, this proposal has not been taken up.

EIA usage, on the other hand, is predominantly C and D Case, with an increasing number of power supply applications requiring higher ratings without consuming more real estate.

For this reason, the latest proposal to EIA is for an E Case part with the same footprint (L and W dimensions and termination configuration) as the existing D Case, but having a higher profile to accommodate a larger tantalum pellet.

The advantages of this configuration, apart from the extended ratings available, are the lower intrinsic ESR giving greater power handling and enhanced ripple performance with no significant increase in inductance over the D case. The actual dimensions, ratings and mounting recommendations are shown in Tables 3b and 3c. (Note that the E case will be accommodated by existing D case layouts on IR or VPR (Vapor Phase Reflow) soldering; for wave solder, the pad set length may need extending to allow for shadowing, depending on what direction the part is sent through the wave.)

Table 3a

Capacitance Range (letter denotes case code)								
Capacitance	Rated voltage d.c.							
µF	4V	6.3V	10V	16V	20V	25V	35V	50V
0.1							A	A
0.15							A	a
0.22							A	B
0.33							A	B
0.47						A	b	b
0.68					A	a	B	C
1.0				A	a		B	C
1.5			A	a		B	b	
2.2		A	a	B	B	b	C	D
3.3	A	a		B	b	C	C/D	D
4.7	a		B	C	C	C/D	c	d
6.8		B	b	C	C/D	c	D	
10	B	b	C	C/D	c	D	D	
15	b	C	C/D	c	D	D	d	
22	C	C/D	c	D	D	d		
33	C	c	D	D	d			
47	c	D	D	d				
68	D	D	d					
100	D	d						
150	d							
Standard Range Values: Upper Case Extended Range Values: Lower Case								

Table 3b

Case Dimensions (millimeters)

Code	L	W	H	W1	A	S
	±0.2	+0.2 -0.1	+0.2 -0.1	±0.1	+0.3 -0.2	Min.
D	7.3	4.3	2.9	2.4	1.3	4.4
E	7.3	4.3	4.1	2.4	1.3	4.4

Table 3c

Capacitance Range (letter denotes case code)								
Capacitance	Rated voltage d.c.							
mF	4V	6.3V	10V	16V	20V	25V	35V	50V
3.3								D
4.7							D	D
6.8						D	D	
10						D	D	E
15					D	D	D	
22				D	D	D	E	
33			D	D	D	E		
47	D	D	D	D	E			
68	D	D	D	E				
100	D	D	E					
150	D	E						
220	E	E						

Fused Chip Capacitors

These devices operate by sensing when the capacitor is in the process of failing and then switching the short circuit mode to open circuit.

There are two methods of achieving this which can be simplified as:

1) THERMAL FUSING: When the part goes into short circuit mode the current developed through the failure site (if unlimited) will cause large-scale overheating. A thermal fuse link will sense the rise in temperature and melt (or vaporize) deactivating the device.

2) ELECTRICAL FUSING: An electrical fuse senses the increase in DCL as the part goes to the threshold of S/C. The fuse element reacts fast enough to deactivate the device before major overheating occurs.

Before the merits of either type are discussed, let's look at a "want-list" of requirements for a fuse device:

MUST	MUST NOT
1) Activate before overheating occurs.	Activate during extended IR or wave soldering or rework.
2) Activate as soon as excessive current is drawn.	Activate as a result of low impedance surges during switch-on, power cycling, or high ripple applications.
3) Activate with low current densities over extended periods.	Activate with thermal cycling only.
4) Blow "very open", i.e., 10M resistance.	Increase internal resistance slowly, giving rise to further heat dissipation.
5) Blow permanently.	Be allowed to reform.

6) Have fusing characteristics that can be defined and tested independently, and can also be made applications specific.	Have characteristic affected by the final assembly package.
7) Allow optimum parametric performance.	Increase intrinsic ESR or inductance (i.e., adversely impact high frequency performance).

A typical electrical fuse will perform better for items 1, 2, 4, 5, 6 and 7, whereas thermal fuse characteristics best address item 3.

Early fuse chip designs employed thermal, or pyro, fuses which were, in effect, short solder wire links at the cathode or anode end. These would sense the thermal runaway of a short-circuiting device and melt, breaking the circuit connection.

While these operated satisfactorily in most cases, there were some associated disadvantages:

a) The circuit could reform on cooling. The conducting metal was melted, not vaporized and there was no place for the fuse debris to escape, potentially allowing the circuit to reform on resolidification.

b) The fusing characteristics would be affected by the amount of surrounding encapsulate acting as a heat-sink and delaying activation. This would be more predominant in larger case sizes (see Graph 4a). In addition, tracking due to carbonization was possible.

c) ESR and inductance would be greater than for equivalent non-fused parts.

d) The activation would take place after the part had become a short circuit and starting passing current, which would still allow damage to other components even if local burning was prevented.

e) Fusing could be activated by excessive temperature excursions.

Refinements have been made to these designs to address some of the above points. Fuse alloys have been designed which will partially vaporize at higher currents which makes for more permanent fusing; coatings on the fuse links will help prevent carbonization of the surrounding molding epoxy. These developments make the link act more as an electrical fuse.

One fuse design having the advantage of both thermal and electrical characteristics is available, being based on a binary metal system.

The fuse element is incorporated onto a leadframe (specifically configured for this application) by hybrid techniques immediately prior to final assembly as an additional automated process step.

The advantages of this type of element are:

1) using is permanent and irreversible.

2) using characteristics are less sensitive to the final assembly.

3) using characteristics can be moved (i.e., application specific for fast-blow or slow-blow).

4) the fuse elements can be incorporated into existing EIA case sizes (specifically D-case) allowing retrofitting of existing designs.

It should be noted that the short circuit failure mode may be generated in several ways. The more common ways is when the part is subjected to a high, unlimited current/voltage surge which will cause a random spot on the dielectric to break down under intense local heating. This is the prime failure mode that the fused chip is designed to address.

At the other end of the spectrum, however, it is possible to generate failures in parts operated at low voltage levels, but which are subjected to continual high levels of ripple voltage (maybe even including reverse bias). In these parts, a multiplicity of voltage breakdown sites may gradually occur which will pass steady, but large amounts of current and cause significant heating above ambient. In these cases, the fuse window needs to be set for low current densities.

Many applications for fused chips (and also extended range) will involve power supply filtering where there is high current availability with minimal external series resistance.

In these cases, care must be taken when designing in fused parts if there are any other components in parallel; the open circuit failure mode will effectively shunt A.C. current across these parts which may become secondary failures.

Conclusion

In conclusion, it should be noted that all the above product developments give design engineers the flexibility they need in addressing application specific problems for a given base reliability level.

However, tantalum technology is not standing still; high-purity powders are being developed which will give greater dielectric stability, and preconditioning techniques are constantly being refined so that an increasing number potential infant mortalities can be effectively eliminated at the source.

In fact, one spin-off from the electrical fuse is that failures generated by overstress are “frozen” before they become totally immeasurable.

In this way, failure modes now can be characterized in greater detail, which in turn will lead to ongoing improvements in base reliability.

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