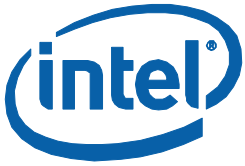

White Paper

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Considerations for Designing an Embedded Intel® Architecture System with System Memory Down

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Executive Summary

What is memory down? How can I use it in my platform? How do I design with it? If these are some of the questions you have when the term "Memory Down" comes up, then this paper may be for you. Since memory down is a solution often considered in the embedded market this paper will look at all the aspects of preparing for and designing a low power or scalable system with memory down instead of using the traditional memory connectors. Each level of a system design will be addressed in this paper.

"Memory down is a solution often considered in the embedded market…"

The levels of a system design that will be covered include:

- Product Planning
- Aspects of Board Design
- SW Considerations

After reading this paper a board designer or product planner will be more aware of what it takes to design memory down into their system and be ready to take on the task of implementing their specific design.

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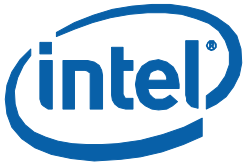


Background

The term "Memory Down" is used to describe when memory components such as DRAM devices are physically soldered onto a Printed Circuit Board (PCB). This is an alternative to using mechanical connectors to attach memory modules onto a system.

Memory down is a solution that is often used in the embedded market due to the variety of constraints and usage models embedded customers require. When using memory down a system can be used in many applications where using a memory module/mechanical connector combination would not work due to height, reliability and mechanical connectivity requirements

This paper will go over all the items that need to be considered when looking into designing a low power or scalable system with memory down instead of using the traditional memory connectors. Each level of a system design will be addressed in this paper including checklists to aid in determining if memory down is the right solution for your application, schematic creation, PCB/layout design, signal integrity and memory DRAM considerations. Examples of each of these design levels are included as a reference. The goal of this paper is to provide an aid for the creation of an Intel® architecture system with memory down and to help alleviate questions and issues that may come up during the design process.

Planning

Before an actual system is built there are several considerations that need to be looked at in determining if system memory down is right for your design.

Is Memory Down Right For My System?

When determining if memory down is the right application for your system the following checklist is meant to help with the decision making process:

Systems which would benefit from System Memory Down

- The system is subject to ongoing shock and vibe and the reliability of component contact is crucial.
    - Since the DRAM components are directly soldered on the PCB, they can withstand greater amounts of shock and vibe compared to connectors.

- The height of component requirements on my system is very strict.
    - With the minimal height and thickness of the DRAM component they enable memory placement where DIMMs and connecters would not physically fit.
- The design does not require changing or upgrading of memory type/capacity.
    - Since the DRAM components are soldered on the PCB, any change would require massive rework so in most cases they are not changed.
- The overall system BOM is under a tight budget.
    - In many cases the cost of the memory components is less than that of memory modules so it may be an area for system designers to reduce overall BOM costs.

Systems which may not benefit from System Memory Down

- The design requires the option to change memory specification with ease.
    - While it is possible to change memory specification with system memory down it usually is an extra expense as well as a risk since rework can possibly also affect other surrounding components on the PCB.
    - System memory down is not meant to be designed in an application where the memory capacity is not predetermined or left for expansion depending on the user needs.
- Board real estate is more restricted than component height.
    - Placing memory down components on a board can require more real estate than mechanical connectors.

Once it is determined whether memory down is right for your system you can move forward with confidence and start looking into more details.

What Type of DRAM Devices Should My System Use?

Once the memory is placed on the board it is not easily changeable. Care needs to be taken in deciding which memory is right for your system.

Memory options:

- Density
- Depth
- Width
- Voltage
- Package
- Clock rate
- CL
- Data Rate
- Physical size

Does Your System Require Error Correction Code (ECC)?

If ECC is implemented on a system extra DRAM devices may be needed. The standard device width used in ECC designs is x8.

If x16 wide devices are the preferred type then they may still be used in ECC designs if supported by the architecture of the memory controller but more factors will need to be considered. With most of the Embedded Intel® architecture processors and chipsets, DRAM devices (which can behave like x8 devices) would mostly likely need to be used when trying to use x16 devices with ECC. Also, the data signals not used on the DRAM ECC component may need to be pulled high.

Physical Considerations

Let us look at a couple of the DRAM memory options that have to deal with physical design.

Package type: there are several types of packages that may be available.

- LQFP (Low Profile Quad Flat Package)
- TQFP (Thin Quad Flat Package),
- TSOP (Thin Small Outline Package) ,
- FBGA (Fine Ball Grid Array),

- LGA (Land Grid Array),
- WBGA (Window Ball Grid Array)

With all these options it basically boils down to either choosing a pin grid array (PGA) or ball grid array (BGA) design. For an embedded design the most popular choice is BGA. This is due to how it enables designs with multiple layers to ease the necessary routing, instead of having to route first from pins on one layer then fan out to the rest of the board.

Physical Size: DRAM devices range in size with the most common size being around ~9x12 mm.

This paper will focus on newer platforms that make use of DDR2 and DDR3 for system memory. DDR2 and DDR3 are specified for BGA only, with DDR3 also making use of the TSOP package type.

Figure 1. Sample Picture of DRAM Devices

Board Design

When designing the PCB, there are a few points that need to be considered for utilizing a memory down implementation. Let us walk through each step of the board design focusing on schematics and layout.

Schematics

Since we are not using a memory module for our memory implementation there are several things we have to account for. Instead of connecting signals from the memory controller to a connector we need to ensure all lines are connected to each DRAM component.

Figure 2 and Figure 3 are examples are for DDR3 DRAM components.

Figure 2. Schematics Design

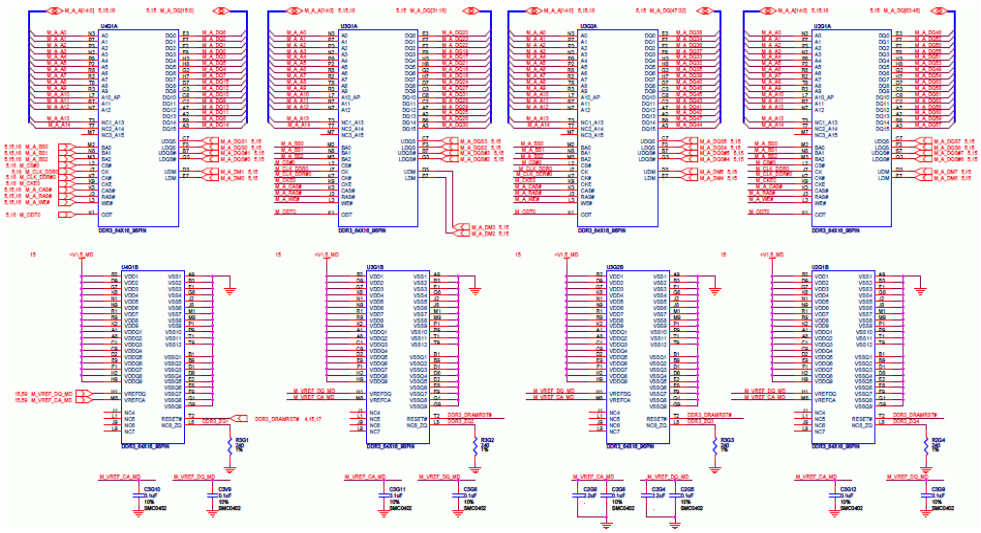
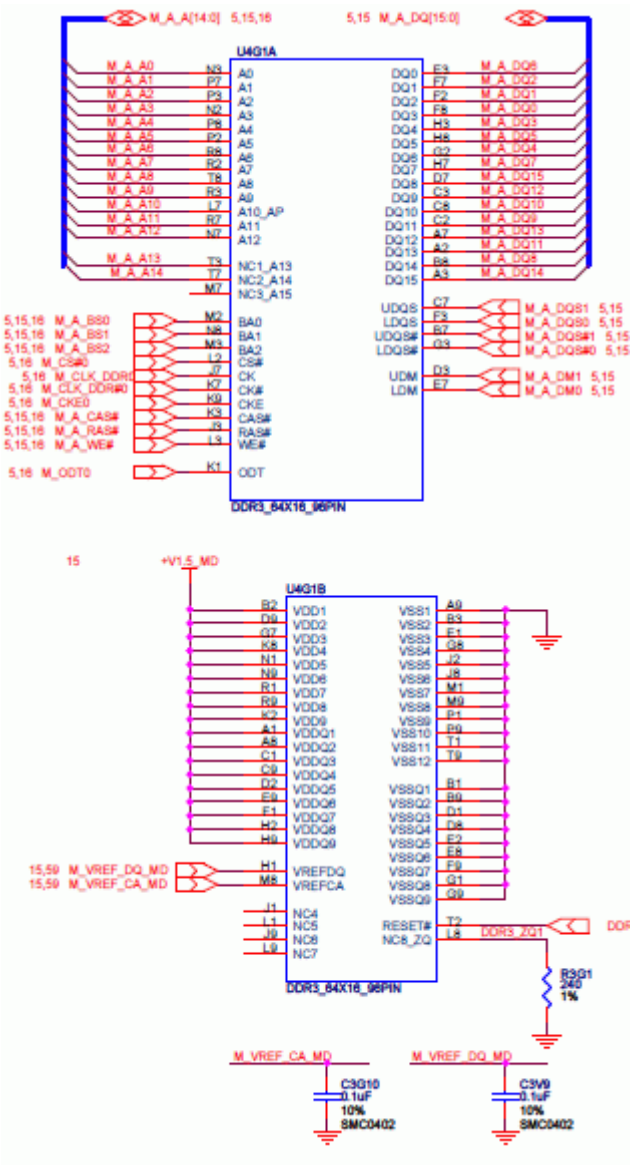


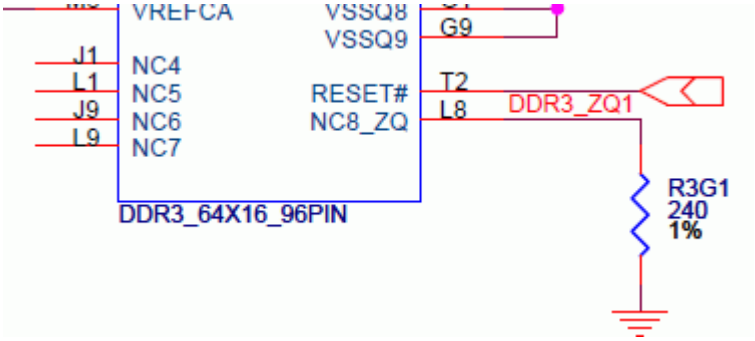
Figure 3. Zoom View



ZQ

ZQ is an external reference ball/pin meant for output drive calibration. This is usually tied to an external 240Ω resistor, which is tied to ground. The processor does not support ZQ calibration with ZQ resistor shared between two SDRAM devices. Hence for Memory Down topology implementation, Intel recommends to use a separate ZQ resistor for each SDRAM device. This resistor should be 240 Ω (±1%) and connected between ZQ signal and GND. For other details on ZQ signal refer to DDR3 JEDEC Specification (refer Section 1.2).

Figure 4. ZQ



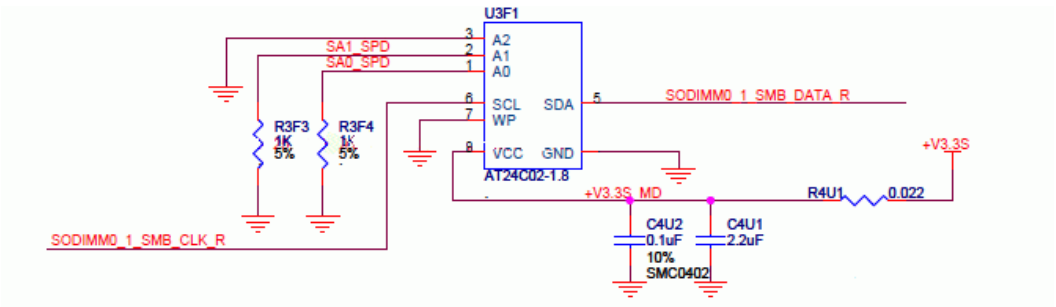
ECC

If ECC is required on the system and the memory controller is ECC-capable, an extra DRAM component will be needed per memory channel. The 8 bits of ECC data would be connected to the DQ signals of this extra DRAM component. The coordinating data strobes (DQS and DQS#) would also be connected to the extra DRAM component. Another consideration is the additional data mask (DM) that is associated with ECC that may need to be connected depending on your design

SPD

A programmed SPD component may also need to be placed on the system for information on memory configuration if it is not integrated into the BIOS.

Figure 5. SPD



Layout

While there are many ways and fashions to route out your memory implementations, the following sections are in place as an example to reference.

Length Considerations and Routing Strategy

When looking at clock length matching requirements special attention is needed while routing memory down topologies. The recommended approach is to test route the data and strobe signals first and find out the longest byte lane. The second step is to define the clock target length, as short as possible, while ensuring that clock-to-strobe length matching formula is met. This will provide the least amount of serpentine requirement for the entire data bus. Command and control signals can more or less follow clock routing. Again, it is important to have similar segment lengths in DRAM loaded sections among clock, control and command signals to achieve optimal timing margin. Each of these segments can be validated with the help of a Trace Length Calculator that is usually available for each platform.

Intel recommends that the entire memory channel be routed completely on one internal layer with all routing implemented as stripline, except as required to make surface layer component connections. This scheme ensures data and data strobes are routed on the same layer, minimizing skew associated with layer-to-layer PCB variances, and also provides for a uniform distribution of routing density across the two primary routing layers. In the case of single-channel designs which require the use of multiple internal layers, no preference is given as to how the overall signal set is partitioned between internal routing layers, except to recommend that individual byte lanes be routed as a group on the same layer.

Utilizing Raw Card Standards

When developing your design topologies a common practice is to base them on the available raw card standards. Two examples would be DIMM and SODIMM raw card standards. It is beneficial to use the raw card standard as they are a proven topology used in the layout of memory modules. Using the raw card standards could also ease the modification of MRC since they may have already been taken account for in the MRC available for the platform you are designing.

DDR3 Design Topologies

Since DDR3 is a popular type of memory used in the latest generation for embedded platforms, this section contains information and details on the DDR3 topologies based on the DIMM raw card standards. A topology example is provided for each corresponding signal group. While these may change for each type of platform it gives the general idea on what needs to be considered for memory down designs.

Throughout these examples:

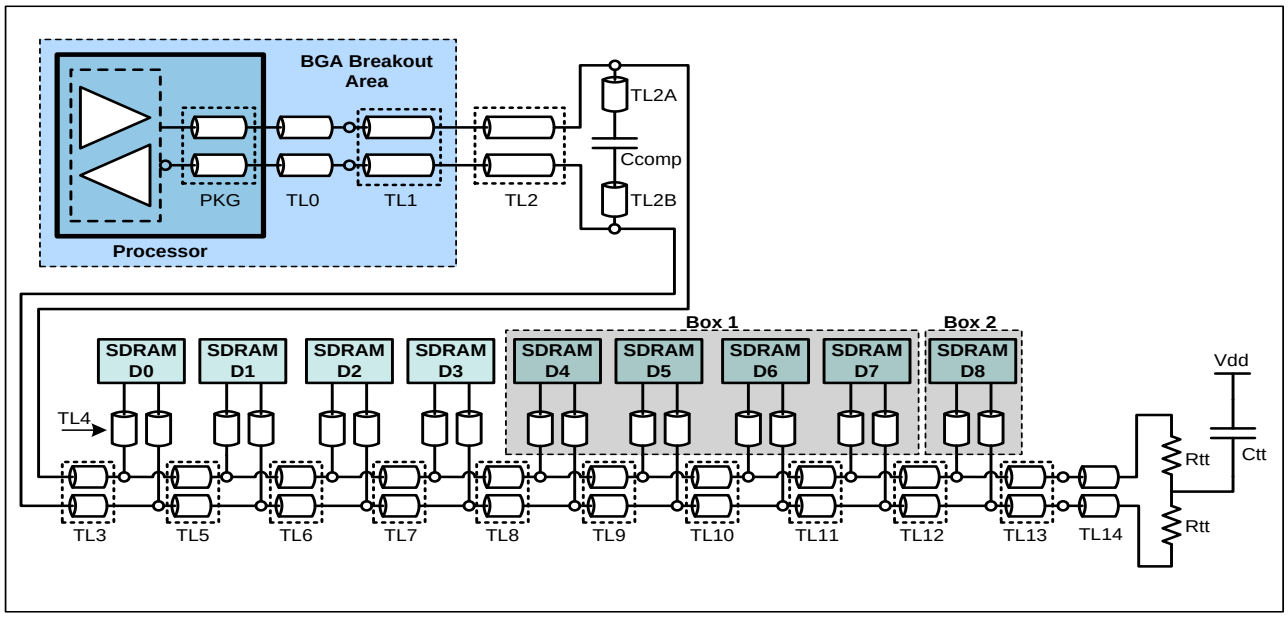
- Processor/Memory Controller are on the same BGA package

- TLx (ie TL1, TL5)= A given trace length
- Vdd=Supply Voltage
- Vtt=Reference Voltage
- Ctt=Termination Capacitance
- Rtt=Termination Resistance

DDR3 Clock Signals

Figure 6 and Table 1 below depict the recommended topology for the DDR3 differential clocks signals.

Figure 6. Clock Signal Topology



For different memory down configurations, certain dashed box(es), their corresponding stubs, and TLx may need to be removed from the above topology diagram. Table 1 shows the details of topology for each memory down configuration.

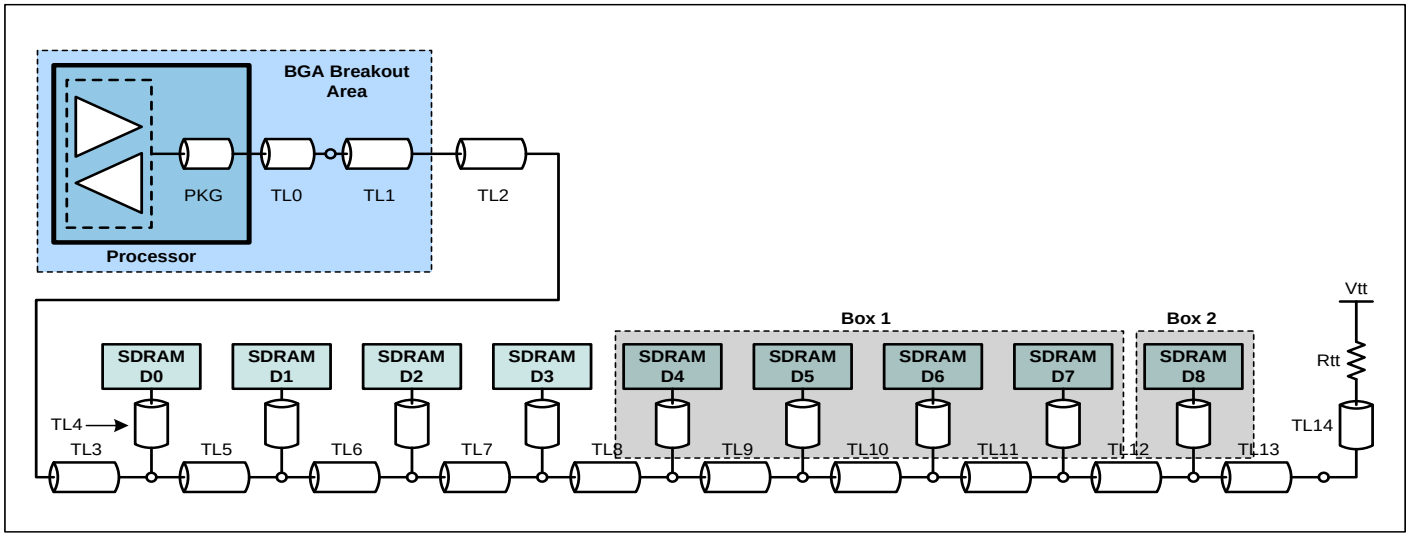
Table 1. Clock Signal Topology for Different Memory Down Configurations

Config Index	Memory Down Configurations				Dashed Box (SDRAM and stub) needs to be removed from the topology diagram above
	# of Ranks	SDRAM Organization	# of SDRAM Devices	Non-ECC or ECC	
1	1 Rank	x8	8	Non-ECC	Box 2 and TL12
2	1 Rank	x8	9	ECC	None
3	1 Rank	x16	4	Non-ECC	Box 1, Box 2 and TL8~TL12
4	2 Ranks	x16	8	Non-ECC	Box 1, Box 2 and TL8~TL12
5	2 Ranks	x8	16	Non-ECC	Box 2 and TL12
6	2 Ranks	x8	18	ECC	None

DDR3 Control Group signals

Figure 7 and Table 2 below depict the recommended topology for the control signals.

Figure 7. Control Group Signal Topology Diagram



For different memory down configurations, certain dashed box(es) and their corresponding stubs and TLx may need to be removed from the above topology diagram. The following table shows the details of topology for each memory down configuration. If layer transition is needed for main route, it could be broken into TL2 and TL3 segments with a via in between.

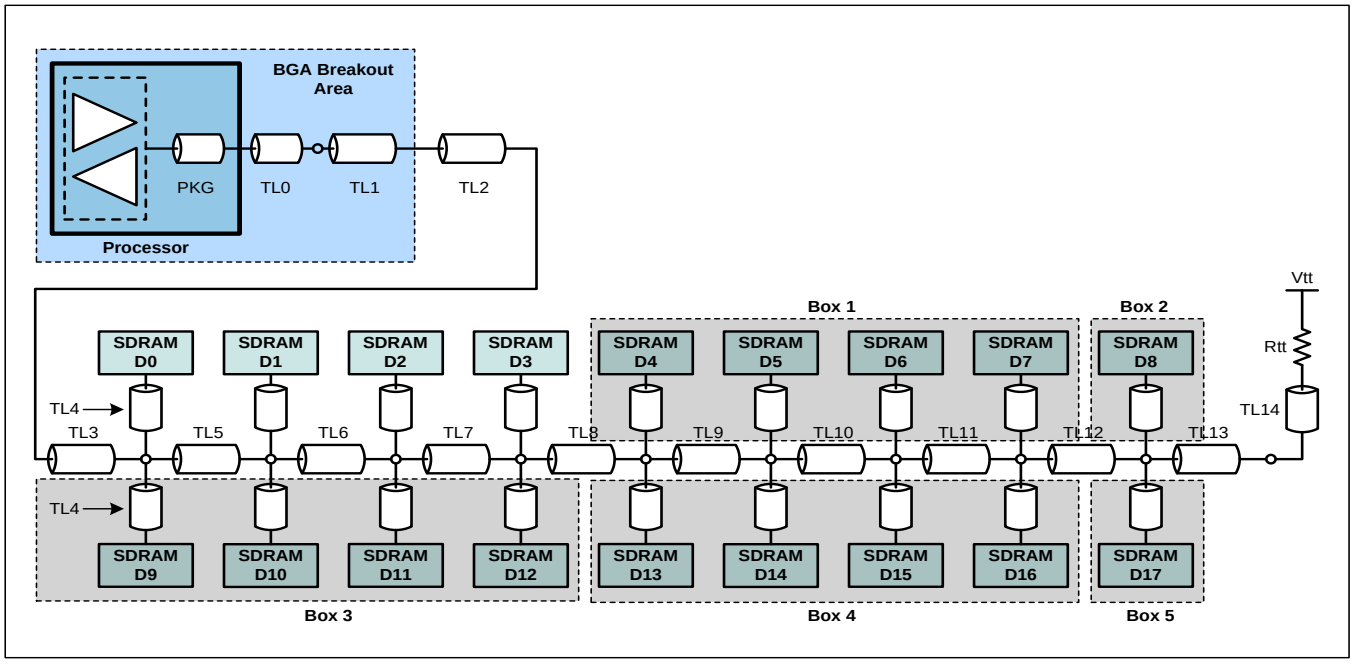
Table 2. Control Group Signal Topology for Different Memory Down Configurations

Config Index	Memory Down Configurations				Dashed Box (SDRAM and stub) needs to be removed from the topology diagram above
	# of Ranks	SDRAM Organization	# of SDRAM Devices	Non-ECC or ECC	
1	1 Rank	x8	8	Non-ECC	Box 2 and TL12
2	1 Rank	x8	9	ECC	None
3	1 Rank	x16	4	Non-ECC	Box 1, Box 2 and TL8~TL12
4	2 Ranks	x16	8	Non-ECC	Box 1, Box 2 and TL8~TL12
5	2 Ranks	x8	16	Non-ECC	Box 2 and TL12
6	2 Ranks	x8	18	ECC	None

DDR3 Address/Command Group Signals

Figure 8 and Table 3 below depict the recommended topology for the address/command signals.

Figure 8. Address/Command Group Topology Diagram



For different memory down configurations, certain dashed box(es) and their corresponding stubs and TLx may need to be removed from the above topology diagram. The following table shows the details of topology for each memory down configuration. If layer transition is needed for main route, it could be broken into TL2 and TL3 segments with a via in between.

Table 3. Address/Command Group Signal Topology for Different Memory Down Configurations

Config Index	Memory Down Configurations				Dashed Box (SDRAM and stub) needs to be removed from the topology diagram above
	# of Ranks	SDRAM Organization	# of SDRAM Devices	Non-ECC or ECC	
1	1 Rank	x8	8	Non-ECC	Box 2, Box 3, Box 4, Box5 and TL12
2	1 Rank	x8	9	ECC	Box 3, Box 4, Box5
3	1 Rank	x16	4	Non-ECC	Box 1, Box 2, Box 3, Box 4, Box5 and TL8~TL12
4	2 Ranks	x16	8	Non-ECC	Box 1, Box 2, Box 4, Box5 and TL8~TL12
5	2 Ranks	x8	16	Non-ECC	Box 2, Box5 and TL12
6	2 Ranks	x8	18	ECC	None

DDR3 Data Signals

Figure 9, Figure 10 and Table 4 below depict the recommended topology for the data group signals.

Figure 9. Data Group DQ Topology

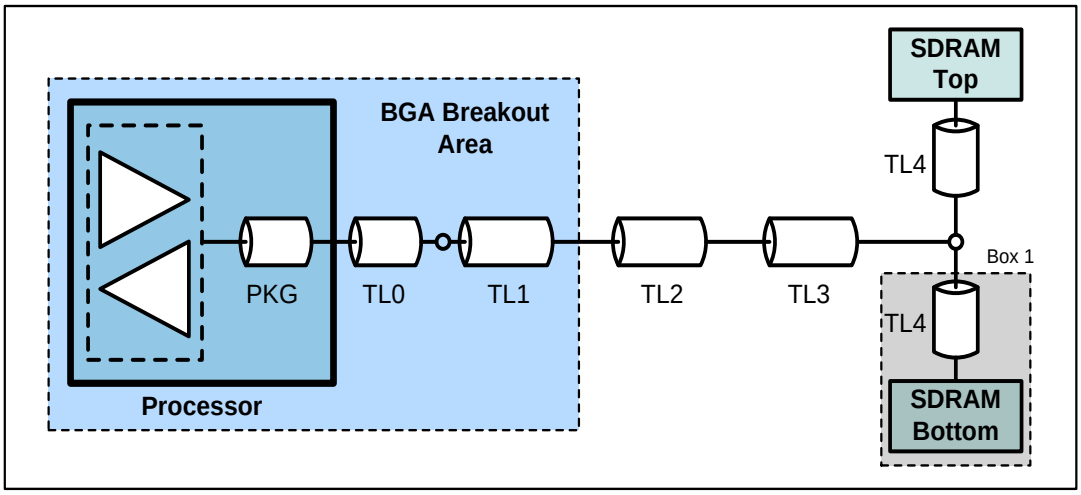
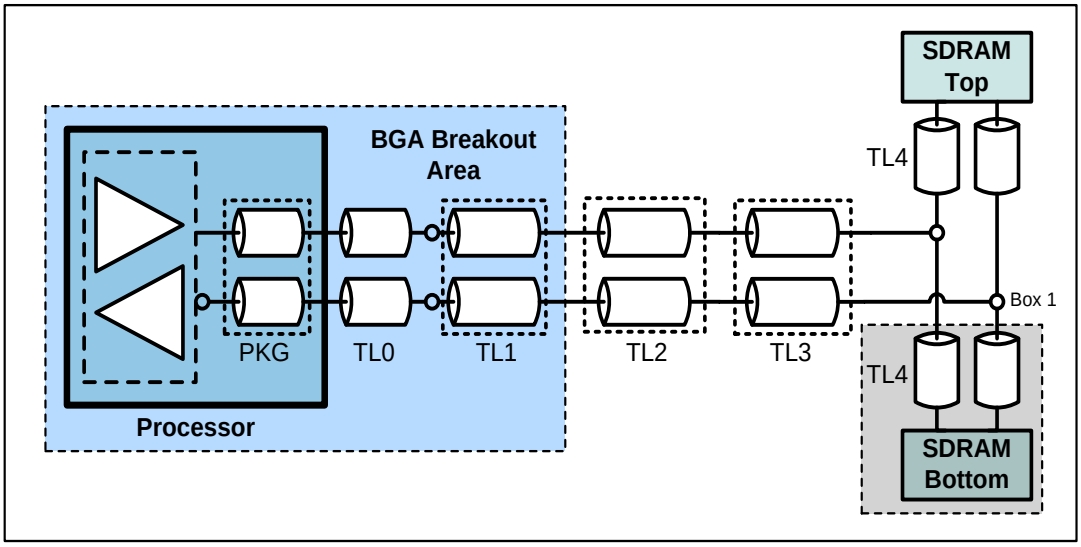


Figure 10. Data Group DQS/DQS# Signal Topology



For different memory down configurations, certain dashed box(es) and their corresponding stubs and TLx may need to be removed from Figure 10. Table 4 shows the details of topology for each memory down configuration.

Table 4. Data Group Signal Topology for Different Memory Down Configurations

Config Index	Memory Down Configurations				Dashed Box (SDRAM and stub) needs to be removed from the topology diagram above
	# of Ranks	SDRAM Organization	# of SDRAM Devices	Non-ECC or ECC	
1	1 Rank	x8	8	Non-ECC	Box 1
2	1 Rank	x8	9	ECC	Box 1
3	1 Rank	x16	4	Non-ECC	Box 1
4	2 Ranks	x16	8	Non-ECC	None
5	2 Ranks	x8	16	Non-ECC	None
6	2 Ranks	x8	18	ECC	None

Layout Examples

The following examples are of a board which has one channel of DDR3 memory down based on a SODIMM raw card standard. As you can see in Figures 11-16, memory components are placed on the top and bottom of the board.

Figure 11. Board example (Top)

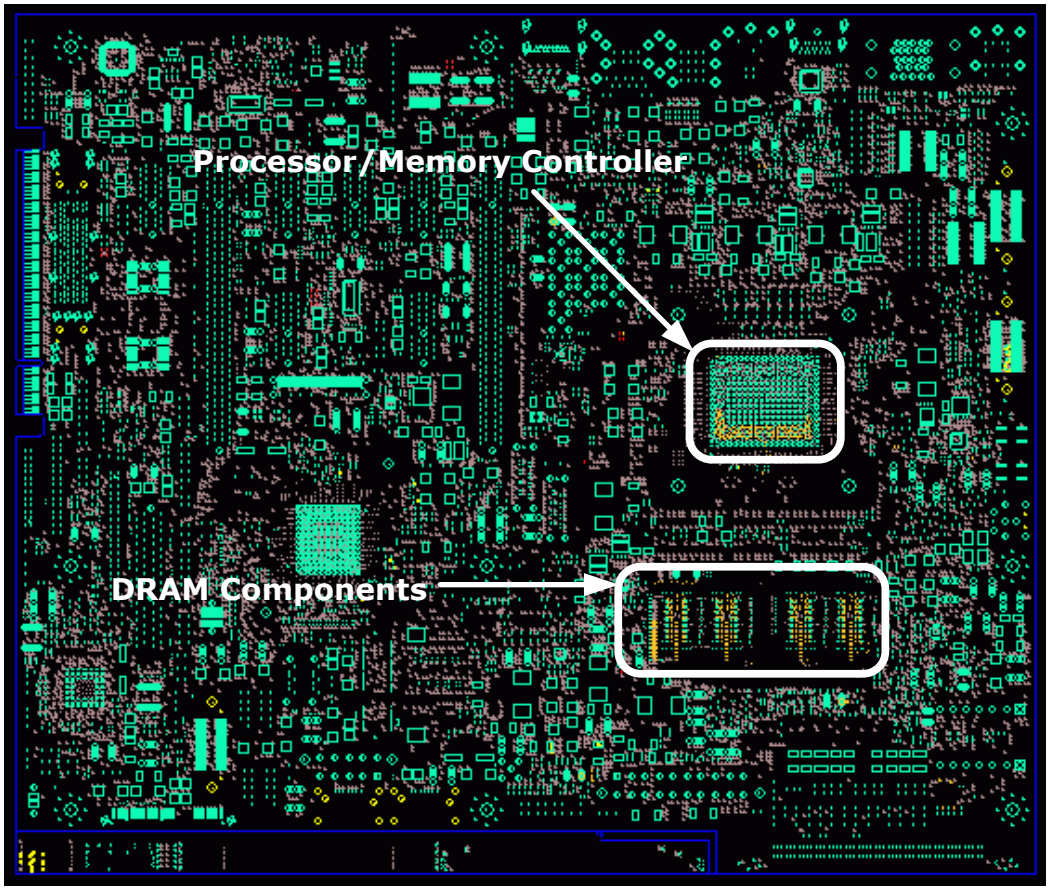


Figure 12. Board example (Bottom)

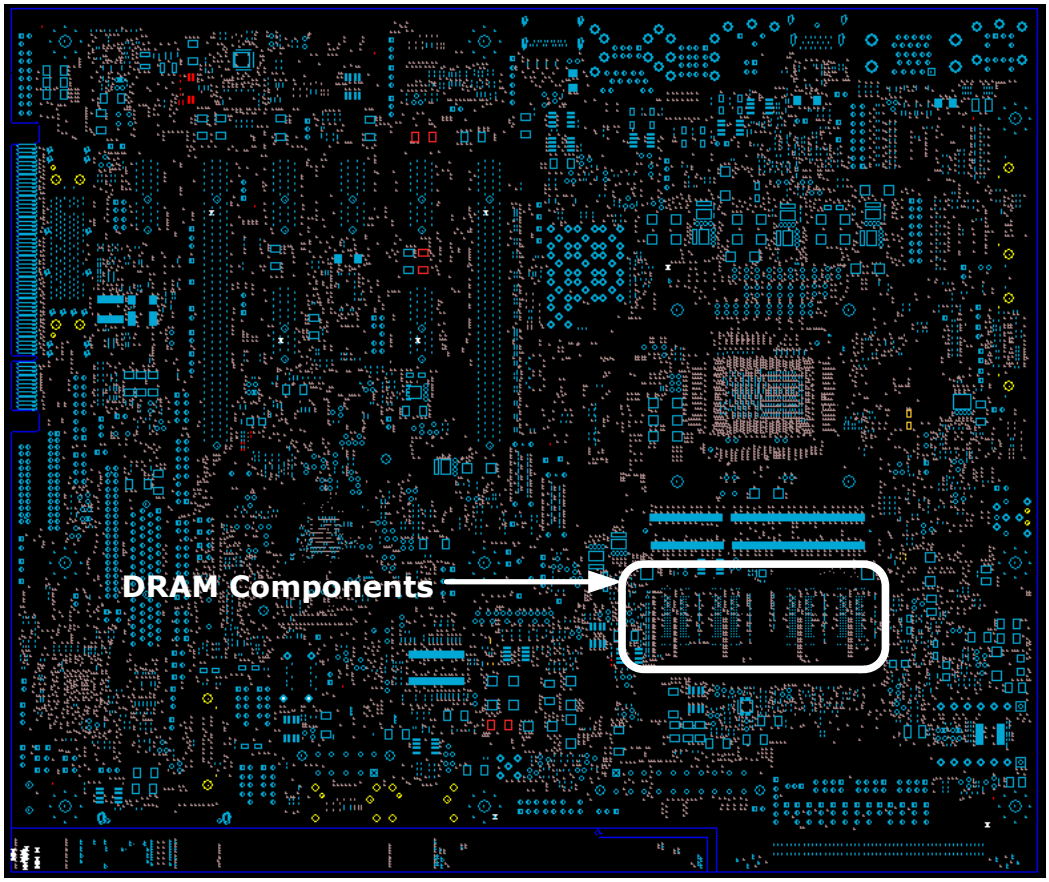


Figure 13. Layer 3 Routing Example

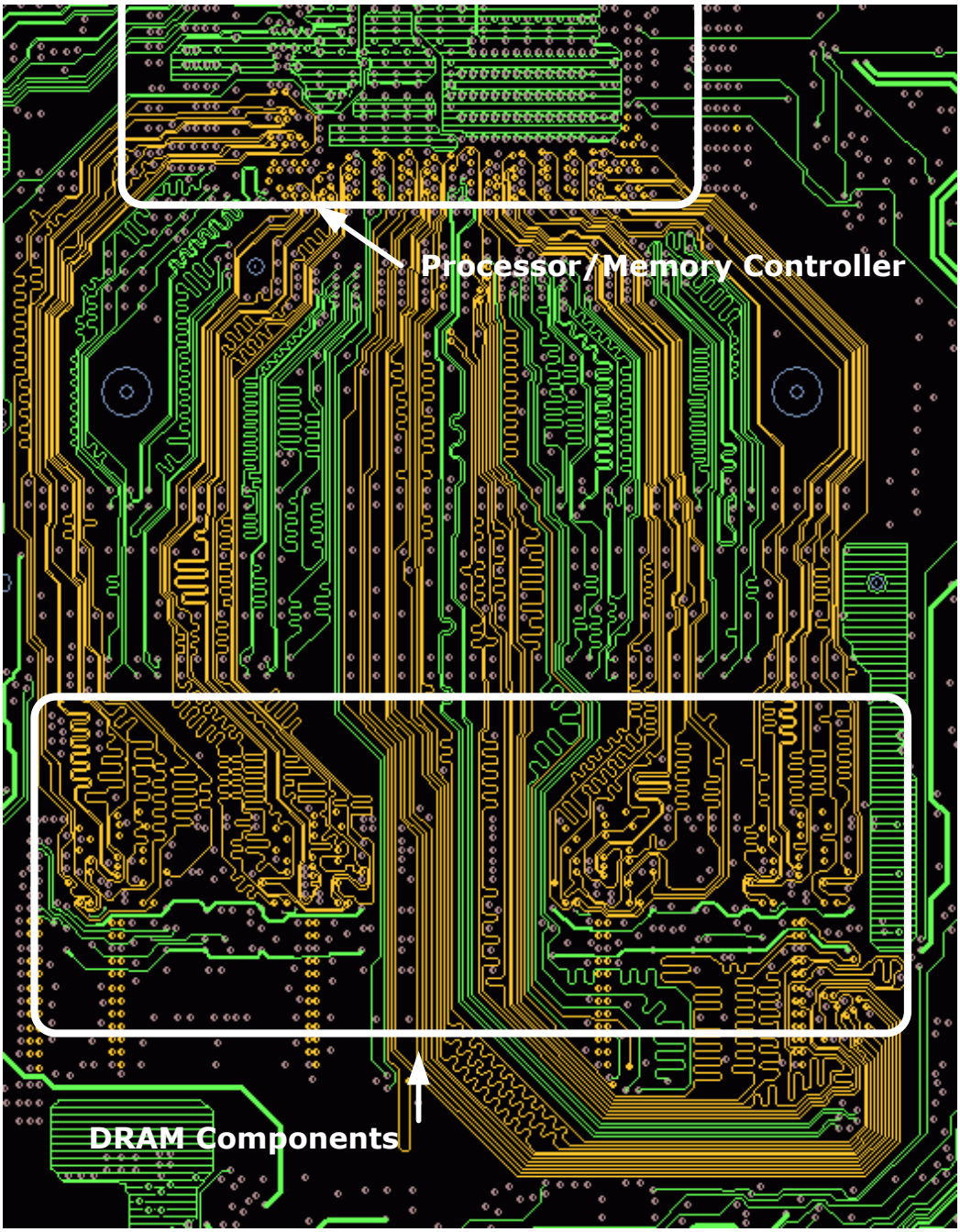


Figure 14. Layer 8 Routing Example

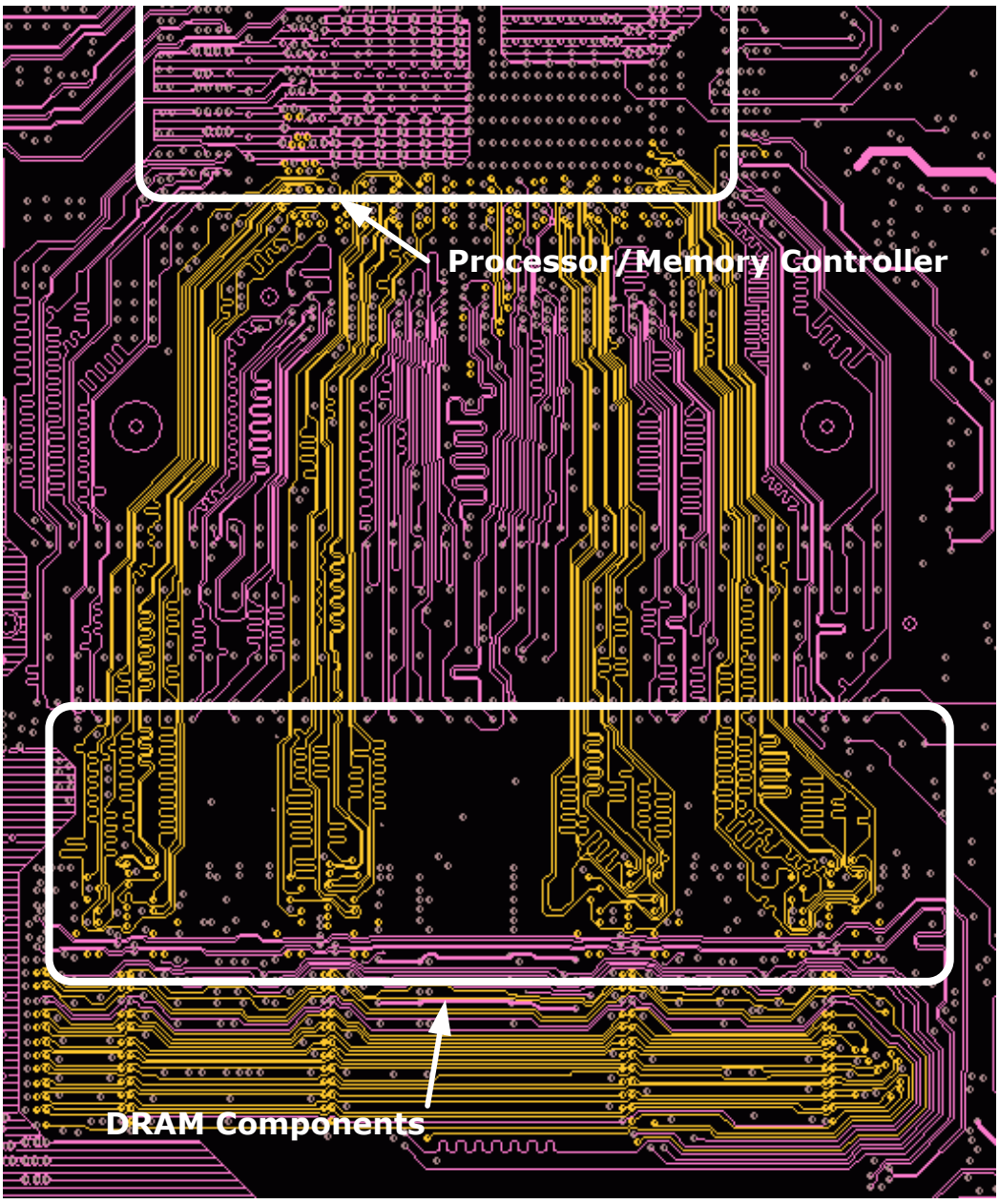


Figure 15. Top/Bottom Layer Routing Example

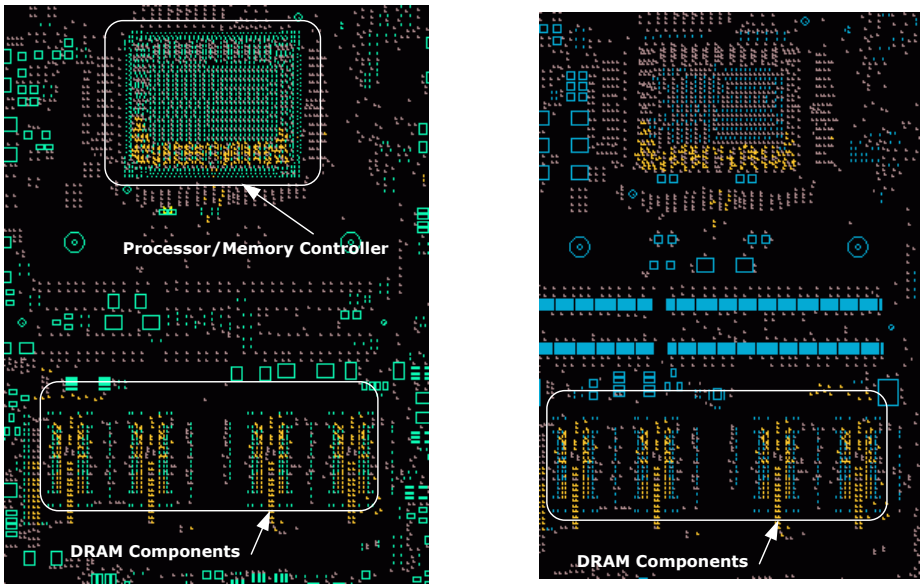
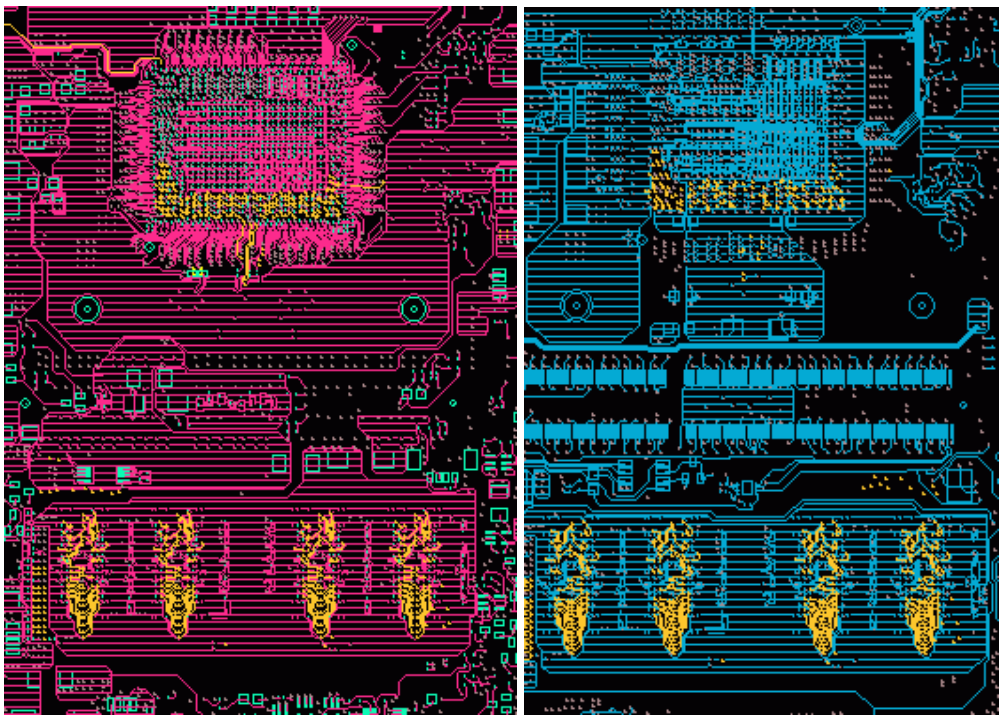


Figure 16. Top/Bottom Layer power routing example



Combining Memory Down With Memory Modules

In the case of implementing one channel for memory down and one channel to a memory module/mechanical connector combination, Intel recommends to connect the first channel (CHA) to memory down, as it is required by the processor architecture in most cases that the first channel has to be populated.

Software Considerations

Memory Reference Code (MRC)

The MRC is responsible for initializing the memory as part of the POST process at power-on. Intel provides support in the MRC for all fully validated memory configurations. For non-validated configurations, a system designer should work with their BIOS vendor to produce a working MRC solution.

Serial Presence Detect (SPD) EEPROM

The MRC in the system BIOS needs to know the specification of the attached system memory. Most of this info should be contained in the onboard SPD. With this in mind care needs to be taken when programming the appropriate values into the SPD. A system designer should work with their memory and BIOS vendors to implement a suitable SPD programming.

Memory Down, Ship It Out!

The goal of this paper was to answer some of the basic questions that come to an engineer's mind when designing an Embedded IA product using system memory down.

For more information on specific memory devices please check with your memory vendor for availability and detailed specs.

The Intel® Embedded Design Center provides qualified developers with web-based access to technical resources. Access Intel Confidential design materials, step-by step guidance, application reference solutions, training, Intel's tool loaner program, and connect with an e-help desk and the embedded community. Design Fast. Design Smart. Get started today. http://intel.com/embedded/edc.

Authors

David Hibler Jr is a Technical Marketing Engineer with ECG at Intel Corporation.

Acronyms

BGA	Ball Grid Array
DDR3	Dynamic Random Access Memory
ECC	Error Correction Code
MRC	Memory Reference Code
PCB	Printed Circuit Board
SDRAM	Synchronous DRAM
SPD	Serial Presence Detect