cal data publicity

california data processors
2019 south ritchey street
santa ana, california 92705
telephone: (714) 558-8211

CONTACT: Ray Ball, President FOR IMMEDIATE RELEASE

NEW COMPUTER FAMILY OFFERS TO SOLVE
OEM'S SINGLE SOURCE DEPENDENCY

SANTA ANA, CALIFORNIA -- California Data Processors (Cal Data) has introduced a microprogrammable family of minicomputers which can give the OEM volume computer user a fully compatible replacement for the sole source computer on which his system, division or business now depends. According to President Ray Ball, in most cases the Cal Data alternative will outperform the computer it replaces while maintaining full software and hardware interfacing compatibility. He said, "We can efficiently and economically emulate many of the mini- or midi-computers currently in high volume production, usually at a lower unit price than the OEM user is now paying. For really the first time in the industry the OEM computer user can second source and control his source of supply for computers on which his systems are critically dependent."

Initial models in the new computer series are the CDP-XI/35 and CDP-XI/I computers based on the CDP-XI/00 microprocessor.

The CDP-XI/00 is a complete microprogrammable computer system for OEM users who wish or need to develop custom firmware for specific applications or system enhancements. Users will be fully supported with hardware and software aids for firmware development later this year. The -XI/00 is the basic vehicle on which an effective family of other

-more-

target machine emulations or optimizations are based. Examples are the CDP-XI/35 computer currently being shipped by Cal Data as a full performance match for the PDP-11/35 and the CDP-XI/I computer which emulates the Tempo I but with an I/O discipline able to take full advantage of all DEC-compatible peripherals and controllers.

Processor features include a 48-bit, 165 ns microcommand, parallel execution of multiple functions per command, 16-bit parallel data word, 16-or more multi-purpose file registers, operable in the word, byte, "nibble" or bit mode, and 256 to 4K word microcontrol memory.

Memory and I/O features include 8KX16 bit (675 ns cycle, 275 ns access) and 16KX16 bit (850 ns cycle, 300 ns access) core memories, interleaved data transfers between paired 8K or paired 16K modules, expansion to 128K words of memory within the 10-1/2" x 19" x 22" cabinet with optional memory management unit. The I/O channel is asynchronous, 16-bit parallel, and permits peak DMA transfer rates of up to 6 megabytes/second.

Key features of Cal Data's basic CDP-XI/35 computer include software and I/O compatibility with the PDP--11/05 through -11/40 machines but with improved throughput, greater packaging density, lower bus load and power demand, more capacity for expansion, broad parts interchangeability with the emulated computer system, availability of a broad range of established peripheral controllers, and compatibility with an equally broad array of other manufacturer's peripherals. The availability of special or proprietary application-oriented macro--instructions and functions provide an excellent

vehicle for enhancement of the basic system for immediate and/or future requirements.

Price for the basic CDP-XI/00 is under $4000 when purchased in moderate quantities. The CDP-XI/35 computer with 32KX16 core memory and memory management in quantities of 25 units sells for under $13,000 as compared to an equivalent PDP-11/40 at $17,775. An 8KX16 CDP-XI/35 lists for $9,300. All Cal Data's CDP-XI computer models can be purchased under industry-standard OEM terms and/or secured by a license which assures the licensee of effective control of his computer's source of manufacture as well as significant cost reductions.

Cal Data is currently making shipments to a backlog of over $3.0 million in OEM orders for their DEC-compatible line of connectors, backplanes, GP wire-wrap boards, expansion cabinets, core memory systems, memory management units, CDP-XI/35 and CDP-XI/I computers.

Since July 1973 the company has operated as a wholly-owned subsidiary of DATA 100, the Minneapolis manufacturer of remote batch computer terminals. Cal Data's business objectives are exclusively dedicated to the support and service of the volume OEM computer user. With the DATA 100 association, Cal Data offers its OEM customers the support of more than 200 professional computer system service engineers established coast-to-coast, in Canada, Australia and in Europe.

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CDP-XI Computer Family

The CDP-XI computer (Figure 1) is a high-speed microprogrammed digital computer designed for application in a wide variety of computing and control applications. Microprogramming, combined with a powerful and flexible hardware architecture, permit the basic computer to be fully optimized to a specific application. The CDP-XI is the basic element of a family of computers (Figure 2) designed for efficient, high-speed emulation of general-purpose computer architectures. In many cases, the emulated machine is outperformed by the hardware/software-compatible CDP-XI, and at a lower unit price. It can also be applied as a direct function processor by implementation of problem-oriented microprograms.

Figure 1. CDP-XI/35 Computer with 80K Words of 8K by 16-Bit, 675-ns Core Memory Modules (Using CDP-16K, 850-ns Core Memory Modules, a Full 128K Works can be installed)

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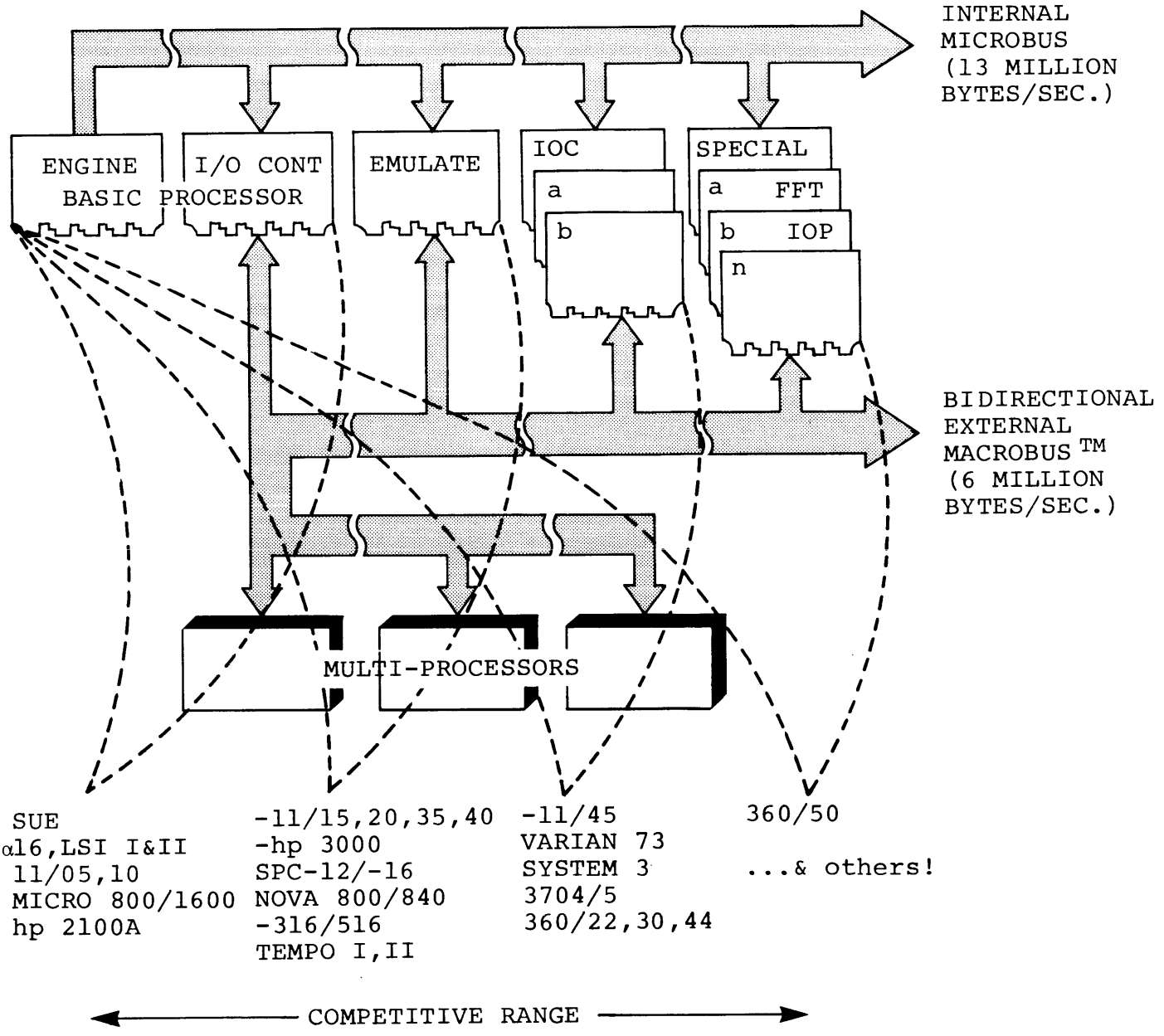

Figure 2. Emulation Capability of the CDP-XI Family

TM - MACROBUS is a trademark of California Data Processors

FEATURES

The CDP-XI family architecture combines general microprogramming capability with specialized optional features to permit high emulation speeds with modest control-memory space utilization. The mechanical design provides full modularity, mounting flexibility and service convenience. Cooling, power distribution and other critical system requirements are optimized for OEM applications. Conservative electronic implementation ensures wide margins, readily available components and reliable operation over a wide environmental range. Subassemblies are designed for easy assembly and automated testing, and the overall system is structured for simple, straightforward manufacturing procedures.

SYSTEM ORGANIZATION

The basic elements of the system are the microengine and I/O control. These elements are controlled by microprogram sequences (firmware) stored in a control memory. By changing the contents of control memory, the entire operation of the system can be altered. An emulation system is implemented by placing the appropriate firmware in control memory, causing the microprocessor to operate like the computer to be emulated.

The I/O channel of the system consists of a bidirectional bus designated the MACROBUS. The MACROBUS is time shared by all elements of the system, including the basic processor. Devices on the MACROBUS can communicate directly with other devices, independent of the microprocessor, for such uses as DMA data transfers.

A macropanel, representing the control panel of a general-purpose computer, is often provided in an emulation application. The macropanel is serviced by the microprocessor as an I/O device interfacing with the MACROBUS. Special console support firmware is normally provided for such a unit.

Memory is attached directly to the MACROBUS and is treated as an I/O device. Core memory modules of 8K words by 16-bits and 16K words by 16-bits capacity are available for addition to the system. Semiconductor memory can also be added in any speed/capacity mix with core memory. All MACROBUS devices can communicate directly with memory.

Peripheral devices and system interfaces are attached to the MACROBUS via controllers. Users can readily interface with the MACROBUS using simple design rules. Cal Data offers several standard peripheral subsystems and breadboard circuit components for the CDP-XI family.

BASIC DESIGN FEATURES OF THE CDP-XI COMPUTER FAMILY ARE:

Processor

- 48-bit microcommand word length.
- Parallel execution of multiple functions per microcommand.
- 150-ns microcommand execution time.
- 16-bit data word length.
- 16 multipurpose file registers (16-bits each).
- Nine additional registers accessible by microcommand.
- 16-level hardware pushdown stack.
- Microcommand sequence repeat loop counter.
- Optional high-speed emulation instruction decode, function generation and interrupt response hardware.
- Bit, byte and word manipulations.
- 256- to 4096-word control memory using bipolar ROM or PROM devices.
- Power-failure/restart circuitry included in the computer.
- Unique, control memory "overlay" provisions.
- Optional asynchronous I/O channel and line-frequency clock available.
- Multiple, divide and double-precision shift microcommands available.

Electrical and Electronic

- Bipolar TTL integrated circuits (multisourced).
- Extensive use of MSI and LSI.
- Wide timing margins.
- Single-phase, square-wave clock.
- Conservative component derating.
- Metal can transistors and hermetically sealed passive devices only.
- High noise immunity I/O drivers and receivers.

Memory and Input/Output

- 8K-word (675-ns cycle, 275-ns access) and 16K-word (850-ns cycle, 300-ns access) core memory modules.
- Interleaved data transfers between identical memory modules.
- Expansion to 124K or 127K of directly addressable memory with optional Memory Management Unit.
- Universal asynchronous I/O channel (MACROBUS) with direct-memory-access capability.
- Four external priority interrupt levels.
- 16-bit parallel, word or byte-mode transfers.
- Automatic MACROBUS delay timeout protection.

Microprogramming Aids

- Microcontrol panel.
- Symbolic microassembler.
- Alterable control memory and support software.
- PROM programmer.

Packaging, Power and Environmental

- 10-1/2 inch processor chassis with vertical board mounting from the top.
- Printed-circuit backplane with up to eight spare slots for memory and I/O controller boards.
- Four fans for high volume, positive-pressure air flow through the chassis with provision for air filters.
- Modular power supply providing 36 A at +5 V.
- Low-noise internal power distribution and grounding system.
- Convenient external I/O cable scheme.
- System designed to meet UL standards.
- 0 to 50^{o} C ambient operating temperature.
- 10 to 90% humidity (without condensation).

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SYSTEM OPERATING SPEED

COMPARISONS

CDP-XI/35 VS. -11/40 VS. -11/05

INTRODUCTION

The attached tables provide a comparison of the California Data Processors (Cal Data) CDP-XI/35, vs. the -11/40, and -11/05 instruction execution times and bus operation timing. The list of instructions compared is not complete, but is believed very representative of the more useful instructions.

The analysis assumes the Cal Data system is implemented with a CDP-8K (675 ns cycle/275 ns access) core memory and a teletype controller. The -11/40 and -11/05 systems are assumed to be implemented with 8K of ME11 or MF11 900 ns cycle core.

Readers unfamiliar with the subject systems should consult the manufacturer's literature for definition of instructions and bus operations.

Comparisons

Table 1 gives timing examples for various bus operations. Specifications for memory interleave rates in -11/40 and -11/05 systems are not given in manufacturer's published literature.

Table 2 compares execution times of most of the control branch and miscellaneous instructions.

Table 3 compares execution times of most of the single operand instructions. Note that execution time for the CDP-XI/35 is the same for word or byte mode operations; execution of -11/40 and -11/05 instructions is slower in byte mode at an odd byte operand location.

Table 4 compares execution times of the double operand Move - MOV or MOVB - instruction. This is a particularly important function since a high percentage of data transfers to/from memory and I/O devices generally involve its use.

Table 5 compares an additional set of double operand instructions which have equal execution times.

Analysis

Examination of the information given shows that a quantitative measure of relative speed is dependent on the mix of instructions and bus I/O operations being performed. As evident from the tables, some operations in the Cal Data systems are faster and some are slower than in the -11/40. Both systems are considerably faster than the -11/05 which is in a lower price/performance category.

The following general conslusions are made:

1. The Cal Data system has a faster bus structure than the -11/40 and -11/05. This derives partly from faster memory access and cycle times, partly from the bus circuit implementation, and partly from the microcode techniques used to implement the CDP-XI/35. Cal Data's wider bus bandwidth directly enhances overall system thruput in all applications since all information transfers - program and I/O - use this common facility; systems with heavy DMA traffic will benefit more than those with limited I/O activity. (Refer to Table 1).

2. The control, branch, and miscellaneous instructions are in most cases faster in the CDP-XI/35 than in the -11/40. (Refer to Table 2).

3. Except for address mode 0 (register address), the CDP-XI/35 is equal to or faster than the -11/40 for almost all single operand instructions. The same is generally true for other single operand instructions not shown in the table. (Refer to Table 3).

4. The relative execution speeds between the CDP-XI/35 and -11/40 for the MOV varies considerably with the mode. Generally, the -11/40 is faster in the simple register modes and slower in the more complex modes. Byte manipulations are generally slower in the -11/40 than in the CDP-XI/35 because of the odd byte location penalty. (Refer to Table 4).

5. The -11/40 is generally faster in most other double operand instructions in word mode. Byte manipulations will suffer in the -11/40 overall because of the penalty for handling odd byte locations. (Refer to Table 5).

6. Test measurements show the CDP-XI/35 and -11/40 to be esentially equal in overall program execution speed with no DMA bus activity. Timing of extensive sequenced instruction diagnostics resulted in overall execution time differences of less than 5%. The CDP-XI/35 should exhibit higher thruput with heavy bus I/O activity and programs with heavy byte manipulations.

7. Both the CDP-XI/35 and -11/40 are considerably faster than the -11/05, probably by a factor of 2-3, depending on the particular application.

TABLE 1

Bus Timing Examples

Operation	CDP-XI/35	-11/40	-11/05
Interrupt response time, μs max. (1)	5.0	5.4	7.0
DMA latency time, μs max.	1.5	3.5	3.5
Wait on interrupt check period, μs	.33	1.12	Unknown
Max. bus transfer rates (3)			
Write, words/sec. X 10^6	3.5	2.5	2.5
Read, words/sec. X 10^6	3.0	2.2	2.2
Max. memory DMA rates			
Non-interleaved, words/sec. X 10^6	1.48	1.1	1.1
Interleaved, write, words/sec. X 10^6	2.35	Unknown	
Interleaved, read, words/sec. X 10^6	2.94	Unknown	

NOTES:

(1) Measured from interrupt recognition at end of current instruction to fetch of first interrupt routine instruction, assuming no intervening DMA transfers

(2) Non-memory device, minimum response time design

TABLE 2

Control, Branch, Trap and Miscellaneous Instruction Times (Microseconds)

		CDP-XI/35	-11/40	-11/05
Conditional Branches	No Branch	2.0	1.8	2.5
	Branch	1.5	1.4	1.9
RTS		2.1	2.4	3.8
RTI		3.0	2.9	4.4
RTI		3.1	2.9	-
Traps		5.6	5.8	8.2
Branch (BR)		1.7	1.8	2.5
SCC		1.5	1.7	2.5
CCC		1.5	2.0	2.5
WAIT		1.3(2)	2.2(1)	1.8
HALT		1.5	2.4	1.8
MARK		2.3	2.6	-
SOB	No Branch	1.5	2.0	-
	Branch	1.6	2.4	

NOTES:

(1) Interrupts checked at 1.12 μs intervals

(2) Interrupts checked at .33 μs intervals

TABLE 3

Single-Operand Instruction
Times (Microseconds)

		ADDRESS MODE							
INSTRUCTION	SYSTEM	0	1	2	3	4	5	6	7
JMP	CDP-XI/35	-	1.5	1.8	2.1	2.0	2.3	2.1	2.8
	11/40	-	1.8	2.1	2.3	1.9	2.3	2.4	2.9
	11/05	-	3.4	3.4	4.4	3.4	4.4	4.4	5.7
JSR	CDP-XI/35	-	2.8	3.0	3.3	3.0	3.4	3.3	4.0
	11/40	-	2.9	3.2	3.4	3.0	3.4	3.5	4.1
	11/05	-	6.2	6.2	7.2	6.2	7.2	7.2	8.5
TST(B)	CDP-XI/35	1.6	2.0	2.6	3.0	2.6	3.1	3.0	3.8
	11/40	1.0	2.6/3.0	2.6/3.0	3.5/4.0	2.6/3.1	3.5/4.0	3.2/3.7	4.1/4.6
	11/05	2.2	4.6/5.9	4.6/5.9	5.6/6.9	4.6/5.9	5.6/6.9	5.6/6.9	6.9/8.2
CLR(B)	CDP-XI/35	1.6	2.1	2.5	2.6	2.5	2.8	2.6	3.5
	11/40	1.0	2.6/3.0	2.6/3.1	3.5/4.0	2.6/3.1	3.5/4.0	3.2/3.7	4.1/4.6
	11/05	3.4	5.8/8.2	5.8/8.2	6.8/9.2	5.8/8.2	6.8/9.2	6.8/9.2	8.1/10.5
COM(B) INC(B) DEC(B) NEG(B) ASL(B) ADC(B) SBC(B)	CDP-XI/35	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0
	11/40	1.0	2.6/3.0	2.6/3.0	3.5/4.0	2.6/3.1	3.5/4.0	3.2/3.7	4.1/4.6
	11/05	3.4	5.8/8.2	5.8/8.2	6.8/9.2	5.8/8.2	6.8/9.2	6.8/9.2	8.1/10.5
ASR(B) ROR(B)	CDP-XI/35	1.6	2.8	3.1	3.3	3.1	3.5	3.3	4.0
	11/40	1.3/1.4	2.8/3.3	2.9/3.4	3.8/4.3	2.9/3.4	3.8/4.3	3.5/4.0	4.4/4.9
	11/05	3.4	5.8/8.2	5.8/8.2	6.8/9.2	5.8/8.2	6.8/9.2	6.8/9.2	8.1/10.5

NOTE: Longer time applies to odd byte address.

Example: 2.6/3.0 means 3.0 μs for odd byte address,
2.6 μs for word and even byte address.

TABLE 4

MOV(B) Instruction Times
(Microseconds)

SYSTEM	DEST. MODE	SOURCE MODE 0	1	2	3	4	5	6	7
CDP-XI/35		2.0	2.6	2.6	3.3	2.6	3.3	3.3	4.1
-11/40	0	.9/1.8	2.2/2.6	2.3/2.6	3.2/3.5	2.3/2.6	3.2/3.5	2.9/3.3	3.8/4.2
-11/05		3.1/3.7	4.0/6.9	4.0/6.9	5.5/8.4	4.0/6.9	5.5/8.4	5.5/8.4	6.5/9.4
CDP-XI/35		2.5	3.1	3.1	3.8	3.1	3.8	3.8	4.6
-11/40	1	2.4/2.6	3.2/3.3	3.3/3.4	4.2/4.3	3.3/3.4	4.2/4.3	3.9/4.0	4.8/4.9
-11/05		5.5/8.5	7.0/10.7	7.0/10.7	8.5/12.2	7.0/10.7	8.5/12.2	8.5/12.2	9.5/13.2
CDP-XI/35		2.8	3.6	3.6	4.3	3.6	4.3	4.3	5.1
-11/40	2	2.4/2.6	3.2/3.3	3.3/3.4	4.2/4.3	3.3/3.4	4.2/4.3	3.9/4.0	4.8/4.9
-11/05		5.5/8.5	7.0/10.7	7.0/10.7	8.5/12.2	7.0/10.7	8.5/12.2	8.5/12.2	9.5/13.2
CDP-XI/35		3.0	3.8	3.8	4.5	3.8	4.5	4.5	5.6
-11/40	3	3.2/3.3	4.0/4.1	4.0/4.2	4.9/5.1	4.0/4.2	4.9/5.1	4.6/4.8	5.5/5.7
-11/05		6.5/9.5	8.0/11.7	8.0/11.7	9.5/13.2	8.0/11.7	9.5/13.2	9.5/13.2	10.5/14.2
CDP-XI/35		2.8	3.6	3.6	4.3	3.6	4.3	4.3	5.1
-11/40	4	2.4/2.6	3.2/3.3	3.3/3.4	4.2/4.3	3.3/3.4	4.2/4.3	3.9/4.0	4.8/4.9
-11/05		5.5/8.5	7.0/10.7	7.0/10.7	8.5/12.2	7.0/10.7	8.5/12.2	8.5/12.2	9.5/13.2
CDP-XI/35		3.1	4.0	4.0	4.6	4.0	4.6	4.6	5.4
-11/40	5	3.2/3.3	4.0/4.1	4.0/4.2	4.9/5.1	4.0/4.2	4.9/5.1	4.6/4.8	5.5/5.7
-11/05		6.5/9.5	8.0/11.7	8.0/11.7	9.5/13.2	8.0/11.7	9.5/13.2	9.5/13.2	10.5/14.2
CDP-XI/35		3.0	3.8	3.8	4.5	3.8	4.5	4.5	5.3
-11/40	6	2.8/3.0	4.0/4.1	4.0/4.2	4.9/5.1	4.0/4.2	4.9/5.1	4.6/4.8	5.5/5.7
-11/05		6.5/9.5	8.0/11.7	8.0/11.7	9.5/13.2	8.0/11.7	9.5/13.2	9.5/13.2	10.5/14.2
CDP-XI/35		3.6	4.5	4.5	5.1	4.5	5.1	5.1	5.9
-11/40	7	3.7/3.8	4.8/5.0	4.9/5.0	5.8/5.9	4.9/5.0	5.8/5.9	5.5/5.6	6.4/6.5
-11/05		7.8/10.8	9.3/13.0	9.3/13.0	10.5/14.2	9.3/13.0	10.5/14.2	10.5/14.2	11.5/15.2

NOTE: Slower execution times given for -11/40 and -11/05 are for odd byte address.

TABLE 5

Typical Double Operand Instruction Times
(Microseconds)
BIS(B), BIC(B), ADD, SUB

SYSTEM	DEST. MODE	SOURCE MODE 0	1	2	3	4	5	6	7
CDP-XI/35		2.0	2.6	2.6	3.3	2.6	3.3	3.3	4.1
-11/40	0	1.0	2.4/2.7	2.4/2.8	3.3/3.7	2.4/2.8	3.3/3.7	3.1/3.4	4.0/4.3
-11/05		3.7	4.6/5.9	4.6/5.9	6.1/7.4	4.6/5.9	6.1/7.4	6.1/7.4	7.1/8.4
CDP-XI/35		3.1	3.8	3.8	4.5	3.8	4.5	4.5	5.3
-11/40	1	2.7/3.0	3.0/4.0	3.4/4.1	4.3/5.0	3.4/4.1	4.3/5.0	4.0/4.7	4.9/5.6
-11/05		6.1/8.5	7.0/10.7	7.0/10.7	8.5/12.2	7.0/10/7	8.5/12.2	8.5/12.2	9.5/13.2
CDP-XI/35		3.5	4.1	4.1	4.8	4.1	4.8	4.8	5.6
-11/40	2	2.6/3.0	3.4/4.1	3.4/4.1	4.3/5.0	3.4/4.1	4.3/5.0	4.1/4.7	5.0/5.6
-11/05		6.1/8.5	7.0/10.7	7.0/10.7	8.5/12.2	7.0/10.7	8.5/12.2	8.5/12.2	9.5/13.2
CDP-XI/35		3.6	4.3	4.3	4.9	4.3	4.9	4.9	6.1
-11/40	3	3.6/3.9	4.3/5.0	4.3/5.0	5.2/5.9	4.3/5.0	5.2/5.9	5.0/5.6	5.9/6.5
-11/05		7.1/9.5	8.0/11.7	8.0/11.7	9.5/13.2	8.0/11.7	9.5/13.2	9.5/13.2	10.5/14.2
CDP-XI/35		3.5	4.1	4.1	4.8	4.1	4.8	4.8	5.6
-11/40	4	2.7/3.0	3.4/4.1	3.4/4.1	4.3/5.0	3.4/4.1	4.3/5.0	4.1/4.7	5.0/5.6
-11/05		6.1/8.5	7.0/10.7	7.0/10.7	8.5/12.2	7.0/10.7	8.5/12.2	8.5/12.2	9.5/13.2
CDP-XI/35		3.8	4.5	4.5	5.1	4.5	5.1	5.1	5.9
-11/40	5	3.6/3.9	4.3/5.0	4.3/5.0	5.2/5.9	4.3/5.0	5.2/5.9	4.9/5.6	5.9/6.5
-11/05		7.1/9.5	8.0/11.7	8.0/11.7	9.5/13.2	8.0/11.7	9.5/13.2	9.5/13.2	10.5/14.2
CDP-XI/35		3.6	4.3	4.3	5.0	4.3	5.0	5.0	5.6
-11/40	6	3.5/3.8	4.0/4.7	4.1/4.7	5.0/5.6	4.1/4.7	5.0/5.6	4.7/5.4	5.6/6.3
-11/05		7.1/9.5	8.0/11.7	8.0/11.7	9.5/13.2	8.0/11.7	9.5/13.2	9.5/13.2	10.5/14.2
CDP-XI/35		4.9	4.9	4.9	5.6	4.9	5.6	5.6	6.4
-11/40	7	4.4/4.7	4.9/5.6	5.0/5.6	5.9/6.5	5.0/5.6	5.9/6.5	5.6/6.3	6.5/7.2
-11/05		8.4/10.8	9.3/13.2	9.3/13.0	10.5/14.2	9.3/13.0	10.5/14.2	10.5/14.2	11.5/15.2

NOTES: 1) Sub instruction in -11/40 is 0.1-0.2 μs slower than shown for most modes.
2) Slower execution times given for -11/40 and -11/05 are for odd byte address.

MAGNETIC CORE MEMORIES
CDP 8KX16 AND CDP 16KX16

cal data product

The CDP 8KX16 (Figure 1) and 16KX16 (Figure 2) Magnetic Core Memory modules are plug-compatible storage elements for the CDP-XI and PDP-11 series of computers. The CDP memory modules offer several outstanding features and advantages, including:

High Speed: The CDP memory modules comprise a fast core-memory system for PDP-11 series machines.

Full Compatibility: The CDP memory modules can be installed in all models of the PDP-11 series, thus eliminating the need for different versions or expensive, space consuming auxiliary mounting boxes, power supplies and interface cables.

Reduced Bus Loading: The CDP memory modules have but one-half of the UNIBUS load specification, permitting expansion in large systems.

Low Power Consumption: The CDP memory modules consume less power than other available memories.

No Special Voltage-Sequencing: The CDP memory modules do not require sequencing of the +5 and -15 volt power supplies.

7K-Word Option: This option to the CDP 8KX16 module permits PDP-11 systems to be expanded to 31K words (versus 28K words) without addition of a memory management unit. Memory management permits expansion to 127K words. Use of the 7K-word option reduces the 1/0 device-address availability from 4K to 1K addresses.

15K-Word Option: This option to the CDP 16KX16 module permits the same expansion as the 7K word option does for the CDP 8KX16. Capacity data for the two options are identical.

The CDP memory modules are random-access, coincident-current ferrite core devices with a "three-wire, 3D" configuration. The CDP 8KX16 module has a capacity of 8K (8,192) 16-bit words per module while the CDP 16KX16 has a capacity of 16K words per module. Each module comprises:

a. A single full-size printed circuit board containing the memory electronic circuitry.
b. A plug-in magnetic core plane assembly.

The CDP memory module can be operated in one of four modes:

a. Read/restore (equivalent to PDP-11 DATI).
b. Half-cycle read (equivalent to PDP-11 DATIP).
c. Clear/write (equivalent to PDP-11 DATO).
d. Clear/write byte (equivalent to PDP-11 DATOB).

The full memory cycle (clear/write or read/restore) time is 675 ns for the CDP 8KX16 in the worst case, measured at the memory interface connector, and the read-data access time (worst case) is 275 ns. Analogous figures for the CDP 16KX16 are 850 and 300 ns, respectively.

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Since the CDP memory modules are directly compatible within the PDP-11 computer series, the memory interface follows all rules of the standard UNIBUS. The CDP memory modules are functionally complete modules that require no additional supporting electronics (other than dc power) for operation in a UNIBUS interface environment.

A pair of identical CDP memory modules can be set for interleaved operation in which words at even and odd word addresses are written into or read from alternate modules. A clear or read operation can begin in one module while a write or restore operation is being completed in the alternate module, giving a higher effective memory-transfer rate. This configuration is prepared by interchanging the least-significant word-address bit with the least-significant module-address bit. Interleaving is always associated with a pair of CDP memory modules, and the interleaved pair is effectively treated as a contiguous series of locations. Interleaved modules must be ordered in this configuration.

CDP 8KX16 Memory General Specifications

Characteristic	Specification		
Type	Ferrite magnetic core, random access, coincident current.		
Organization	3-wire, 3-D planar core array.		
Word length	16 bits.		
Storage capacity	8,192 words (16,384 bytes).		
Operating times:	Cycle Time (1)		Access Time (1)
	Noninterleaved	Interleaved (2)	
Read/restore (DATI0	675 ns	425 ns	275 ns
Read (DATIP)	275 ns	275 ns	275 ns
Clear/write (DATO)	675 ns	340 ns	-
Half-cycle write	425 ns	450 ns	-
Interface signals:	Input	Bidirectional	Output
High (False)	+2.5 V min.	+2.5 V min.	
Low (True)	+1.4 V max.	+1.4 V max.	+0.5 V max. at 50 mA
Input current	+120 µA max. at 2.5 V	+120 µA max. at 2.5 V	+120 µA max. at 2.5 V
Power:	Operating (3) Amperes	Standby (3) Amperes	Voltage Tolerance
+5 Vdc	2.8	1.80	±5%
-15 Vdc	4.4	0.34	±5%
Ambient temperature	0° to 55°C with 200 lfm (61 lmm) airflow (4).		
Ambient humidity	0 to 90% without condensation.		
Dimensions	8.94 by 13.245 by 0.869 inches (22.70 by 33.642 by 2.21 cm).		
Mounting centers	1 inch (2.54 cm) recommended minimum.		

Notes for the CDP 8KX16 and 16KX16 specification tables:

1. Worst case, measured at the memory module interface connector.
2. Effective cycle time for sequential access to contiguous interleaved memory locations.
3. Maximum current drain for continuous operation, worst case pattern. If two CDP 8KX16 modules are interleaved, both should be considered as operating for power calculations.
4. lfm = linear feet per minute; lmm = linear meters per minute.

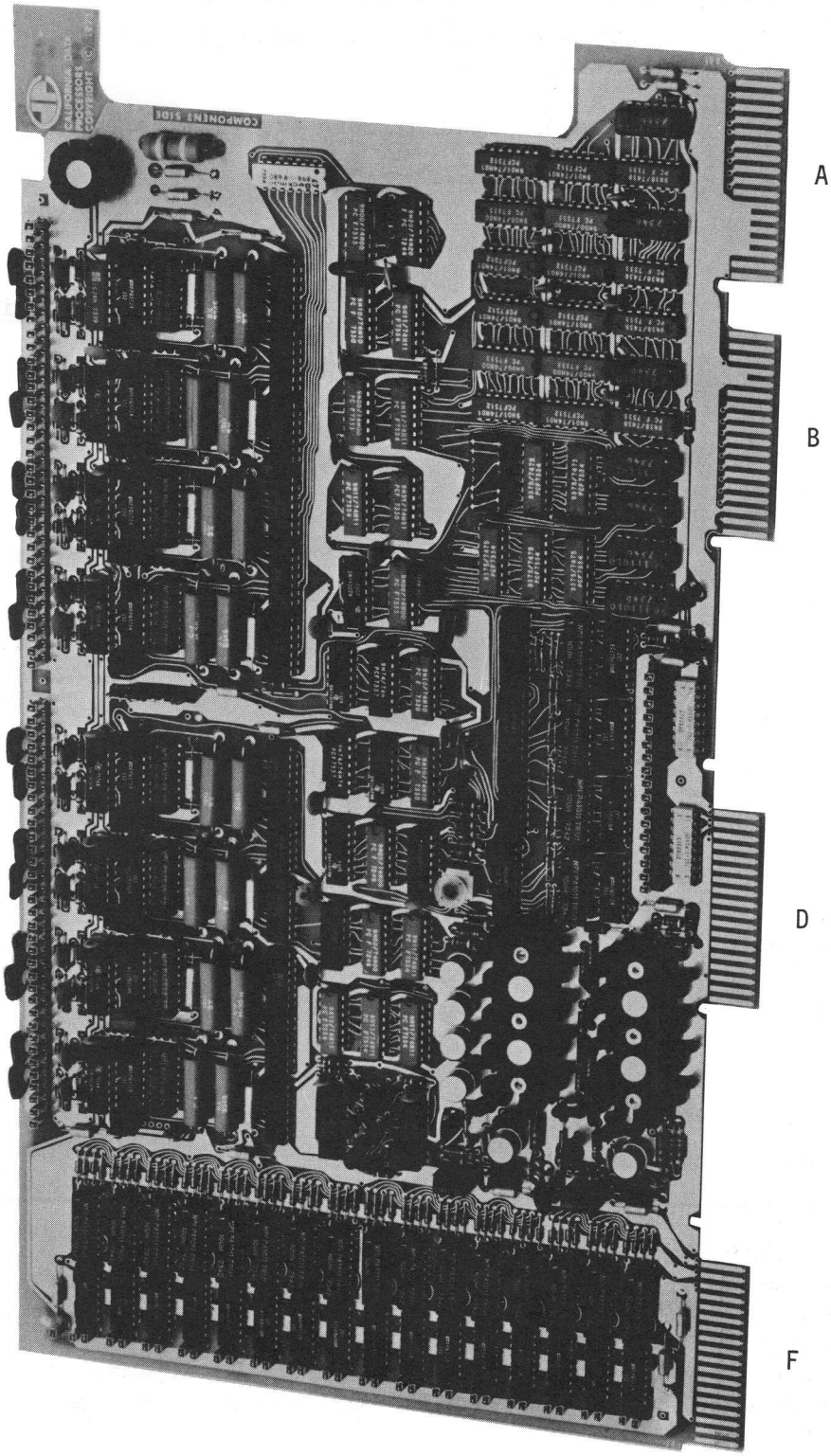

Figure 2. CDP 16KX16 Magnetic Core Memory

MAGNETIC CORE MEMORIES
CDP 8KX16 AND CDP 16KX16

cal data product

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Full Compatibility: The CDP memory modules can be installed in all models of the PDP-11 series, thus eliminating the need for different versions or expensive, space consuming auxiliary mounting boxes, power supplies and interface cables.

Reduced Bus Loading: The CDP memory modules have but one-half of the UNIBUS load specification, permitting expansion in large systems.

Low Power Consumption: The CDP memory modules consume less power than other available memories.

No Special Voltage-Sequencing: The CDP memory modules do not require sequencing of the +5 and -15 volt power supplies.

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15K-Word Option: This option to the CDP 16KX16 module permits the same expansion as the 7K word option does for the CDP 8KX16. Capacity data for the two options are identical.

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a. A single full-size printed circuit board containing the memory electronic circuitry.
b. A plug-in magnetic core plane assembly.

The CDP memory module can be operated in one of four modes:

a. Read/restore (equivalent to PDP-11 DATI).
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c. Clear/write (equivalent to PDP-11 DATO).
d. Clear/write byte (equivalent to PDP-11 DATOB).

The full memory cycle (clear/write or read/restore) time is 675 ns for the CDP 8KX16 in the worst case, measured at the memory interface connector, and the read-data access time (worst case) is 275 ns. Analogous figures for the CDP 16KX16 are 850 and 300 ns, respectively.

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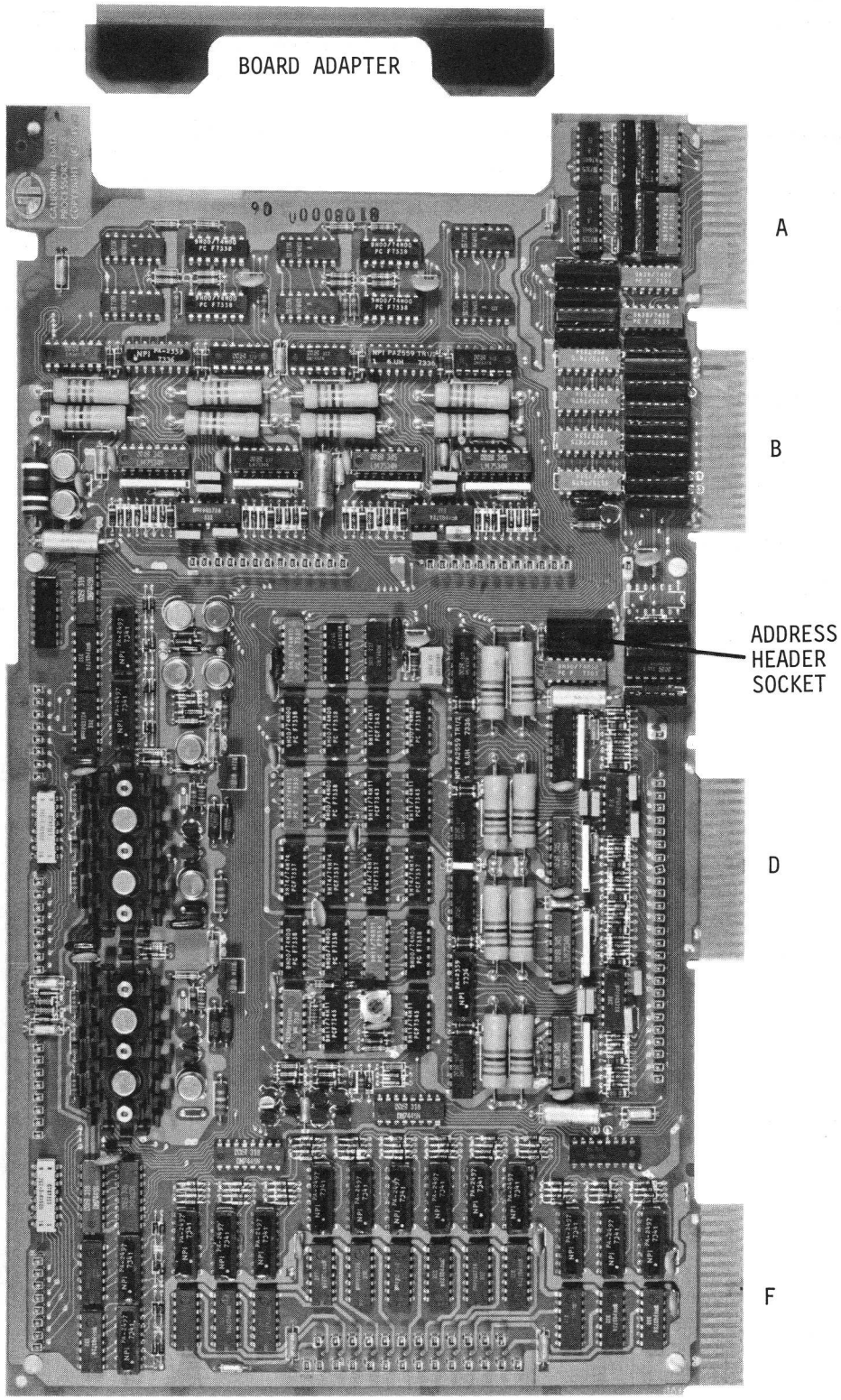

Figure 1. CDP 8KX16 Magnetic Core Memory

CDP 16KX16 Memory General Specifications

Characteristic	Specification		
Type	Ferrite magnetic core, random access, coincident current.		
Organization	3-wire, 3-D planar core array.		
Word Length	16 bits.		
Storage Capacity	16,384 words (32,768 bytes).		
Operating times:	Cycle Time (1)		Access Time (1)
	Noninterleaved	Interleaved (2)	
Read/restore (DATI)	850 ns	450 ns	300 ns
Read (DATIP)	300 ns	300 ns	300 ns
Clear/write (DATO)	850 ns	425 ns	-
Half-cycle write	450 ns	450 ns	-
Interface signals:	Input	Bidirectional	Output
High (False	+2.5 V min.	+2.5 V min.	
Low (True)	+1.4 V max.	+1.4 V max.	+0.5 V max. at 50 mA
Input current	+120 µA max. at 2.5 V	+120 µA max. at 2.5 V	+120 µA max. at 2.5 V
Power:	Operating (3) Amperes	Standby (3) Amperes	Voltage Tolerance
+5 VDC	3.2	2.4	±5%
-15	5.4	0.44	±5%
Ambient temperature	0° to 55° C with 200 lfm (61 lmm) airflow (4)		
Ambient humidity	0 to 90% without condensation.		
Dimensions	8.94 by 13.245 by 0.869 inches (22.70 by 33.642 by 2.21 cm).		
Mounting centers	1 inch (2.54 cm) recommended minimum.		

cal data publicity

california data processors
2019 south ritchey street
santa ana, california 92705
telephone: (714) 558-8211

CONTACT: Ray Ball, President

FOR IMMEDIATE RELEASE

CAL DATA 8K & 16K MEMORIES PERMIT PDP-11 EXPANSION TO 128K

SANTA ANA, CALIFORNIA - California Data Processors (Cal Data) has announced that it is now shipping 8K and 16K X 16 memories which are mechanically and electrically compatible with the entire line of PDP-11 computers. When used with or in place of DEC-supplied memories in Models -11/05, -11/10, -11/35, -11/40 and -11/45, the Cal Data memories can be installed directly in prewired locations in the computer cabinet. When used with or in place of DEC-supplied memories in Models -11/15 and -11/20, they allow either 8K, 16K, 24K or 32K of Cal Data memory to be added in the computer cabinet within the space equivalent to one DEC system unit.

A PDP-11 series computer system using the Cal Data memories may be expanded to a maximum capacity of 128K words by paralleling sixteen 8K units, eight 16K units or appropriate combinations of both. Most -11 series machines limit memory expansion to 24K words of memory. Cal Data opens memory expansion to 128K words in the -11/35, -11/40 and -11/45 by installation of an optional memory management unit. Cal Data will also provide expanded memory addressing for -11/05, -11/10, -11/15 and -11/20 models to meet custom requirements.

The new 8K and 16K memories offer an option which provides for operation of up to 31K of memory in systems without either a DEC or Cal Data memory management unit. In these configurations, Cal Data

- more -

reserves 1024 addresses for non-memory I/O devices instead of the 4096 addresses reserved in the standard configurations.

Full cycle/access time is 675nsec/275nsec for the 8K memory and 850nsec/300nsec for the 16K memory. Interleaved operation may be effected with pairs of 8K or 16K units. Each of these memory designs operates with less power consumption per bit at higher speeds and with less than half of the bus loading factor of comparably sized modules available from DEC and other independent suppliers.

List prices are $2,250 for the 8K unit and $3,250 for the 16K unit. Quantity discounts to 50% may be negotiated. Delivery is currently 7 days for single 8K units and 30 days for single 16K units.

Cal Data manufactures an extensive line of DEC-compatible products including connectors, backplanes, GP wire-wrap boards, power supplies, expansion cabinets, core memory systems, memory management units and several PDP-11 series compatible computer options.

The company was recently acquired by DATA 100, the Minneapolis manufacturer of remote batch computer terminals. With the DATA 100 association, Cal Data can now offer its customers the support of more than 200 professional computer system service engineers established coast-to-coast, in Canada and in Europe.

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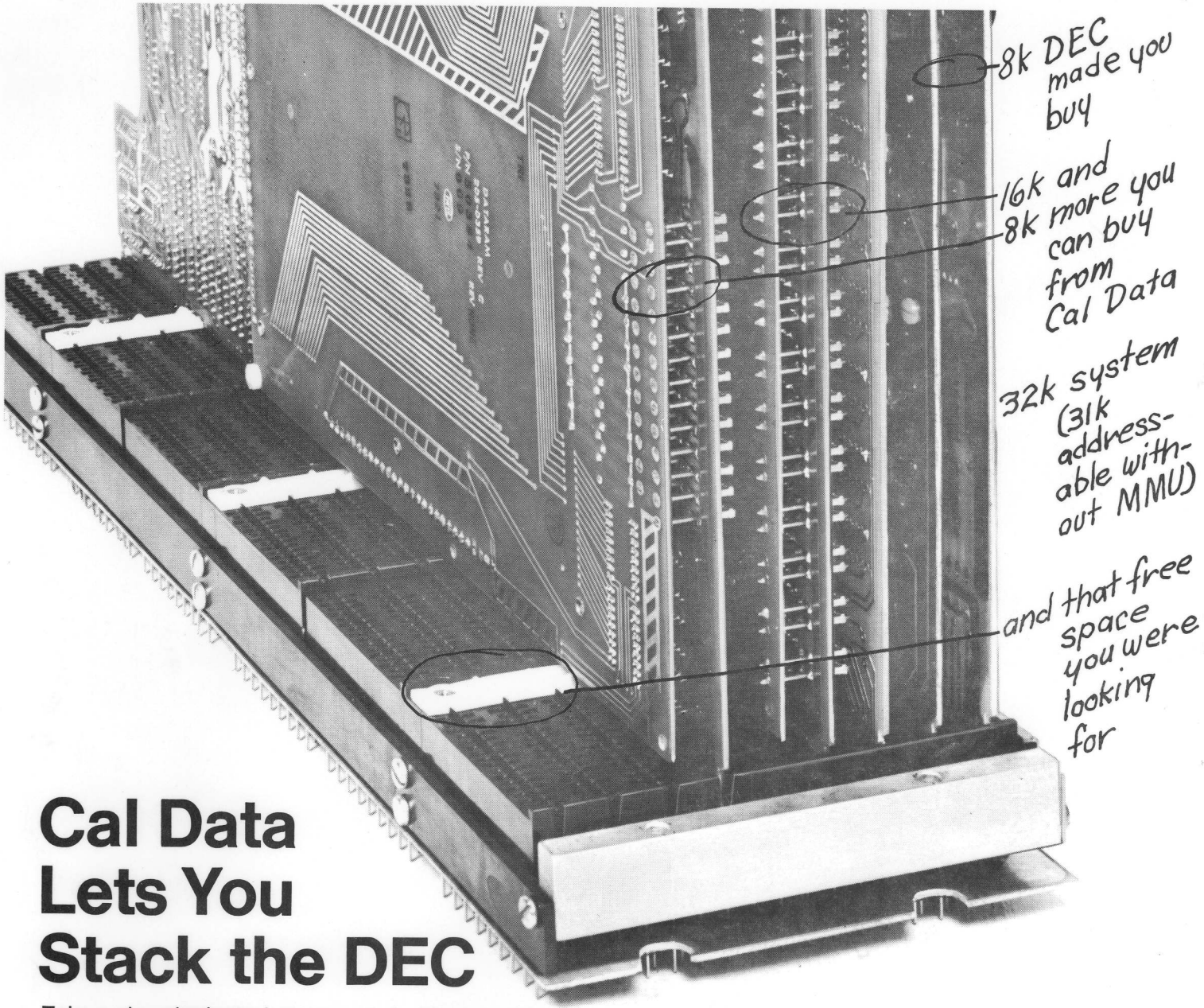

Cal Data Lets You Stack the DEC

Take a close look at what you can do. You can add 24K of Cal Data memory to DEC's 8K PDP-11, create a 32K system and gain that extra space you need for your other requirements. And Cal Data can help you **beat the memory management rap** with a special option available on either their 8K or their 16K memory products. That's a saving of up to $4500 right there not to mention a few thousand more on the memories themselves.

Cal Data's memories are electronically and mechanically compatible with the entire line of PDP-11 computers. Otherwise there is no comparison between them and their DEC counterparts or any other "11" series compatible add-on for that matter. Cal Data memories cost less, are faster, cut the bus load in half and require less power.

The 8K unit with a full cycle time of 675 nsec and an access time of 275 nsec lists for $2250 and discounts to 50% in quantity. The 850/300 nsec 16K unit goes for $3250 with the same kind of discount.

Right now our line extends far beyond memories to include DEC compatible connectors, backplanes, wirewrap boards, power supplies, core memory systems, expansion cabinets and . . . you just might guess what's next. Try us. For more information, call, write or fill out the coupon today.

Gentlemen:
The idea of a 32K system with space left over intrigues me:

- ☐ Tell me how you do it without a memory management unit.
- ☐ Send details on your 8K and 16K core memories.
- ☐ Tell me about the rest of your line.
- ☐ Put me on your mailing list.

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Company_____

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