

# 400 Mb/s/pin SLDRAM

# 4M x 18 SLDRAM

PIPELINED, EIGHT BANK, 2.5V  
OPERATION

## FEATURES

- Very High Speed - 400 MHz data rate
- 800 MB/s peak I/O Bandwidth - provides very high bandwidth over narrow system memory bus
- Pipelined (Concurrent) Operation - Up to 8 transactions (in one bank, or spread across multiple banks)
- Eight (this data sheet) or more internal banks for hiding row access/precharge
- Programmable burst lengths of 4 or 8
- 100% peak bandwidth sustainable over random row as well as random column accesses, even with 8 byte bursts.
- Packet Oriented Protocol - Provides pin compatibility across multiple densities
- Auto Refresh and Self Refresh
- Command Clock for commands and addresses; Bidirectional Data Clocks for read and write data
- Dual Data Clocks provide smooth handoff from one data source to another
- Programmable Offset between Data and Data Clocks
- Programmable Read Delays - Adjustable in coarse increments equal to one data bit time, and fine increments which are a fraction of a bit time; allows for specific temporal placement of data at the memory controller data pins
- Programmable Write Delays - Adjustable in coarse increments equal to one data bit time. Allows for optimally adjusted write data temporal placement by the memory controller
- Supports bank accesses (bank initially idle) and page accesses (bank active, row open)
- 64ms, 8192-cycle refresh
- SLIO Interface Technology -  
Drivers : calibrated VOH and VOL levels,  
Receivers : narrow set-up and hold windows
- Single +2.5V  $\pm$  5% power supply

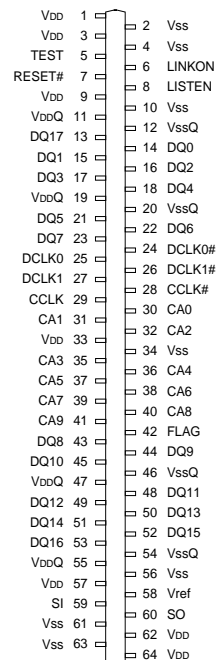
## OPTIONS

- Timing  
400 MHz data rate -400
- Plastic Package  
64-pin VSMP (400mil width, .4/.8mm pitch) VS
- Part Number Example: SLD4M18DR400VS-400

## MARKING

## PIN ASSIGNMENT (TOP VIEW)

### 64-Pin VSMP



## GENERAL DESCRIPTION

The SLD4M18DR400 SLDRAM is a synchronous, very high-speed, packet-oriented, pipelined dynamic random access memory containing 75,497,472 bits. The SLD4M18DR400 SLDRAM is internally configured as eight banks of 128K x 72; each of the 128K x 72 banks is organized as 1024 rows by 128 columns by 72 bits. The 72 bits per column access are transferred over the I/O interface in a burst of four 18-bit words.

All transactions begin with a request packet. Read and write request packets contain the specific command and address information required. Read and write data are transferred in packets; a single-column access involves the transfer of a single data packet, which is a burst of four 18-bit words. Data from either one or two columns in a page may be accessed with a single request packet; the latter results in a continuous burst of eight 18-bit data words.

**GENERAL DESCRIPTION (continued)**

Read or write requests may be issued to idle banks, or to the open row in active banks. Read or write requests indicate whether to leave the row open after the access, or to perform a self-timed precharge at the completion of the access (auto-precharge).

The SLD4M18DR400 uses a pipelined architecture and multiple internal banks to achieve high-speed operation and high effective bandwidth. Precharging one bank while accessing another bank will hide the precharge cycles, and provide seamless high-speed random access operation.

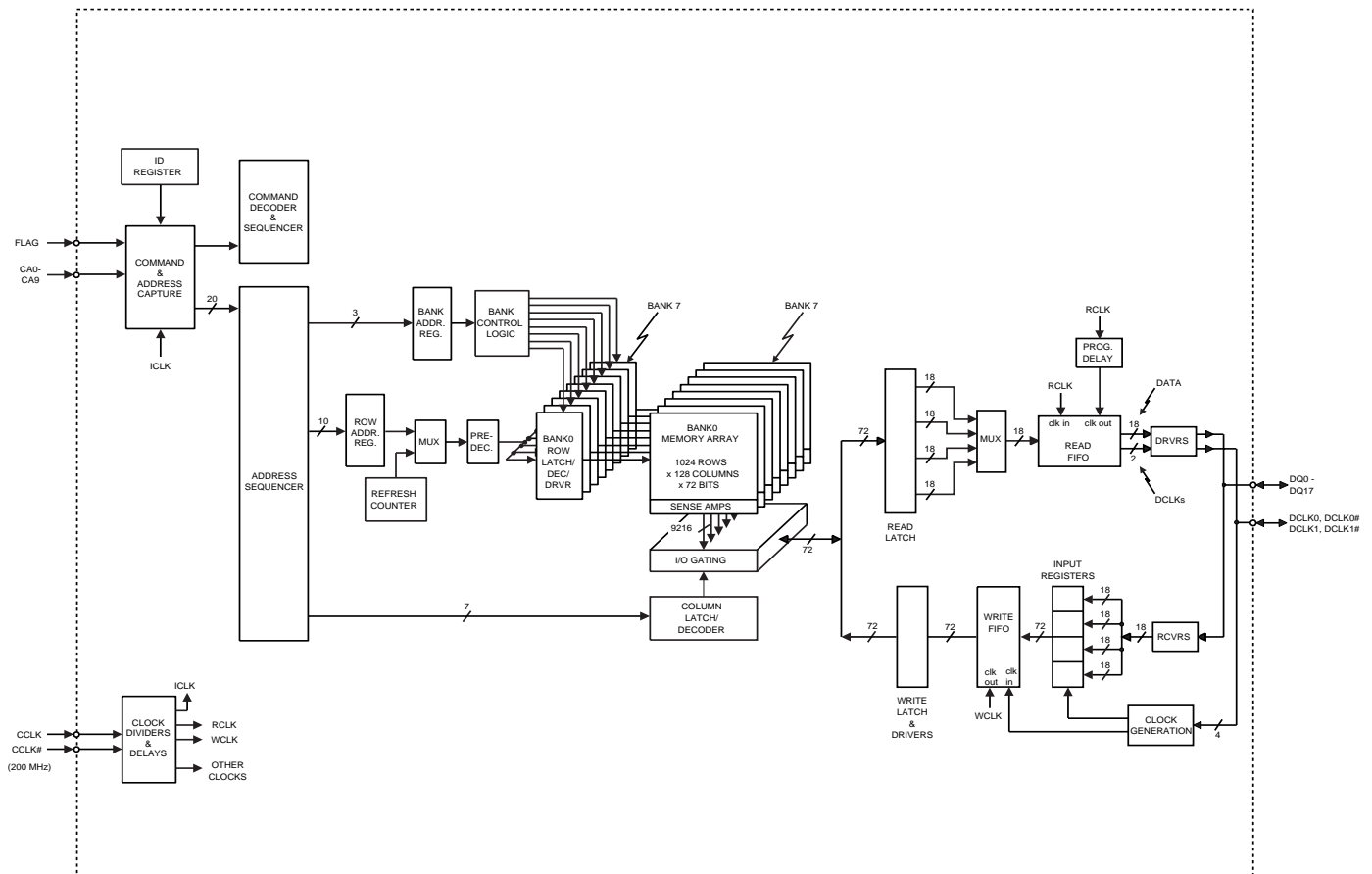
The SLD4M18DR400 is designed to operate in 2.5V memory systems. An auto-refresh mode is provided along with two power saving modes, standby and shutdown. Self-refresh is provided in the shutdown mode. The SLD4M18DR400 includes SLIO interface technology.

SLDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a very high data rate with automatic column-

address generation, the ability to interleave between several internal banks in order to hide precharge time, and the capability to provide a continuous burst of data across random row and/or column locations, even with 8-byte granularity.

Terminology - the term "tick" is used throughout this data sheet as the equivalent of one-half of the CCLK clock period. Also, for simplicity, the clocks will be referred to and shown as CCLK, DCLK0 and DCLK1. It should be understood that these are differential clocks and that each has a complementary signal. Any reference to a specific edge of a particular clock refers to the true version of that clock (e.g. CCLK) not the complement (e.g. CCLK#).

**FUNCTIONAL BLOCK DIAGRAM**



## PIN DESCRIPTIONS

VSMP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
29, 28	CCLK, CCLK#	SLIO Input	Command Clock (differential): CCLK is driven by the memory controller (or a separate clock chip) coincident with the leading edges of the command bits. SLDRAM command input signals are effectively sampled at each crossing of internally delayed versions of CCLK/CCLK#. Read clocks, write clocks, and other internal clocks are derived from CCLK.
25, 24, 27, 26	DCLK0, DCLK0#, DCLK1, DCLK1#	SLIO Input/ Output	Data Clocks (differential): For a read access, the specified pair of DCLK0/DCLK0# or DCLK1/DCLK1# is driven by the SLDRAM, and for write accesses, the specified pair is driven by the memory controller. During read accesses, the SLDRAM provides 2 crossings on the selected DCLK pair prior to, and then 1 crossing coincident with, the beginning of each valid data word. During write accesses, the SLDRAM uses a delayed version of the DCLK pair received with the data to capture the data.
59, 60	SI, SO	LVC MOS Input, Output	Select In, Select Out: The controller and all SLDRAMs on a channel are connected in series using these pins. This connection is used to initialize the SLDRAMs.
6	LINKON	LVC MOS Input	Link On: Used to enter and exit Shutdown mode.
7	RESET#	LVC MOS Input	Reset#: Provides a hardware reset; resets all logic, including the ID register. Memory contents are not affected. An SLDRAM must be initialized following a hardware reset.
8	LISTEN	LVC MOS Input	Listen: Used to enter and exit Standby mode.
42	FLAG	SLIO Input	Flag: FLAG HIGH indicates the start of a valid request packet; FLAG then goes LOW for the remainder of the packet. FLAG LOW at any other time is interpreted as a NOP.
30-32, 35-41	CA0-CA9	SLIO Input	Command, Address: Commands, Addresses and/or Register Write Data are transferred on these signals, in packets of four words.
14-18, 21-23, 43-45, 48-53, 13	DQ0- DQ17	SLIO Input/ Output	Data I/O: Data bus.
5	TEST	—	Test Pin: Should be tied to Vss during normal operation.
58	VREF	—	Reference voltage.
11, 19, 47, 55	VDDQ	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
12, 20, 46, 54	VSSQ	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
1, 3, 9, 33, 57, 62, 64	VDD	Supply	Power Supply: +2.5V ± 5%.
2, 4, 10, 34, 56, 61, 63	VSS	Supply	Ground.

## FUNCTIONAL DESCRIPTION

The specific SLDRAM described in this data sheet is an octal 128K x 72 DRAM which operates at 2.5V and includes a highspeed, packet-oriented, synchronous 18-bit interface, and a pipelined architecture. Each of the 128K x 72 bit banks is organized as 1024 rows by 128 columns by 72 bits.

Read and write accesses begin with the application of a request packet which includes all necessary address bits. The request packet is followed, after a specific programmed delay, by a data packet, to complete the transaction.

Prior to normal operation, the SLDRAM must be initialized. The following sections provide detailed information covering device initialization, packet definition, command descriptions, register definition, and device operation.

### Initialization

#### POWER-UP/HARDWARE RESET

SLDRAMs must be powered-up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to VDD and VDDQ, then after a delay of tVTD, power must be applied to system VTERM. VTERM must be applied after VDDQ to avoid device latch-up, which may cause permanent damage to the device. VREF can be applied any time after VDDQ, but is expected to be nominally coincident with VTERM. Inputs are not recognized as valid until after VREF is applied. Upon power-up, the SLDRAM DQ and DCLK outputs will be High-Z and SO output will be driven LOW. The RESET# input should be held active for at least tRST. This hardware reset sets the internal ID Register to a value of 255, the SUB-ID Register to a value of 15, and sets programmable read and write delays to the minimum values.

#### EXIT SHUTDOWN/CONTROLLER DRIVER ADJUST

A LOW level on LINKON, and a stable CCLK, must be applied prior to deasserting RESET#; then after deasserting RESET#, continue the initialization sequence as if exiting the Shutdown mode (LISTEN LOW before LINKON HIGH, bring LINKON HIGH, wait tLHHC for DLLs to lock, then bring LISTEN HIGH). [Note: external buffer devices may require that LISTEN be LOW prior to deasserting RESET#, and that an additional lock delay must occur between LINKON going HIGH and LISTEN going HIGH]. After the exit Shutdown sequence, the device is active, and the command and write timing synchronization should be performed.

At some point prior to the start of command and write timing synchronization, the controller must perform a self-calibration of VOH and VOL on it's SLIO outputs and I/O pins.

## COMMAND AND WRITE TIMING SYNCHRONIZATION

For command and write timing synchronization, the controller transmits the specified pattern on the FLAG, CA, DQ and DCLK signals, repetitively, until a LOW-to-HIGH transition is eventually detected on it's SI input (which occurs only after all devices on the channel are successfully synchronized). The controller brings it's SO output HIGH after transmitting the first cycle of the specified pattern. The pattern is broadcast to all devices connected directly to the controller and is identified by successive "1" levels on the FLAG input. During this operation, the SLDRAM devices use the SI/SO daisy-chain link to communicate to the controller that command and write timing synchronization has been completed. This is achieved by passing a LOW-to-HIGH transition from the controller SO output to the first SLDRAM SI input, and then from the first SLDRAM SO output to the second SLDRAM SI input, etc. through the last SLDRAM SO output driving SI input of the controller. Each SLDRAM device begins command and write timing synchronization upon detecting the specified pattern but does not drive it's SO output until both the transition at it's SI input, and the completion of command and write timing synchronization have occurred.

The receipt of the special pattern on FLAG prior to the LOW-to-HIGH transition on SI differentiates this activity on the SI/SO link from the similar procedure used during ID assignment. The controller stops sending the specified pattern after detecting SI HIGH, and then waits 16 ticks before sending a valid command or resetting the SI/SO link (the FLAG signal should be LOW for 16 ticks). This delay allows the SLDRAM devices to detect the absence of the special pattern on the FLAG input and to recognize the next HIGH level on the FLAG input as being the start of a valid command packet. The controller resets the SI/SO link by bringing it's SO LOW and waiting for it's SI to go LOW; HIGH-to-LOW transitions propagate through the link independent of device status or operation.

Although this data sheet describes a 400 Mb/s/p device, it is noted for future designs that faster devices up through 800 Mb/s/p will include the capability to synchronize at the 400 Mb/s/p rate.

## ID ASSIGNMENT

Next, each SLDRAM on the channel(s) is sequentially assigned a unique ID and SUB-ID combination. Each SLDRAM is individually selected in turn by using the SI/SO link. This mode of operation is identified by a LOW-to-HIGH transition on SI followed by an ID Register Write Request Packet. Each ID Register Write Request will be followed by a corresponding SUB-ID Register Write Re-

quest Packet (meeting tCC), and n of these request pairs will be issued (where n equals the number of SLDRAM devices in the system). Only the SLDRAM which has SI HIGH, ID = 255 and SUB-ID = 15 will react to the ID Register Write Request Packet in any given request pair. The corresponding SUB-ID Register Write Request Packet in each request pair must use the device ID just assigned by the ID Register Write Request Packet in that pair. Only the SLDRAM with that ID, with SI HIGH, and with SUB-ID = 15, will react to the SUB-ID Register Write Request Packet.

The selected SLDRAM reacts by writing the ID contained in the first packet to its internal ID Register, writing the SUB-ID contained in the second packet to its internal SUB-ID Register, and then driving its SO HIGH. The controller provides enough delay (tID plus related maximum routing delays) between the assertion of its SO output HIGH and the first issued request pair (and between subsequent issued request pairs) to allow for SO to propagate to the SI of the next device. ID assignment is complete when SI of the controller goes HIGH. Then the controller again resets the SI/SO link, as before.

#### PRE-CONFIGURATION/SLDRAM DRIVER ADJUST

At this point the SLDRAMs can receive commands, and each SLDRAM is uniquely addressable. Next, the SLDRAM operating frequency should be programmed, and then V<sub>OH</sub> and V<sub>OL</sub> calibration should be performed. The information indicating the appropriate operating frequency will either be contained in the controller itself, or can be obtained by the controller by polling some other component (jumpers, Serial Presence Detect device, etc.). The appropriate values are then written to the respective registers of each SLDRAM. For programmed operating frequencies other than 200 MHz (400 Mb/s/p) the command and write synchronization would be repeated at this point for the new frequency.

V<sub>OH</sub> calibration is performed for each SLDRAM by sending a Drive DCLKs HIGH command and iteratively sending Increment/Decrement V<sub>OH</sub> commands and observing the output level until the desired level is achieved. V<sub>OL</sub> calibration is performed similarly using the Drive DCLKs LOW and Increment/Decrement V<sub>OL</sub> commands. The controller should then issue a Disable DCLKs command packet.

#### READ TIMING SYNCHRONIZATION

At this point the controller can send commands to individual SLDRAMs, and the operating frequency is selected, so read timing synchronization can be performed.

For each SLDRAM, the controller should first send at least 16 Increment Fine Read Vernier commands for DQs and DCLK0 so that the coarse counter is incremented from the reset value (minimum). This allows room for subsequent adjustments. Then the controller should send a Read Sync Request packet to that SLDRAM. The specified data

pattern is returned by the SLDRAM, with a delay equal to the Actual Page Read Delay. The specific delays are unknown to the controller at this point, so the controller should enable the data synchronization circuitry immediately after sending a Read Sync Request command.

The controller should then adjust internal timing to capture data. This is accomplished by adjusting the Fine Read and Data Offset Verniers until the known data pattern is captured and the capture timing is optimized. Although several approaches are possible, one suggested approach would be as follows. The first step would be to achieve data capture of the sync pattern using DCLK0, by sending Increment/Decrement Data Offset Vernier commands. Then, issue Increment/Decrement Fine Read Vernier commands for DQs and DCLK0 until the desired relationship between DCLK0 and an internal clock within the controller is achieved. Note that the capture relationship between DCLK0 and DQs established in the first step above is not changed by this second step. Next (or along with the Increment/Decrement Fine Read Vernier commands for DQs and DCLK0), issue Increment/Decrement Fine Read Vernier commands for DCLK1 to align DCLK1 with DCLK0. The final adjustment for placing read data at the controller is the programming of the coarse latency, which is performed later.

At this point, the controller should issue a Stop Read Sync Packet, which instructs the SLDRAM to discontinue sending the sync pattern. After this is done for each SLDRAM, the controller can read data from each SLDRAM, but at an unspecified latency.

Command and Write Timing Synchronization, Write Timing Synchronization, Read Timing Synchronization or output level calibration may be repeated periodically if necessary for a given system design and environment. Such re-synchronizations or re-calibrations should be performed when no accesses are in progress.

#### DETECTING AND REPROGRAMMING READ AND WRITE LATENCIES

The controller may now detect the actual read latency in the system for each SLDRAM by sending a DRIVE DCLKs HIGH command followed (after tDD) by a Read Status Register Request. The controller should start monitoring the appropriate DCLK immediately after issuing the Read Status Register Request and should count clocks between sending the command and detecting the first HIGH-to-LOW transition on that DCLK. The read latency can be derived from this number. After detecting the latency, the controller should issue a Disable DCLKs command to prepare the DCLKs for normal operation.

With the latency (including system delays) now known, the remaining status registers can be read as in normal operation (i.e. without first issuing the DRIVE DCLKs



HIGH command). Data from status registers is provided in a burst of 4 by the SLDRAM, at the Actual Read Latency of the device (which appears as the observed system latency at the controller).

After reading the status registers of all SLDRAMs, the controller uses the data provided, as well as the observed latencies, to determine the appropriate read latency to be programmed into the SLDRAMs.

In one suggested system design approach, the devices with shorter observed read latencies would be programmed with additional latency so as to match that of the SLDRAM(s) with the longest observed latency (for both bank and page accesses). This way, all read data arrives at the controller with the same latency from command to data, regardless of which SLDRAM device provides the data.

At this point the controller determines the optimum write latency corresponding to the above read latency at the controller I/O pins (optimizing the tradeoff of internal bus turnaround time and external bus turnaround time) and then must determine the corresponding write latency value for each SLDRAM (the write latency at a given SLDRAM may be different than that at the controller I/O pins, and may be different from that of other SLDRAMs). There are several possible methods for determining the appropriate values, depending on system configuration; these will be covered in separate documentation.

Once the IDs have been assigned and the timing adjusted for each SLDRAM, the channel is ready for normal operation.

**Figure 1**  
**Command and Data Sync Patterns**

SIGNAL	REPEATING PATTERN
Flag	1 1 1 1 0 1 0 1 1 1 0 0 1 0 0 0 ...
CA9	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 1 ...
CA8	1 1 1 1 0 1 0 1 1 1 0 0 1 0 0 0 ...
CA7	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 1 ...
CA6	1 1 1 1 0 1 0 1 1 1 0 0 1 0 0 0 ...
CA5	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 1 ...
CA4	1 1 1 1 0 1 0 1 1 1 0 0 1 0 0 0 ...
CA3	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 1 ...
CA2	1 1 1 1 0 1 0 1 1 1 0 0 1 0 0 0 ...
CA1	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 1 ...
CA0	1 1 1 1 0 1 0 1 1 1 0 0 1 0 0 0 ...
DQ17	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 1 ...
DQ16	1 1 1 1 0 1 0 1 1 1 0 0 1 0 0 0 ...
DQ15	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 1 ...
DQ14	1 1 1 1 0 1 0 1 1 1 0 0 1 0 0 0 ...
DQ13	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 1 ...
DQ12	1 1 1 1 0 1 0 1 1 1 0 0 1 0 0 0 ...
DQ11	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 1 ...
DQ10	1 1 1 1 0 1 0 1 1 1 0 0 1 0 0 0 ...
DQ9	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 1 ...
DQ8	1 1 1 1 0 1 0 1 1 1 0 0 1 0 0 0 ...
DQ7	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 1 ...
DQ6	1 1 1 1 0 1 0 1 1 1 0 0 1 0 0 0 ...
DQ5	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 1 ...
DQ4	1 1 1 1 0 1 0 1 1 1 0 0 1 0 0 0 ...
DQ3	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 1 ...
DQ2	1 1 1 1 0 1 0 1 1 1 0 0 1 0 0 0 ...
DQ1	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 1 ...
DQ0	1 1 1 1 0 1 0 1 1 1 0 0 1 0 0 0 ...
DCLK1	1 0 ...
DCLK0	1 0 ...

## Packet Definition

General definitions for the various packets included in the protocol are shown in the following figures. More specific definitions are included, when necessary, in the Register Definition, Command Description and Device Operation sections of this data sheet.

### READ, WRITE, OR ROW OP REQUEST PACKET

The Read, Write, or Row Op Request Packet is used to initiate any Read or Write Access, or to open or close a specific row in a specific bank.

A Read or Write request will result in the transfer of a Data Packet on the data bus at a specific time later. The Data Packet is driven by the SLDRAM for a READ, or by the

memory controller for a Write. An Open Row or Close Row request generates no response.

Although unused address bits are not recognized by the SLDRAM device, zeroes should be applied for those bits, as shown.

### REGISTER READ REQUEST PACKET

The Register Read Request Packet is used to initiate a Read access to a register address. In response to a Register Read Request Packet, the SLDRAM will provide a Data Packet on the data bus at a specific time later.

Although bits REG6-REG4, and the other unused bits of the packet are not needed or recognized by the SLDRAM, zeroes should be applied for those bits, as shown.

**Figure 2**  
**READ, WRITE, OR ROW OP REQUEST PACKET DEFINITION**

Flag	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
0	x	x	x	x	x	x	x	x	x	x
1	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	CMD5
0	CMD4	CMD3	CMD2	CMD1	CMD0	BNK2	BNK1	BNK0	ROW9	ROW8
0	ROW7	ROW6	ROW5	ROW4	ROW3	ROW2	ROW1	ROW0	0	0
0	0	0	0	COL6	COL5	COL4	COL3	COL2	COL1	COL0

ID8-ID0 = Device ID Value  
CMD5-CMD0 = Command Code  
BNK2-BNK0 = Bank Address

ROW9-ROW0 = Row Address  
COL6-COL0 = Column Address  
0 = Unused, apply 0 for this bit

**Figure 3**  
**REGISTER READ PACKET DEFINITION**

Flag	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
0	x	x	x	x	x	x	x	x	x	x
1	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	CMD5
0	CMD4	CMD3	CMD2	CMD1	CMD0	REG6=0	REG5=0	REG4=0	REG3	REG2
0	REG1	REG0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0

ID8-ID0 = Device ID Value  
CMD5-CMD0 = Command Code

REG6-REG0 = Register Address  
0 = Unused, apply 0 for this bit

**REGISTER WRITE REQUEST PACKET**

The Register Write Request Packet is used to initiate a Write access to a register address. This packet consists of four words, with the latter two being the data to be written to the selected register.

Although bits REG6-REG4, and the other unused bits of the packet are not needed or recognized by the SLDRAM, zeroes should be applied for those bits, as shown.

**EVENT REQUEST PACKET**

The Event Request Packet is used to initiate a hard or soft reset, an Autorefresh, or a Close All Rows command, or to enter or exit Self Refresh, adjust output voltage levels, adjust the Fine Read Vernier or adjust the Data Offset Vernier.

The output voltage levels, or the fine read or data offset verniers can be adjusted using a dedicated Adjust Settings Event Request Packet or as part of an Autorefresh Event. In either case, the bits ADJ0-ADJ4 and DO0-DO4 determine the specific adjustment to be made, according to Truth Table 3. An autorefresh without adjustment is performed when ADJ0-ADJ4 are all 0.

The default values shown should be applied to the unused bits. For events other than Autorefresh or Adjust Settings, the ADJ0-ADJ4 bits are unused and zeroes should be applied to these bits. Note: bits DO0-DO4 are defined for future use, the default value for these bits is, and will be, all ones.

**Figure 4**  
**REGISTER WRITE PACKET DEFINITION**

Flag	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
0	x	x	x	x	x	x	x	x	x	x
1	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	CMD5
0	CMD4	CMD3	CMD2	CMD1	CMD0	SID4	SID3	SID2	SID1	SID0
0	REG6=0	REG5=0	REG4=0	REG3	REG2	REG1	REG0	0	0	0
0	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

ID8-ID0 = Device ID Value  
SID4-0 = Device Sub-ID Value  
RD9-RD0 = Register Data

CMD5-CMD0 = Command Code  
REG6-REG0 = Register Address

**Figure 5A**  
**EVENT PACKET DEFINITION**

Flag	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
0	x	x	x	x	x	x	x	x	x	x
1	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	CMD5
0	CMD4	CMD3	CMD2	CMD1	CMD0	SID4	SID3	SID2	SID1	SID0
0	E6	E5	E4	E3	E2	E1	E0	0	0	0
0	ADJ4*	ADJ3*	ADJ2*	ADJ1*	ADJ0*	DO4*	DO3*	DO2*	DO1*	DO0*

\* = For Autorefresh and Adjust Settings events only, otherwise unused (ADJx = 0, DOx=1)

ID8-ID0 = Device ID Value  
SID4-0 = Device Sub-ID Value  
ADJ4-0 = Adjust Setting Code

CMD5-CMD0 = Command Code  
E6-E0 = Event Index Code  
DO4-0 = Data Offset DQ Select (future use)



**DATA SYNC REQUEST PACKET**

A Data Sync Request Packet is used to control the output

logic values and patterns used for level adjustment, latency detection, and timing synchronization.

**Figure 5B**  
**DATA SYNC REQUEST PACKET DEFINITION**

Flag	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
0	x	x	x	x	x	x	x	x	x	x
1	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	CMD5
0	CMD4	CMD3	CMD2	CMD1	CMD0	SID4	SID3	SID2	SID1	SID0

ID8-ID0 = Device ID Value  
SID4-0 = Device Sub-ID Value

CMD5-CMD0 = Command Code

**DATA PACKET**

A Data Packet is provided by the controller for each Write Request, and by the SLDRAM for each Read Request. Each Data Packet contains either 8 bytes or 16 bytes, depending on whether the burst length was set to 4 or 8, respectively, in the corresponding request packet. There are no output

disable or write masking capabilities within the data packet.

When the burst length of 8 is selected, the first 8 bytes in the packet correspond to the column address contained in the request packet, and the second 8 bytes correspond to the same column address except with an inverted LSB (i.e. the burst 'wraps').

**Figure 6**  
**DATA PACKET DEFINITION (FOR BURST LENGTH = 4)**

DQ17	DQ16	DQ15	DQ14	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Byte 0								Byte 1									
Byte 2								Byte 3									
Byte 4								Byte 5									
Byte 6								Byte 7									

**Figure 7**  
**DATA PACKET DEFINITION (FOR BURST LENGTH = 8)**

DQ17	DQ16	DQ15	DQ14	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Byte 0								Byte 1									
Byte 2								Byte 3									
Byte 4								Byte 5									
Byte 6								Byte 7									
Byte 8								Byte 9									
Byte 10								Byte 11									
Byte 12								Byte 13									
Byte 14								Byte 15									

Truth Table 1 - Commands

CMD5	CMD4	CMD3	Command	CMD2	CMD1	CMD0	Subcommand
0	0	0		0	0	0	Read Access, Leave Row Open, Drive DCLK0
0	0	0		0	0	1	Read Access, Leave Row Open, Drive DCLK1
0	0	0		0	1	0	Read Access, Close Row, Drive DCLK0
0	0	0	Page Access, Burst of 4	0	1	1	Read Access, Close Row, Drive DCLK1
0	0	0		1	0	0	Write Access, Leave Row Open, Use DCLK0
0	0	0		1	0	1	Write Access, Leave Row Open, Use DCLK1
0	0	0		1	1	0	Write Access, Close Row, Use DCLK0
0	0	0		1	1	1	Write Access, Close Row, Use DCLK1
0	0	1		0	0	0	Read Access, Leave Row Open, Drive DCLK0
0	0	1		0	0	1	Read Access, Leave Row Open, Drive DCLK1
0	0	1		0	1	0	Read Access, Close Row, Drive DCLK0
0	0	1	Page Access, Burst of 8	0	1	1	Read Access, Close Row, Drive DCLK1
0	0	1		1	0	0	Write Access, Leave Row Open, Use DCLK0
0	0	1		1	0	1	Write Access, Leave Row Open, Use DCLK1
0	0	1		1	1	0	Write Access, Close Row, Use DCLK0
0	0	1		1	1	1	Write Access, Close Row, Use DCLK1
0	1	0		0	0	0	Read Access, Leave Row Open, Drive DCLK0
0	1	0		0	0	1	Read Access, Leave Row Open, Drive DCLK1
0	1	0		0	1	0	Read Access, Close Row, Drive DCLK0
0	1	0	Bank Access, Burst of 4	0	1	1	Read Access, Close Row, Drive DCLK1
0	1	0		1	0	0	Write Access, Leave Row Open, Use DCLK0
0	1	0		1	0	1	Write Access, Leave Row Open, Use DCLK1
0	1	0		1	1	0	Write Access, Close Row, Use DCLK0
0	1	0		1	1	1	Write Access, Close Row, Use DCLK1
0	1	1		0	0	0	Read Access, Leave Row Open, Drive DCLK0
0	1	1		0	0	1	Read Access, Leave Row Open, Drive DCLK1
0	1	1		0	1	0	Read Access, Close Row, Drive DCLK0
0	1	1	Bank Access, Burst of 8	0	1	1	Read Access, Close Row, Drive DCLK1
0	1	1		1	0	0	Write Access, Leave Row Open, Use DCLK0
0	1	1		1	0	1	Write Access, Leave Row Open, Use DCLK1
0	1	1		1	1	0	Write Access, Close Row, Use DCLK0
0	1	1		1	1	1	Write Access, Close Row, Use DCLK1
1	0	0		0	0	0	Reserved
1	0	0		0	0	1	Open Row
1	0	0	Register	0	1	0	Close Row
1	0	0	Access,	0	1	1	Register Write
1	0	0	Row Op,	1	0	0	Register Read, Use DCLK0
1	0	0	or Event	1	0	1	Register Read, Use DCLK1
1	0	0		1	1	0	Reserved
1	0	0		1	1	1	Event
1	0	1		0	0	0	Read Sync (Drive both DCLKs)
1	0	1		0	0	1	Stop Read Sync
1	0	1		0	1	0	Drive DCLKs LOW
1	0	1	Data	0	1	1	Drive DCLKs HIGH
1	0	1	Sync	1	0	0	Reserved
1	0	1		1	0	1	Reserved
1	0	1		1	1	0	Disable DCLKs
1	0	1		1	1	1	Drive DCLKs Toggling
1	1	0	Reserved	x	x	x	NOP (See Note)
1	1	1	Reserved	x	x	x	Reserved

Note: Reserved for buffer-only commands; must be treated as NOP by SLDRAMs.

*Index Range	Description
0 - 15	Defined Events - See Event Truth Table
16 - 63	Reserved
64 - 127	Vendor Dependent

\* Index = value of E6-E0 in Event Request Packet

**Figure 8**  
**Event Index Codes**

**Truth Table 2 - Events**

E6-E3	E2	E1	E0	Event
0	0	0	0	Set ID Register to 255, SUB-ID to 15, reset device
0	0	0	1	Reset device, except ID and SUB-ID Registers
0	0	1	0	Autorefresh
0	0	1	1	Close all rows
0	1	0	0	Enter Self Refresh
0	1	0	1	Exit Self Refresh
0	1	1	0	Adjust Settings
0	1	1	1	Reserved

Truth Table 3 - Adjust Settings

ADJ4	ADJ3	ADJ2	ADJ1	ADJ0	ADJUSTMENT
0	0	0	0	0	No Adjustment
0	0	0	0	1	Decrement Data Offset Vernier (move DQs sooner in time relative to DCLK0)
0	0	0	1	0	Increment Data Offset Vernier (move DQs later in time relative to DCLK0)
0	0	0	1	1	Reset Data Offset Vernier to Zero
0	0	1	0	0	Reserved
0	0	1	0	1	Decrement Fine Read Vernier for DQs and DCLK0
0	0	1	1	0	Increment Fine Read Vernier for DQs and DCLK0
0	0	1	1	1	Reset Fine Read Vernier for DQs and DCLK0 to Zero
0	1	0	0	0	Reserved
0	1	0	0	1	Decrement Fine Read Vernier for DCLK1
0	1	0	1	0	Increment Fine Read Vernier for DCLK1
0	1	0	1	1	Reset Fine Read Vernier for DCLK1 to Zero
0	1	1	0	0	Reserved
0	1	1	0	1	Decrement VOH Level
0	1	1	1	0	Increment VOH Level
0	1	1	1	1	Reset VOH to center of range
1	0	0	0	0	Reserved
1	0	0	0	1	Decrement VOL Level
1	0	0	1	0	Increment VOL Level
1	0	0	1	1	Reset VOL to center of range
1	0	1	0	0	Reserved
1	0	1	0	1	Reserved
1	0	1	1	0	Reserved
1	0	1	1	1	Reserved
1	1	0	0	0	Reserved
1	1	0	0	1	Reserved
1	1	0	1	0	Reserved
1	1	0	1	1	Reserved
1	1	1	0	0	Reserved
1	1	1	0	1	Reserved
1	1	1	1	0	Reserved
1	1	1	1	1	Reserved

## Command Descriptions

Truth Table 1 provides a quick reference of available commands. Detailed descriptions are provided in the following sections. All command packets must start on a positive edge of CCLK (with CCLK in this context being specific, not generic).

### NO OPERATION (NOP)

FLAG HIGH indicates the start of a valid request packet; FLAG then goes LOW for the remainder of the packet. FLAG LOW at any other time results in a NO OPERATION (NOP). A NOP prevents unwanted commands from being registered during idle states. NOPs do not affect operations already in progress.

### OPEN ROW

The OPEN ROW command is used to open (or activate) a row in a particular bank in preparation for a subsequent, but separate, column access command. The row remains open (or active) for accesses until a CLOSE ROW command or an access-and-close-row type command is issued to that bank. After an OPEN ROW command is issued to a given bank, a CLOSE ROW command or an access-and-close-row type command must be issued to that bank before a different row in that same bank can be opened.

The OPEN ROW command may be useful when a page access is anticipated, but the column address is not yet known, or when splitting a bank access into two components will facilitate scheduling.

### CLOSE ROW

The CLOSE ROW command is used to close a row in a specific bank.

The CLOSE ROW command is used when it is desired to close a row that was previously left open in anticipation of subsequent page accesses.

### READ

Page Read commands and Bank Read commands are used to initiate a read access to an open row, or to a closed row, respectively. The commands indicate the burst length, the selected DCLK, and whether to leave the row open after the access. Read data appears on the DQs subject to the corresponding Read Delay Register value and Fine Read Vernier and Data Offset Vernier settings previously programmed into the device.

### WRITE

Page Write commands and Bank Write commands are used to initiate a write access to an open row, or to a closed row, respectively. The commands indicate the burst length, the selected DCLK, and whether to leave the row open after

the access. Write data is expected on the DQs at a time determined by the corresponding Write Delay Register value previously programmed into the device.

### REGISTER READ

Used to read the contents of the device status registers. The register data is available on the DQs after the delay determined by the Page Read Delay Register value and the Fine Read Vernier and Data Offset Vernier settings previously programmed into the device.

### REGISTER WRITE

Used to write to the control registers of the device. The register data is included within the request packet containing the command.

### EVENT

Used to issue commands not requiring a specific address within a device or devices.

**Hard Reset** - Sets ID register to 255, SUB-ID register to 15, and resets device, except VOH/VOL levels.

**Soft Reset** - Resets device, except ID and SUB-ID registers and VOH/VOL levels.

**Autorefresh** - Performs a refresh operation to the row or group of rows addressed by the internal refresh counter. All banks must be idle prior to performing an autorefresh event. The same adjustments that are possible with an Adjust Settings event may also be performed during an Autorefresh event

**Close All Rows** - Closes any open rows in any banks.

**Enter Self Refresh** - Causes the device to enter the Self Refresh mode of operation.

**Exit Self Refresh** - Causes the device to exit the Self Refresh mode of operation.

**Adjust Settings** - Used to adjust the Data Offset Vernier, Fine Read Verniers, VOH levels, and VOL levels.

### READ SYNC (STOP READ SYNC)

Instructs the SLDRAM to start (stop) transmitting the specified synchronization pattern to be used by the controller to adjust input capture timing.

### DRIVE DCLKs LOW (HIGH)

Instructs the SLDRAM to drive the DCLK outputs LOW (HIGH) until overridden by another DRIVE DCLK or READ

command. DCLK is specific in this context; the DCLK# outputs will be in the opposite state.

#### DRIVE DCLKs TOGGLING

Instructs the SLDRAM to drive the DCLK outputs toggling at the operating frequency of the device (i.e. DCLKn and DCLKn# will cross every tCK/2 ns) until overridden by another DRIVE DCLK or READ command.

#### DISABLE DCLKs

Instructs the SLDRAM to disable (High-Z) the DCLK/DCLK# outputs until overridden by another DRIVE DCLK or READ command.

### Register Definition

The SLDRAM includes two sets of registers, the control registers and the status registers. The control registers are

write-only registers which are logically 20-bits wide. Physically, all control registers are currently 8-bits or less, so the remaining bits are 'don't care' to the SLDRAM. However, to allow for future revision, the controller should write a 0 to each 'don't care' bit. Data to be written to a control register is provided via the Command/Address bus as part of the Register Write Packet.

The status registers are read-only registers which are logically 72-bits wide. Physically, all status registers are currently 32-bits, so the remaining bits are driven LOW during status register reads. Data being read from a status register is provided in a burst of 4, after a delay equal to the Actual Page Read Delay previously programmed into the device.

REG3	REG2	REG1	REG0	CONTROL REGISTER	STATUS REGISTER
0	0	0	0	ID	Configuration
0	0	0	1	SUB-ID	Actual Delays
0	0	1	0	Operating Frequency	Minimum Delays
0	0	1	1	Test	Maximum Delays
0	1	0	0	Page Read Delay	Test
0	1	0	1	Page Write Delay	tRAS/tRP
0	1	1	0	Bank Read Delay	tRC1/tRC2
0	1	1	1	Bank Write Delay	tRRD/tXSR
1	0	0	0	Reserved	tWR/tWRD
1	0	0	1	Reserved	tPR/tBR
1	0	1	0	Reserved	tPW/tBW
1	0	1	1	Reserved	Reserved
1	1	0	0	Reserved	Reserved
1	1	0	1	Reserved	Reserved
1	1	1	0	Reserved	Reserved
1	1	1	1	Reserved	Reserved

**Figure 9**  
**REGISTER NAMES AND ADDRESSES**



**CONTROL REGISTERS**

**ID Register**

The ID Register consists of eight bits which are all set to 1 (= ID value 255) upon hardware reset, and are subsequently programmed to a unique value during initialization. Each SLDRAM monitors the Command/Address Bus for the start of a request packet, and then performs a comparison between the ID contained in the request packet and the one contained in its internal ID Register. If there is a match within a given SLDRAM, this device will process the request packet. The 9th ID bit in the request packet allows for an SLDRAM to be accessed either individually or as part of a group (multicast or broadcast). For Register Write and Event Request Packets, the SUB-ID value must also be a match (individual, multicast, or broadcast) to select a given SLDRAM. Refer to Appendix I in this data sheet for specific multicast/broadcast address allocation.

The ID Register is programmed using one of the Write ID Register Request packets shown below. The first shows the specific form of the packet used during initialization; the second shows the general form of the packet.

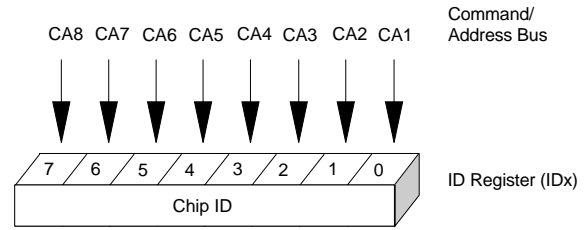
CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	x	1	1	1	1
0	0	0	0	0	0	0	0	0	0
0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0

**Figure 10**  
**REGISTER WRITE REQUEST PACKET - ID REGISTER (during initialization)**

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	0	1	1	SID4	SID3	SID2	SID1	SID0
0	0	0	0	0	0	0	0	0	0
0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0

Note: The first ID is the old ID, used to select the device. The second ID (bottom) is the new ID being written.

**Figure 10A**  
**REGISTER WRITE REQUEST PACKET - ID REGISTER (after initialization)**



Note: ID8 is not stored in the SLDRAM

**Figure 11**  
**ID REGISTER DEFINITION**

**SUB-ID Register**

The SUB-ID Register consists of four bits which are all set to 1 (= ID value 15) upon hardware reset, and are subsequently programmed to a unique value (for a given ID value) during initialization. For Register Write and Event Requests, SLDRAMs with an ID that matches that in the request packet will perform a comparison between the SUB-ID also contained in the request packet and the one contained in its internal SUB-ID Register. If there is a match within a given SLDRAM, this device will process the request packet. The 5th SUB-ID bit in the request packet allows for an SLDRAM to be accessed either individually or as part of a group (multicast or broadcast). Refer to Appendix I in this data sheet for specific multicast/broadcast address allocation.

The SUB-ID Register is programmed using one of the Write SUB-ID Register Request packets shown below. The first shows the specific form of the packet used during initialization; the second shows the general form of the packet.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
x	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	0	1	1	x	1	1	1	1
0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	SID3	SID2	SID1	SID0

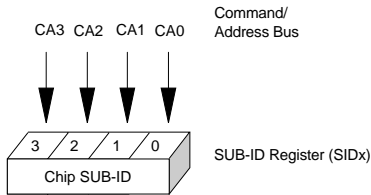
**Figure 12**  
**REGISTER WRITE REQUEST PACKET - SUB-ID REGISTER (during initialization)**

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	0	1	1	SID4	SID3	SID2	SID1	SID0
0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	SID3	SID2	SID1	SID0

Note: The first SUB-ID is the old SUB-ID, used to select the device. The second SUB-ID (bottom) is the new SUB-ID being written.

Figure 12A

REGISTER WRITE REQUEST PACKET - SUB-ID REGISTER (after initialization)



Note: SID4 is not stored in the SLDRAM

Figure 13

SUB-ID REGISTER DEFINITION

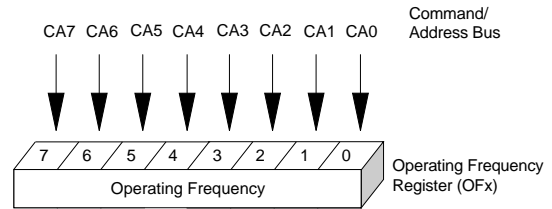
Operating Frequency Register

Future SLDRAM devices will be capable of operating at more than one distinct clock frequency (e.g. 200, 300 or 400 MHz clock frequencies, resulting in 400, 600 or 800 Mb/s per pin data rate, respectively). The desired frequency, of those available, is selected via the Operating Frequency Register, as shown below. This is shown for future planning; for the devices covered by this data sheet, the value written to this register must be 0000000010 (bits 9-0, respectively).

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	0	1	1	SID4	SID3	SID2	SID1	SID0
0	0	0	0	0	1	0	0	0	0
0	0	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0

Figure 14

REGISTER WRITE REQUEST PACKET - OPERATING FREQUENCY REGISTER



Note: One, and only one, bit must be set to 1, and the corresponding operating frequency must be valid for a given device.

OFx:	Clock Frequency/ (data rate per pin)
7 6 5 4 3 2 1 0	
0 0 0 0 0 0 0 1	100 MHz/(200 Mb/s/p)
0 0 0 0 0 0 1 0	200 MHz/(400 Mb/s/p)
0 0 0 0 0 1 0 0	300 MHz/(600 Mb/s/p)
0 0 0 0 1 0 0 0	400 MHz/(800 Mb/s/p)
0 0 0 1 0 0 0 0	500 MHz/(1 Gb/s/p)
0 0 1 0 0 0 0 0	600 MHz/(1.2 Gb/s/p)
All others	Reserved or Illegal

Figure 15

OPERATING FREQUENCY REGISTER/ BIT DEFINITION

Test Register

This register is for vendor specific device testing and should not be written to during normal device operation.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	0	1	1	SID4	SID3	SID2	SID1	SID0
0	0	0	0	0	1	1	0	0	0
T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

Figure 16

REGISTER WRITE REQUEST PACKET - TEST REGISTER

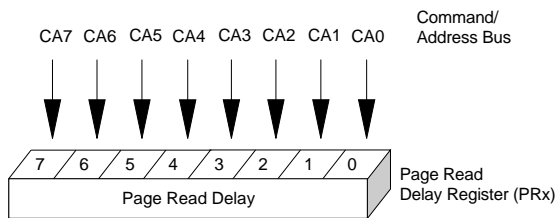
**Page Read Delay Register**

The Page Read Delay Register is used to program the number of integer clock ticks (a.k.a. half cycles, or bit times) between receiving a Page Read Request Packet and providing the corresponding Read Data output. Although the 8-bit register can support a range of 0 to 255 clock ticks, the value programmed must be between the minimum and maximum values as provided in the respective status registers. Different values may be programmed in different SLDRAMs on the same channel in order to compensate for differences in internal SLDRAM and external routing delays.

The value written to this register may subsequently be modified by Increment/Decrement Fine Read Vernier events. Such modifications are reflected in the Actual Delays Status Register.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	0	1	1	SID4	SID3	SID2	SID1	SID0
0	0	0	0	1	0	0	0	0	0
0	0	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0

**Figure 17**  
**REGISTER WRITE REQUEST PACKET -**  
**PAGE READ DELAY REGISTER**



PRx:	
7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

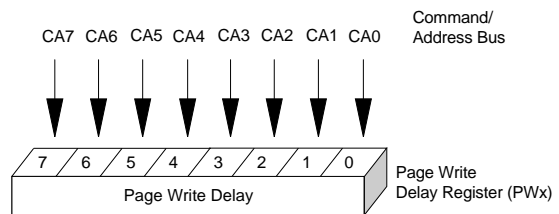
**Figure 18**  
**PAGE READ DELAY REGISTER/BIT**  
**DEFINITION**

**Page Write Delay Register**

The Page Write Delay Register is used to program the number of integer clock ticks (a.k.a. half cycles, or bit times) between receiving a Page Write Request Packet and receiving the corresponding Write Data input. Although the 8-bit register can support a range of 0 to 255 clock ticks, the value programmed must be between the minimum and maximum values as provided in the respective status registers. It is expected, though not required, that the same value would be programmed in all SLDRAMs on a channel. The specific value, from the range of allowable values, can be chosen to achieve the optimum relationship between read latency and write latency.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	0	1	1	SID4	SID3	SID2	SID1	SID0
0	0	0	0	1	0	1	0	0	0
0	0	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0

**Figure 19**  
**REGISTER WRITE REQUEST PACKET -**  
**PAGE WRITE DELAY REGISTER**



PWx:	
7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

**Figure 20**  
**PAGE WRITE DELAY REGISTER/BIT**  
**DEFINITION**

**Bank Read Delay Register**

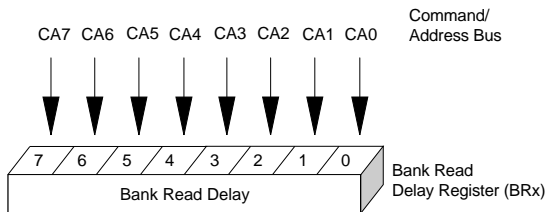
The Bank Read Delay Register is used to program the number of integer clock ticks (a.k.a. half cycles, or bit times) between receiving a Bank Read Request Packet and providing the corresponding Read Data output. Although the 8-bit register can support a range of 0 to 255 clock ticks, the value programmed must be between the minimum and maximum values as provided in the respective status registers. Different values may be programmed in different SLDRAMs on the same channel in order to compensate for differences in internal SLDRAM and external routing delays.

The value written to this register may subsequently be modified by Increment/Decrement Fine Read Vernier events. Such modifications are reflected in the Actual Delays Status Register.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	0	1	1	SID4	SID3	SID2	SID1	SID0
0	0	0	0	1	1	0	0	0	0
0	0	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0

**Figure 21**

**REGISTER WRITE REQUEST PACKET - BANK READ DELAY REGISTER**



BRx:	
7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

**Figure 22**

**BANK READ DELAY REGISTER/BIT DEFINITION**

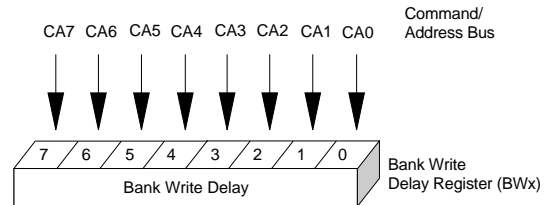
**Bank Write Delay Register**

The Bank Write Delay Register is used to program the number of integer clock ticks (a.k.a. half cycles, or bit times) between receiving a Bank Write Request Packet and receiving the corresponding Write Data input. Although the 8-bit register can support a range of 0 to 255 clock ticks, the value programmed must be between the minimum and maximum values as provided in the respective status registers. It is expected, though not required, that the same value would be programmed in all SLDRAMs on a channel. The specific value, from the range of allowable values, can be chosen to achieve the optimum relationship between read latency and write latency.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	0	1	1	SID4	SID3	SID2	SID1	SID0
0	0	0	0	1	1	1	0	0	0
0	0	BW7	BW6	BW5	BW4	BW3	BW2	BW1	BW0

**Figure 23**

**REGISTER WRITE REQUEST PACKET - BANK WRITE DELAY REGISTER**



BWx:	
7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

**Figure 24**

**BANK WRITE DELAY REGISTER/BIT DEFINITION**

No. of Columns per Row				No. of DQs				No. of Banks				No. of Rows per Bank				Res.	Res.	600 MHz	500 MHz	400 MHz	300 MHz	200 MHz	100 MHz	Data Offset	Manufacturer Code									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
C3	C2	C1	C0	D3	D2	D1	D0	B3	B2	B1	B0	R3	R2	R1	R0	0	0	F5	F4	F3	F2	F1	F0	DO0	M6	M5	M4	M3	M2	M1	M0			

**Figure 25  
CONFIGURATION REGISTER**

**STATUS REGISTERS**

**Configuration Register**

The Configuration Register contains a code which uniquely identifies the memory device vendor, the valid operating frequencies for the device, the number of banks in the device, the number of rows per bank, the number of columns per page and the number of DQs on the device.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

Note: CMD0 is either 0 or 1, to select the appropriate DCLK

**Figure 26  
REGISTER READ REQUEST PACKET -  
CONFIGURATION REGISTER**

DQ17-8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
0	DO0	M6	M5	M4	M3	M2	M1	M0
0	0	0	F5	F4	F3	F2	F1	F0
0	B3	B2	B1	B0	R3	R2	R1	R0
0	C3	C2	C1	C0	D3	D2	D1	D0

**Figure 27  
REGISTER READ DATA PACKET -  
CONFIGURATION REGISTER**

**Configuration Register - Data Offset Bit**

The DO0 bit indicates whether the SLDRAM supports bit level data offset. If DO0 = 0, the device supports word-wide offset only. If DO0 = 1, the device supports both word-wide and bit level offset.

**Configuration Register - Manufacturer Field**

This field contains a code which uniquely identifies the memory device vendor.

Mx:	Manufacturer
6 5 4 3 2 1 0	Fujitsu
0 0 0 0 0 0 0	Hitachi
0 0 0 0 0 0 1	Hyundai
0 0 0 0 0 1 1	IBM
0 0 0 0 1 0 0	LG Semicon
0 0 0 0 1 0 1	Micron
0 0 0 0 1 1 0	Mitsubishi
0 0 0 0 1 1 1	Mosel Vitelic
0 0 0 1 0 0 0	Motorola
0 0 0 1 0 0 1	National/Panasonic
0 0 0 1 0 1 0	NEC
0 0 0 1 0 1 1	Nippon Steel
0 0 0 1 1 0 0	OKI
0 0 0 1 1 0 1	Samsung
0 0 0 1 1 1 0	Siemens
0 0 0 1 1 1 1	Texas Instruments
0 0 1 0 0 0 0	Toshiba
0 0 1 0 0 0 1	Vanguard
0 0 1 0 0 1 0	Reserved
:	:
1 1 1 1 1 1 1	Reserved

**Figure 28  
CONFIGURATION REGISTER -MANUFAC-  
TURER FIELD DEFINITION**

**Configuration Register - Frequency Field**

This field indicates the valid operating frequencies for the device. Each defined bit corresponds to a specific operating frequency. At least one bit, and possibly more than one bit will be 1, indicating that the device supports that operating frequency. A 0 is provided on each reserved bit location as well as the bit locations for each operating frequency not supported. This is shown for future planning; for the devices covered by this data sheet, the value read from this field will be 000010 (bits F5-F0, respectively), indicating 200 MHz (or 400 Mb/s/p) operation.

F5	F4	F3	F2	F1	F0
600 MHz	500 MHz	400 MHz	300 MHz	200 MHz	100 MHz

**Figure 29**  
**CONFIGURATION REGISTER -  
FREQUENCY FIELD DEFINITION**

**Configuration Register - Bank Field**

This field indicates the number of banks in the device.

B3	B2	B1	B0	No. of Banks
0	0	0	0	Reserved (1)
0	0	0	1	Reserved (2)
0	0	1	0	Reserved (4)
0	0	1	1	8
0	1	0	0	16
0	1	0	1	Reserved (32)
0	1	1	0	Reserved (64)
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

**Figure 30**  
**CONFIGURATION REGISTER -  
BANK FIELD DEFINITION**

**Configuration Register - Row Field**

This field indicates the number of rows per bank.

R3	R2	R1	R0	No. of Rows per Bank
0	0	0	0	Reserved
0	0	0	1	Reserved (512)
0	0	1	0	1K
0	0	1	1	2K
0	1	0	0	4K
0	1	0	1	Reserved (8K)
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

**Figure 31**  
**CONFIGURATION REGISTER -  
ROW FIELD DEFINITION**



**Configuration Register - Column Field**

This field indicates the number of columns per row.

C3	C2	C1	C0	No. of Columns per Row
0	0	0	0	Reserved
0	0	0	1	16
0	0	1	0	32
0	0	1	1	64
0	1	0	0	128
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

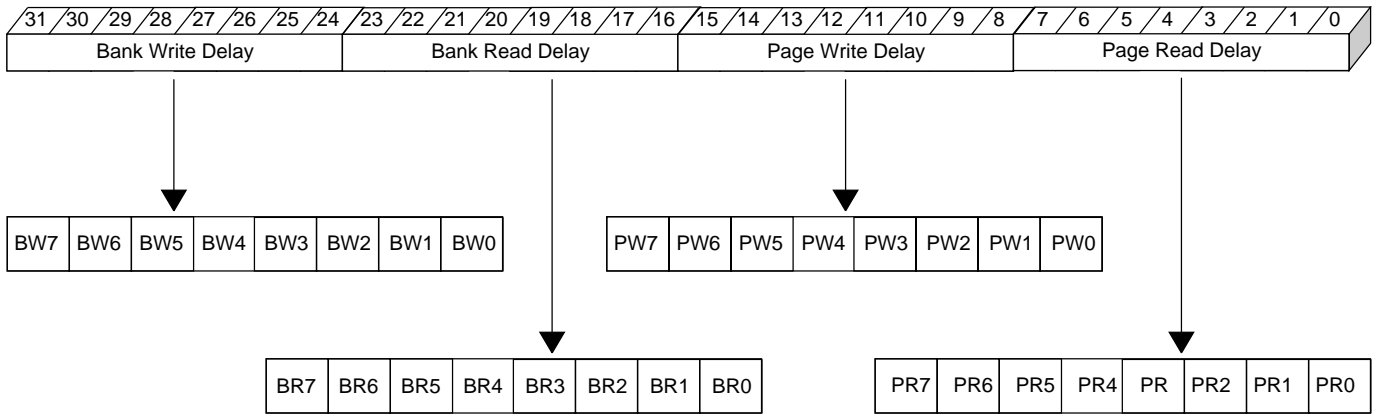
**Figure 32**  
**CONFIGURATION REGISTER -**  
**COLUMN FIELD DEFINITION**

**Configuration Register - DQ Field**

This field indicates the number of DQs per device.

D3	D2	D1	D0	No. of DQs
0	0	0	0	Reserved (4)
0	0	0	1	8
0	0	1	0	Reserved (9)
0	0	1	1	16
0	1	0	0	18
0	1	0	1	32
0	1	1	0	Reserved (36)
0	1	1	1	64
1	0	0	0	Reserved (72)
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

**Figure 33**  
**CONFIGURATION REGISTER -**  
**DQ FIELD DEFINITION**



**Figure 34**  
**ACTUAL DELAY REGISTER FIELDS**

**Actual Delay Register**

This register contains the actual Page Read Delay, Page Write Delay, Bank Read Delay, and Bank Write Delay settings for the device. These values will reflect any subsequent modifications to the initial values; such modifications may result from controller programming of the corresponding Control Registers or from Fine Read Vernier adjustments.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

**Figure 35**  
**REGISTER READ REQUEST PACKET -**  
**ACTUAL DELAY REGISTER**

**Actual Delay Register - Actual Page Read Delay Field**

This register contains the Actual Page Read Delay supported by the device (measured in integer clock ticks between receiving a Page Read Request Packet and providing the corresponding Read Data output, as shown later in this data sheet).

PRx:	
7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

**Figure 37**  
**ACTUAL DELAY REGISTER -**  
**ACTUAL PAGE READ DELAY FIELD**  
**DEFINITION**

DQ17-8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
0	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0
0	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0
0	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
0	BW7	BW6	BW5	BW4	BW3	BW2	BW1	BW0

**Figure 36**  
**REGISTER READ DATA PACKET -**  
**ACTUAL DELAY REGISTER**

**Actual Delay Register - Actual Page Write Delay Field**

This field contains the Actual Page Write Delay supported by the device (measured in integer clock ticks between receiving a Page Write Request Packet and receiving the corresponding Write Data input, as shown later in this data sheet).

PWx:	
7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

**Figure 38**  
**ACTUAL DELAY REGISTER -**  
**ACTUAL PAGE WRITE DELAY FIELD**  
**DEFINITION**

**Actual Delay Register - Actual Bank Write Delay Field**

This register contains the Actual Page Write Delay supported by the device (measured in integer clock ticks between receiving a Page Write Request Packet and receiving the corresponding Write Data input, as shown later in this data sheet).

BWx:	
7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

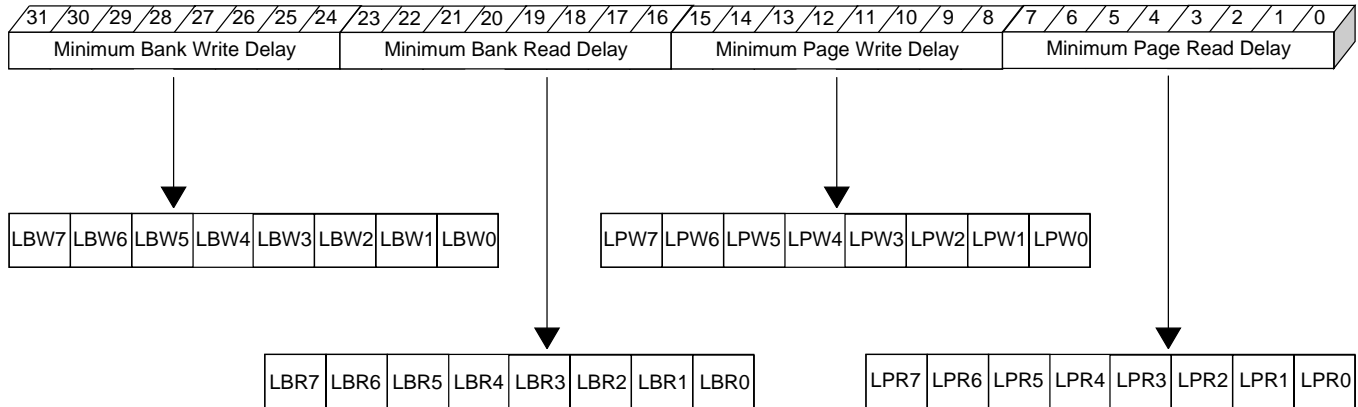
**Figure 40**  
**ACTUAL DELAY REGISTER -**  
**ACTUAL BANK WRITE DELAY FIELD**  
**DEFINITION**

**Actual Delay Register - Actual Bank Read Delay Field**

This register contains the Actual Bank Read Delay supported by the device (measured in integer clock ticks between receiving a Bank Read Request Packet and providing the corresponding Read Data output, as shown later in this data sheet).

BRx:	
7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

**Figure 39**  
**ACTUAL DELAY REGISTER -**  
**ACTUAL BANK READ DELAY FIELD**  
**DEFINITION**



**Figure 41**  
**MINIMUM DELAY REGISTER FIELDS**

**Minimum Delay Register**

This register contains the minimum Page Read Delay, Page Write Delay, Bank Read Delay, and Bank Write Delay settings for the device.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

**Figure 42**  
**REGISTER READ REQUEST PACKET - MINIMUM DELAY REGISTER**

DQ17-8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
0	LPR7	LPR6	LPR5	LPR4	LPR3	LPR2	LPR1	LPR0
0	LPW7	LPW6	LPW5	LPW4	LPW3	LPW2	LPW1	LPW0
0	LBR7	LBR6	LBR5	LBR4	LBR3	LBR2	LBR1	LBR0
0	LBW7	LBW6	LBW5	LBW4	LBW3	LBW2	LBW1	LBW0

**Figure 43**  
**REGISTER READ DATA PACKET - MINIMUM DELAY REGISTER**

The value contained in a particular Minimum Delay Register is the sum of the analog and digital values in the corresponding timing parameter registers, with the analog value having been converted to digital using the minimum CCLK cycle time of the device and rounding up to the next highest integer value. If the device is used at a slower frequency, the controller should compute these values using the timing parameter values and the actual operating frequency, and disregard the values of the Minimum Delay registers.

**Minimum Delay Register - Minimum Page Read Delay Field**

This register contains the minimum Page Read Delay supported by the device (measured in integer clock ticks between receiving a Page Read Request Packet and providing the corresponding Read Data output, as shown later in this data sheet).

LPRx:	Integer Number of Clock Ticks
7 6 5 4 3 2 1 0	
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

**Figure 44**  
**MINIMUM DELAY REGISTER - MINIMUM PAGE READ DELAY FIELD DEFINITION**

**Minimum Delay Register - Minimum Page Write Delay Field**

This register contains the minimum Page Write Delay supported by the device (measured in integer clock ticks between receiving a Page Write Request Packet and receiving the corresponding Write Data input, as shown later in this data sheet).

LPWx:	Integer Number of Clock Ticks
7 6 5 4 3 2 1 0	
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

**Figure 45**  
**MINIMUM DELAY REGISTER -**  
**MINIMUM PAGE WRITE DELAY FIELD**  
**DEFINITION**

**Minimum Delay Register - Minimum Bank Write Delay Field**

This register contains the minimum Page Write Delay supported by the device (measured in integer clock ticks between receiving a Page Write Request Packet and receiving the corresponding Write Data input, as shown later in this data sheet).

LBWx:	Integer Number of Clock Ticks
7 6 5 4 3 2 1 0	
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

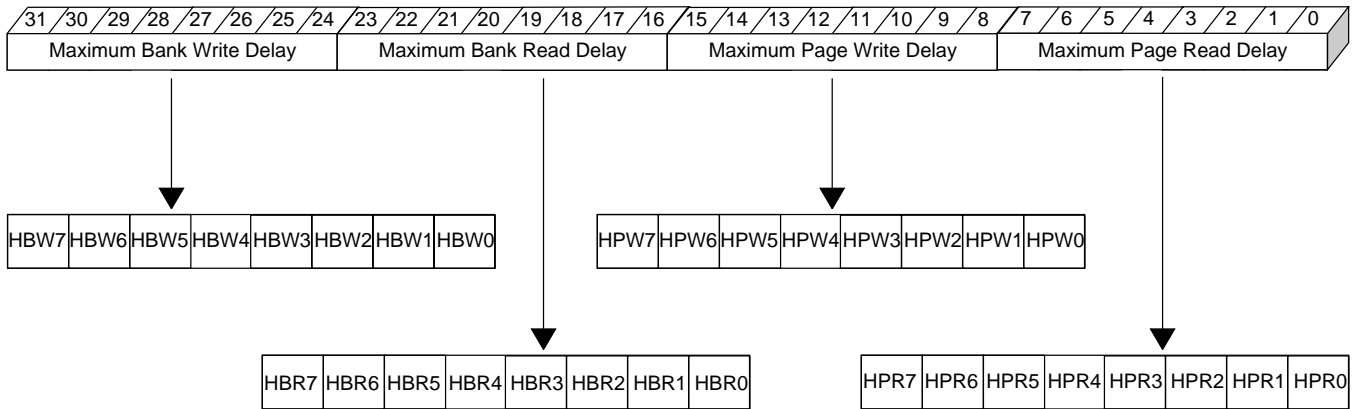
**Figure 47**  
**MINIMUM DELAY REGISTER -**  
**MINIMUM BANK WRITE DELAY FIELD**  
**DEFINITION**

**Minimum Delay Register - Minimum Bank Read Delay Field**

This register contains the minimum Bank Read Delay supported by the device (measured in integer clock ticks between receiving a Bank Read Request Packet and providing the corresponding Read Data output, as shown later in this data sheet).

LBRx:	Integer Number of Clock Ticks
7 6 5 4 3 2 1 0	
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

**Figure 46**  
**MINIMUM DELAY REGISTER -**  
**MINIMUM BANK READ DELAY FIELD**  
**DEFINITION**



**Figure 48**  
**MAXIMUM DELAY REGISTER FIELDS**

**Maximum Delay Register**

This register contains the maximum Page Read Delay, Page Write Delay, Bank Read Delay, and Bank Write Delay settings for the device.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

**Figure 49**  
**REGISTER READ REQUEST PACKET -**  
**MAXIMUM DELAY REGISTER**

DQ17-8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
0	HPR7	HPR6	HPR5	HPR4	HPR3	HPR2	HPR1	HPR0
0	HPW7	HPW6	HPW5	HPW4	HPW3	HPW2	HPW1	HPW0
0	HBR7	HBR6	HBR5	HBR4	HBR3	HBR2	HBR1	HBR0
0	HBW7	HBW6	HBW5	HBW4	HBW3	HBW2	HBW1	HBW0

**Figure 50**  
**REGISTER READ DATA PACKET -**  
**MAXIMUM DELAY REGISTER**

The value contained in a particular Maximum Delay Register is the sum of the analog and digital values in the corresponding timing parameter registers, with the analog value having been converted to digital using the minimum CCLK cycle time of the device and rounding up to the next highest integer value. If the device is used at a slower frequency, the controller should compute these values using the timing parameter values and the actual operating frequency, and disregard the values of the Maximum Delay registers.

**Maximum Delay Register - Minimum Page Read Delay Field**

This register contains the maximum Page Read Delay supported by the device (measured in integer clock ticks between receiving a Page Read Request Packet and providing the corresponding Read Data output, as shown later in this data sheet).

HPRx:	
7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

**Figure 51**  
**MAXIMUM DELAY REGISTER -**  
**MAXIMUM PAGE READ DELAY FIELD**  
**DEFINITION**



**Maximum Delay Register - Maximum Page Write Delay Field**

This register contains the maximum Page Write Delay supported by the device (measured in integer clock ticks between receiving a Page Write Request Packet and receiving the corresponding Write Data input, as shown later in this data sheet).

HPWx:	Integer Number of Clock Ticks
7 6 5 4 3 2 1 0	
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

**Figure 52  
MAXIMUM DELAY REGISTER -  
MAXIMUM PAGE WRITE DELAY FIELD  
DEFINITION**

**Maximum Delay Register - Maximum Bank Write Delay Field**

This register contains the maximum Page Write Delay supported by the device (measured in integer clock ticks between receiving a Page Write Request Packet and receiving the corresponding Write Data input, as shown later in this data sheet).

HBWx:	Integer Number of Clock Ticks
7 6 5 4 3 2 1 0	
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

**Figure 54  
MAXIMUM DELAY REGISTER -  
MAXIMUM BANK WRITE DELAY FIELD  
DEFINITION**

**Maximum Delay Register - Maximum Bank Read Delay Field**

This register contains the maximum Bank Read Delay supported by the device (measured in integer clock ticks between receiving a Bank Read Request Packet and providing the corresponding Read Data output, as shown later in this data sheet).

HBRx:	Integer Number of Clock Ticks
7 6 5 4 3 2 1 0	
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

**Figure 53  
MAXIMUM DELAY REGISTER -  
MAXIMUM BANK READ DELAY FIELD  
DEFINITION**

**Test Register**

This register contains test data meaningful only to the specific device vendor.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

**Figure 55**  
**REGISTER READ REQUEST PACKET -**  
**TEST REGISTER**

**Timing Parameter Registers**

The timing parameter registers contain representations of the corresponding timing parameters included in the device data sheet. The controller can use this information to program optimal timing based on the performance level(s) of the devices actually resident in the system.

Each register contains values for two timing parameters, and there is a digital component and an analog component for each parameter. The general format for data from a timing parameter register read is shown below (Parameter 0 corresponds to the first parameter listed in the register name, e.g. tRAS = Parameter 0 in the tRAS/tRP register).

DQ17-8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
0	PARAMETER 0 DIGITAL VALUE							
0	PARAMETER 0 ANALOG VALUE							
0	PARAMETER 1 DIGITAL VALUE							
0	PARAMETER 1 ANALOG VALUE							

**Figure 56**  
**GENERAL DATA FORMAT -**  
**TIMING PARAMETER REGISTER READ**

The digital component is an integer value (from 0-255) that is independent of operating frequency. The analog value (in ns) is calculated by multiplying the step size represented by A7-A5 (Truth Table 4) by the decimal value represented by A4-A0 (the number of steps).

The total value (analog plus digital) for a given parameter may be obtained, if necessary, by converting the analog value to a digital value (by dividing by the actual CCLK cycle time of the device and rounding up to the next highest integer value) and adding the result to the stored digital value.

DQ17-8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
0	A7	A6	A5	A4	A3	A2	A1	A0

**Figure 57**  
**FORMAT FOR ANALOG VALUE BYTES**  
**WITHIN TIMING REGISTER READ DATA**  
**PACKETS**

A7	A6	A5	STEP SIZE (ns)	RANGE (ns)
0	0	0	8	0-248
0	0	1	4	0-124
0	1	0	2	0-62
0	1	1	1	0-31
1	0	0	0.5	0-15.5
1	0	1	0.25	0-7.75
1	1	0	0.125	0-3.875
1	1	1	0.0625	0-1.9375

**TRUTH TABLE 4 -**  
**ANALOG VALUE STEP SIZES AND**  
**RANGES**

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	0	1
0	1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

**Figure 58**  
**REGISTER READ REQUEST PACKET -**  
**tRAS/tRP**  
**TIMING PARAMETER REGISTER**

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	1	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

**Figure 61**  
**REGISTER READ REQUEST PACKET -**  
**tWR/tWRD**  
**TIMING PARAMETER REGISTER**

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

**Figure 59**  
**REGISTER READ REQUEST PACKET -**  
**tRC1/tRC2**  
**TIMING PARAMETER REGISTER**

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	1	0
0	1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

**Figure 62**  
**REGISTER READ REQUEST PACKET -**  
**tPR/tBR**  
**TIMING PARAMETER REGISTER**

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

**Figure 60**  
**REGISTER READ REQUEST PACKET -**  
**tRRD/tXSR**  
**TIMING PARAMETER REGISTER**

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	1	0
1	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

**Figure 63**  
**REGISTER READ REQUEST PACKET -**  
**tPW/tBW**  
**TIMING PARAMETER REGISTER**

## READ ACCESSES

Read accesses are initiated with a Read request packet, as shown in Figures 68 and 69.

When accessing an idle bank (bank read access), the request packet includes the bank, row, and column addresses, the burst length, and a bit indicating whether or not to close the row after the access. When accessing the open row in an active bank (a page read access), the same is true, except that the row address will be ignored.

During a Read access, the first of four (or eight) data words in the data packet will be available following the total read delay; the remaining three (or seven) data words will follow, one each, every tick (2.5ns) later. The total read delay is equal to the coarse delay (Bank Read Delay or Page Read Delay) stored in the SLDRAM registers plus the fine delays of the Data Offset Vernier and the Fine Read Vernier for DQs and DCLK0.

Figure 68 shows minimum and maximum total read delays for a bank read access, and Figure 69 shows the same for a page read access. For clarity, the DCLK timing is shown only for the minimum read delay data timing.

The selected DCLK signal is driven by the SLDRAM along with the data, but with a leading cycle to allow for internal sampling edge adjustment in the controller.

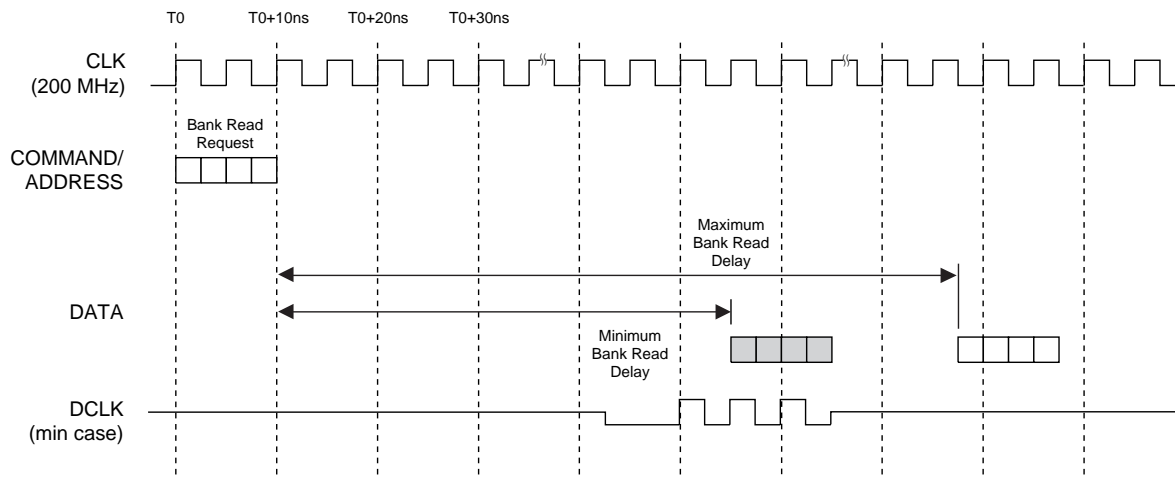
## READ DELAY TIMING

The SLDRAM clocking scheme is designed to provide for the temporal alignment, at the memory controller data pins,

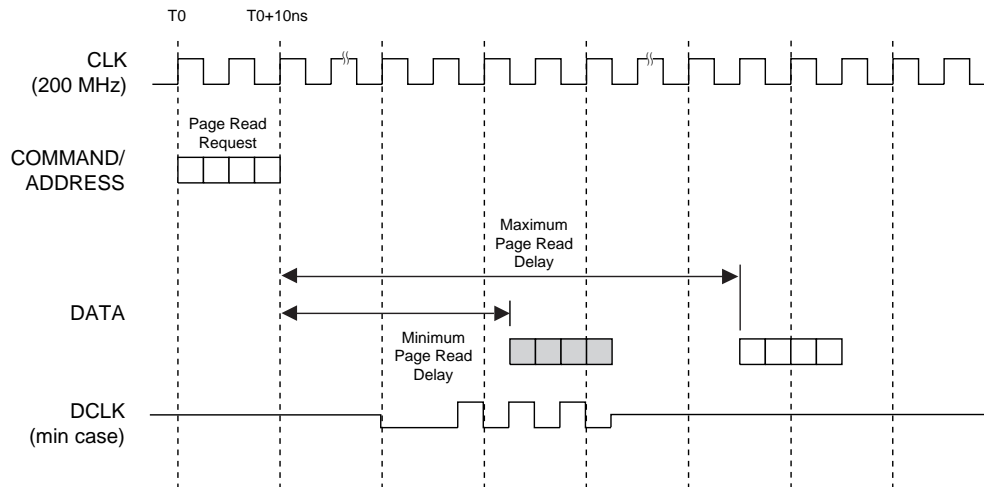
of all read data, regardless of the source SLDRAM. Upon system-power up, the controller will program initial values selected to achieve the preferred timing relationships. It is expected that periodic or continuous observation, combined with calibration as needed, will be performed by the memory controller to maintain the desired timing relationships.

The temporal alignment scheme can be broken down into different levels. At the lowest level (device-level data capture) the DCLK transitions and DQ transitions of an individual SLDRAM are adjusted (moved in time) relative to each other to facilitate the capture (by the controller) of the DQ signals using the DCLK signals. This scheme recognizes that to achieve the desired relationship at the controller inputs might mean starting with a different relationship at the memory outputs, and further, that different such relationships might be necessary for different memory devices on the memory bus. The SLDRAM clocking scheme allows for individual device adjustment, but without requiring the memory controller to implement memory-device-specific internal adjustments. It is expected, though not required, that the desired relationship at the controller is edge-aligned.

At the next level of timing alignment (device-level optimization), the DCLK and DQ transitions are moved (as a group) in time to align the DCLK edges with the preferred phase of an internal controller clock. This phase could be chosen to optimize hand-off of data from the input capture circuitry to the core logic of the controller, and/or to opti-



**Figure 68**  
**BANK READ ACCESS**



**Figure 69**  
**PAGE READ ACCESS**

mize internal read to write turn-around time in the controller. Note that the capture relationship established at the lowest level remains unchanged.

The first two levels of timing alignment are sub-tick level adjustments. At the next level (system-level optimization), coarse (integer tick value) adjustments are made. The objective is to establish the same latency between a read command being issued by the controller and the corresponding data arriving back at the controller for all SLDRAM devices in the system. This scheme allows for different latencies among SLDRAM devices as well as among the logical and electrical paths between the controller and different SLDRAMs.

The sub-tick level adjustments are accomplished using the Data Offset Vernier and the two Fine Read Verniers. The Data Offset Vernier provides adjustment of the temporal placement of data output (DQs) in nominal steps of  $t_{CK}/32$  or less. The DQ adjustments are stated relative to DCLK0, but are effectively relative to the command input and to DCLK1 as well.

When the Data Offset Vernier is incremented beyond the maximum step for a given bit time (e.g. counter value=15), the counter wraps to 0 and the Actual Read Delay registers (Bank and Page) are incremented by 1. Similarly, when this vernier is decremented below the minimum step (counter value=0), the counter wraps to the maximum value, and the Actual Read Delay registers (Bank and Page) are decremented by 1. This change indicates that a fine adjust-

ment has caused the DQs to cross a coarse (integer) tick boundary.

The Actual Read Delay registers will be incremented or decremented no more than once as a result of Data Offset Vernier adjustment commands. If adjustment commands continue to be applied such that a vernier counter boundary is reached a second time, no further adjustment will be made in that direction (such commands will be treated as NOPs). Target systems using an edge-aligned clocking scheme should not require more than  $\pm 1/4$  bit time of adjustment between DQs and DCLKs.

The default or reset value for the Data Offset Vernier is zero, meaning that in this state, the DQs and DCLK0 will appear nominally coincident (with up to the specified skew between them), both subject to the programmed coarse delay.

The Fine Read Vernier for DQs and DCLK0 provides adjustment of the temporal placement of the DQs and DCLK0 as a group (relative to the read command, and with the programmed coarse delay as the base latency). The resolution is the same as for the Data Offset Vernier. When the Fine Read Vernier for DQs and DCLK0 is incremented beyond the maximum step for a given bit time (e.g. counter value=15), the counter wraps to 0 and the Actual Read Delay registers (Bank and Page) are incremented by 1. Similarly, when this vernier is decremented below the minimum step (counter value=0), the counter wraps to the maximum value, and the Actual Read Delay registers (Bank

and Page) are decremented by 1. This change indicates that a fine adjustment has caused the DQs to cross a coarse (integer) tick boundary.

The Actual Read Delay registers may be incremented or decremented more than once as a result of Fine Read Vernier for DQs and DCLK0 adjustment commands, subject to the following limitations. First, the controller must keep track of the Actual Delay Register values (directly or indirectly) and avoid issuing adjustment commands that would cause an Actual Delay Register value to exceed the corresponding Maximum Delay Register or Minimum Delay Register value as a result of the vernier counter wrapping. Second, the controller must ensure that the DQ timing is not adjusted away from DCLK1 timing by more than 1 bit time. This can be accomplished by applying a complementary adjustment command to the Fine Read Vernier for DCLK1 for each adjustment command applied to the Fine Read Vernier for DQs and DCLK0 (if adjustments specific to the Fine Read Vernier for DCLK1 are needed to align DCLK1 with DCLK0 at the controller, these can be made in the next step).

The reset or default value for Fine Read Vernier for DQs and DCLK0 is zero (meaning that in this state, the DCLK0 output timing is determined by the coarse delay settings only, and that the DQ output timing is determined by the coarse delay settings combined with the Data Offset Vernier setting).

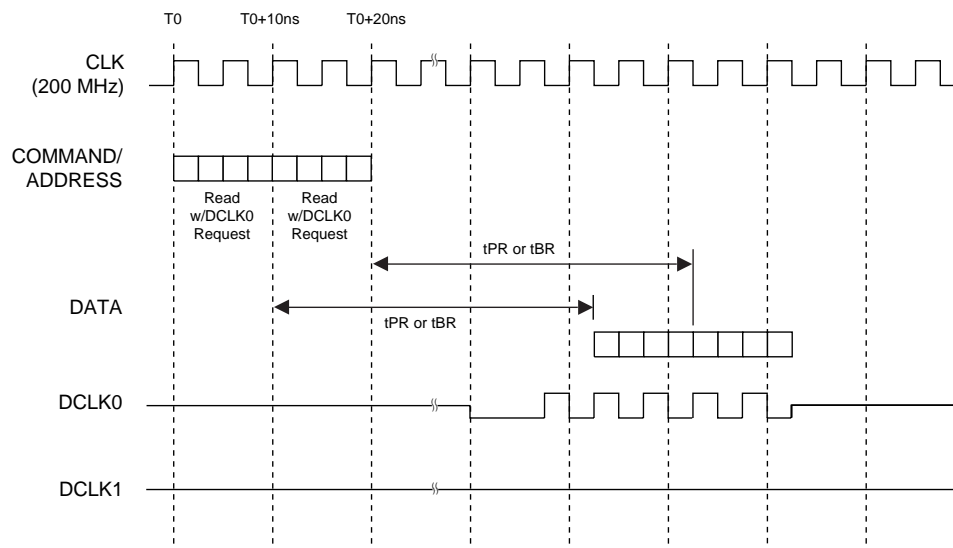
The Fine Read Vernier for DCLK1 provides adjustment of the temporal placement of the DCLK1 output (again relative to the read command, and with the programmed coarse delay as the base latency). Note that adjusting this vernier does not cause a change in read data delay; this vernier is intended for use in aligning DCLK1 with DCLK0 (which in turn would have an established relationship with the DQs and with an internal controller clock phase). DCLK1 timing can be adjusted away from DQ timing by up to 1 bit time. The reset or default value for this vernier is zero (meaning that in this state the DCLK1 output timing is determined by the coarse delay settings only).

The coarse (integer tick value) adjustments are made by writing values to the appropriate Read Delay Registers.

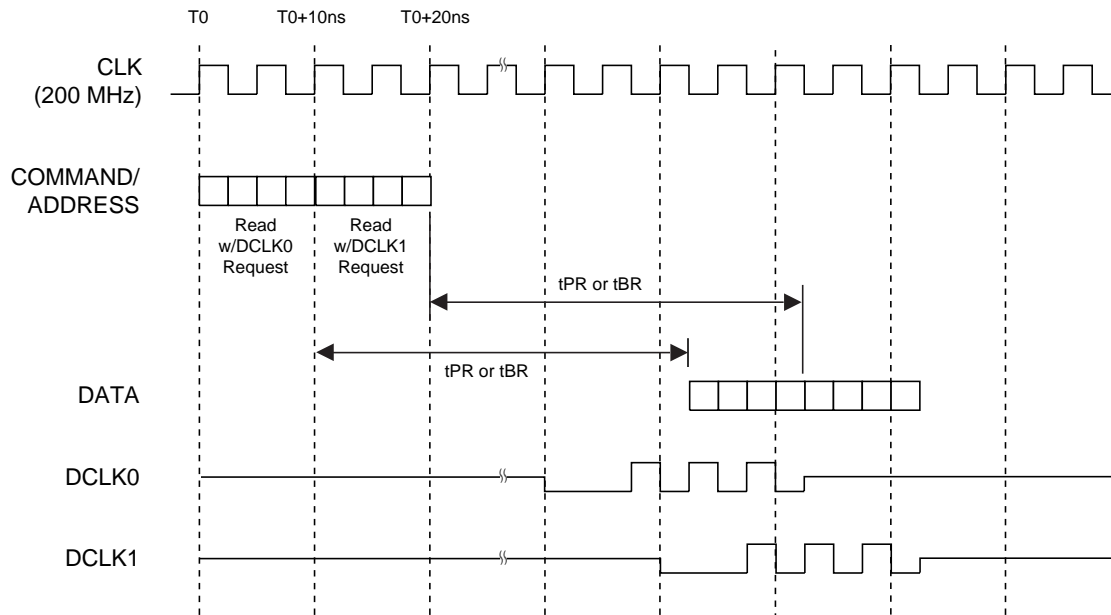
### DUAL DCLK SIGNALS

The two DCLK signals provided by each SLDRAM (as well as the memory controller) provide increased effective bandwidth when switching between different sources of data on the bus (e.g. a read from one SLDRAM followed by a read from another SLDRAM, read-to-write or write-to-read transitions). The preamble and leading cycle in a given DCLK sequence can be hidden (overlapped with data associated with the other DCLK signal).

The following sections describe the DCLK operation for successive reads (both contiguous and non-contiguous) to the same device. Note that although switching between



**Figure 69A**  
**CONTIGUOUS READ REQUESTS USING SAME DCLK**



**Figure 69B**  
**CONTIGUOUS READ REQUESTS USING DIFFERENT DCLKs**

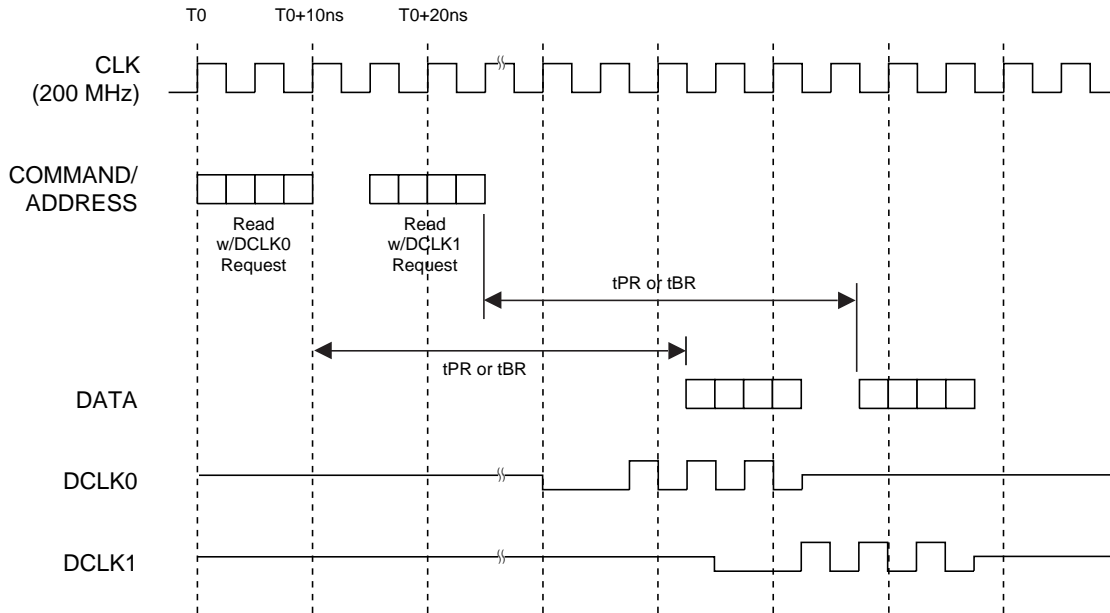
DCLKs for reads was designed for use when switching between devices, switching between DCLKs on the same device is described for completeness.

Contiguous successive reads can be performed to the same device by using either the same DCLK or different DCLKs. When using the same DCLK, the preamble and leading cycle occur only for the first read access (see Figure 69A). When switching between DCLKs, the preamble and leading cycle occur for both accesses, but the data from both accesses appears contiguously (see Figure 69B).

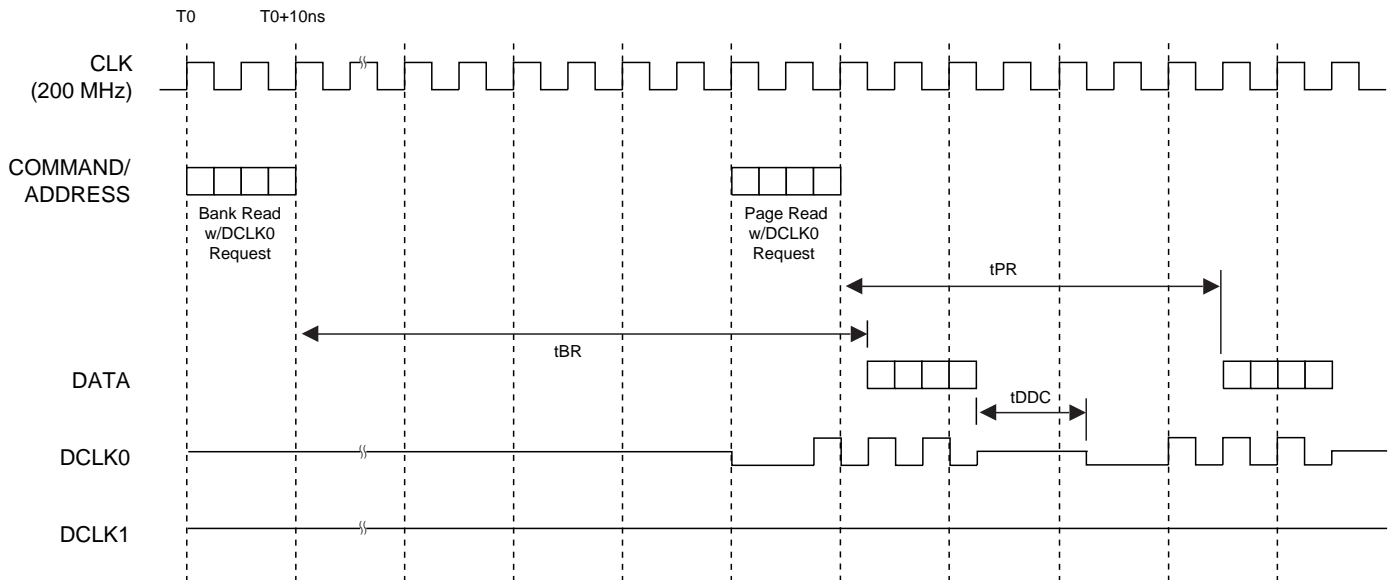
Due to the pipelined nature of memory controllers, it is expected that successive read requests to the same device

would be either contiguous, or spaced more than a few clock cycles apart. However, if for some reason there is a need to issue successive read requests very close together, but not contiguously, this can be achieved by alternating DCLKs. Figure 69C illustrates this operation for the smallest possible non-zero gap between read requests (as determined by the 2n rule). The execution of close, but non-contiguous, successive read requests using the same DCLK is limited by parameter tDDC as shown in Figure 69D (a Page Read Request is shown following a Bank Read Request so that the minimum value for this parameter can be illustrated; the latencies shown are arbitrary).





**Figure 69C**  
**NON-CONTIGUOUS READ REQUESTS USING DIFFERENT DCLKS**



**Figure 69D**  
**NON-CONTIGUOUS READ REQUESTS USING SAME DCLK**

**WRITES**

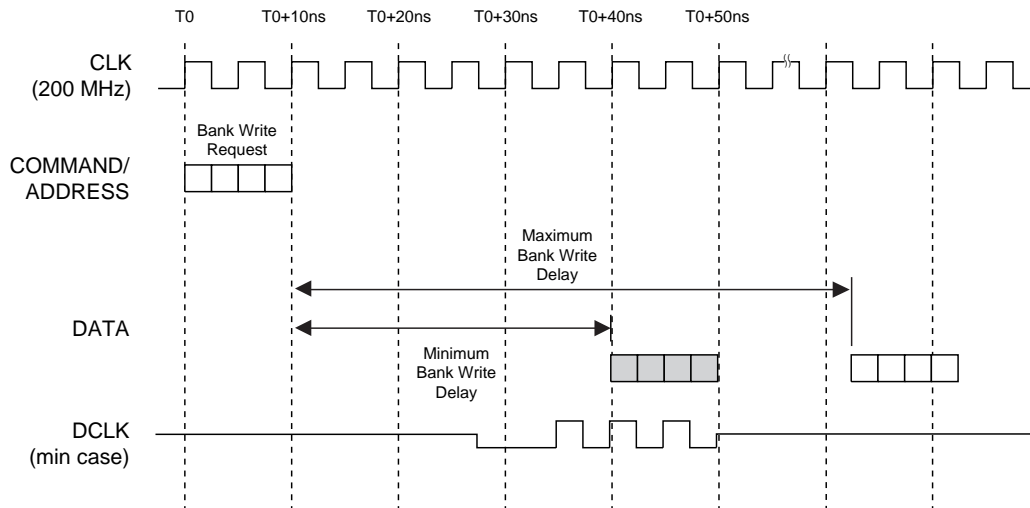
WRITE accesses are initiated with a WRITE packet request, as shown in Figures 70 and 71.

When accessing an idle bank (bank write access), the request packet includes the bank, row, and column addresses, the burst length, and a bit indicating whether or not to close the row after the access. When accessing the open row in an active bank (a page write access), the same is true, except that the row address will be ignored.

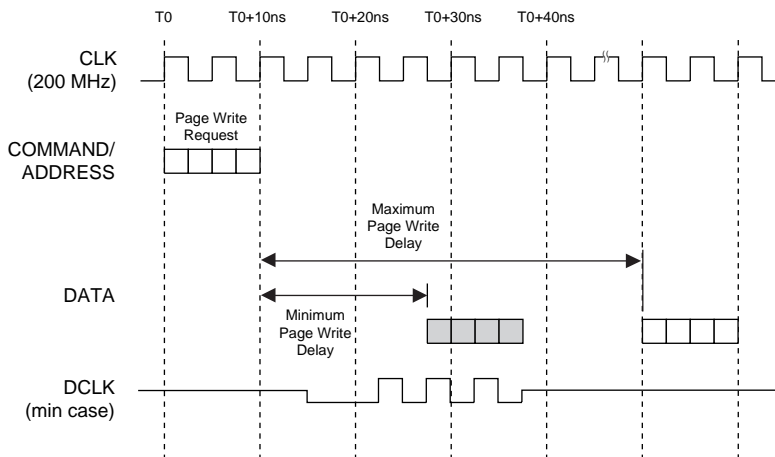
During a WRITE access, the first of four (or eight) data words in the data packet is driven by the controller, aligned with the selected DCLK, and after a delay (Bank Write Delay or Page Write Delay) programmed into the SLDRAM registers. The remaining three (or seven) data words will

follow, one each, every 2.5ns later. Figure 70 shows the minimum and maximum delay before arrival of data at the SLDRAM during a bank write access. Figure 71 shows the same for a page write access. For clarity, the DCLK timing is shown only for the minimum write delay data timing.

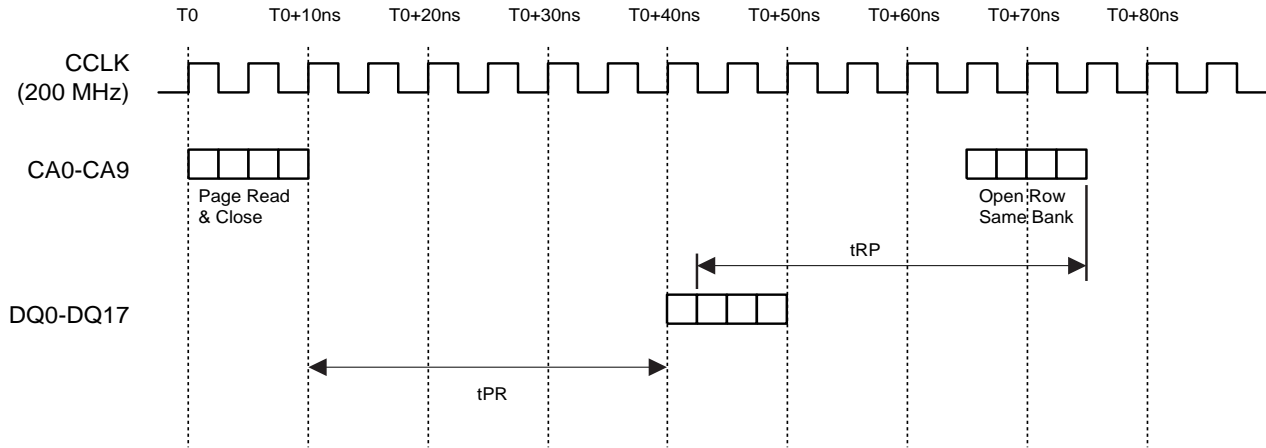
The selected DCLK signal is driven by the controller along with the data, but with a leading cycle to allow for internal sampling edge adjustment in the SLDRAM. The Data and DCLK transitions must be nominally coincident. Although the commands and data travel in the same direction for write accesses there may be routing delay differences between the command bus and data bus. The leading LOW time on the DCLK signal allows for such differences.



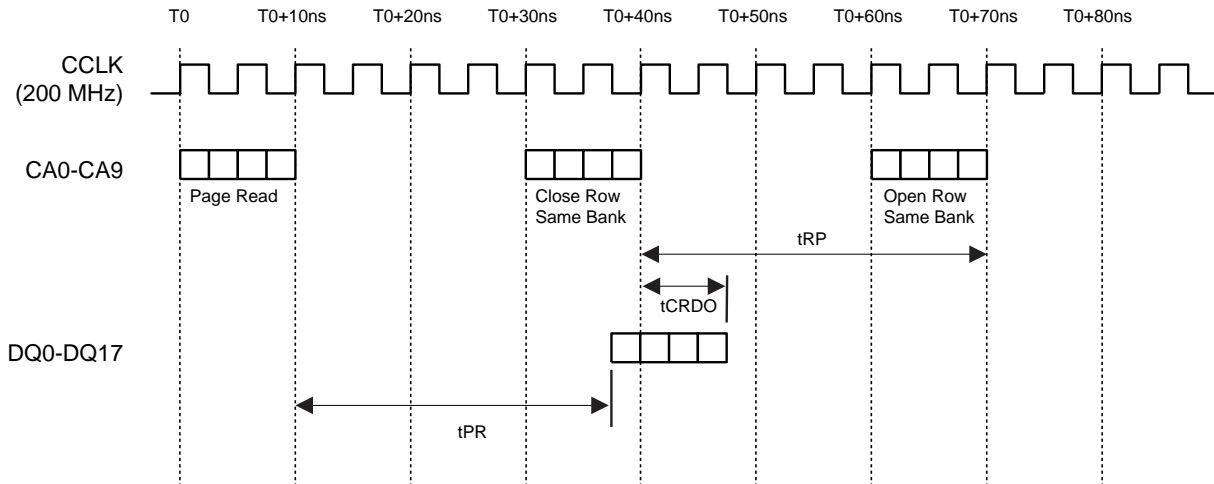
**Figure 70**  
**BANK WRITE ACCESS**



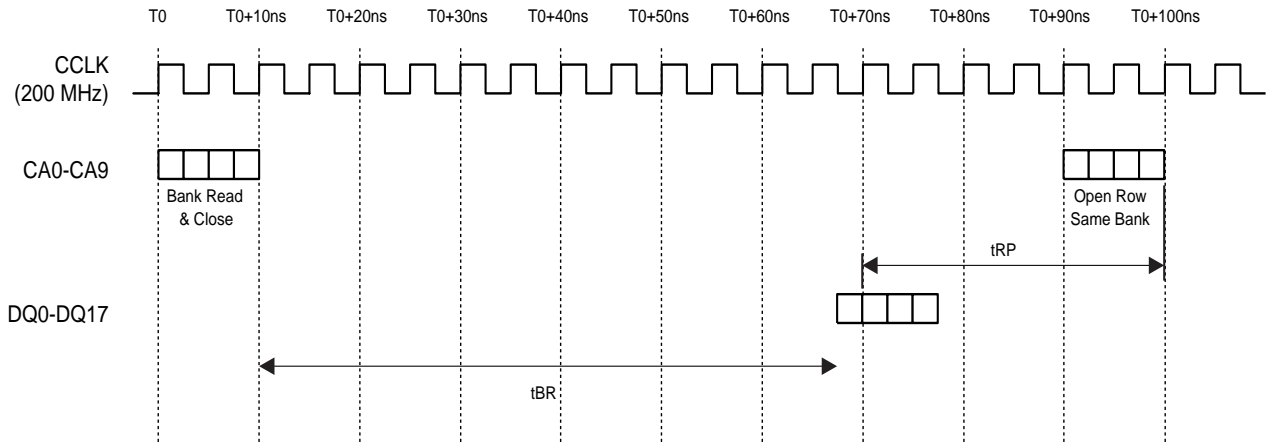
**Figure 71**  
**PAGE WRITE ACCESS**



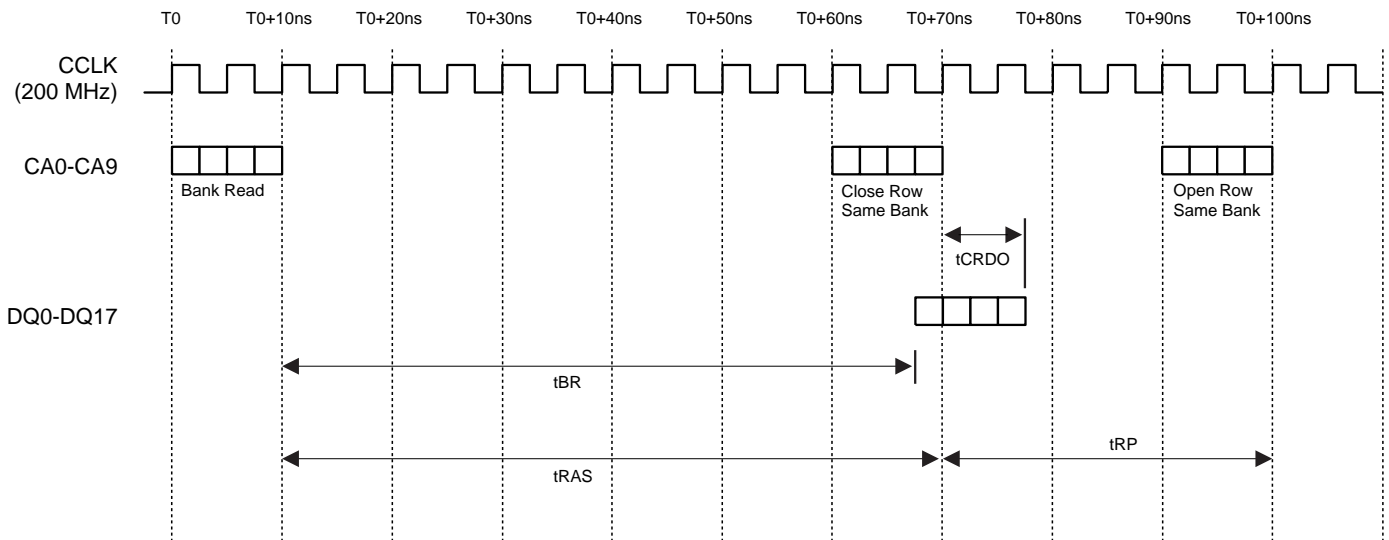
**Figure 72**  
**PAGE READ TIMING PARAMETERS**



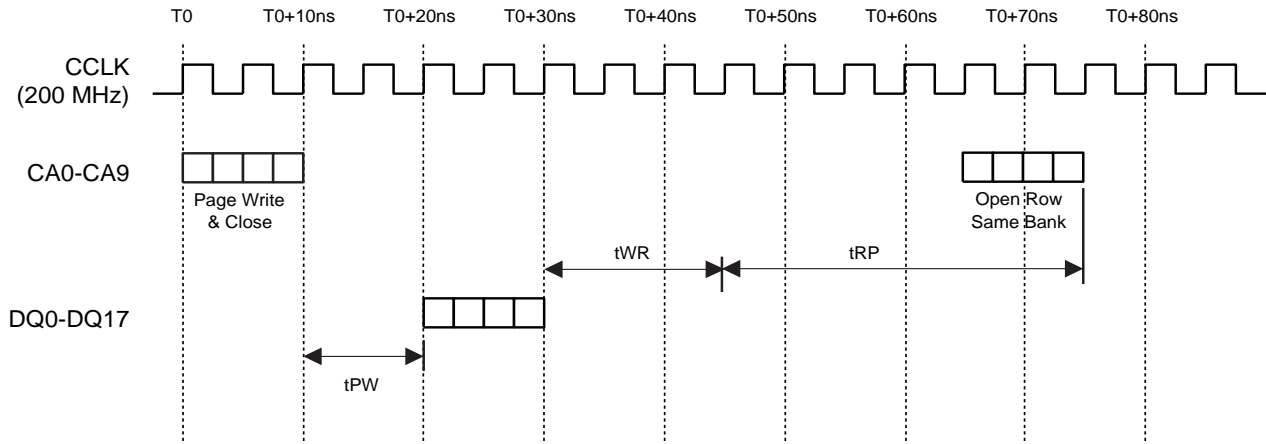
**Figure 72A**  
**PAGE READ TIMING PARAMETERS -**  
**DISCRETE CLOSE ROW COMMAND**



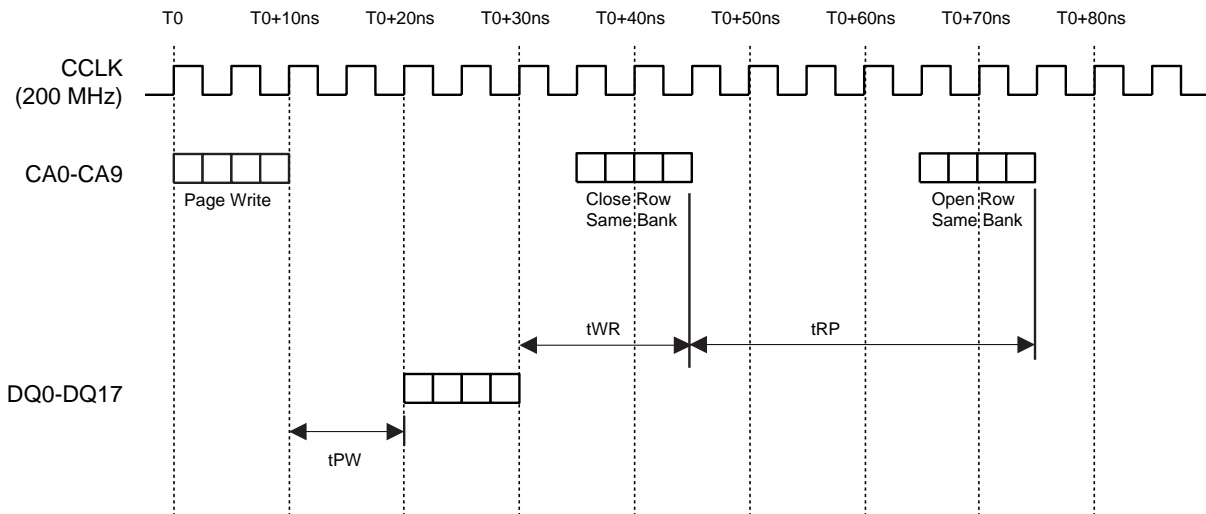
**Figure 73**  
**BANK READ TIMING PARAMETERS**



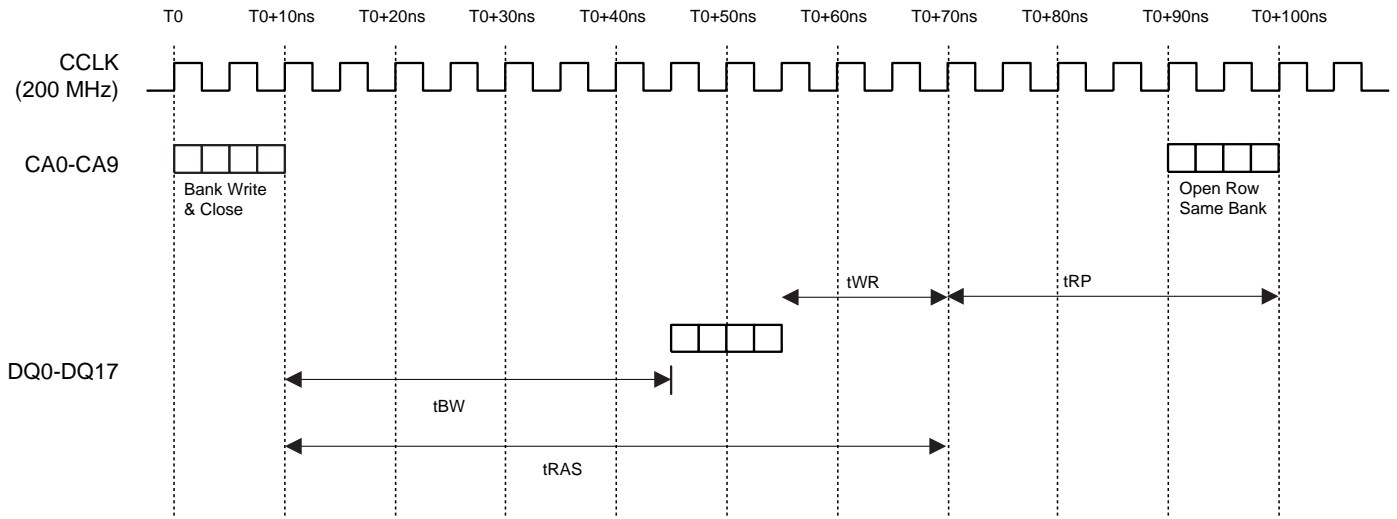
**Figure 73A**  
**BANK READ TIMING PARAMETERS -**  
**DISCRETE CLOSE ROW COMMAND**



**Figure 74**  
**PAGE WRITE TIMING PARAMETERS**

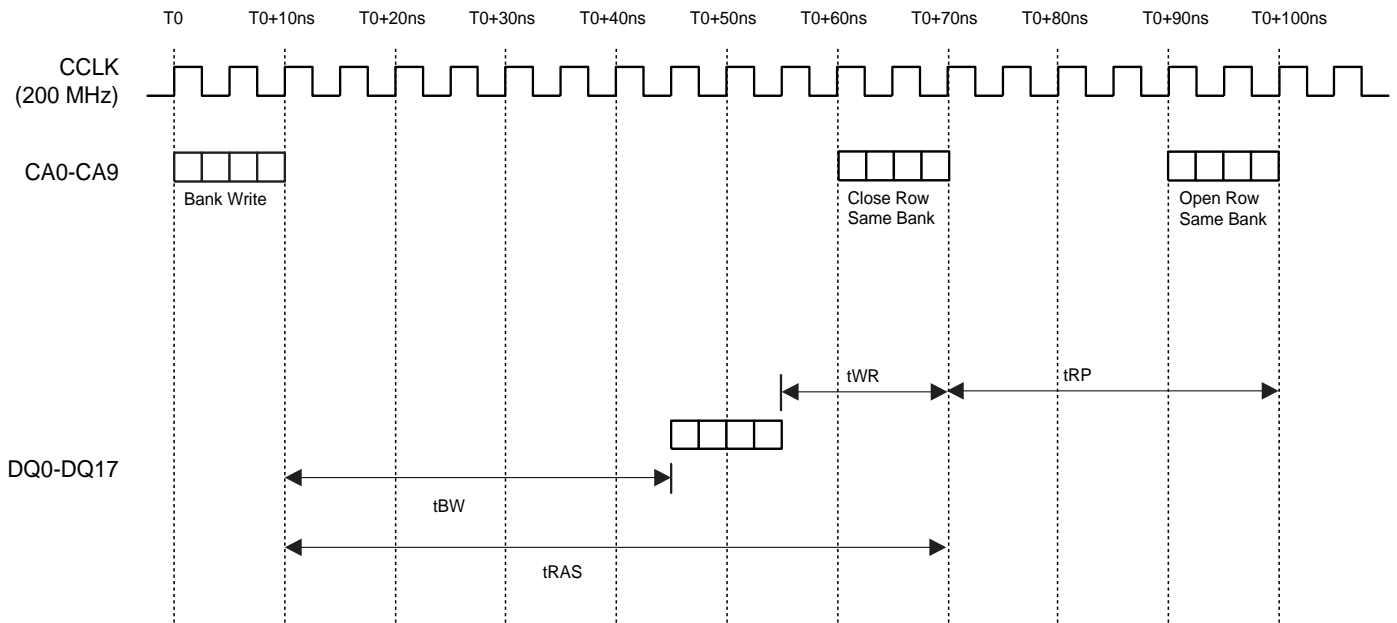


**Figure 74A**  
**PAGE WRITE TIMING PARAMETERS -**  
**DISCRETE CLOSE ROW COMMAND**



Note: the value for tBW must be programmed such that tRAS is met.

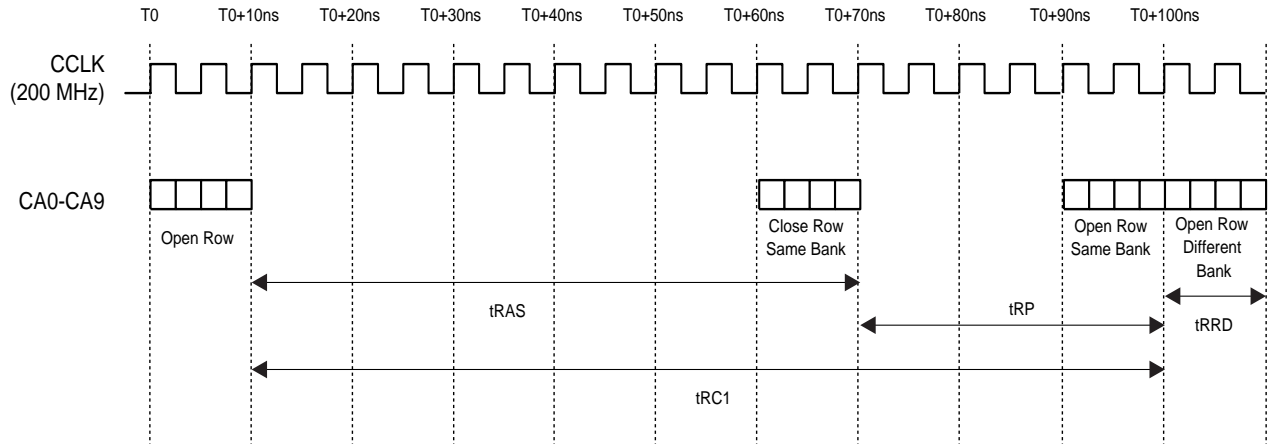
**Figure 75**  
**BANK WRITE TIMING PARAMETERS**



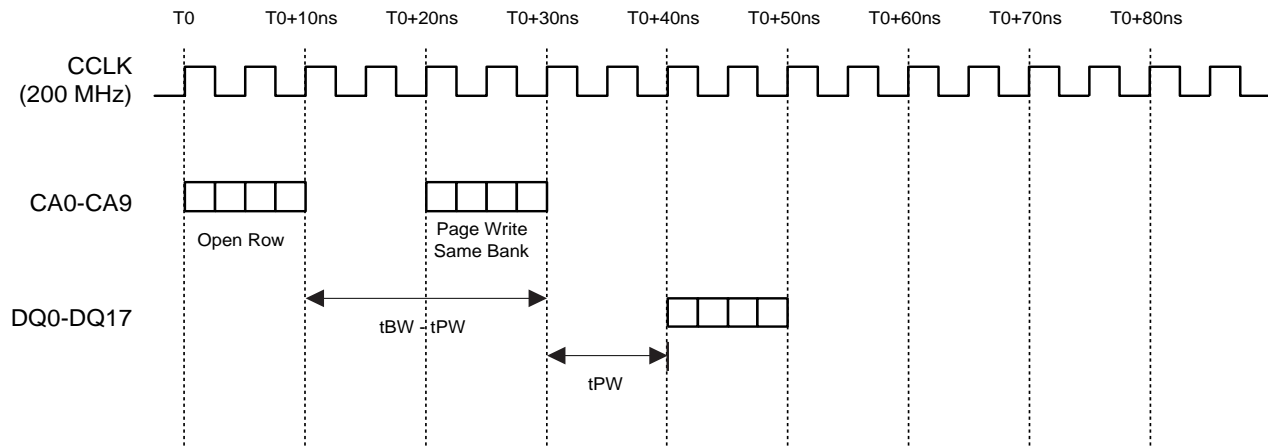
Note: The placement of the Close Row command must meet both tWR and tRAS (i.e. depending on the value programmed for tBW, either of those may be limiting).

**Figure 75A**  
**BANK WRITE TIMING PARAMETERS -**  
**DISCRETE CLOSE ROW COMMAND**

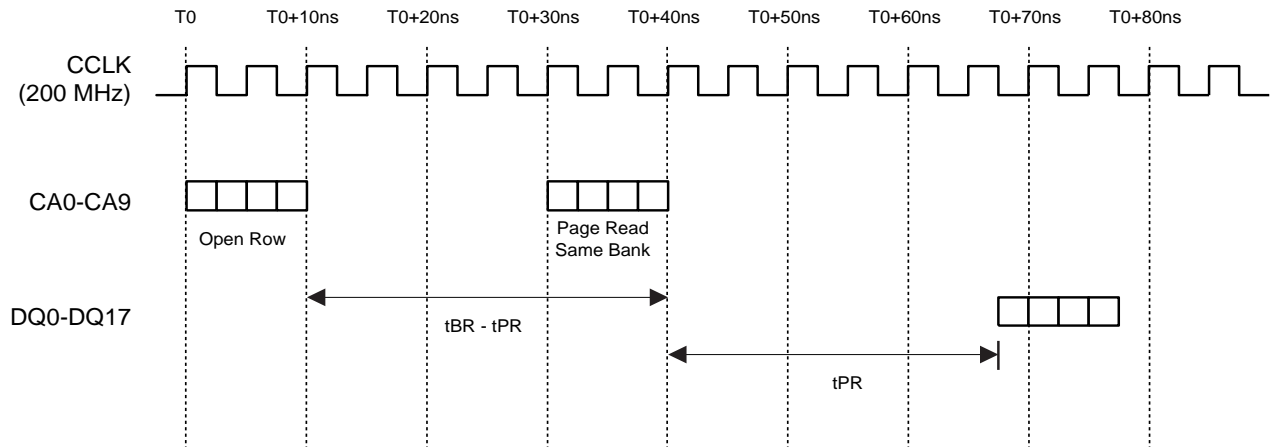




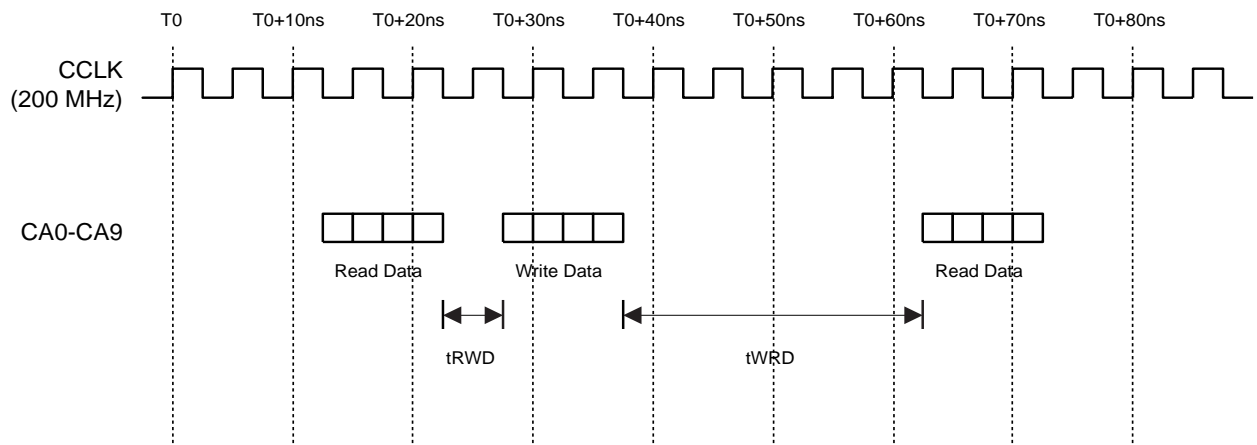
**Figure 76**  
**OPEN/CLOSE ROW TIMING PARAMETERS**



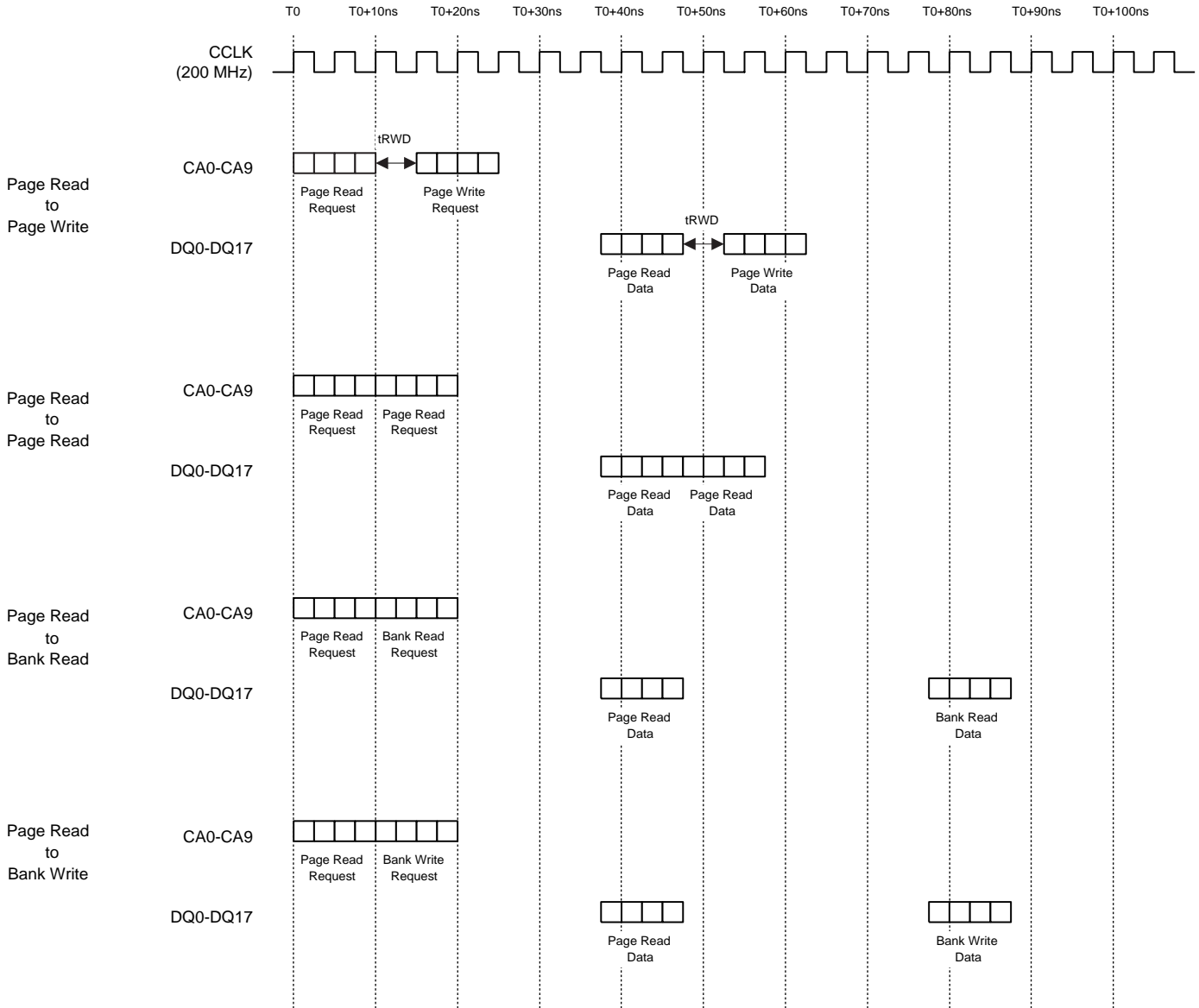
**Figure 77**  
**OPEN ROW TO PAGE WRITE TIMING PARAMETERS**



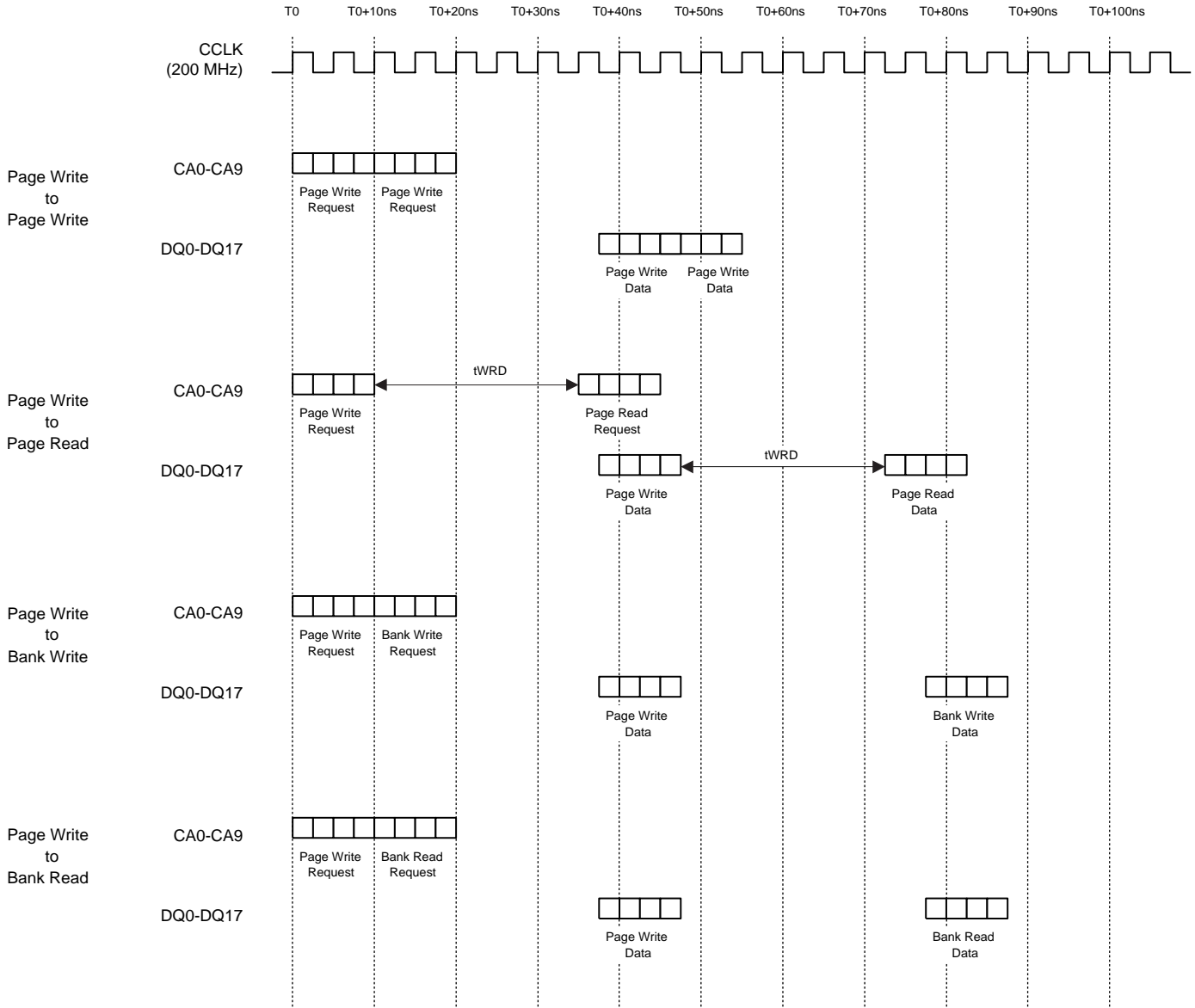
**Figure 78**  
**OPEN ROW TO PAGE READ TIMING PARAMETERS**



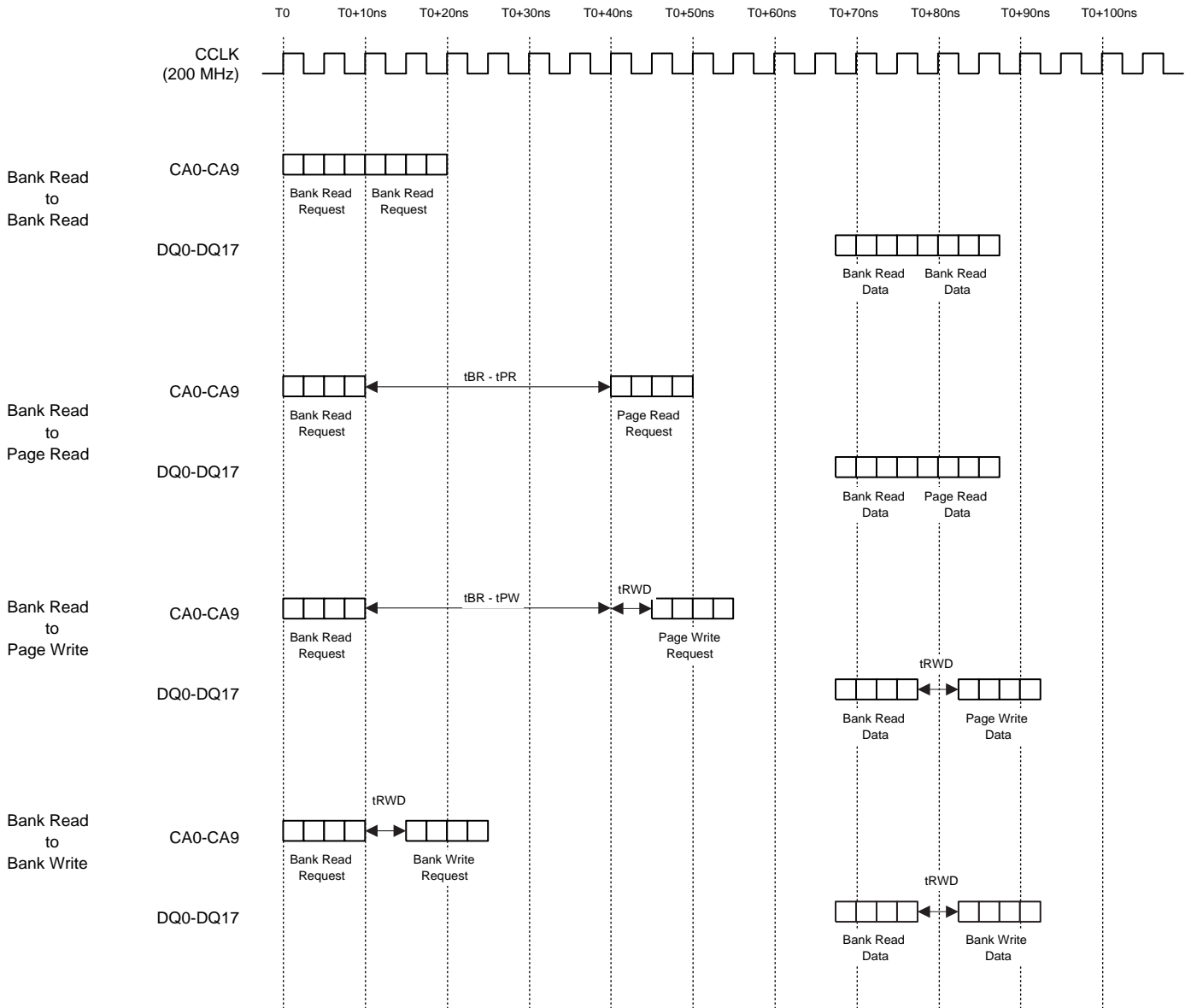
**Figure 79**  
**BUS/PIPE TURNAROUND TIMING PARAMETERS**



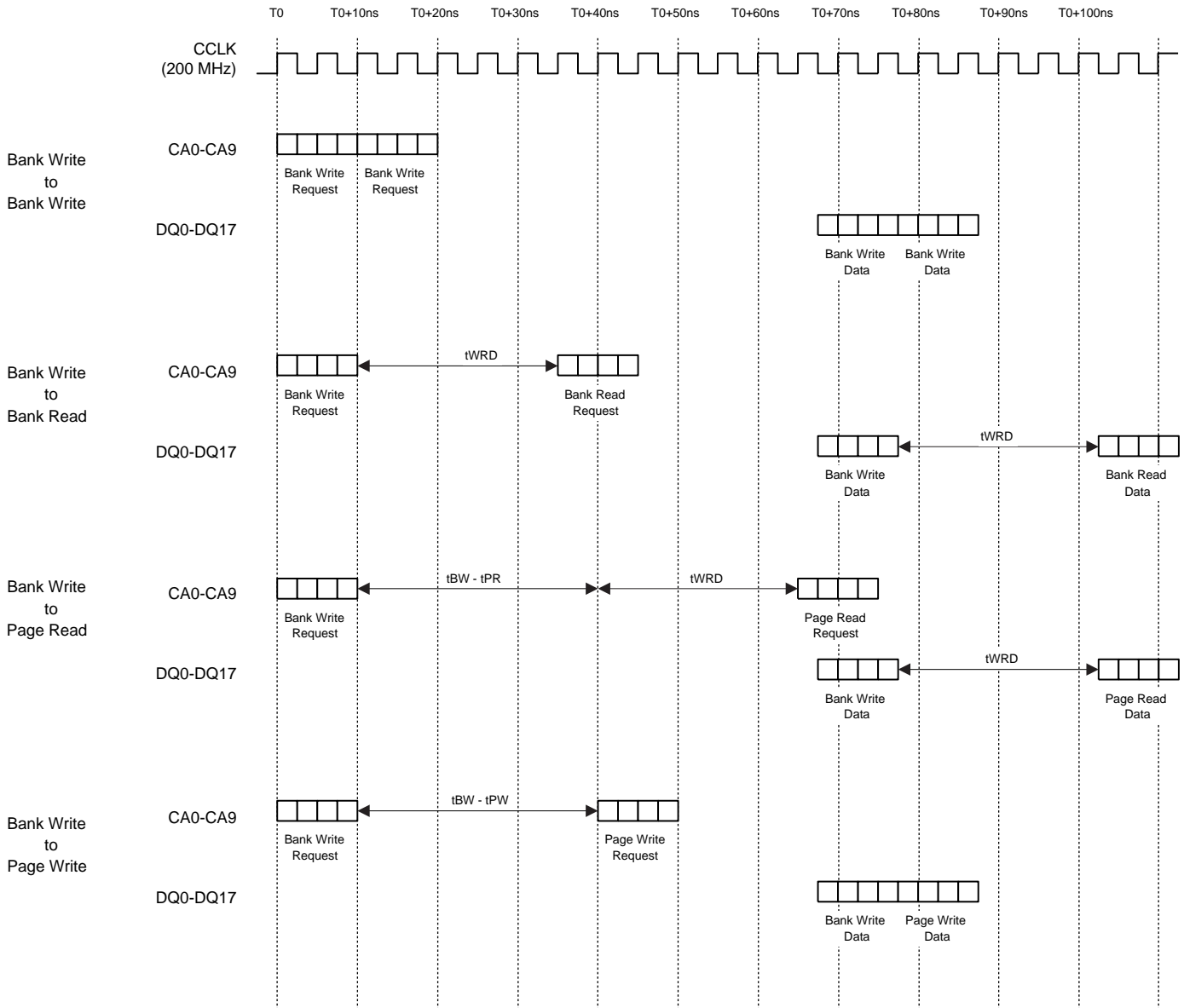
**Figure 80**  
**READ/WRITE COMMAND ISSUE RESTRICTIONS**  
**EXAMPLE 1 - READ LATENCY = MINIMUM,**  
**WRITE LATENCY = READ LATENCY**



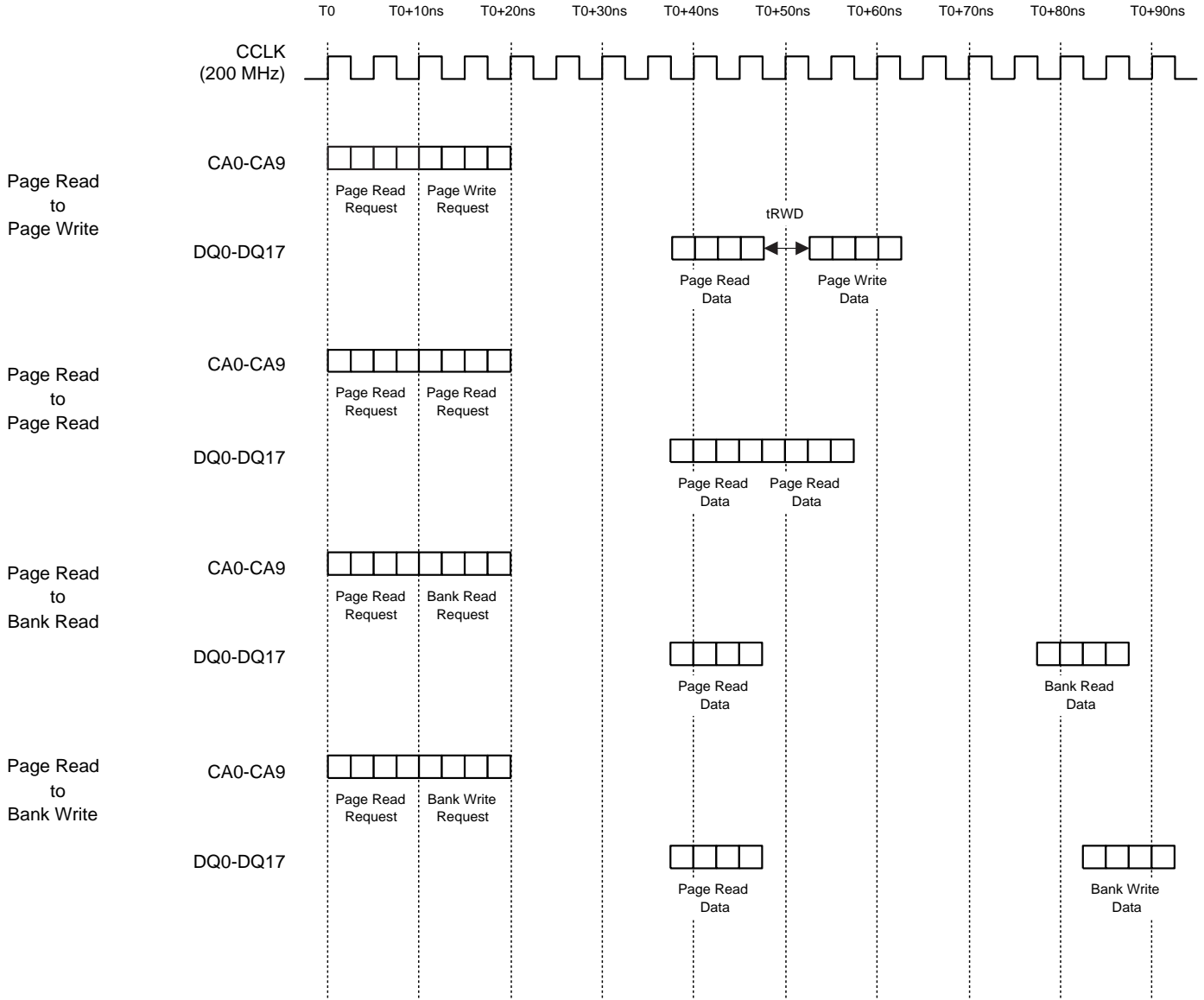
**Figure 81**  
**READ/WRITE COMMAND ISSUE RESTRICTIONS**  
**EXAMPLE 1 - READ LATENCY = MINIMUM,**  
**WRITE LATENCY = READ LATENCY (CONTINUED)**



**Figure 82**  
**READ/WRITE COMMAND ISSUE RESTRICTIONS**  
**EXAMPLE 1 - READ LATENCY = MINIMUM,**  
**WRITE LATENCY = READ LATENCY (CONTINUED)**

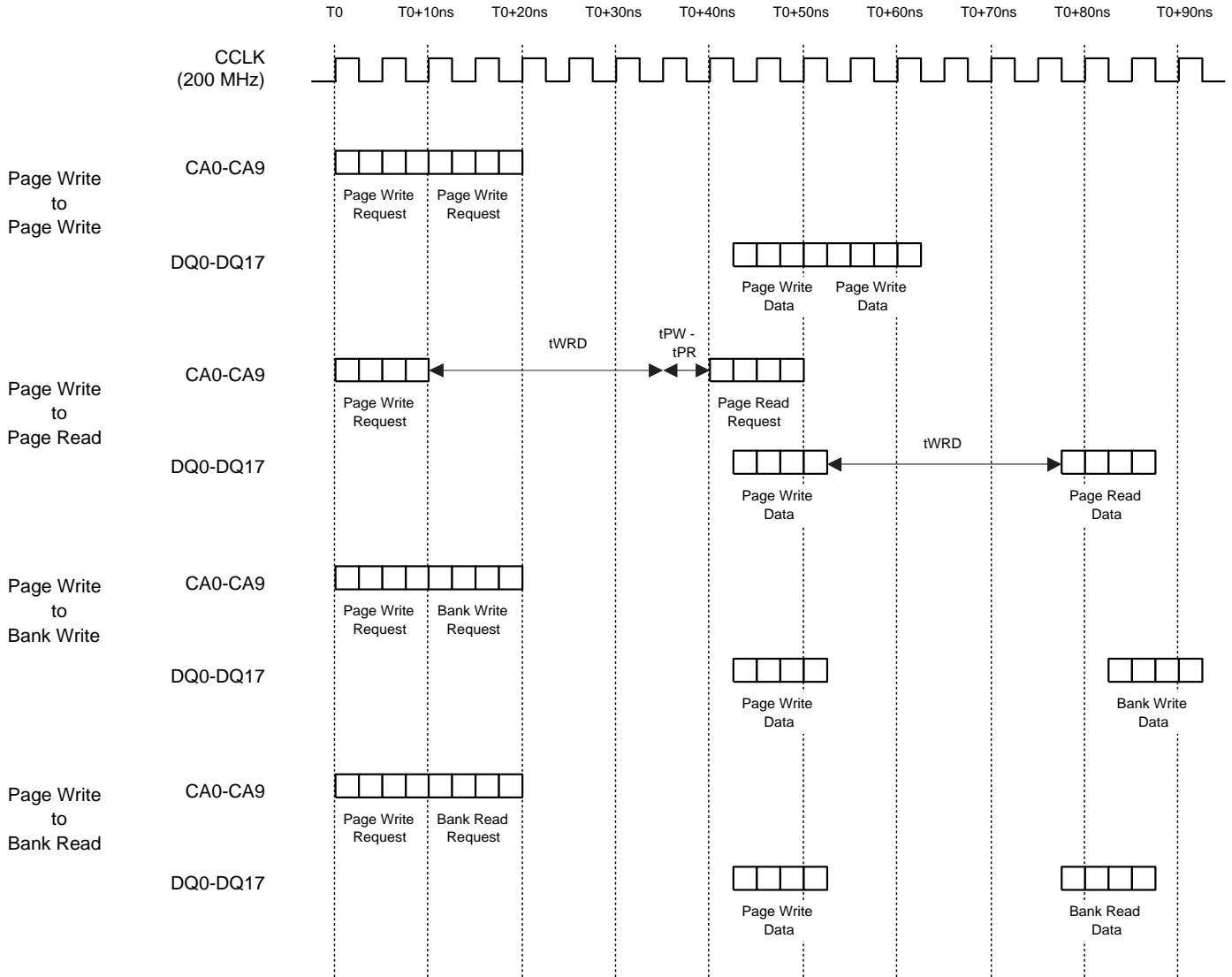


**Figure 83**  
**READ/WRITE COMMAND ISSUE RESTRICTIONS**  
**EXAMPLE 1 - READ LATENCY = MINIMUM,**  
**WRITE LATENCY = READ LATENCY (CONTINUED)**

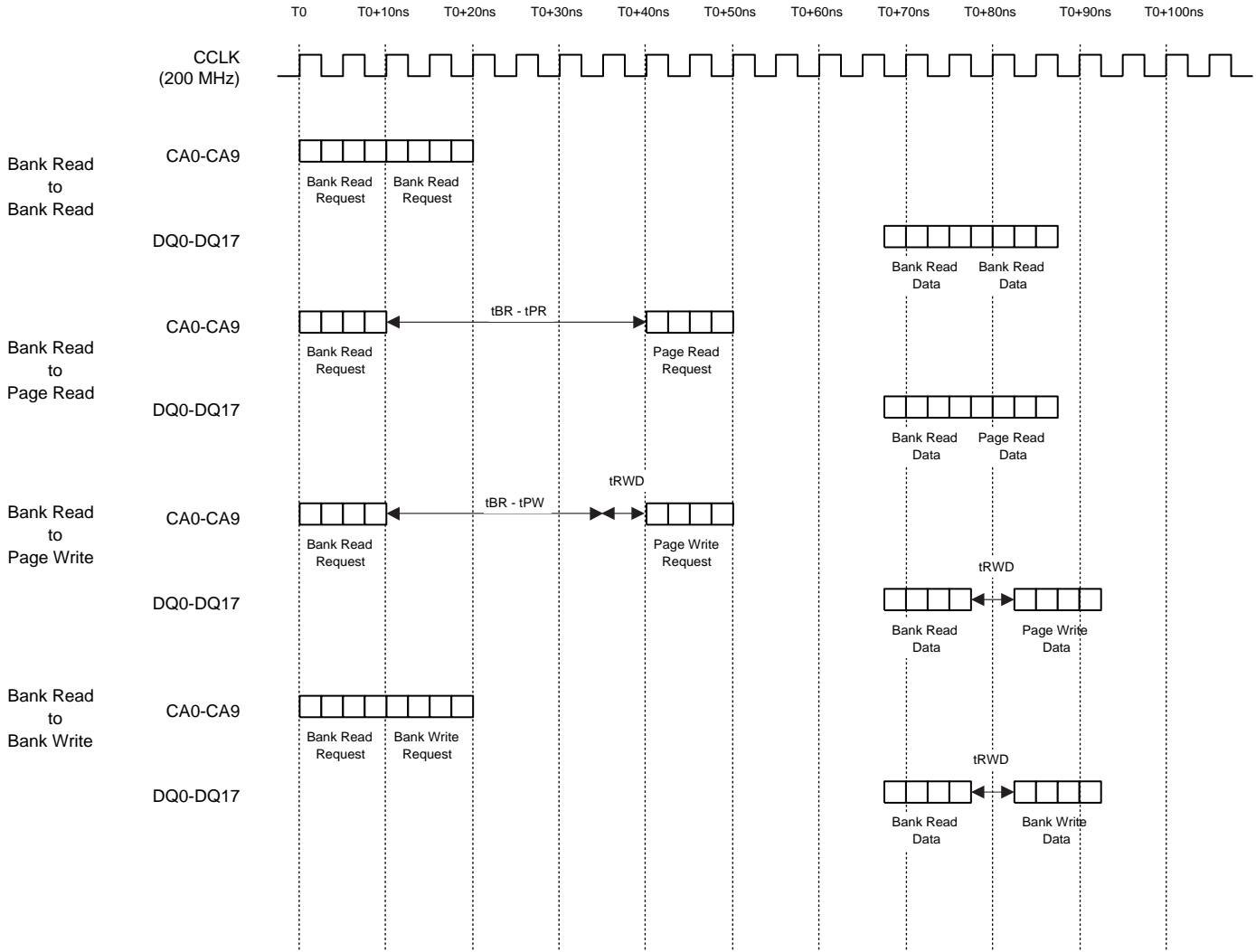


**Figure 84**  
**READ/WRITE COMMAND ISSUE RESTRICTIONS**  
**EXAMPLE 2 - READ LATENCY = MINIMUM,**  
**WRITE LATENCY = READ LATENCY + 2**

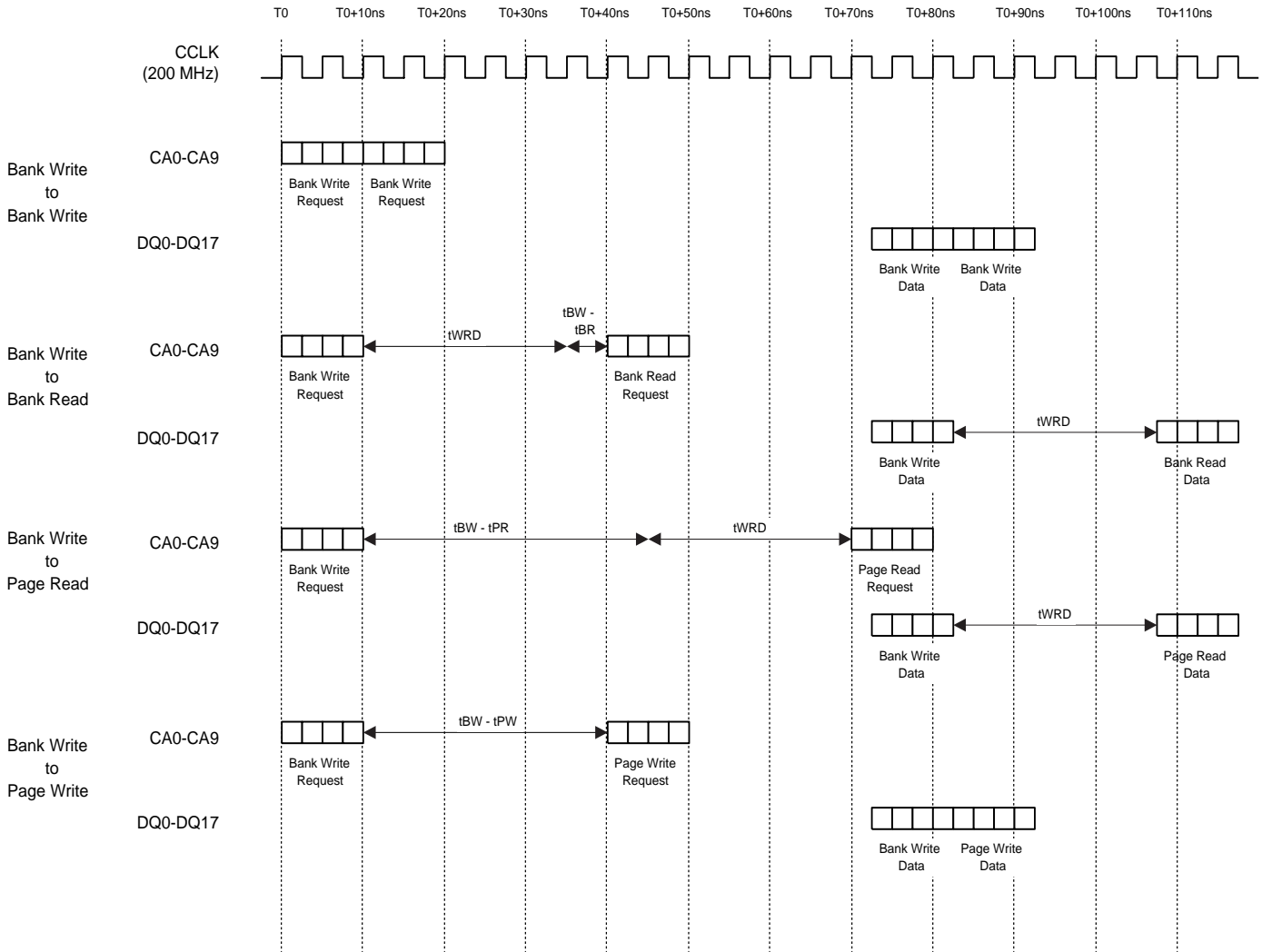




**Figure 85**  
**READ/WRITE COMMAND ISSUE RESTRICTIONS**  
**EXAMPLE 2 - READ LATENCY = MINIMUM,**  
**WRITE LATENCY = READ LATENCY + 2 (CONTINUED)**



**Figure 86**  
**READ/WRITE COMMAND ISSUE RESTRICTIONS**  
**EXAMPLE 2 - READ LATENCY = MINIMUM,**  
**WRITE LATENCY = READ LATENCY + 2 (CONTINUED)**



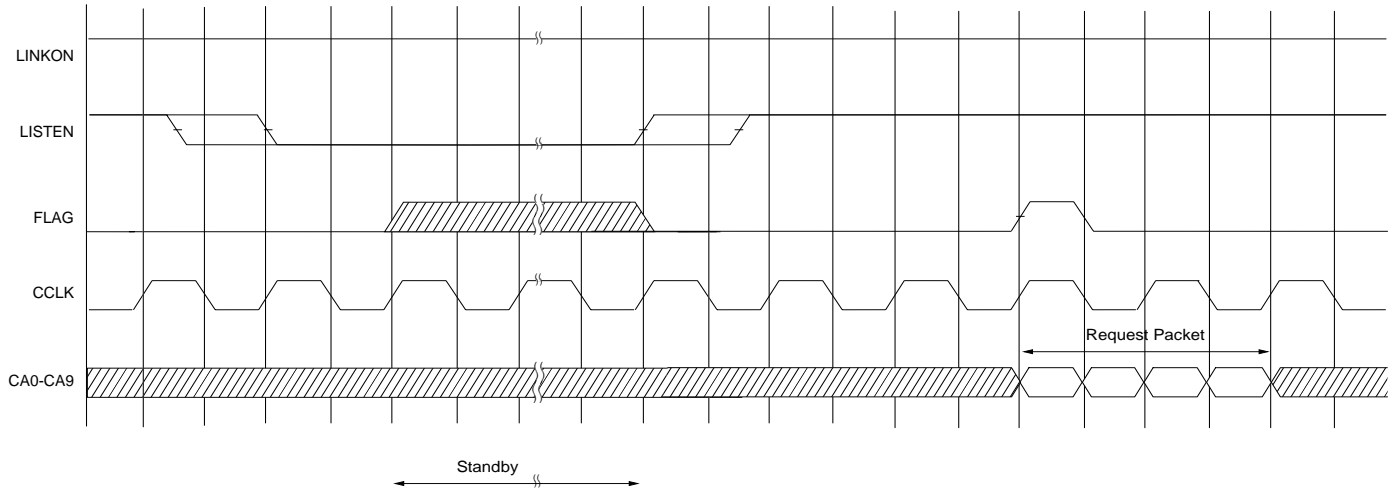
**Figure 87**  
**READ/WRITE COMMAND ISSUE RESTRICTIONS**  
**EXAMPLE 2 - READ LATENCY = MINIMUM,**  
**WRITE LATENCY = READ LATENCY + 2 (CONTINUED)**

**STANDBY MODE**

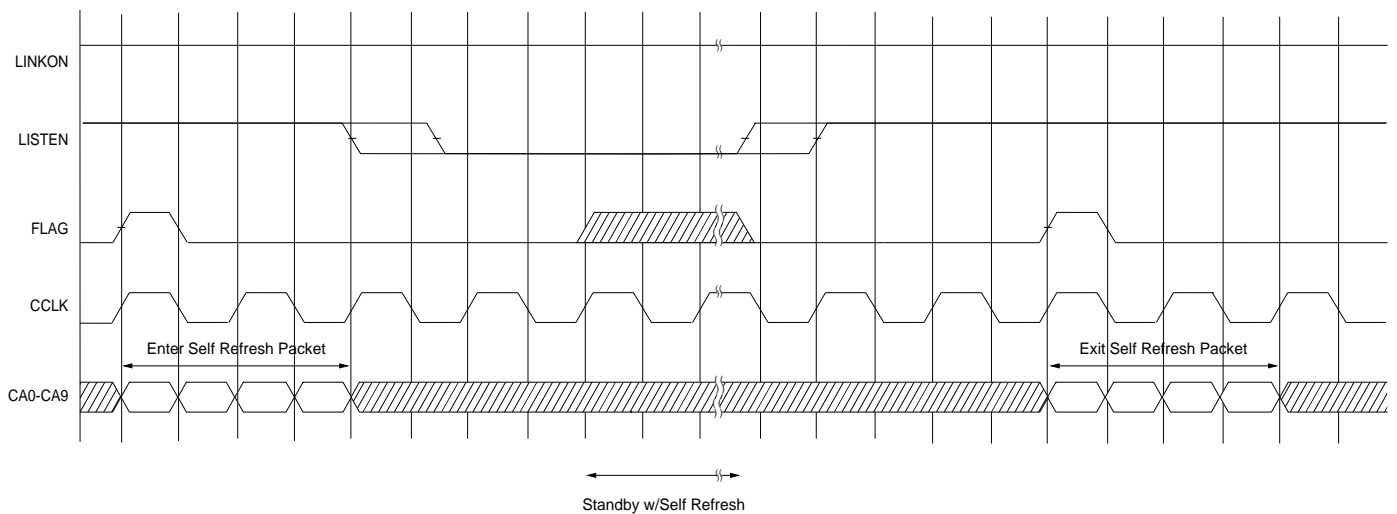
In Standby Mode all output drivers are disabled and all input receivers except those for CCLK, RESET#, LISTEN and LINKON are disabled. In addition, all internal circuitry that can be re-enabled within tLSC is disabled. The Standby

Mode is entered by deactivating the LISTEN signal at any time except during the transfer of a request packet.

The Standby Mode may be nested within the Self Refresh Mode as shown in Figure 89.



**Figure 88**  
**STANDBY MODE - GENERAL TIMING**



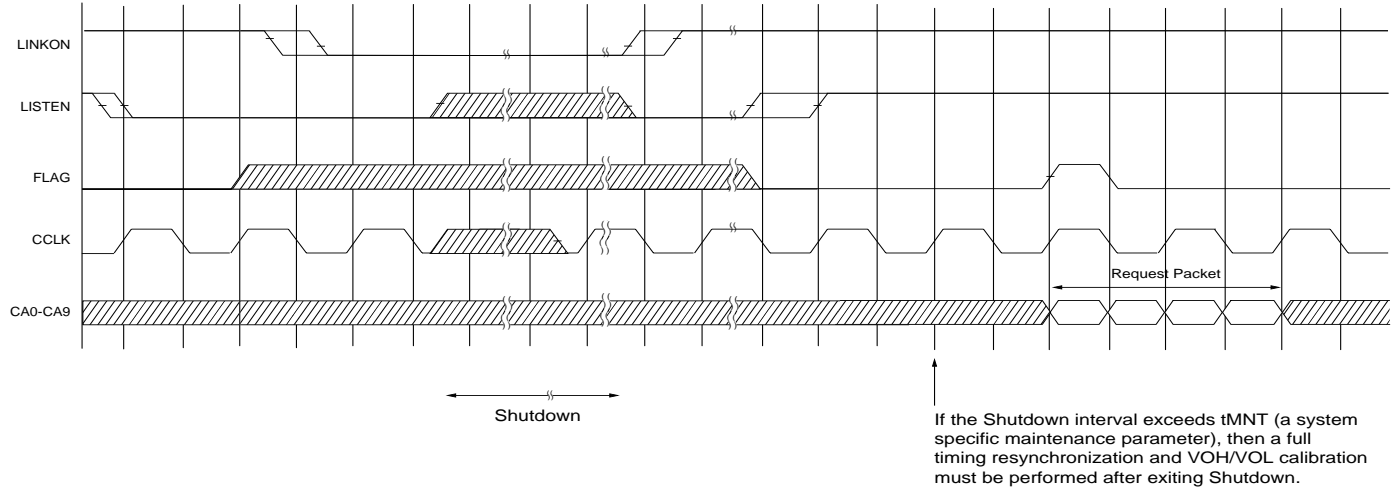
**Figure 89**  
**STANDBY MODE NESTED WITHIN SELF REFRESH MODE - GENERAL TIMING**

**SHUTDOWN MODE**

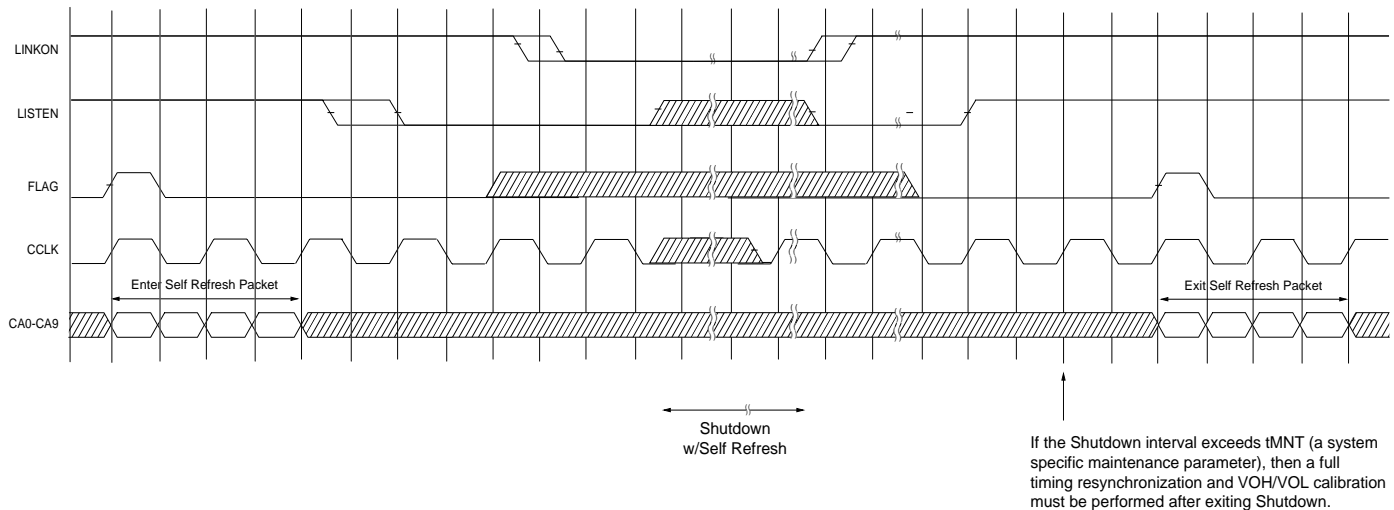
In Shutdown Mode all internal clocks are disabled, in addition to all output drivers and all input receivers except for LINKON and RESET#. The Shutdown Mode is entered

by deactivating the LINKON signal while the device is already in Standby Mode.

The Shutdown Mode may be nested within the Self Refresh Mode as shown in Figure 91.



**Figure 90**  
**SHUTDOWN MODE - GENERAL TIMING**

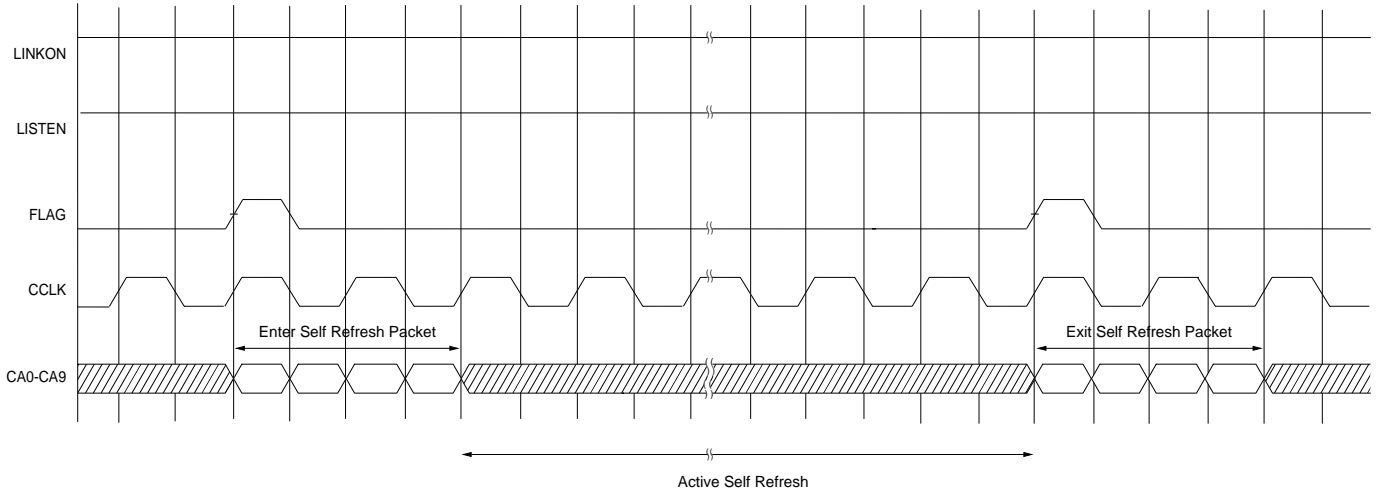


**Figure 91**  
**SHUTDOWN MODE NESTED WITHIN SELF REFRESH MODE - GENERAL TIMING**

**SELF-REFRESH MODE**

In Self-Refresh Mode an on-chip oscillator and refresh logic are enabled, thereby suspending the requirement for periodic Auto Refresh Events initiated by the memory

controller. Standby and/or Shutdown Modes may be nested within the Self-Refresh Mode. No other commands/accesses are permitted to the SLDRAM while in Self-Refresh.



**Figure 92**  
**SELF REFRESH MODE - GENERAL TIMING**

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on V <sub>DD</sub> /V <sub>DDQ</sub> supply relative to V <sub>SS</sub> .....	-0.5V to +3.6V
Voltage on Inputs relative to V <sub>SS</sub> .....	-0.5V to +3.6V
Voltage on SLIO Outputs or SLIO I/O pins relative to V <sub>SS</sub> .....	-0.5V to V <sub>DDQ</sub> +0.5V
Voltage on LVC MOS Outputs relative to V <sub>SS</sub> .....	-0.5V to V <sub>DD</sub> +0.5V
Operating Temperature, T <sub>A</sub> (ambient) .....	0°C to +70°C
Storage Temperature (plastic) .....	-55°C to +150°C
Power Dissipation .....	1.3W
Short Circuit Output Current .....	50mA

\*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(Note: 1, 4) (0°C ≤ T<sub>A</sub> ≤ 70°C; V<sub>DD</sub>/V<sub>DDQ</sub> = +2.5V ±0.125V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V <sub>DD</sub> /V <sub>DDQ</sub>	2.375	2.625	V	2
Input High (Logic 1) Voltage, SLIO	V <sub>IH</sub>	V <sub>REF</sub> +0.2	V <sub>DDQ</sub> +0.3	V	
Input Low (Logic 0) Voltage, SLIO	V <sub>IL</sub>	V <sub>SSQ</sub> -0.3	V <sub>REF</sub> -0.2	V	
Input High (Logic 1) Voltage, LVC MOS	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub> +0.3	V	
Input Low (Logic 0) Voltage, LVC MOS	V <sub>IL</sub>	V <sub>SS</sub> -0.3	0.3V <sub>DD</sub>	V	
Input Reference Voltage (SLIO)	V <sub>REF</sub>	0.5V <sub>DD</sub> -0.05	0.5V <sub>DD</sub> +0.05	V	3
INPUT LEAKAGE CURRENT Any input 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> +0.3 (All other pins not under test = 0V)	I <sub>I</sub>	-2	2	μA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V <sub>OUT</sub> ≤ V <sub>DDQ</sub> + 0.3V LVC MOS, 0V ≤ V <sub>OUT</sub> ≤ V <sub>DDQ</sub> + 0.3V SLIO)	I <sub>OZ</sub>	-10	10	μA	
OUTPUT LEVELS - SLIO Output High Voltage	V <sub>OH</sub>	1.6		V	10
Output Low Voltage	V <sub>OL</sub>		0.9	V	
Calibrated Output High Voltage	V <sub>OH</sub>	1.6	1.625	V	
Calibrated Output Low Voltage	V <sub>OL</sub>	0.875	0.9	V	
OUTPUT LEVELS - LVC MOS Output High Voltage (I <sub>OH</sub> = -100μA)	V <sub>OH</sub>	V <sub>DD</sub> -0.2		V	
Output Low Voltage (I <sub>OL</sub> = 100μA)	V <sub>OL</sub>		V <sub>SS</sub> +0.2	V	



## CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: SLIO Inputs	C <sub>IS</sub>	3	pF	5
Input Capacitance: LVCMOS Inputs	C <sub>IL</sub>	5	pF	5
Input/Output Capacitance: SLIO I/O	C <sub>IOS</sub>	3	pF	5
Input/Output Capacitance: LVCMOS I/O	C <sub>IOL</sub>	6.5	pF	5

I<sub>DD</sub> SPECIFICATIONS AND CONDITIONS(Note: 1, 6, 13) (0°C ≤ T<sub>A</sub> ≤ 70°C; V<sub>DD</sub>/V<sub>DDQ</sub> = +2.5V ±0.125V)

PARAMETER/CONDITION	SYMBOL	-400 MAX		UNITS	NOTES
		@333Mb/s/p	@400Mb/s/p		
OPERATING CURRENT: Random Bank Reads and/or Bank Writes, Burst Length = 4, t <sub>RC1</sub> ≥ t <sub>RC1</sub> MIN	I <sub>DD1</sub>	TBD	TBD	mA	
OPERATING CURRENT: Page Reads and/or Page Writes to open rows, Burst Length = 4, t <sub>PR</sub> ≥ t <sub>PR</sub> MIN, t <sub>PW</sub> = t <sub>PR</sub>	I <sub>DD2</sub>	TBD	TBD	mA	
AUTO REFRESH CURRENT: t <sub>RC2</sub> ≥ t <sub>RC2</sub> MIN	I <sub>DD3</sub>	TBD	TBD	mA	
STANDBY CURRENT: Standby mode, LISTEN ≤ V <sub>IL</sub> (MAX)	I <sub>DD4</sub>	TBD	TBD	mA	
STANDBY CURRENT: Shutdown mode, LINKON ≤ V <sub>IL</sub> (MAX)	I <sub>DD5</sub>	TBD	TBD	mA	
SELF REFRESH CURRENT:	I <sub>DD6</sub>	TBD	TBD	uA	
STANDBY CURRENT: Standby-Self Refresh Mode, LISTEN ≤ V <sub>IL</sub> (MAX)	I <sub>DD7</sub>	TBD	TBD	uA	
STANDBY CURRENT: Shutdown-Self Refresh Mode, LINKON ≤ V <sub>IL</sub> (MAX)	I <sub>DD8</sub>	TBD	TBD	uA	

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T<sub>A</sub> ≤ +70°C)

AC CHARACTERISTICS PARAMETER	SYM	-400		UNITS	NOTES
		MIN	MAX		
Command Input (CAn, FLAG) Valid time	<sup>t</sup> CIV	950		ps	11
Command Input (CAn, FLAG) Skew	<sup>t</sup> CIS		775	ps	11
Command Clock (CCLK) Input Valid time	<sup>t</sup> CCV	1380		ps	11
Command Clock (CCLK) Input Skew	<sup>t</sup> CCS		560	ps	11
Clock Cycle time	<sup>t</sup> CK	5	10	ns	
CCLK Frequency Stability/Long Term Jitter	-		4	%	
CCLK/DCLK Short Term (edge-to-edge) Jitter	-		1	%	12
Command to DCLK Delay (for DCLK HIGH, LOW, TOGGLING or HIGH-Z)	<sup>t</sup> DD		20	ns	
Data Input (DQn) Valid Time	<sup>t</sup> DIV	950		ps	11
Data Input (DQn) Skew	<sup>t</sup> DIS		775	ps	11
Data Clock Input (DCLKn) Valid Time	<sup>t</sup> DCIV	1380		ps	11
Data Clock Input (DCLKn) Skew	<sup>t</sup> DCIS		560	ps	11
Data Output (DQn) Valid Time	<sup>t</sup> DOV	1900		ps	11
Data Output (DQn) Skew	<sup>t</sup> DOS		300	ps	11
Data Clock Output (DCLKn) Valid Time	<sup>t</sup> DCOV	2080		ps	11
Data Clock Output (DCLKn) Skew	<sup>t</sup> DCOS		210	ps	11
Data-out high-impedance time	<sup>t</sup> HZ		125	ps	6, 11
Data-out low-impedance time	<sup>t</sup> LZ	125		ps	6, 11
Open Row to Close Row command period (same bank)	<sup>t</sup> RAS	60	64	ns/us	7, 14
Open Row to Open Row command period (same bank)	<sup>t</sup> RC1	88		ns	7
Auto Refresh to Auto Refresh Command period	<sup>t</sup> RC2	88		ns	7
Refresh period (8,192 cycles)	<sup>t</sup> REF		64	ms	
Close Row (precharge) command period	<sup>t</sup> RP	28		ns	7
Open Row to Open Row command period (different bank)	<sup>t</sup> RRD	10		ns	7
Reset Inactive to Linkon Active Set Up Time	<sup>t</sup> RL	0		ns	
Write recovery time	<sup>t</sup> WR	15		ns	7
Exit SELF REFRESH to Open Row command	<sup>t</sup> XSR	88		ns	7
Minimum Page Read Delay	<sup>t</sup> PR ( <sup>t</sup> AA)		26-30	ns	7
Minimum Bank Read Delay	<sup>t</sup> BR ( <sup>t</sup> RAC)		56-64	ns	7
Minimum Page Write Delay	<sup>t</sup> PW	17		ns	7
Minimum Bank Write Delay	<sup>t</sup> BW	30		ns	7
Maximum Page Read Delay	<sup>t</sup> PR_MAX		32	ticks	
Maximum Bank Read Delay	<sup>t</sup> BR_MAX		64	ticks	
Maximum Page Write Delay	<sup>t</sup> PW_MAX		32	ticks	
Maximum Bank Write Delay	<sup>t</sup> BW_MAX		64	ticks	
Minimum Read to Write Delay (external I/O turnaround)	<sup>t</sup> RWD	5		ns	
Minimum Write to Read Delay	<sup>t</sup> WRD	45		ns	7,8
VDD/VDDQ to Vterm Set Up Time	<sup>t</sup> VD	2		us	
VREF to Inputs Valid Set Up Time	<sup>t</sup> IV	0		ns	
Reset# Pulse Width	<sup>t</sup> RST	100		ns	
Input Set Up Time	<sup>t</sup> SI	10		ns	11

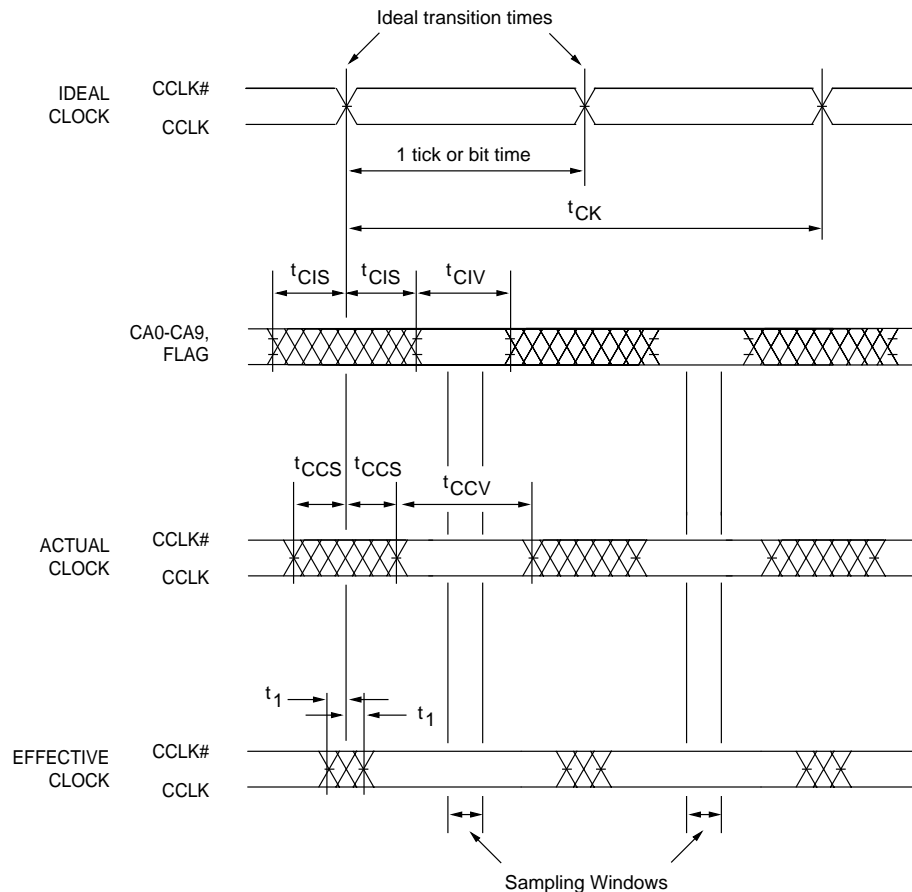
## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T<sub>A</sub> ≤ +70°C)

AC CHARACTERISTICS		-400			
PARAMETER	SYM	MIN	MAX	UNITS	NOTES
ID Write Request to SO Output Delay	t <sub>ID</sub>		20	ns	
Listen to Linkon Low Set Up Time	t <sub>LLS</sub>	5		ns	
Listen to Linkon Low Hold Time	t <sub>LLH</sub>	5		ns	
Listen to Linkon High Set Up Time	t <sub>LHS</sub>	0		ns	
Listen to Linkon High Hold Time - Cold	t <sub>LHHC</sub>	15		us	11,13
Listen to Linkon High Hold Time - Warm	t <sub>LHHW</sub>	1		us	11,13
Input to Listen Set Up Time	t <sub>ILS</sub>	0		ns	
Input to Listen Hold Time	t <sub>ILH</sub>	5		ns	
Listen to Next Command Set Up Time	t <sub>LSC</sub>	10		ns	
Vernier Adjust to Output Delay (no accesses in progress)	t <sub>VO</sub>		10	ns	
VOH/VOL Adjust to Output Delay (no accesses in progress)	t <sub>LO</sub>		10	ns	
Control Register Write to Next Command Set Up Time (all banks closed)	t <sub>CC</sub>	10		ns	15
Clock Stable to Reset# Inactive Set Up Time	t <sub>CSI</sub>	100		ns	9
Clock Stable to Linkon High Set Up Time	t <sub>CS</sub>	1		t <sub>CK</sub>	
Last Command to Listen Low Set Up Time	t <sub>PLI</sub>	0		ns	
Close Row to Last Data Out Set Up Time	t <sub>CRDO</sub>		3	ticks	
Last Previous Data to Next DCLK Preamble Delay	t <sub>DDC</sub>	4		ticks	
VDD to RESET# High Set Up Time	t <sub>VRST</sub>	50		us	

## NOTES

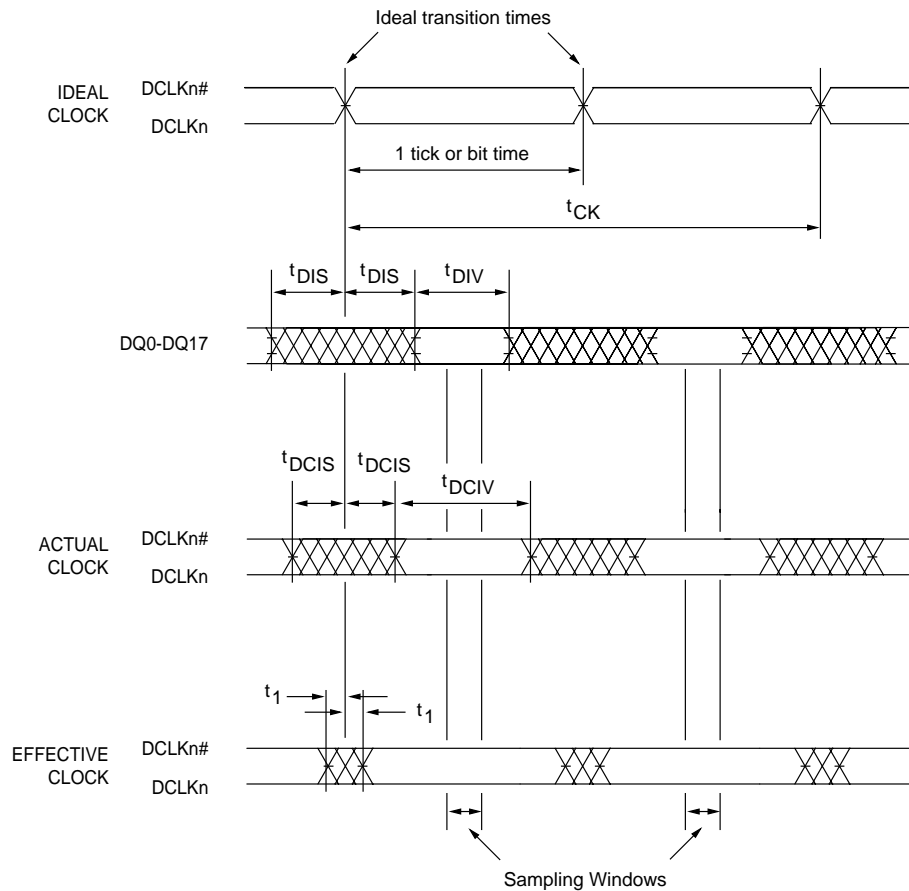
- All voltages referenced to V<sub>SS</sub>.
- V<sub>DDQ</sub> ≤ V<sub>DD</sub>.
- |V<sub>TERM</sub> - V<sub>REF</sub>| ≤ 50mV.
- Variations in V<sub>DDQ</sub>, V<sub>TERM</sub> and V<sub>REF</sub> must track each other.
- This parameter is sampled. V<sub>DD</sub>, V<sub>DDQ</sub> = +2.5V ± 0.125V; f = 1 MHz, t<sub>A</sub> = 25 deg C.
- t<sub>HZ</sub> and t<sub>LZ</sub> specifications reflect the transition time between the V<sub>TERM</sub> voltage to which the signal is terminated in the system and the valid input logic levels. These parameters are not tested directly, but are indirectly verified in testing the skew of the output signals.
- This parameter may consist of analog and digital components, such that the total value can be optimized at different clock frequencies. The values of the analog and digital components can be obtained from the corresponding Timing Parameter register. The total value contained in this table is calculated using t<sub>CK</sub> = t<sub>CK</sub> MIN.
- This parameter includes margin to cover t<sub>AA</sub> guardband and possible rounding error.
- An external buffer device in the system may have a more restrictive value for this parameter.
- The output voltage is measured on the bus side of the series (stub) resistor, with a parallel resistor to V<sub>TERM</sub>. The output voltages are shown for a series resistor value of 20 ohms and a parallel resistor value of 28 ohms.
- This value is specific to 400Mb/s/p operation and must be recalculated for other data rates.
- This specification is actually a combined jitter and “duty cycle” specification. The value shown represents that portion of the total output uncertainty appearing on DCLK or CCLK signals which is allocated to jitter and/or “duty cycle” variation. This is accounted for in the output valid and output skew specifications for those signals.
- Cold applies when following reset; Warm applies after exiting shutdown (with no reset).
- Min is in ns, Max is in us. Only the Min value is represented in the corresponding Timing Parameter register.
- Measured from end of one command packet to start of next command packet.



## Notes:

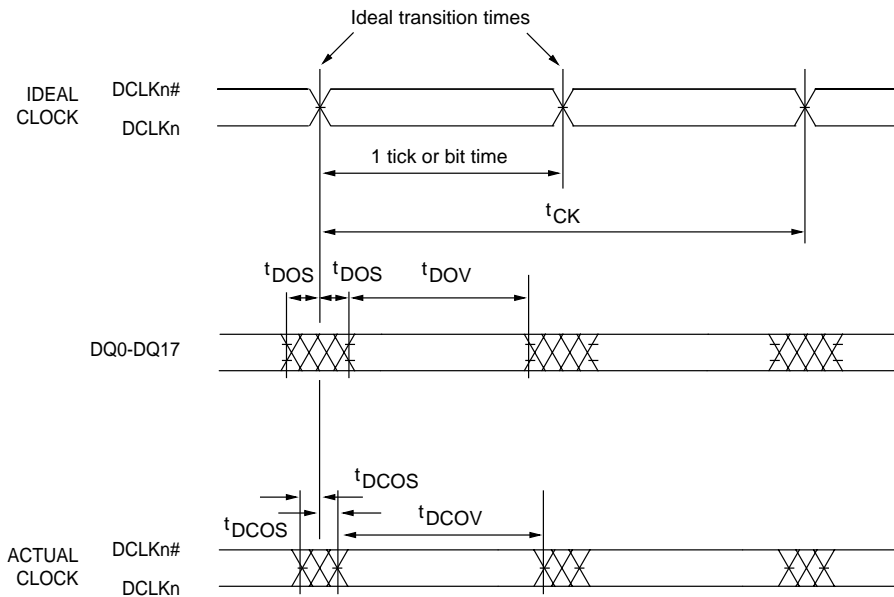
1. The Command and Actual Clock signals are shown as they are required to appear at the inputs to the receiving device. These signals are required to exhibit much less skew when leaving the transmitting device (as show for the output data in Figure 95).
2. Additional skew may occur in the input stage of the receiving device; this skew is accounted for in the device timing specifications.
3. The Effective Clock signal is shown to illustrate the effects of the timing adjustments supported by SLDRAM devices. The remaining clock skew after adjustment is equal to the resolution of the input sampling vernier (the same resolution as the Data Offset vernier,  $t_{CK}/32$ ) plus the budgeted system dynamic skew. Parameter  $t_1$  represents one-half this amount and is defined to show the total skew centered on the imaginary ideal transition. The internal sampling occurs within the same size window, located one-half bit time later (in the center of the data eye).
4. Details related to the system level analysis and timing budget will be provided in separate documentation.

**Figure 93**  
**COMMAND INPUT TIMING**

**Notes:**

1. The Input Data and Actual Data Clock signals are shown as they are required to appear at the inputs to the receiving device. These signals are required to exhibit much less skew when leaving the transmitting device (as show for the output data in Figure 95).
2. Additional skew may occur in the input stage of the receiving device; this skew is accounted for in the device timing specifications.
3. The Effective Clock signal is shown to illustrate the effects of the timing adjustments supported by SLDRAM devices. The remaining clock skew after adjustment is equal to the resolution of the input sampling vernier (the same resolution as the Data Offset vernier,  $t_{CK}/32$ ) plus the budgeted system dynamic skew. Parameter  $t_1$  represents one-half this amount and is defined to show the total skew centered on the imaginary ideal transition. The internal sampling occurs within the same size window, located one-half bit time later (in the center of the data eye).
4. Details related to the system level analysis and timing budget will be provided in separate documentation.

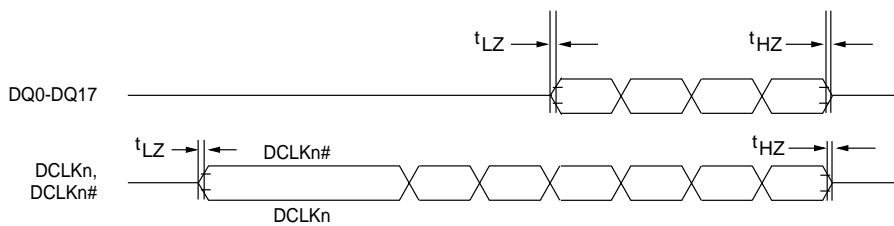
**Figure 94**  
**DATA INPUT TIMING**



Notes:

1. The Output Data and Data Clock signals are shown as they are required to appear at the outputs of the transmitting device. These signals will incur additional skew in the system before reaching the receiving device; this skew is accounted for in the device timing specifications.
2. Details related to the system level analysis and timing budget will be provided in separate documentation.

**Figure 95**  
**DATA OUTPUT TIMING**

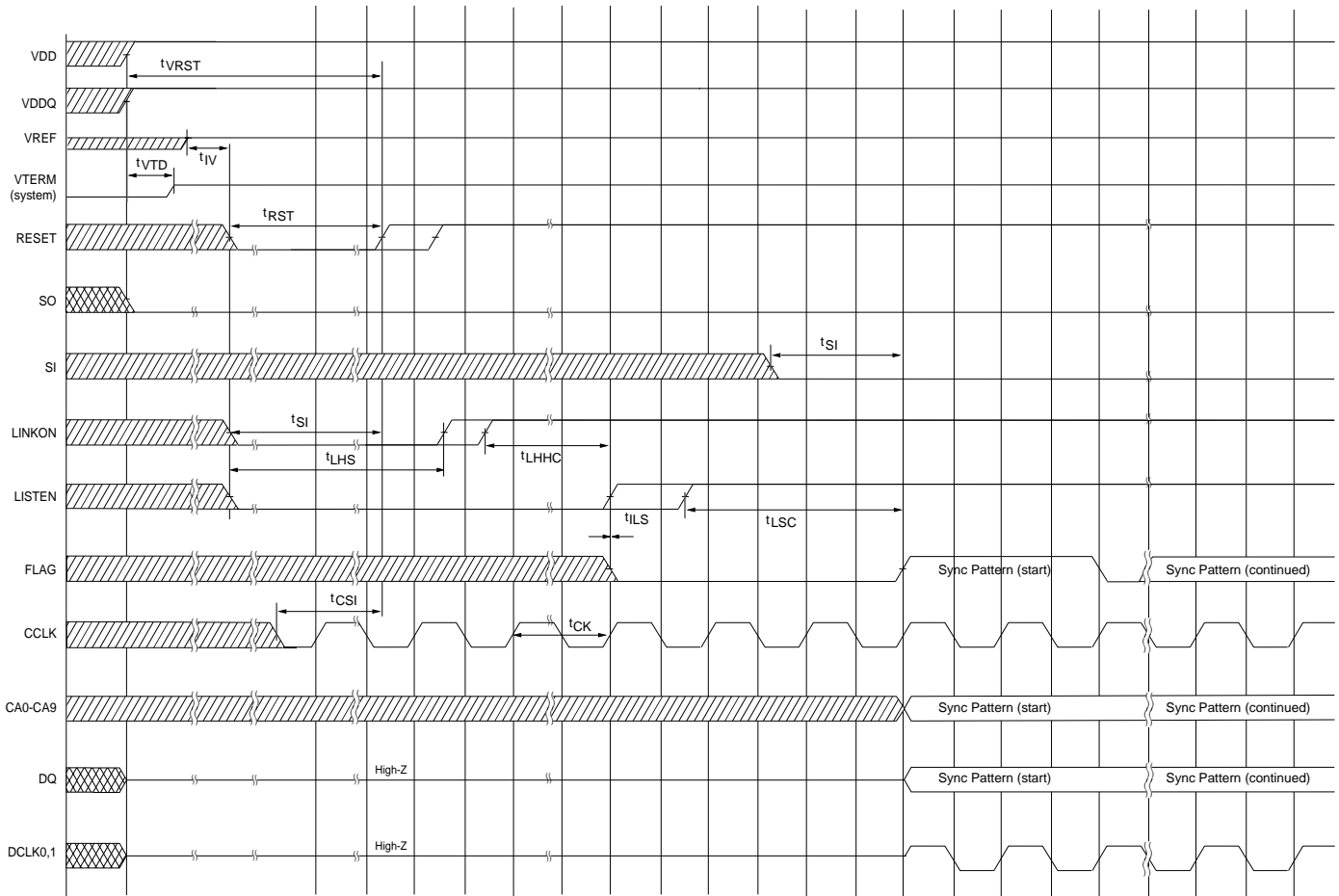


Notes:

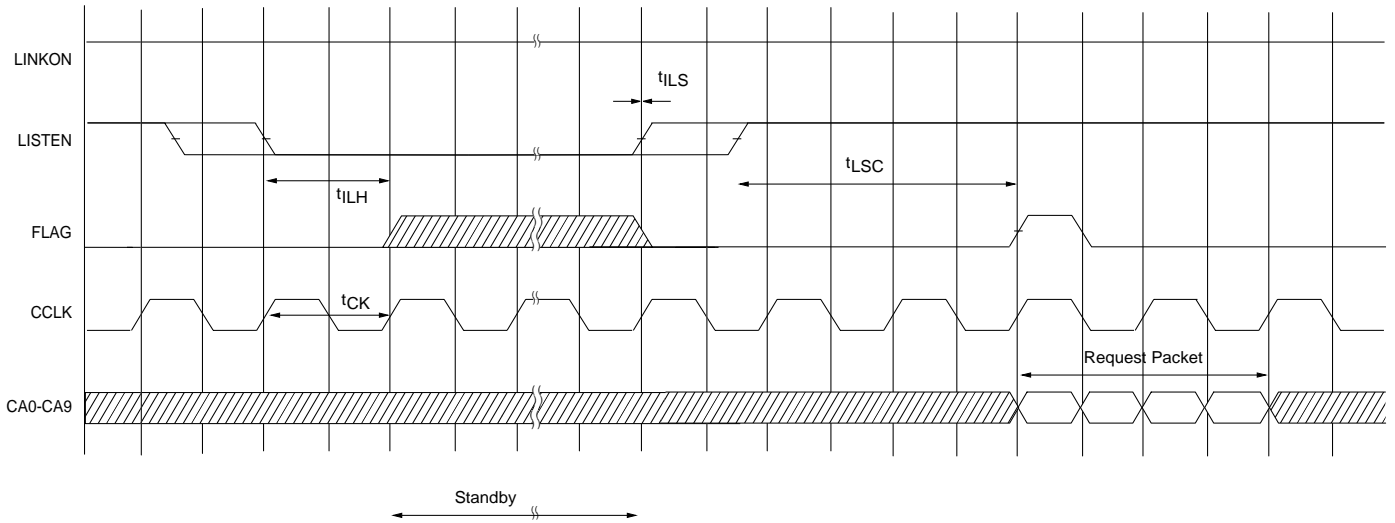
1. The High-Z to Low-Z edge on the DQs (tLZ) is subject to the same skew requirements as other DQ transitions relative to the nominally coincident DCLK transition.
2. The tLZ and tHZ parameters values for the DCLK signals need not meet the same specification as for the DQs, but will be similar by design.

**Figure 96**  
**DATA OUTPUT ENABLE/DISABLE TIMING**

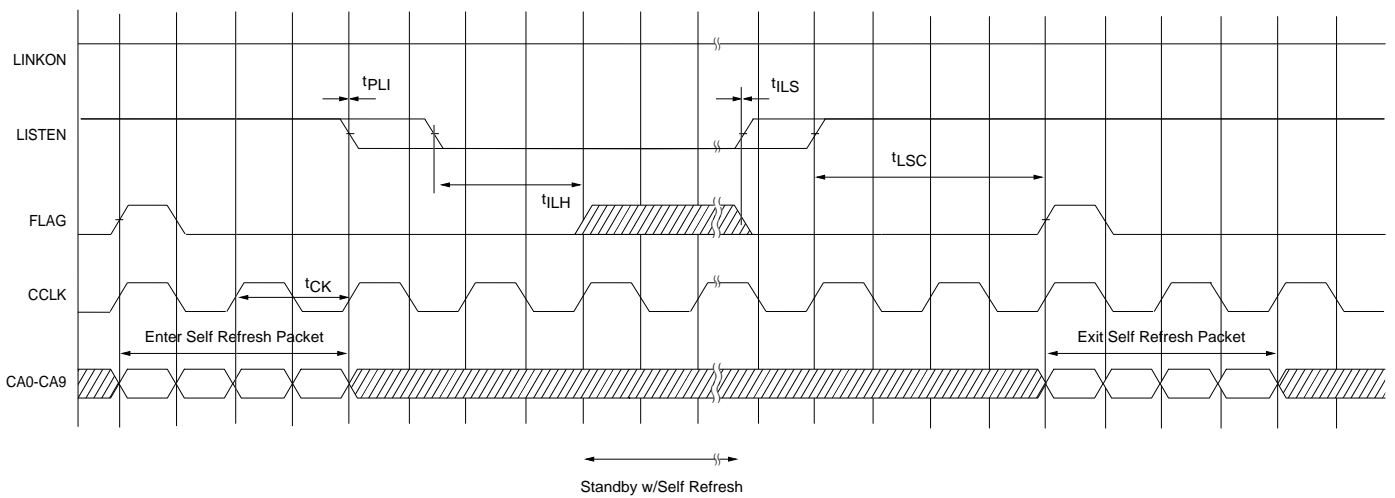
INITIALIZATION TIMING



### STANDBY MODE TIMING

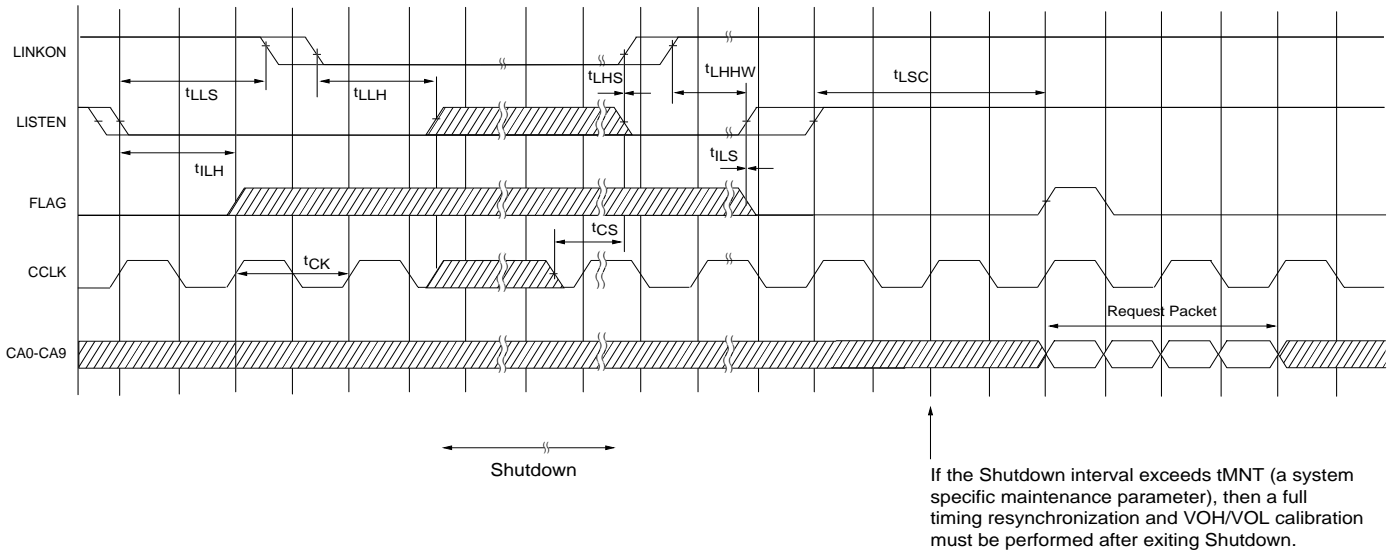


### STANDBY WITH SELF REFRESH MODE TIMING

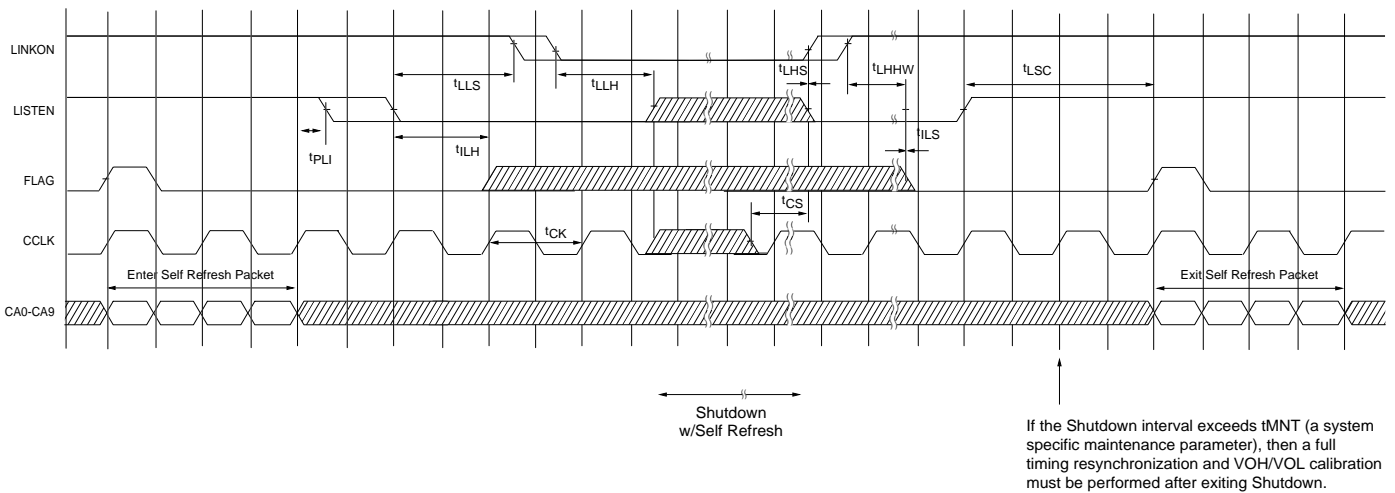




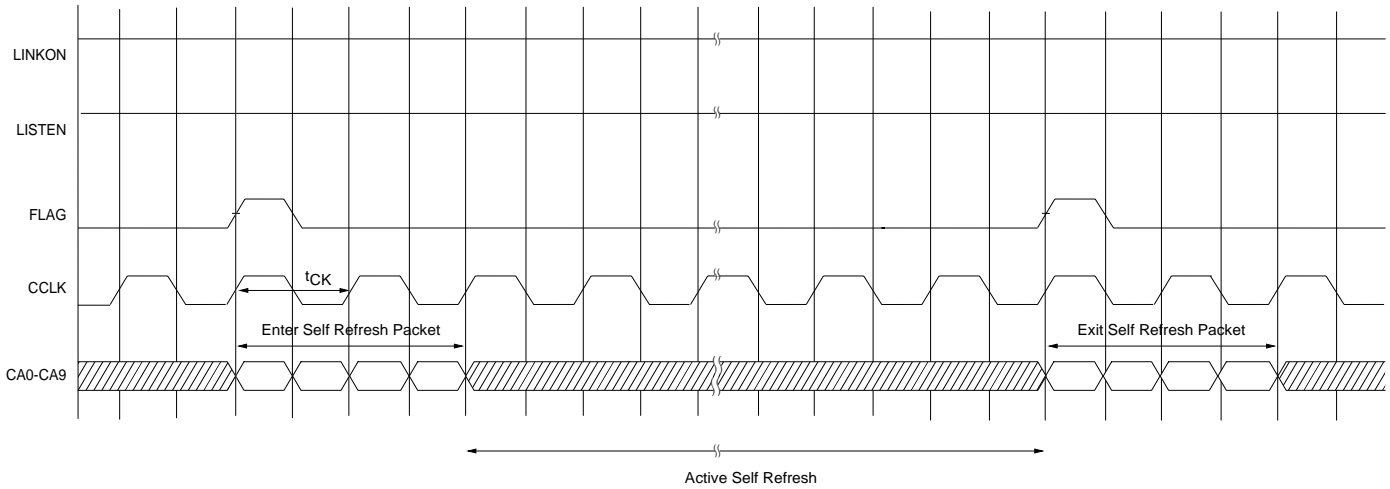
SHUTDOWN MODE TIMING



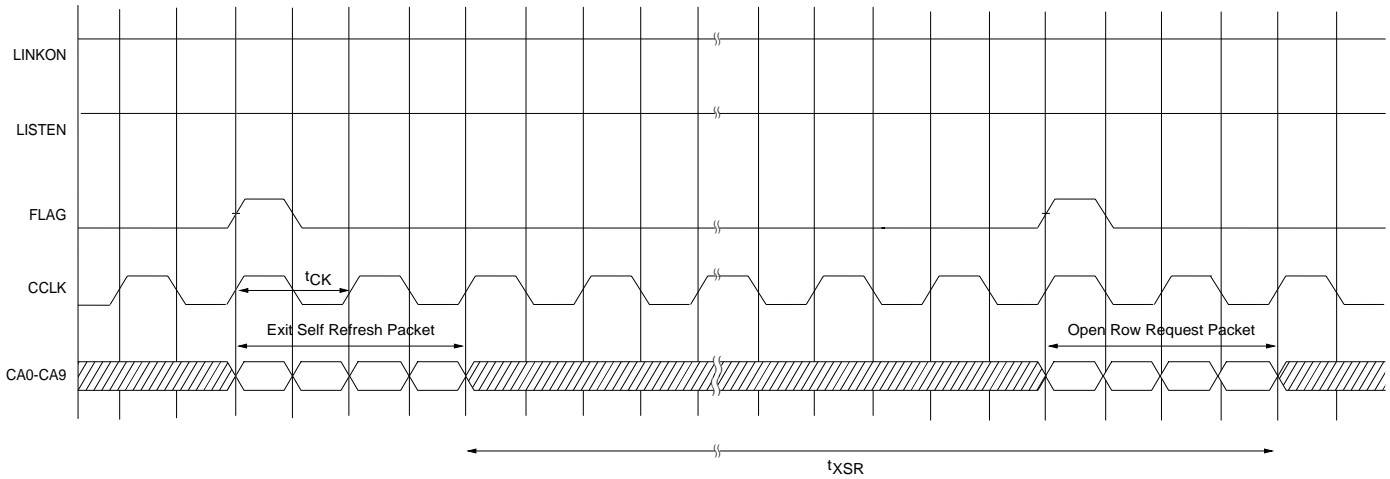
SHUTDOWN WITH SELF REFRESH MODE TIMING



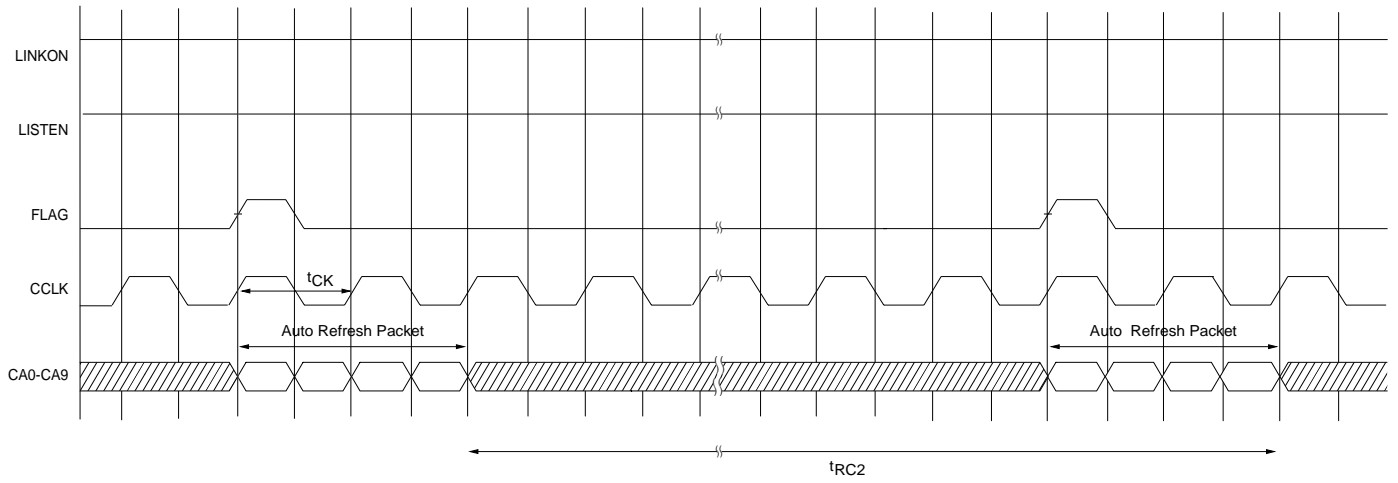
### SELF REFRESH MODE TIMING



### EXIT SELF REFRESH MODE TIMING



AUTO REFRESH TIMING



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## APPENDIX I

### ID Multicast Addressing

A packet ID value of 0-255 selects a single device (or a group of devices) with that ID value stored in it's (their) ID register(s). When a group of devices with the same ID is selected, the Sub-ID field will be used for certain types of requests to select all, or a subset of, devices within that group.

A packet ID value of 256-511 selects a subset of devices (or a subset of groups of devices) according to the table on the following page. When a subset of groups of devices is selected, the Sub-ID field will be used for certain types of requests to select all, or a subset of, devices within those groups.

Packet ID Value	Multi-cast Range
256	0 - 1
257	0 - 3
258	2 - 3
259	0 - 7
260	4 - 5
261	4 - 7
262	6 - 7
263	0 - 15
264	8 - 9
265	8 - 11
266	10 - 11
267	8 - 15
268	12 - 13
269	12 - 15
270	14 - 15
271	0 - 31
272	16 - 17
273	16 - 19
274	18 - 19
275	16 - 23
276	20 - 21
277	20 - 23
278	22 - 23
279	16 - 31
280	24 - 25
281	24 - 27
282	26 - 27
283	24 - 31
284	28 - 29
285	28 - 31
286	30 - 31
287	0 - 63
288	32 - 33
289	32 - 35
290	34 - 35
291	32 - 39
292	36 - 37
293	36 - 39
294	38 - 39
295	32 - 47
296	40 - 41
297	40 - 43
298	42 - 43
299	40 - 47
300	44 - 45
301	44 - 47
302	46 - 47
303	32 - 63
304	48 - 49
305	48 - 51
306	50 - 51
307	48 - 55
308	52 - 53
309	52 - 55
310	54 - 55
311	48 - 63
312	56 - 57
313	56 - 59
314	58 - 59
315	56 - 63
316	60 - 61
317	60 - 63
318	62 - 63
319	0 - 127

Packet ID Value	Multi-cast Range
320	64 - 65
321	64 - 67
322	66 - 67
323	64 - 71
324	68 - 69
325	68 - 71
326	70 - 71
327	64 - 79
328	72 - 73
329	72 - 75
330	74 - 75
331	72 - 79
332	76 - 77
333	76 - 79
334	78 - 79
335	64 - 95
336	80 - 81
337	80 - 83
338	82 - 83
339	80 - 87
340	84 - 85
341	84 - 87
342	86 - 87
343	80 - 95
344	88 - 89
345	88 - 91
346	90 - 91
347	88 - 95
348	92 - 93
349	92 - 95
350	94 - 95
351	64 - 127
352	96 - 97
353	96 - 99
354	98 - 99
355	96 - 103
356	100 - 101
357	100 - 103
358	102 - 103
359	96 - 111
360	104 - 105
361	104 - 107
362	106 - 107
363	104 - 111
364	108 - 109
365	108 - 111
366	110 - 111
367	96 - 127
368	112 - 113
369	112 - 115
370	114 - 115
371	112 - 119
372	116 - 117
373	116 - 119
374	118 - 119
375	112 - 127
376	120 - 121
377	120 - 123
378	122 - 123
379	120 - 127
380	124 - 125
381	124 - 127
382	126 - 127
383	0 - 255

Packet ID Value	Multi-cast Range
384	128 - 129
385	128 - 131
386	130 - 131
387	128 - 135
388	132 - 133
389	132 - 135
390	134 - 135
391	128 - 143
392	136 - 137
393	136 - 139
394	138 - 139
395	136 - 143
396	140 - 141
397	140 - 143
398	142 - 143
399	128 - 159
400	144 - 145
401	144 - 147
402	146 - 147
403	144 - 151
404	148 - 149
405	148 - 151
406	150 - 151
407	144 - 159
408	152 - 153
409	152 - 155
410	154 - 155
411	152 - 159
412	156 - 157
413	156 - 159
414	158 - 159
415	128 - 191
416	160 - 161
417	160 - 163
418	162 - 163
419	160 - 167
420	164 - 165
421	164 - 167
422	166 - 167
423	160 - 175
424	168 - 169
425	168 - 171
426	170 - 171
427	168 - 175
428	172 - 173
429	172 - 175
430	174 - 175
431	160 - 191
432	176 - 177
433	176 - 179
434	178 - 179
435	176 - 183
436	180 - 181
437	180 - 183
438	182 - 183
439	176 - 191
440	184 - 185
441	184 - 187
442	186 - 187
443	184 - 191
444	188 - 189
445	188 - 191
446	190 - 191
447	128 - 255

Packet ID Value	Multi-cast Range
448	192 - 193
449	192 - 195
450	194 - 195
451	192 - 199
452	196 - 197
453	196 - 199
454	198 - 199
455	192 - 207
456	200 - 201
457	200 - 203
458	202 - 203
459	200 - 207
460	204 - 205
461	204 - 207
462	206 - 207
463	192 - 223
464	208 - 209
465	208 - 211
466	210 - 211
467	208 - 215
468	212 - 213
469	212 - 215
470	214 - 215
471	208 - 223
472	216 - 217
473	216 - 219
474	218 - 219
475	216 - 223
476	220 - 221
477	220 - 223
478	222 - 223
479	192 - 255
480	224 - 225
481	224 - 227
482	226 - 227
483	224 - 231
484	228 - 229
485	228 - 231
486	230 - 231
487	224 - 239
488	232 - 233
489	232 - 235
490	234 - 235
491	232 - 239
492	236 - 237
493	236 - 239
494	238 - 239
495	224 - 255
496	240 - 241
497	240 - 243
498	242 - 243
499	240 - 247
500	244 - 245
501	244 - 247
502	246 - 247
503	240 - 255
504	248 - 249
505	248 - 251
506	250 - 251
507	248 - 255
508	252 - 253
509	252 - 255
510	254 - 255
511	0 - 255

**SUB-ID Multicast Addressing**

A packet SUB-ID value of 0-15 selects a single device within a group of devices having the same main ID. The single device selected is the one with the matching value (0-15) stored in its SUB-ID register.

A packet SUB-ID value of 16-31 selects a subset of devices within a group of devices having the same main ID. The subset selected is defined by the table below (where the numbers shown in the multicast range column represent the values stored in the SUB-ID registers of the devices). Please refer to the table below.

packet SUB-ID value	multicast range
16	0-1
17	0-3
18	2-3
19	0-7
20	4-5
21	4-7
22	6-7
23	0-15
24	8-9
25	8-11
26	10-11
27	8-15
28	12-13
29	12-15
30	14-15
31	0-15

## Revision History

- 9/22/97 - Corrected skew and valid timing parameter values; moved timing parameter notes to appropriate location, and added reference to note 9; edited parameter symbols for write recovery to be consistent.
- 12/4/97 - Shifted register address bits in the Register Read Request Packet and revised related text. Corrected tRRD entry in Figure 9, and text for Figure 95. Grammatical edits. Corrected treatment of RESET# input receiver in Standby Mode and Shutdown Mode.
- 1/29/98 - Restored the register address bits in the Register Read Request Packet to their original (i.e. pre- 12/4/97) position. Modified Figure 72 to meet 2n requirement and Figure 75 to meet tRAS. Added Figures 72A, 73A, 74A and 75A to show separate Close Row command. Added Appendix I and removed incorrect multicast description in ID and SUB-ID Register sections. Expanded ID and SUB-ID Register sections. In the Initialization section, clarified the ID contained in the Sub-ID Write Request Packets during initialization, and expanded the coverage of read vernier operation. Removed Write Sync Command and added NOP to allow for buffer-only commands. Corrected/clarified Data Offset Vernier adjustment descriptions in Truth Table 3. Clarified Read Accesses section/expanded Read Delay Timing section. Added notes, parameters and values to the AC specifications. Updated the initialization timing diagram.
- 2/12/98 - Changed Consortium to Inc. Added Dual DCLK section. Fixed Note 12, added notes 13 and 14. Editorial corrections. Removed obsolete tRSO; added tDDC, added tRAS max. tDICR now covered with tWR. Changed tCRDO value.
- 7/9/98 - Added Data Sync Request Packet definition. Clarified parameter order in timing parameter registers. Modified/clarified read and write latency detection procedures. Added Note 15 for tCC and added explicit reference to tCC being applicable between ID and SUB-ID writes. Clarified ID/SUB-ID assignment. Modified Notes 7 and 14, and removed analog and digital components from spec table. Added tRL. Added exceptions to hard and soft reset events.