



News Fact Sheet

Intel Discloses Architecture Features of Next Itanium Processor at Hot Chips 2011

Aug. 19, 2011 — Intel Corporation today revealed architecture features of the next Itanium processor codenamed “Poulson.” Scheduled for launch in 2012, “Poulson,” the most sophisticated Intel processor to date, will offer the strongest RAS features as well as the biggest leap in performance compared to previous Itanium generations.

New disclosed features:

- **Intel Instruction Replay Technology** – New capability to enable errant instructions to be re-issued and thereby automatically recover from severe errors to help prevent system crashes and data corruptions.

In addition, Poulson adds extensive RAS protection to nearly all the major structures in the Itanium core design. This includes the Last Level Cache (LLC), Mid-level Instruction cache (MLI), Mid-level Data cache (MLD), Integer Execution Unit (IEU) and Floating Point Unit (FPU), to name a few.

- **Intel Hyper-Threading Technology**, enhanced with dual-domain multi-threading support – new architecture enables independent front and backend pipeline execution to improve multi-thread efficiency and performance.

Major hardware investments on multi-threading include: dual threaded register files, dual threaded data side Translation buffers (TLBs), and a new fairness mechanism. Together, these additions enable the dual domain multi-threading support to significantly improve Poulson’s multi-threading performance over that of the previous generation.

- **Intel Itanium New Instructions** -- new instructions simplify common tasks and branch operations to help take future Itanium performance to the next level and to lay the foundation for the future of Itanium computing.

The above features are “designed to take full advantage of the 8-core, 12-wide issue architecture by enabling the maximum amount of parallel execution,” said Pauline Nist, General Manager of Mission Critical Segment at Intel. Poulson is on track for 2012 delivery and the follow-on future Kittson processor is under development.

Additional “Poulson” Highlights:

- Eight high-capacity cores

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- 54MB on-die memory (50MB SRAM)
- 3.1 billion transistors on 32nm process technology
- 33 percent higher system bandwidth improvement with higher bus speeds (QPI and SMI)
- Next-generation architecture with new data and instruction pipelines, floating-point pipeline and instruction buffers
- 2x max execution width vs. current architecture from 6- to 12-issue
- Advances in reliability, availability and serviceability (RAS) features
- Improved power management features and reduced overall socket power consumption
- Pin compatibility with the current Intel Itanium 9300 Processor Series

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