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Evaluation of SMT Polymer Film Capacitors Using Newly Developed, Low Shrinkage PET

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ABSTRACT

Advances in polymer film dielectric technology, coupled with a revolutionary processing system has made possible high value and miniaturized electrostatic capacitors which compete favorably against ceramic and tantalum capacitors in many critical applications.

The challenge over the last several years has been to make polymer film capacitors both smaller in size and also suitable for high temperature surface mount reflow soldering processes. Most thin polymer films are intentionally biaxially orientated at elevated temperature during their manufacture. This results in relatively high linear shrinkage factors should the unsupported film be heated (such as is the case during component surface mounting by reflow soldering methods). Recently, Hoechst-Diafoil, a world leader in thin polymer film technology, announced a modified PET material (Hostaphan SMD Re) which features significantly lower shrinkage characteristics at elevated temperature. Hoechst's intent is to provide a surface mount compatible film while avoiding the use of exotic and expensive films such as PEN or PPS. Paktron's evaluation objective is to make use of the properties of this low shrinkage PET to make high density chip capacitors at both low and high voltage with an incremental stability improvement over the current generation PET.

BACKGROUND

The move to surface mount reflow soldering has created an application gap because of the incompatibility of traditional metallized film capacitor technology with the inherent thermal stresses of most surface mounting methods. To meet the changing needs of its customers, the polymer film capacitor industry has been doing extensive research and development on the production of a truly practical, surface mountable, metallized polymer film capacitor. Multilayer ceramic and tantalum capacitors have previously been the only types of capacitor used in volume for such applications, but as more critical circuit applications such as RFI filtering, Sample and Hold, EMI suppression or LC ripple voltage conditioning are transferred to using the surface mount construction technique, many engineers have found that they now require certain electrical performance characteristics that can only be obtained from polymer film capacitors.

Polymer film dielectric capacitors are sought after for both thru-hole and surface mount applications because of their electrical stability, power-handling capability and proven reliability. As the types of applications using surface mount components has shifted from being strictly signal processing or low power type applications to those which actually do power handling, the necessity of having film chip capacitors has become paramount. These new power-handling applications require inherent reliability under high dv/dt or di/dt usage and are therefore helping drive the need for surface mount film chip capacitors. At high voltage levels (48 volt bus through HVAC) ceramic and tantalum capacitors may not be suitable due to severe capacitance roll-off and dissipation factor increases under the application conditions making a film chip capacitor the component of choice.

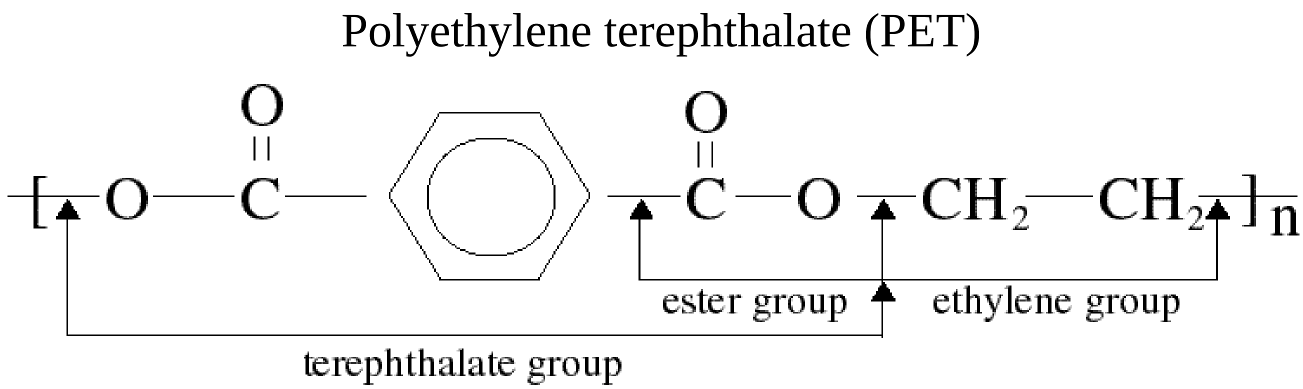


Fig. 1 (Polyester—PET)

Film capacitors that are produced by the conventional "winding" process are highly suspect to film shrinkage at elevated temperature and for this reason surface mounting has been an insurmountable challenge for most film capacitor companies. The Paktron division of Illinois Tool Works recognized this limitation of biaxially orientated films and took this into account while developing a new system to make film chip capacitors. In the process of making linear stacks of polymer film, the memory of the film is partially "erased" so the finished chip component has limited shrinkage and swelling during surface mount heat exposure. With this memory "erasing", chip capacitors are produced that can withstand reflow soldering methods with the currently specified limitation of 220 degrees Celsius. Combining both the advent of ultra thin polymer dielectric films of 1.4 micron thickness and below and the Interleaf Technology (film chip capacitor) production system has allowed Paktron to meet the industry challenge of smaller size and surface mount compatibility. By utilizing the new Hoechst-Diafoil SMD Re film, its improvements to the thermo-mechanical properties of the polymer film will further contribute to the stability of film-chip capacitors through reflow soldering systems.

DIELECTRIC FILM PRODUCTION

The dielectric used in the manufacture of film capacitors is a polymer. A polymer is a string of small molecules called monomers that are chemically linked to form a large, or macromolecule. The workhorse dielectric for DC film capacitors is a polymer called polyethylene terephthalate. It is more commonly referred to as polyester or PET. Polyester has a hydrocarbon backbone that contains ester linkages, hence the common name (see Figure 1). Polyester is a synthetic polymer, made by combining (linking) thousands of monomers into long chains through a process called polymerization. The typical structure of a single molecule is chain-like or in more chemical terms an expanded random coil (see Figure 2). In such a molecular system the atoms of the system exert forces on one another due to various physical interactions. This exertion leads to a continual change in the molecule's structure (i.e. conformations). The shape and structure of the molecular system has a direct bearing on both its chemical and mechanical characteristics.

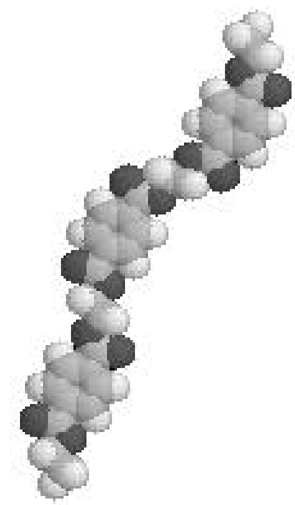


Fig. 2 (PET macromolecule)

In various forms, polyester is one of the most commonly used and versatile polymers in the world. It is used in a multitude of products. In its plastic form polyester is used to produce bottles, decorative balloons, microwave wrap, packaging and numerous types of film including capacitor grade. In its fiber form polyester is used in the production of carpet and clothing. The composition of polyester's chain structure allows the ester groups of nearby chains to readily line up with each other in crystal form to create strong fibers which are in high demand in the textile industry.

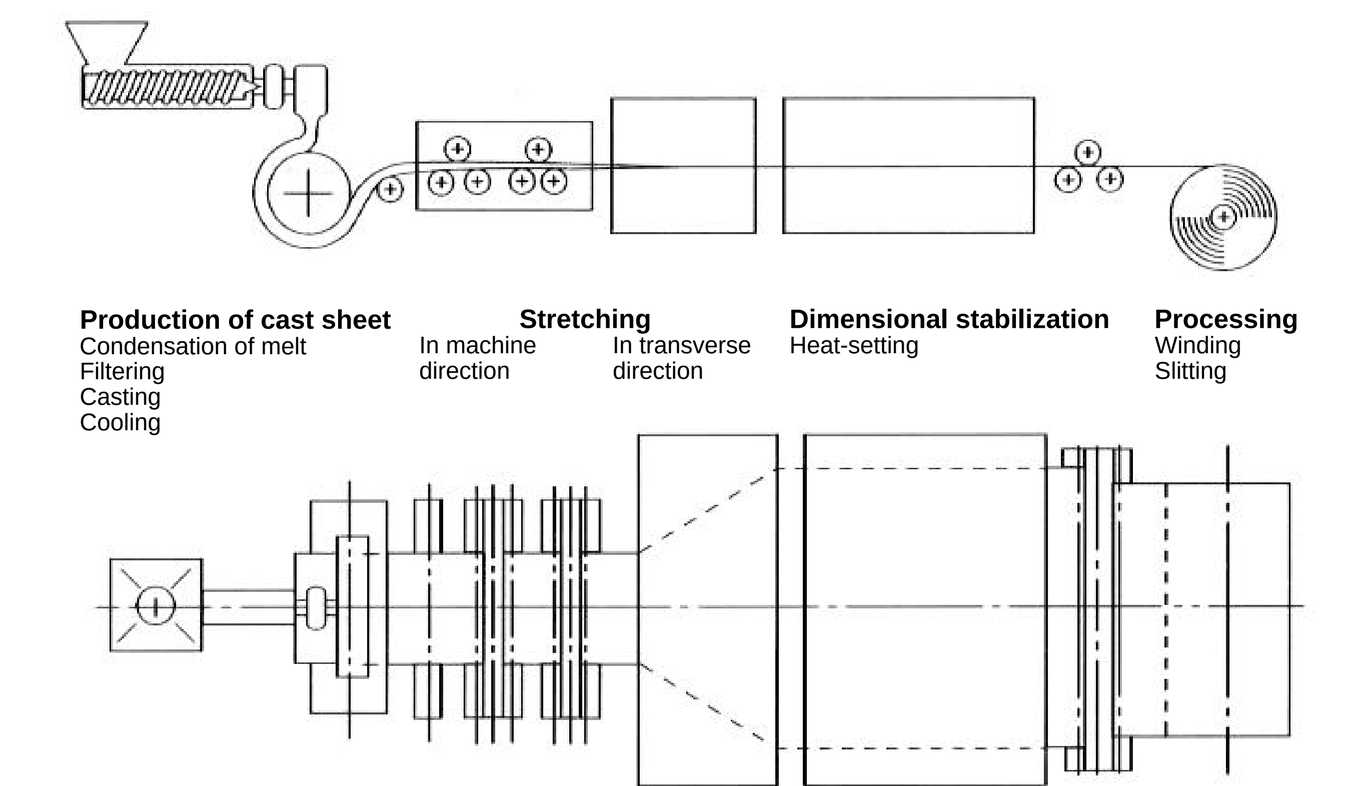


Fig. 3 (courtesy of Hoechst-Diafoil)

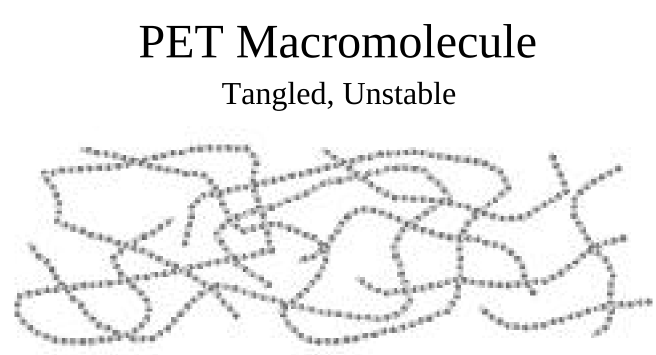


Fig. 4

While polyester is manufactured by a large number of companies throughout the world, the “big three” in capacitor grade film production are Hoechst-Diafoil (Europe/Japan), Dupont (Europe/US) and Toray (Japan). Dupont has been in the business for so long that its trademark name for polyester, Mylar, has become as interchangeable with capacitor grade polyester film as Kleenex (a trademark of Kimberly-Clarke) is with paper tissue or Xerox is with photocopying. Many end-user specifications actually call out Mylar® capacitors in place of the generic term of polyester.

Turning PET resin into a film as thin as 0.000056” (1.4 microns) thick requires an extremely complex set of mechanical processes. Although there are various manufacturer specific nuances in manufacture, PET dielectric grade film is all produced in the same basic three step manner of **forming**, **stretching** and **stabilizing** (see Figure 3). The primary physical (mechanical) difference that is readily discernable between polyester manufacturers, as viewed from a capacitor manufacturer’s prospective, is:

1. The percent crystallization of the film.

2. The additives used to set the surface topology, which defines the mechanical handling characteristics of the film.

3. The cleanliness of the film (the degree of impurities), which, if excessive, is detrimental to the ultimate dielectric strength of the film.

These mechanical differences manifest themselves in variations in the electrical characteristics of the films and in various handling properties.

During the **forming** process the dielectric material is formed into a continuous film or cast sheet. At this point the material is a relatively thick, highly amorphous and isotropic film. The chain structure is un-orientated (tangled) and highly unstable at this stage (see Figure 4).

During the **stretching** process the macromolecules in the film start out being randomized with no or little orientation. The film is stretched first in the machine direction (MD) and then in the transverse direction (TD). This stretching orientates the film so that the chain segments orientate themselves in the direction of the stretch (see Figure 5). At this point the film is now relatively stable, but will shrink if subjected to any thermal exposure.

During the **stabilizing** process the film is subjected to a thermal treatment (thermo-setting or heat-setting) which establishes cross-links between the orientated molecular chains (see Figure 6). This stabilizing provides for the reduced shrinkage during any subsequent thermal exposures such as the tempering process used by capacitor manufacturers.

INTERLEAF® TECHNOLOGY

The Interleaf Process utilizes wide webbed rolls of material, completely metallized on one side. In the first production step, eight minute safety margins are laser ablated (demetallized) along the length of the film. The two margined rolls are then wound together on a large diameter wheel while being precisely slit into eight segments. This "winding" process creates eight separate stacks of well-aligned film that are called ropes. The ropes are cut to a consistent length, then loaded into fixtures and placed under high pressure. Pure aluminum is deposited on the rope edges which penetrates into the very small but precise film extensions to provide a highly conductive termination consisting of like metals. After a "reforming" process under high level thermal and pressure conditions (Patent #4741876), the dielectric film layers are not only laminated together, but also "reformed" at a molecular level so that their ability to handle any subsequent application of thermal stress has been greatly enhanced. At this point the ropes become perfectly flat, large capacitor "sticks" approximately 19 inches in length. For SMT devices that are directly mounted to the circuit board, a barrier layer is applied to the aluminum end termination and the barrier layer is coated with a lead (Pb) free solderable surface to facilitate board termination. These large stick capacitors are electrically tested and then severed into capacitor "blocks" that are the heart of the finished capacitor. Figure 7 shows the cross section of the capacitor stack to illustrate the construction.

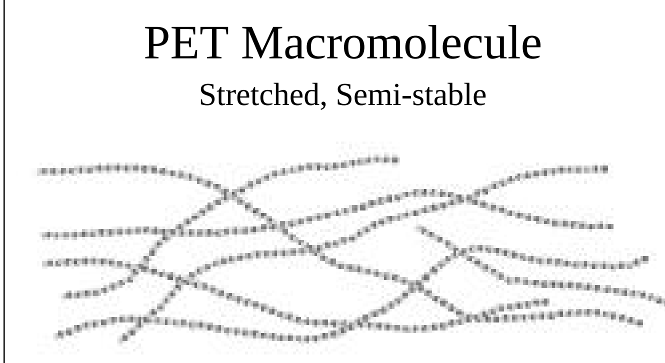


Fig. 5

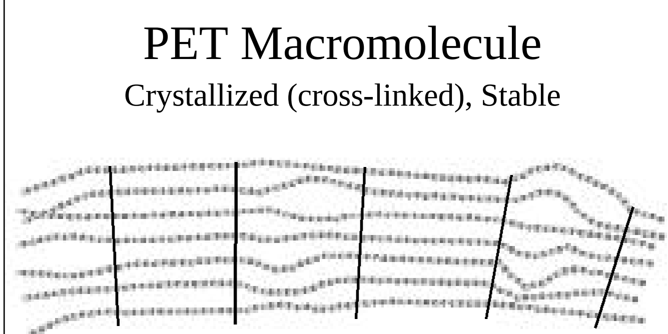


Fig. 6

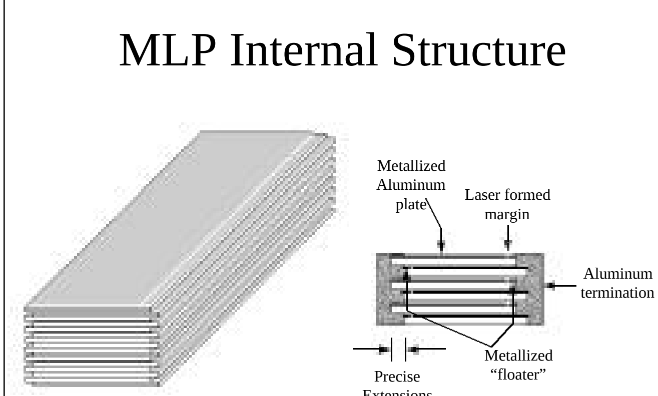


Fig. 7

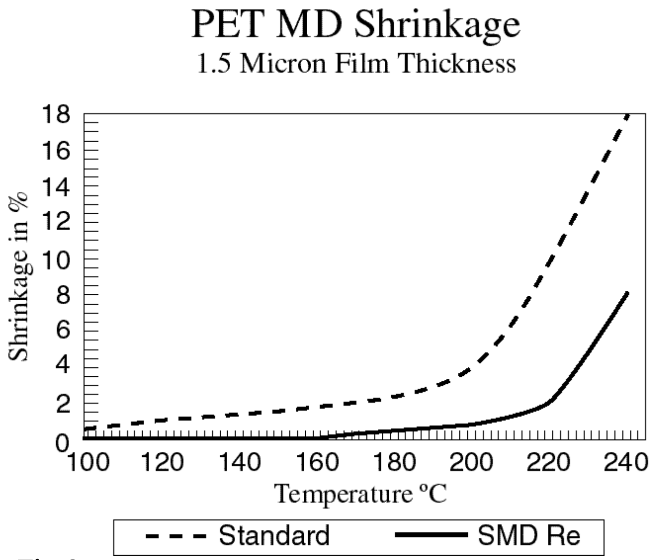


Fig. 8

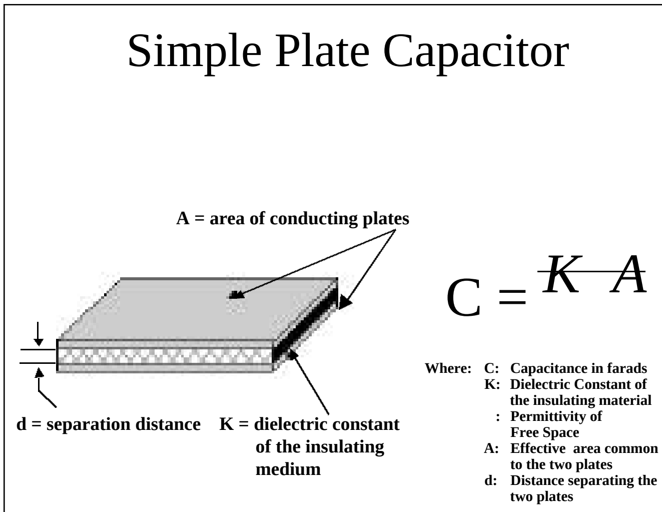


Fig. 9.

SMD RE CAPACITOR FILM

The new Hoechst-Diafoil modified PET film is not in itself a new high temperature film. It is produced with standard PET resin. Its maximum use temperature, physical characteristics and electrical characteristics therefore are identical to that of the Hoechst-Diafoil standard PET film. The difference is that it has had its thermo-mechanical properties altered so that it can be pre-conditioned by the capacitor manufacturer at higher times and temperatures in order to better withstand the rigors of surface mount reflow soldering (see Figure 8).

The Hoechst-Diafoil's SMD Re film modification appears to be, in effect, a material supplier version of Paktron's memory "erasing" process. When biaxially orientated film undergoes thermal exposure at elevated temperatures the cross-links start to dissolve and the molecular chains become mobile (trying to revert to the tangled state). This releases the stresses that were locked in when the film was originally stretched causing shrinkage in unrestrained film. If the film can be restrained during the heat-setting process, given enough time, the molecular chains will find conformations of lower tension (change of entropy), producing a film with a lower shrinkage potential. Because the film will shrink less, capacitor manufacturers can precondition their capacitors at elevated temperatures without concern of damaging physical deformations and excessive loss of capacitance. The exact thermos exposures are time and temperature dependent, but would be at such a level to allow the capacitor to withstand reflow soldering. There are upper limits to this preconditioning as excessive times or temperatures will cause the film to become brittle (excessive crystallization) and adversely effect both its mechanical and electrical characteristics.

In order to understand the significance of having a lower shrinkage film it is necessary to understand how shrinkage effects the capacitor. A layered polymer film capacitor is manufactured by stacking hundreds to thousands of layers of metallized film with offset alternate layers. This type of capacitor follows the common capacitor formula of:

$$C = n \times \frac{K \times \quad \times A}{d}$$

Where
C is capacitance
n is the number of paired layers
K is the dielectric constant of the system
  is the permittivity of free space
A is the common area between layers
d is the distance between layers.

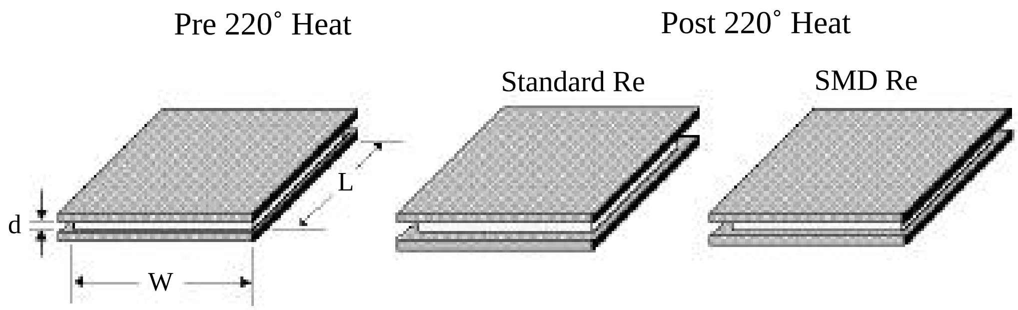
If A (which is L in the machine direction (MD) times W in the transverse direction (TD)) is reduced because of shrinkage, so too is the capacitance value. Excessive shrinkage will reduce the capacitance value to unacceptable levels.

The differences in standard PET film and the SMD Re film become very evident when tested per DIN 40634, under the test conditions of 220˚C for 15 minutes with an unrestrained single layer test sample.

At 220˚C, after 15 minutes of exposure, unrestrained standard PET will shrink by 19.2% in the machine direction and 4.1% in the transverse direction. Using the simple C = K * * A / d, and ignoring any changes in d, the capacitance value of the capacitor would change from a base of 1 to 0.775 for a drop of 22.5%.

Relative Shrink Comparisons

1.4 Micron PET



$C_0 = K * A/d$	$C_1 = K * A/d$	$C_1 = K * A/d$
$C_0 = K * L * W/d$	$C_1 = K * L * W/d$	$C_1 = K * L * W/d$
$C_0 = K * 1 * 1/0.000056$	$C_1 = K * 0.808 * 0.959/0.000056$	$C_1 = K * 0.936 * 0.980/0.000056$
$C_0 = K * 17857.14$	$C_1 = K * 13837$	$C_1 = K * 16380$
let $C_0 = 1$	$C_1 = 0.000056 * 13837$	$C_1 = 0.000056 * 16380$
$d = 0.000056$	$C_1 = 0.775$	$C_1 = 0.917$

Fig. 10

At 220˚C, after 15 minutes of exposure, unrestrained modified PET (SMD Re) will shrink by 6.4% in the machine direction and 2.0% in the transverse direction. Using the simple $C = K * \quad * A / d$, and ignoring any changes in d, the capacitance value of the capacitor would change from a base of 1 to 0.917 for a drop of only 8.3%.

When looking at these change of capacitance values it must be kept in mind that under standard reflow conditions, the parts will only be exposed to 220˚C for 1 minute and therefore the capacitance changes would be much less than the above two examples.

THERMAL WITHSTANDING

Using test boards like that shown in Figure 11 and a convection reflow solder profile as shown in Figure 12, the data table in Figure 13 represents testing done on the usability of PET film chip capacitors when board attached using convection reflow soldering.

As can be seen by the data table (see Figure 13), the parts easily withstood the rigors of surface mounting with little change in electrical parameters.

Any part failure caused by overheating in reflow soldering will be evident as an immediate electrical reject, usually a low capacitance failure. Other than this process-related phenomenon, no other long term aging characteristics are known that would effect usability.

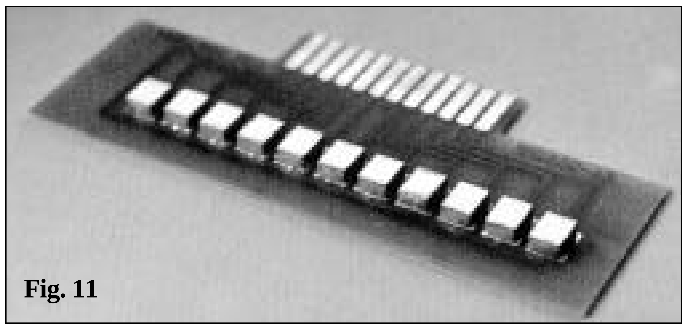


Fig. 11

Convection Reflow Profile (Typical)

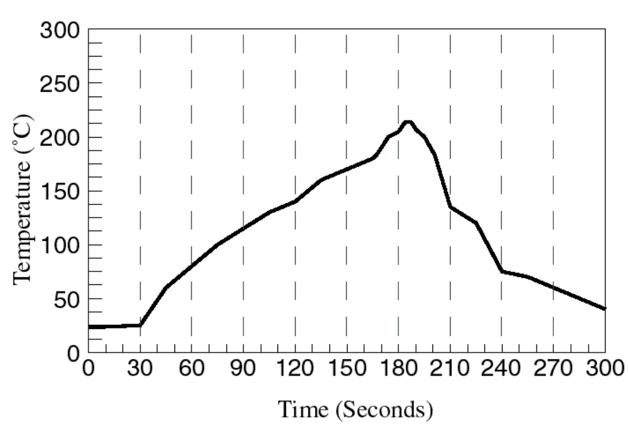


Fig. 12

Convection Reflow Test Results (2824 PET)

Type Test	Convection Reflow
Part Number	105K100ST2824, SMD Re
Part Description	1.00µ.fd, 100 RVDC, ST, 2824

	Pre Test		Post Test		
Unit No.	Cap (µfds)	DF (E-4)	Cap (µfds)	DF (E-4)	Cap (%Δ)
1	1.057	49	1.0566	57	-0.04
2	1.042	55	1.0415	59	-0.05
3	1.073	53	1.0720	58	-0.09
4	1.059	50	1.0586	55	-0.04
5	1.040	54	1.0362	59	-0.36
6	0.997	57	0.9941	61	-0.28
7	1.032	65	1.0265	64	-0.53
8	1.080	53	1.0790	58	-0.09
9	1.035	52	1.0346	58	-0.04
10	1.041	53	1.0408	58	-0.02
11	1.074	56	1.0287	57	-0.32
12	1.008	58	1.0707	55	-0.31
Max	1.080	65	1.0790	64	-0.53
Avg.	1.044	54	1.0417	59	-0.14
Min	0.997	49	0.9941	55	-0.02

Fig. 13

Tests indicate that the thermal withstanding capability of the polyester based chip capacitors is more than adequate for reflow solder surface mount applications. As can be seen in Figure 14, reflow soldering at 220˚C for less than three minutes will have minimal effect on capacitance value. Since the standard convection reflow system would subject these capacitors to less than 220˚C for less than 1 minute, the percent change in capacitance would be under 0.5%.

PERFORMANCE AND RELIABILITY DATA

Unlike capacitors made with other dielectric systems, polymer film capacitors are designed and tested for use at 100% of rated voltage at rated temperature. To accomplish this, they are subjected to established reliability testing of 125% of rated voltage at the maximum rated temperature. Statistically reducing the data back to actual use temperatures and voltages allows the users to determine the MTBF of their application. The inherent reliability of polymer film capacitors is so high that it should be one of the least concerns that the equipment designer has in computing MTBF.

After being surface mounted on a number of test boards, the capacitors were subjected to accelerated dry life testing to ascertain their long term reliability. A summary of one such test is shown in Figure 15.

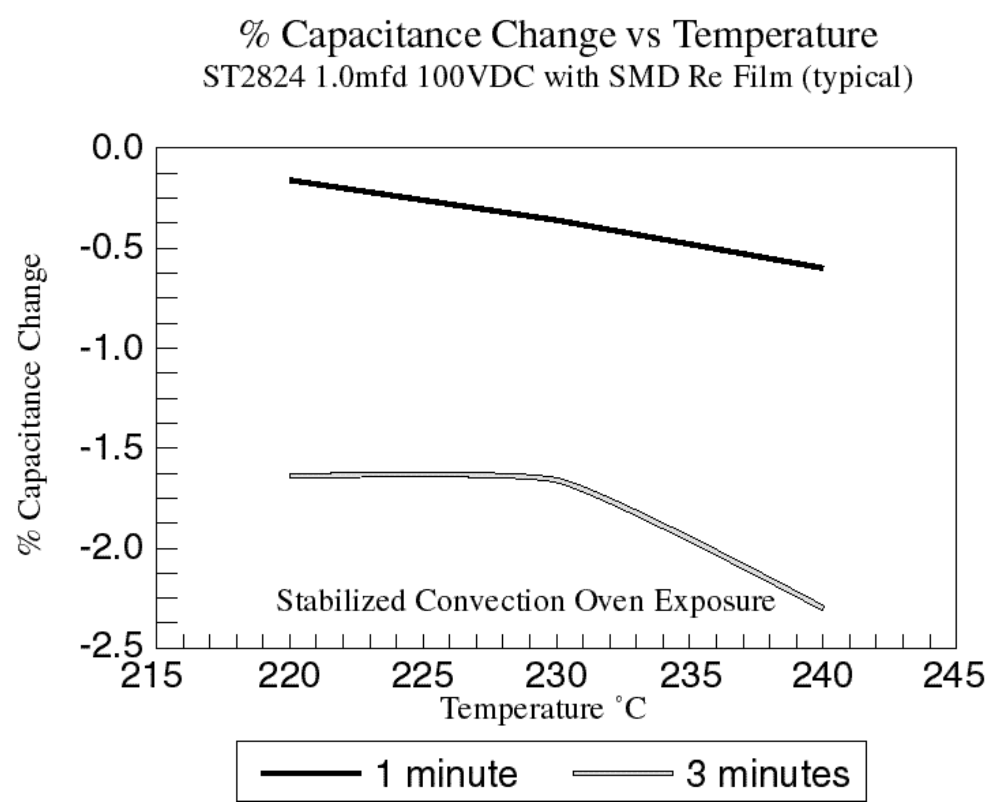


Fig. 14

Capacitor Level Testing			
Type Test	Accelerated Dry Life		
Parameters	85˚C/125VDC/1000Hrs		
Part Number	105K100ST2824, SMD RE		
Part Description 2824	1.0 fd, 100 Rated VDC, ST,		
Averages	Cap	%DF	IR
Pre	1.063	<.60	>3,000Meg

Fig. 15

Multiple sets of accelerated testing are done in order to accumulate significant number of component working hours. From these millions of component working hours it is then possible to statistically derive the potential percent failure rate of the capacitors under various conditions. The data table in Figure 16 shows just how low this potential rate currently is for standard polyester based surface mount film capacitors. Since the surface mount style capacitor is relatively new, it does not yet have the 10's to 100's of millions of component hours of test time that is normally associated with film capacitors. As further testing is completed to increase the total component test time, the % failure rate will continue to drop.

% Failure Rate per 1000 Hours @ 90% Confidence Level			
	@%RVDC and 40˚C		
Part Number	50%	75%	100%
105K100ST2824	0.0000	0.0003	0.0015

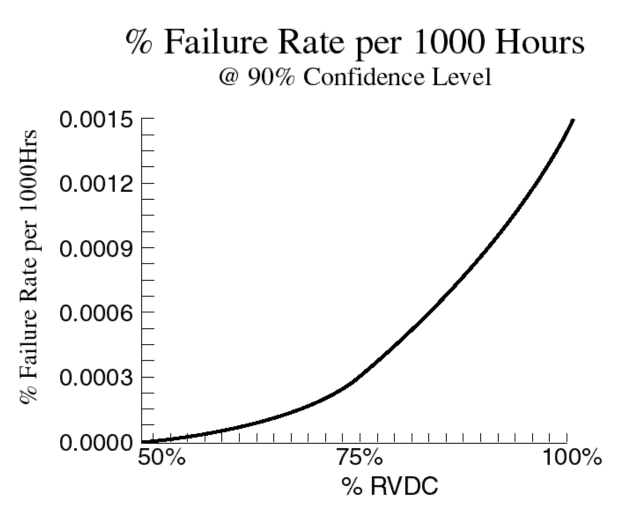


Fig. 16

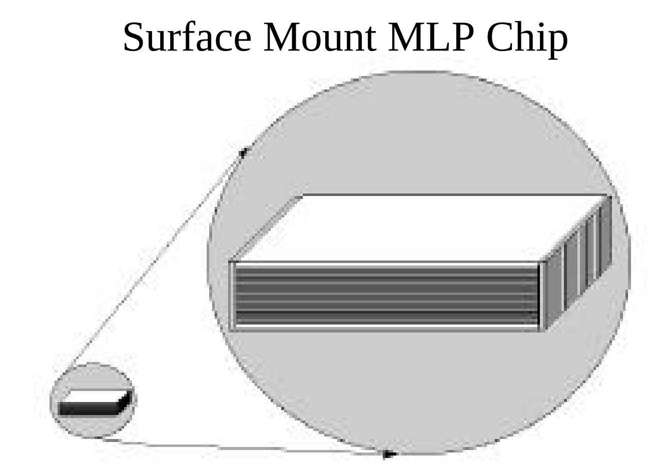


Fig. 17

SUMMARY

The new Hoechst-Diafoil modified PET film, when combined with the Interleaf manufacturing system, will allow for the production of film chip capacitors in surface mount packages that are fully compatible with standard convection reflow process parameters.

Having a polymer film capacitor which can withstand the extremes of standard mass production solder reflow processing rather than forcing the end user into an off-line, manual attachment system will allow the component engineer access to the reliability and performance characteristics available only with polymer film capacitors.

While many film capacitor manufacturers have tried to address this problem by using the same standard capacitor cartridge as used with their leaded parts, along with a bulky protective enclosure and special terminations for board attachment, Hoechst-Diafoil's SMD Re PET film modification will allow for the production of true chip film capacitors utilizing a dielectric with an abundance of history in terms of its reliability and performance.

REFERENCES

1. Dr. Holger Kliesch & Annegrete Bursch, "Hostaphan SMD, A PET film offering good performance in SMD Capacitors", CARTS Europe, October, 1997