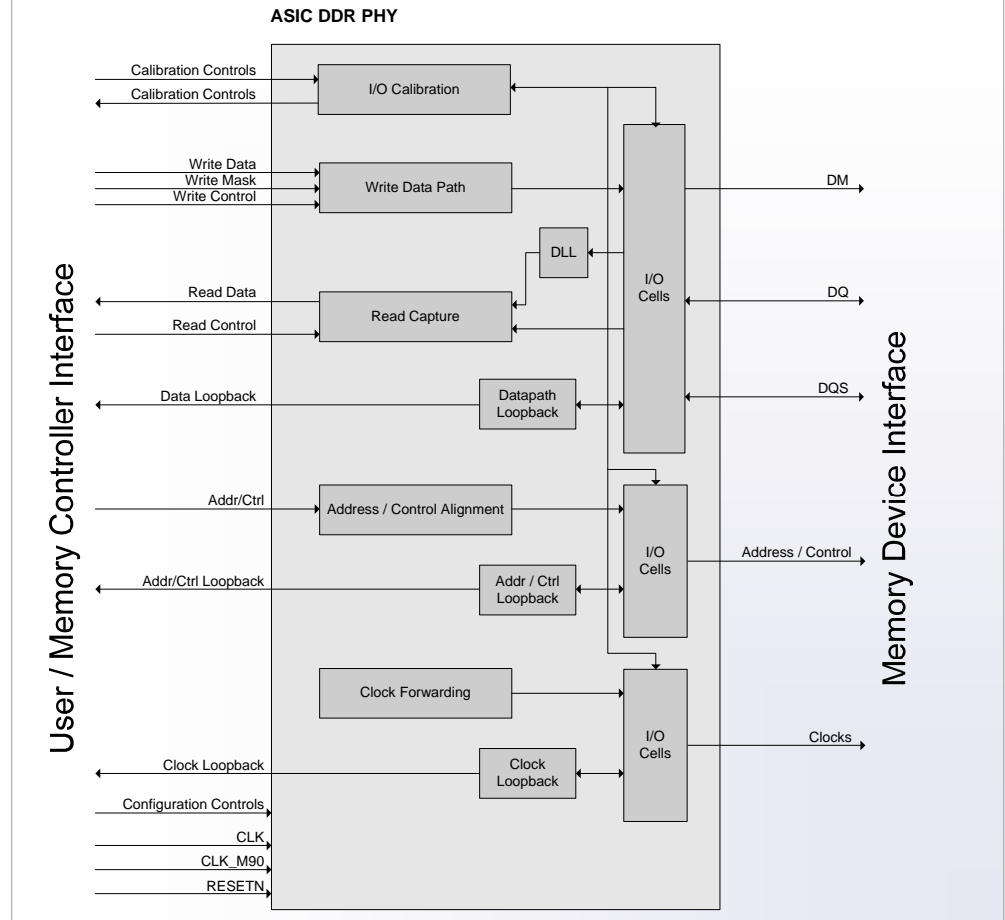**NORTHWEST LOGIC**

Product Highlights

- Silicon-proven DDR PHY for use in ASICs

- Supports DDR3 SDRAM 1333, DDR2 SDRAM 1066, DDR SDRAM 800, Mobile DDR SDRAM 400 SDRAM, RLDRAM II 1066 Mbit/s/pin operation

- Uses robust windowing data capture method

- Uses proven off-the-shelf DDR I/O and DLL

- Supports Byte and Nibble DQS

- Supports a broad range of programmable features including timing, termination, drive strengths, etc.

- Supports DFT and JTAG boundary scan

- Supports comprehensive loopback testing via add-on BIST Core

- Provided as a soft core with timing constraints enabling optimization for a target process and pinout

- Customization and Integration services available

Block Diagram

Product Overview

The combination of Northwest Logic's Memory Controller Cores and ASIC DDR PHY is designed for use in ASICs requiring high memory throughput, high clock rates and full programmability.

Versions of the ASIC DDR PHY are available which support DDR3 SDRAM 1333, DDR2 SDRAM 1066, DDR SDRAM 800, Mobile DDR SDRAM 400 SDRAM, RLDRAM II 1066 Mbit/s/pin operation. Multi-mode versions are also available.

To ensure robust operation the DDR PHY uses a windowing data capture method, uses proven off-the-shelf DDR I/O and DLL, and supports ASIC-side ODT and calibrated output impedance.

The DDR PHY is specifically designed for flexibility. This includes a broad range of programmable features including various timing parameters, termination settings and drive strengths.

The DDR PHY can be put into loopback for complete, at-speed production test. This test is orchestrated by the BIST Core in conjunction with the Memory Controller Core. The DDR PHY also supports DFT scan and JTAG boundary scan.

The combination of the Memory Controller Core and DDR PHY can be fully tested using Northwest Logic's Memory Test Core and Data Analyzer Core. The Memory Test Core provides a complete memory test using random and directed reads and writes. The Data Analyzer Core provides access to the actual and expected memory test results for analysis.

The DDR PHY is delivered as a soft core with timing constraints. This enables the DDR PHY to be optimized for a target process and pinout.

Northwest Logic can provides DDR PHY related services including DDR I/O and DLL replacement, process porting and DDR PHY hardening. Contact Northwest Logic for a quote.

Product Deliverables:

- Core (Netlist or Source Code)
- Timing constraints
- Comprehensive Verification Suite (Source Code)
- Complete Documentation
- Expert Technical Support & Maintenance Updates