Technical Note

Low-Power Versus Standard DDR SDRAM

Introduction

This technical note provides an overview of the initialization and clocking differences between low-power DDR SDRAM and standard DDR SDRAM and low-power DDR SDRAM features, such as temperature-compensated self refresh (TCSR), partial-array self refresh (PASR), deep power-down (DPD), and clock stop mode, that are not found in standard DDR SDRAM.

Designing hybrid systems that use either low-power DDR SDRAM or standard DDR SDRAM is a common practice. Understanding the functional and architectural differences between the two types of DDR SDRAM memory devices can enhance the design of these systems.

Differences Between Low-Power and Standard DDR SDRAM

Below is a list of functional and architectural differences between low-power DDR SDRAM and standard DDR SDRAM devices:

- Initialization
- Input/output
- Clocking (CAS latency)

Initialization

Table 1 on page 2 describes the key initialization differences between low-power DDR SDRAM and standard DDR SDRAM.

Table 1: Initialization Differences Between Low-Power DDR and Standard DDR SDRAM

Initialization Steps	Low-Power DDR SDRAM	Standard DDR SDRAM
Step 1	Power up V_{DD} and $V_{DD}Q$ simultaneously	Power up V_{DD} and $V_{DD}Q$ simultaneously, and then apply to V_{REF} and V_{TT}
Step 2	Prior to applying any command, apply 200µs delay after CKE HIGH	Apply 200µs delay; after 200µs, issue NOP or DESELECT command followed by CKE HIGH
Step 3	Issue a PRECHARGE ALL command	Issue a PRECHARGE ALL command
Step 4	Issue NOP or DESELECT for at least ^{t}RP time	Wait ^{t}RP, and then use LOAD MODE REGISTER command to program the extended mode register to enable delay-locked loop (DLL) and to set drive strengths
Step 5	Issue AUTO REFRESH command followed by NOP for ^{t}RFC time	Wait at least ^{t}MRD time followed by LOAD MODE REGISTER command to program the mode register to set operating parameters and to reset DLL; at least 200 clock cycles are required between a RESET and any READ command
Step 6	Issue LOAD MODE REGISTER command	Wait at least ^{t}MRD time followed by a PRECHARGE ALL command; wait ^{t}RP time
Step 7	Issue NOP or DESELECT command for at least ^{t}MRD time	Issue an AUTO REFRESH command followed by NOP for^{t}RFC time
Step 8	Issue LOAD MODE REGISTER command	Issue an AUTO REFRESH command followed by NOP for^{t}RFC time
Step 9	Issue NOP or DESELECT command for at least ^{t}MRD time	Issue LOAD MODE REGISTER command to clear the DLL bit; use the same operating parameters as described in Step 5

Notes: 1. See product-specific data sheets for detailed information on initialization.

Although the initialization steps for low-power DDR SDRAM and standard DDR SDRAM seem identical, some differences, such as command sequences, should be accounted for when designing hybrid systems.

Both low-power DDR SDRAM and standard DDR SDRAM power up V_{DD} and $V_{DD}Q$ simultaneously, but with standard DDR SDRAM, the system is also required to provide power to V_{REF} and V_{TT}.

Another difference between the two forms of DDR SDRAM is the way the LOAD MODE REGISTER command is used. In standard DDR SDRAM, the LOAD MODE REGISTER command is used to set delay-locked loop (DLL) along with other parameters, such as drive strengths.

Differences also exist in the sequences used for loading the LOAD MODE REGISTER command. For example, in standard DDR SDRAM, the LOAD MODE REGISTER command is issued after the PRECHARGE command; however, in low-power DDR SDRAM, the LOAD MODE REGISTER command is issued PRECHARGE, followed by AUTO REFRESH, and then followed by LOAD MODE REGISTER.

Input/Output

The implementation of the LVCMOS interface is simple and has very minimal DC-power consumption. It provides steady high and low signals; however, due to the uncertainty in its threshold voltages, input/output buffers require a higher voltage swing to ensure reliable switching.

DDR SDRAM uses the JEDEC standard 2.5V (SSTL_2 compatible) inputs and outputs. Benefits of the SSTL_2 interface include symmetrical LOW and HIGH logic levels, improved signal integrity, and better noise immunity. Also, SSTL_2 assumes transmission lines to have termination. For high-speed signaling, it is important to have termina-

tion to reduce reflections, noise, and timing margins. Because standard DDR SDRAM runs at a higher speed than low-power DDR SDRAM, it is logical to use the SSTL_2 interface for standard DDR SDRAM inputs and outputs.

Clocking Differences

Standard DDR SDRAM uses delay-locked loop (DLL) circuitry that aligns the data with the clock edge; however, due to the power consumption constraints on low-power DDR SDRAM, DLL circuitry was removed from low-power DDR SDRAM. In the case of low-power DDR SDRAM, data fires from the CLK HIGH pulse and arrives ^{t}AC later. This results in valid data prior to the rising edge of the clock on low-power DDR SDRAM. Figure 1 on page 3 and Figure 2 on page 4 highlight the data clocking differences between low-power DDR SDRAM and standard DDR SDRAM.

Clock jitter is not specified on the low-power DDR SDRAM data sheets due to the absence of the DLL circuit. JEDEC does not specify this parameter on low-power DDR; however, scenarios exist where clock jitter can be calculated. For instance, for tCK of 7.5ns and assuming a 50 percent duty cycle (^{t}CL = 3.0ns and ^{t}CH = 3.0ns), allowable clock jitter on the rising or falling edge is calculated as follows:

Clock jitter = ^{t}CK - ^{t}CL - ^{t}CH

Clock jitter = 7.5ns - 3ns - 3ns = 1.5ns

Figure 1: CAS Latency of Low-Power DDR SDRAM

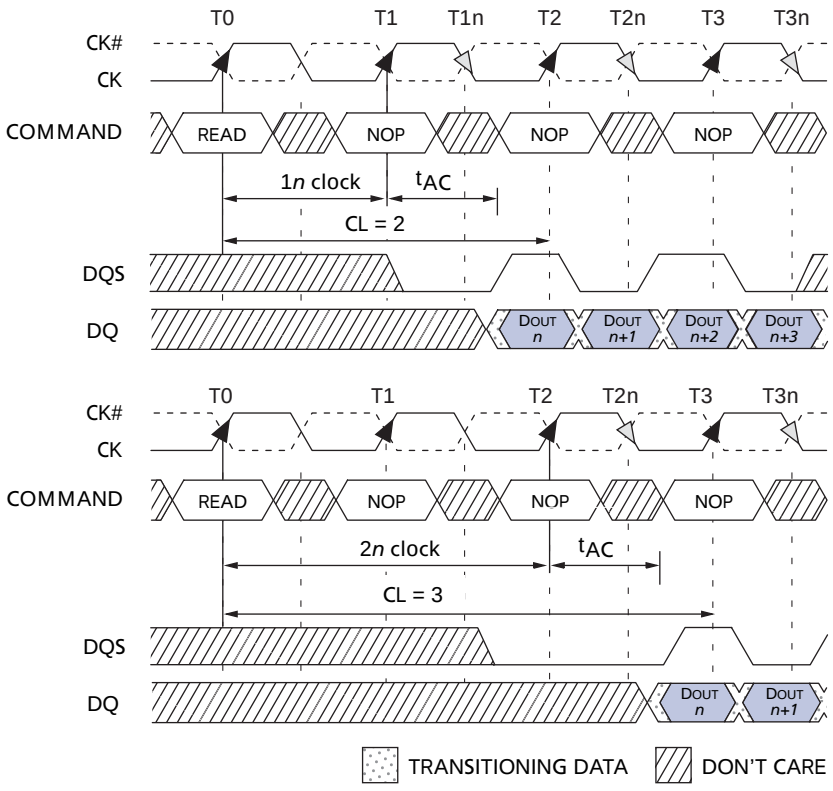
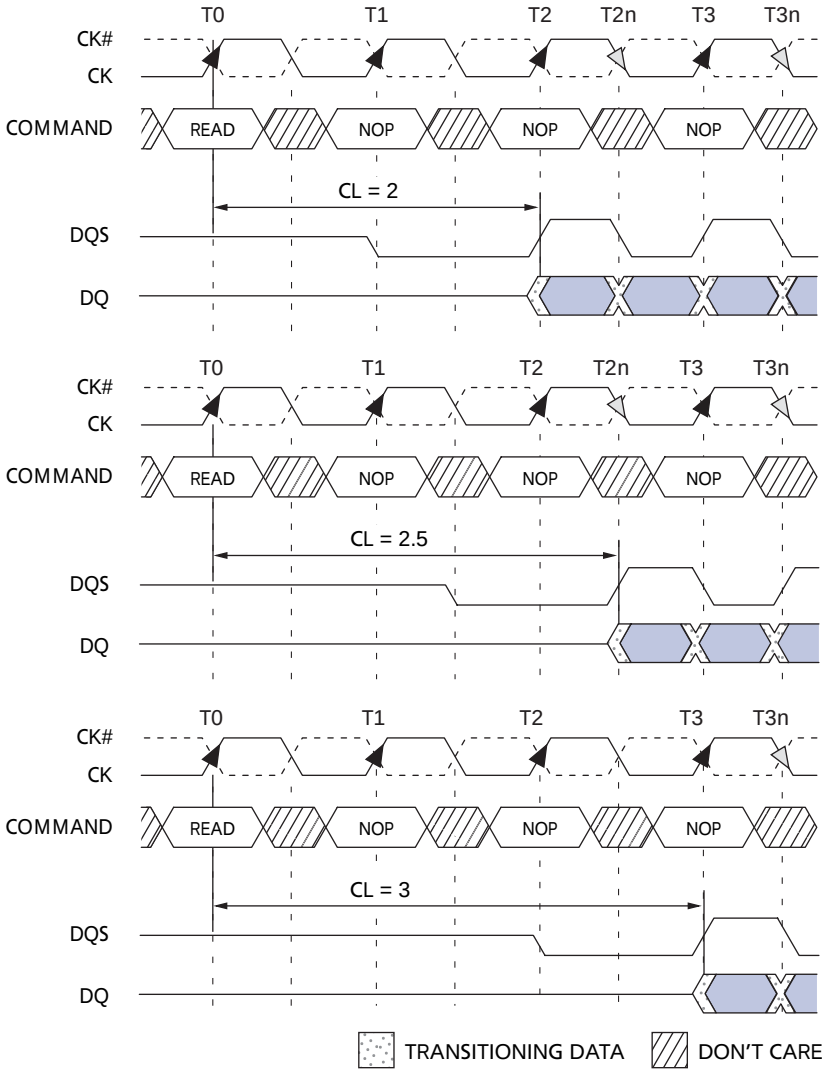


Figure 2: CAS Latency of Standard DDR SDRAM



Exclusive Features of Low-Power DDR SDRAM

The following features are exclusive to low-power DDR SDRAM:

- Temperature-compensated self refresh (TCSR)
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- Clock stop mode

Temperature-Compensated Self Refresh

Low-power DDR SDRAM uses an on-chip temperature sensor that controls the refresh interval based on the device temperature. Programming the JEDEC-standard TCSR bits will not have an effect on the device. The on-chip self refresh oscillator will continue to refresh the array at the factory-optimized rate for the device temperature. TCSR only applies to the self refresh mode and not to the auto refresh mode.

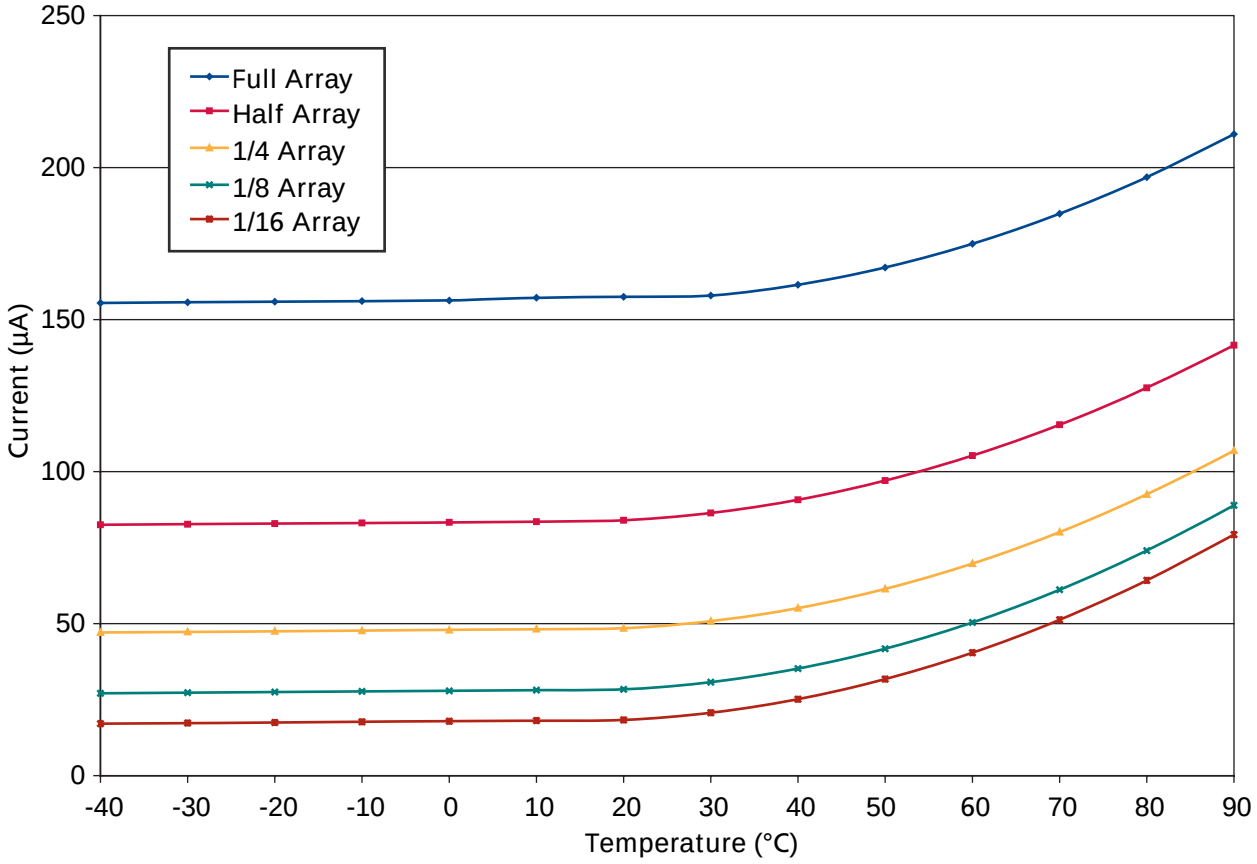
Partial-Array Self Refresh

For power savings, the PASR feature enables the controllers to select the amount of memory that will be refreshed during the self refresh. The refresh options include the following:

- Full array: banks 0, 1, 2, and 3
- Half array: banks 0 and 1
- One-quarter array: bank 0
- One-eighth array: bank 0 with row address MSB = 0
- One-sixteenth array: bank 0 with row address MSB and MSB-1 both equal to zero

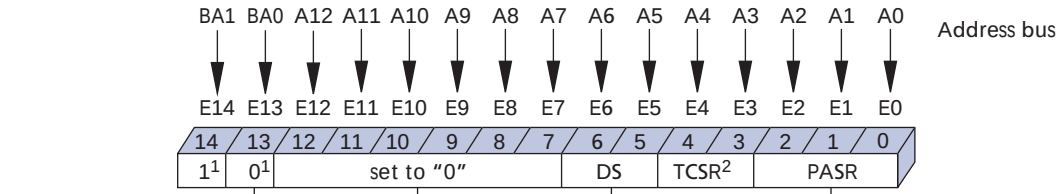
Figure 3 shows the self refresh current response of different PASR configurations.

Figure 3: Typical Self Refresh Current Response to LP DDR Operating Temperature (512Mb)



The self refresh current decreases with the amount of array that is being refreshed. Also, with any given PASR option, the current increases as the temperature increases. At higher temperatures, the array is refreshed more frequently. Depending on which PASR option is selected, data will not be retained in the portion of arrays that are not refreshed. The memory controller must access only the selected portion of the array. PASR can be enabled by setting bits 0–2. These bits are shown in Figure 4 on page 6.

Figure 4: Low-Power DDR SDRAM Extended Mode Register



E	E13	Mode Register Definition
0	0	Standard mode register
0	1	Reserved
1	0	Extended mode register
1	1	Reserved

E6	E5	Driver Strength
0	0	Full-strength driver[3]
0	1	Half-strength driver
1	0	Quarter-strength driver
1	1	One-eighth-strength driver

E12	E11	E10	E9	E8	E7		
0	0	0	0	0	0	Valid	Normal operation
–	–	–	–	–	–	–	All other states reserved

E2	E1	E0	Partial-Array Self Refresh Coverage
0	0	0	Full array (all banks)[3]
0	0	1	Half array (BA1 = 0)
0	1	0	Quarter array (BA1 = BA0 = 0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	One-eighth array (BA1 = BA0 = row address MSB = 0)
1	1	0	One-sixteenth array (BA1 = BA0 = row address MSB = 0)
1	1	1	Reserved

Notes:
1. E14 and E13 (BA1and BA0) must be "1,0" to select the extended mode register (vs. the standard mode register).
2. On-die temperature sensor is used in place of TCSR. Setting these bits will have no effect.
3. Default setting.

Deep Power-Down

Low-power DDR SDRAM offers a deep power-down (DPD) feature that effectively cuts the power to the array and decreases leakage current. Applications that do not require data retention can use the DPD feature while the system power is maintained. Data is not retained after the device enters DPD mode.

Before entering DPD mode, all banks must be in an idle state with no activity on the data bus (^{t}RP time must be met). This mode is entered by holding CS# and WE# LOW, with RAS and CAS HIGH at the rising edge of the clock while CKE is LOW. CKE must be held LOW to maintain the DPD mode, and clock must be stable prior to exiting DPD mode. Exit DPD mode by asserting CKE HIGH with either a NOP or DESELECT command present on the command bus. Upon exiting DPD mode, 200µs of valid clocks with either NOP or DESELCT commands present on the command bus are required. Also, a PRECHARGE ALL command and a full DRAM initialization sequence is required.

Clock Stop Mode

The clock stop mode feature enables power savings in applications due to fewer possible transitions on clock path. Power savings can be achieved by initiating either of the following methods:

- Change the clock frequency when the data transfers require a different rate of speed
- Hold CKE HIGH, with CK LOW and CK# HIGH for the full duration of clock stop mode

Both methods are specific to the application and its requirements, and both methods enable power savings due to the possibility of fewer transitions on the clock path.

Low-power DDR SDRAM enables the clock to change frequency during operation, but only if all the timing parameters are met and all the refresh requirements are satisfied.

The clock can also be stopped altogether if no data accesses, either WRITEs or READs, are in progress that would be affected by this change; for example, if a WRITE or a READ is in progress, the entire data burst must be through the pipeline prior to stopping the clock. CKE must be held HIGH with CK = LOW and CK# = HIGH for the full duration of the clock stop mode. One clock cycle and at least one NOP is required after the clock is restarted before a valid command can be issued.

Conclusion

This technical note provided an overview of the clocking and initialization differences between low-power DDR SDRAM and standard DDR SDRAM memory devices.

Also, this technical note explained the following low-power DDR SDRAM features that are not found in standard DDR SDRAM:

- Temperature-compensated self refresh (TCSR)
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- Clock stop mode

A DDR SDRAM controller should be able to use the low-power DDR SDRAM device using the same hardware interface, provided that the initialization and clocking differences are accounted for in software.

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