MMC Card Specification

Model Name :

KM032S1CBS

KM032S1CCS

KM064S1DAS

KM128S1EMS

KM256S1EMS

KM256S1FMS

KM512S1EMS

KM512S1FMS

KM01GS1FMS

Ver 1.3

07/08/2004

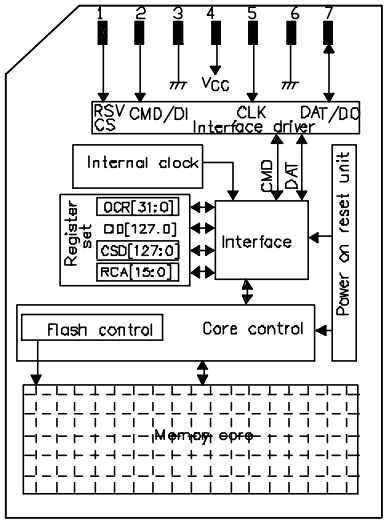
Features

- Capcity:32MB/64MB/128M/256M/512MB/1GByte
- Compliant Specification Ver 3.2
- On card error correction
- Two alternative communication protocols: MultiMedia mode and SPI mode
- Variable clock rate 0~20MHz.
- Voltage range for communication: 2.0~3.6V for operating :2.7~3.6V.
- Low power consumption : automatic power down and automatic wake up, smart power management
- No external programming voltage required.
- Damage free powered card insertion and removal
- High speed serial interface with random access
  ---support dual channels with interleave for flash memory.
  ---FastMDC™ Technology: a cost-effective solution with ultra high performance of flash access time and high reliability of data storage.
- Up to 10 stacked card(at20MHZ,VCC=2.7~3.6V)
- Data Endurance: 100k Program/Erase Cycles
- CE and FCC certificates
- PIP package Technology
- Dimension: 24mm(W)x32mm(L)x1.4mm(T)

Description

These MultiMediaCards are highly integrated flash memories with serial and random access capability. It is accessible via a dedicated serial interface optimized for fast and reliable data transmission. This interface allows several cards to be stacked by through connecting their peripheral contacts. These MultiMediaCards are fully compatible to a new consumer standard, called the MultiMediaCard system standard define in the MultiMediaCard System specification. The MultiMediaCrad system is a new mass-storage system based on innovations in semiconductor technology. It has been developed to provide an inexpensive, mechanically robust storage medium in card form for multimedia consumer applications. MultiMediaCard allows the design of inexpensive players and drivers without moving parts. A low power consumption and a wide supply voltage range favors mobile, battery-powered application such as audio players, organizers, palmtops, electronic books, encyclopedia and dictionaries. Using very effective data compression schemes such as MPEG, the MultiMediaCard will deliver enough capacity for all kinds of multimedia data.

Block Diagram



All units in these MultiMedia cards are clocked by internal clock generator. The interface driver unit synchronizes the DAT and CMD signals from external CLK to the internal used clock signal. The card is controlled by the three line MultiMedia card interface containing the signals: CMD,CLK, DAT(refer to Chapter "Interfaces"). For the identification of the MultiMedia card in a stack of MultiMedia cards, a card identification register (CID) and a relative card address register (RCA) is foreseen. An additional register contains different types of operation parameters. This register is called card specific data register (CSD). The communication using the MultiMedia card lines to access either the memory field or the registers is defined by the MultiMedia crad standard (refer to Chapter "Communication"). The card has its own power on detection unit. No additional master reset signal is required to setup the card after power on. It is protected against short circuit during insertion and removal while the MultiMedia card system is powered up. No external programming voltage supply is required. The programming voltage is generated on card.

These MultiMedia card support a second interface operation mode the SPI interface mode. The SPI mode is activated if the CS signal is asserted (negative) during the reception of the reset command CMD0.(Refer to Chapter "SPI Communication).

Interface

These MultiMedia card interface can operation in two different modes:

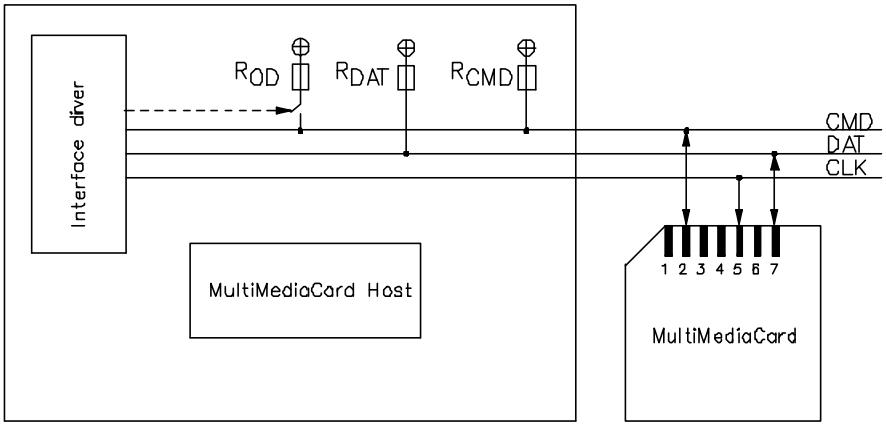
- **MultiMedia card Mode**
- **SPI Mode**

Both modes are using the same pins. The default mode is the MultiMedia card mode. The SPI mode is selected by activating the CS signal and sending the CMD0.

MultiMedia card Mode

In the MultiMedia card mode, all data is transferred over a minimal number of lines:

- **CLK: with each cycle of this signal a one-bit transfer on the command and data lines is done. The frequency may vary between zero and the maximum clock frequency. The MultiMedia card bus master is free to generate these cycles without restrictions in the range from 0 to 20MHz.**
- **CMD: is a bidirectional command channel used for card initialization and data transfer commands. The CMD signal has two operation modes, operation drain for initialization and push pull for fast command transfer. Commands are sent from the MultiMedia card bus master to MultiMedia card and response vice versa.**
- **DAT : is a bidirectional data channel with a width of one line. The DAT signal of the MultiMedia card operates in push pull mode.**
- **RSV: is pulled up with resistor(2MΩ typ) in the MultiMedia card . the external pull-up resistor should be recommended if the system requires.**



MultiMediaCard Mode Interface

All MultiMedia Card are connected directly to the lines of the MultiMedia Card bus. The following table defines the card contacts.

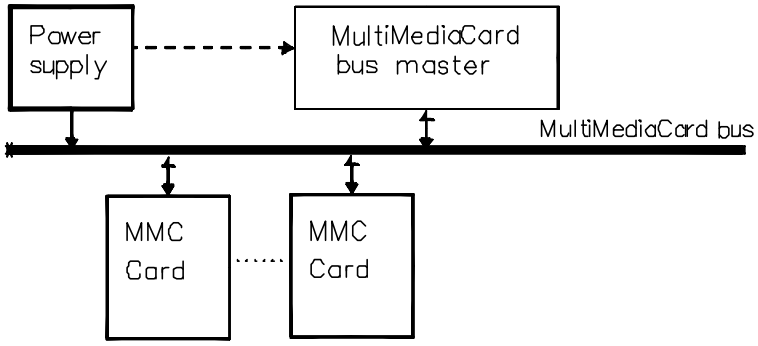
MultiMedia card Mode Pin Definition

Pin No.	Name	Type[1]	Description
1	RSV	NC	Reserved for future use
2	CMD	I/O/PP/OD	Command/Response
3	VSS	S	Supply voltage ground
4	VDD	S	Supply voltage
5	CLK	I	Clock
6	VSS	S	Supply voltage ground
7	DAT	I/O/pp	Data

1). S: power supply; I: input; O: output; PP: push-pull; OD: open-drain; NC: not connected

MultiMedia card Bus Concept

The MultiMedia card is designed to connect either solid-state mass-storage memory devices in a card format to multimedia applications, the bus implementation allows the coverage of application fields from low-cost systems with a fast data transfer rate. It is a single master bus with a variable number of salves. The MultiMedia card bus master is the bus controller and each slave is either a single mass storage card to perform the data transfer.



MultiMediaCard Mode Interface

SPI Mode

The SPI mode consists of a secondary, optional communication protocol which is offered by flash base MultiMEdia cards. This mode is a subset of the MultiMedia card protocol, designed to communicate with a SPI channel, commonly found in Motorola's(and lately a few other vendors) micro-controllers. The interface is selected during first reset command after power up(CMD0) and cannot be changed once the part is power on. The SPI standard defines the physical link only, and not the complete data transfer protocol. The MultiMedia card SPI implementation uses a subset of the MultiMedia card protocol and command set. It is intended to be used by systems which require a small number of cards and have lower data transfer rates. From the application point view, the advantage of SPI mode is the capability of using an off-the-shelf host, hence reducing the design-in effort to minimum. The disadvantage is the loss of performance of the SPI mode versus MultiMedia card mode(low data transfer rate, fewer cards, hardware CS per card etc.).

SPI Mode Pin Definition

Pin No.	Name	Type[1]	Description
1	CS	I	Chip Select
2	DI	I/PP	Data In
3	VSS	S	Supply voltage ground
4	VDD	S	Supply voltage
5	CLK	I	Clock
6	VSS	S	Supply voltage ground
7	DAT	I/O/pp	Data Out

1). S: power supply; I: input; O: output; PP: push-pull; NC: not connected

SPI Interface Concept

The Serial Peripheral Interface(SPI) is a general purpose synchronous serial interface originally found on certain Motirola microcontroller. The MultiMedia card SPI interface is compatible with SPI hosts available on the market. AS any other SPI device the MultiMedia Card channel consists of the following four signals:

- **CS: Host to card chip select signal.**
- **CLK: Host to card clock signal.**
- **DataIn: Host to card data signal.**
- **DataOut: Card to host data signal.**

Another SPI common characteristic are byte transfers, which is implemented in the card as well. All data tokens multiples of bytes(8bit) and always byte aligned to the CS signal.

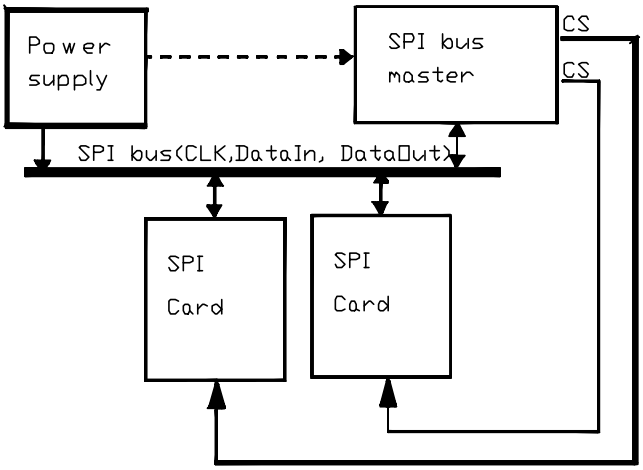
SPI Bus Topology

The card identification and addressing methods are replaced by a hardware Chip Select(CS) signal. There are no broadcast commands. For every command, a card(slave) is selected by asserting the CS signal.

The CS signal must be continuously active for the duration of SPI transaction (Command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.

The bidirectional CMD and DAT lines are replaced by unidirectional dataIn and dataOut signals. This eliminates the ability of executing commands while data is being read or written and, therefore, makes the sequential and multi block read/write operations obsolete. Only single block read/write commands are supported by the SPI channel.

The SPI interface uses the same 7 signals of the standard Multimedia card bus



DC Characteristic

ABSOLUTE MAXIMUM RATINGS

The maximum rating is the limit value that must not be exceeded even at an instant. As long as you use the product within the maximum rating defined, no permanent damage will ever be occurred. However this does not guaranteed the normal logical operation.

Parameter	Symbol	Min.	Max.	Unit	Note
Supply Voltage	V_{CC}	-0.3	4.6	V	
ESD (contact Pads)		-4	4	KV	
Storage Temperature	T_{STG}	-40	85	℃	
Storage Humidity	40℃, 93%				

Bus Signal Line Load

Parameter	Symbol	Min.	Max.	Unit	Note
Pull-up resistance for CMD	R_{CMD}	10	100	KO	Prevent bus floating
Pull-up resistance for DAT	R_{DAT}	10	100	KO	Prevent bus floating
Bus Signal Line Capacitance	C_L	-	250	pF	F_{pp}<5MHz, 30cards
Bus Signal Line Capacitance	C_L	-	1000	pF	F_{pp}<20MHz, 10cards
Signal Card Capacitance	C_{CARD}	-	10	pF	
Maximum Signal line Inductances		-	16	nH	F_{pp}<20MHz

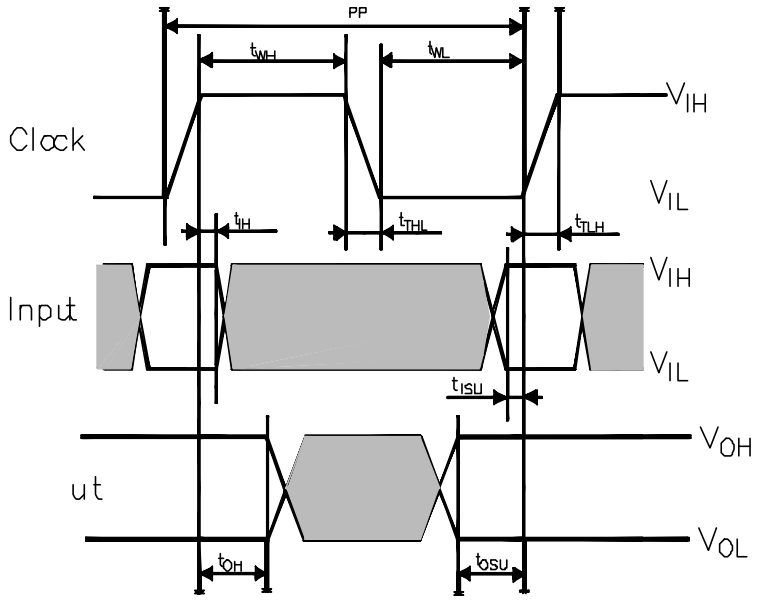
Operating Range

Parameter	Symbol	Min.	Max.	Unit	Note
Operation Temperature	T_{OTG}	-25	85	℃	
Supply Voltage	V_{CC}	2.0	3.6	V	
Supply Voltage Specified in OCR Register		2.7	3.6	V	
Input Low Voltage	V_{IL}	Vss-0.3	0.25x V_{CC}	V	
Input High Voltage	V_{IH}	0.625x V_{CC}	V_{CC}+0.3	V	
Output Low Voltage	V_{OL}		0.125x V_{CC}	V	I_{OL}=100uA@VDD Min
Output High Voltage	V_{OH}	0.75x V_{CC}		V	I_{OH}= -100uA@VDD Min
Input Leakage Current		-10	10	uA	
Output Leakage Current		-10	10	uA	
standby current			75	uA	At 0Hz, 3.6V Standby state
High Speed Supply current			70	mA	At 20Hz, 3.6V
Operation Humidity	25℃, 95%				

AC Characteristic

Bus Timing

Parameter	Symbol	Min.	Max.	Unit	Note
Clock Frequency Data Transfer Mode	F_{PP}	0	20	MHz	C_L≤100pF(10Cards)
Clock Frequency Data Transfer Mode	F_{PP}	0	5	MHz	C_L≤250pF(30Cards)
Clock Frequency identification Mode	F_{OD}	0	400	KHz	
Clock Low time	t_{WL}	10		ns	C_L≤100pF(10Cards)
Clock High time	t_{WH}	10		ns	C_L≤100pF(10Cards)
Clock Rise time	T_{TLH}		10	ns	C_L≤100pF(10Cards)
Clock Fall time	T_{THL}		10	ns	C_L≤100pF(10Cards)
Clock Low time	t_{WL}	50		ns	C_L≤250pF(30Cards)
Clock High time	t_{WH}	50		ns	C_L≤250pF(30Cards)
Clock Rise time	T_{TLH}		50	ns	C_L≤250pF(30Cards)
Clock Fall time	T_{THL}		50	ns	C_L≤250pF(30Cards)
Input Set-up Time	T_{ISU}	5		ns	CMD,DAT Reference to CLK
Input Hold Time	T_{IH}	5		ns	CMD,DAT Reference to CLK
Output Set-up Time	T_{OSU}	5		ns	CMD,DAT Reference to CLK
Output Set-up Time	T_{OH}	5		ns	CMD,DAT Reference to CLK



Transfer Rate

Testing Condition

1. Main Board: Abit BG7

2. CPU: Intel Pentium 4 2GHz

3. DDR Memory: 256MByte

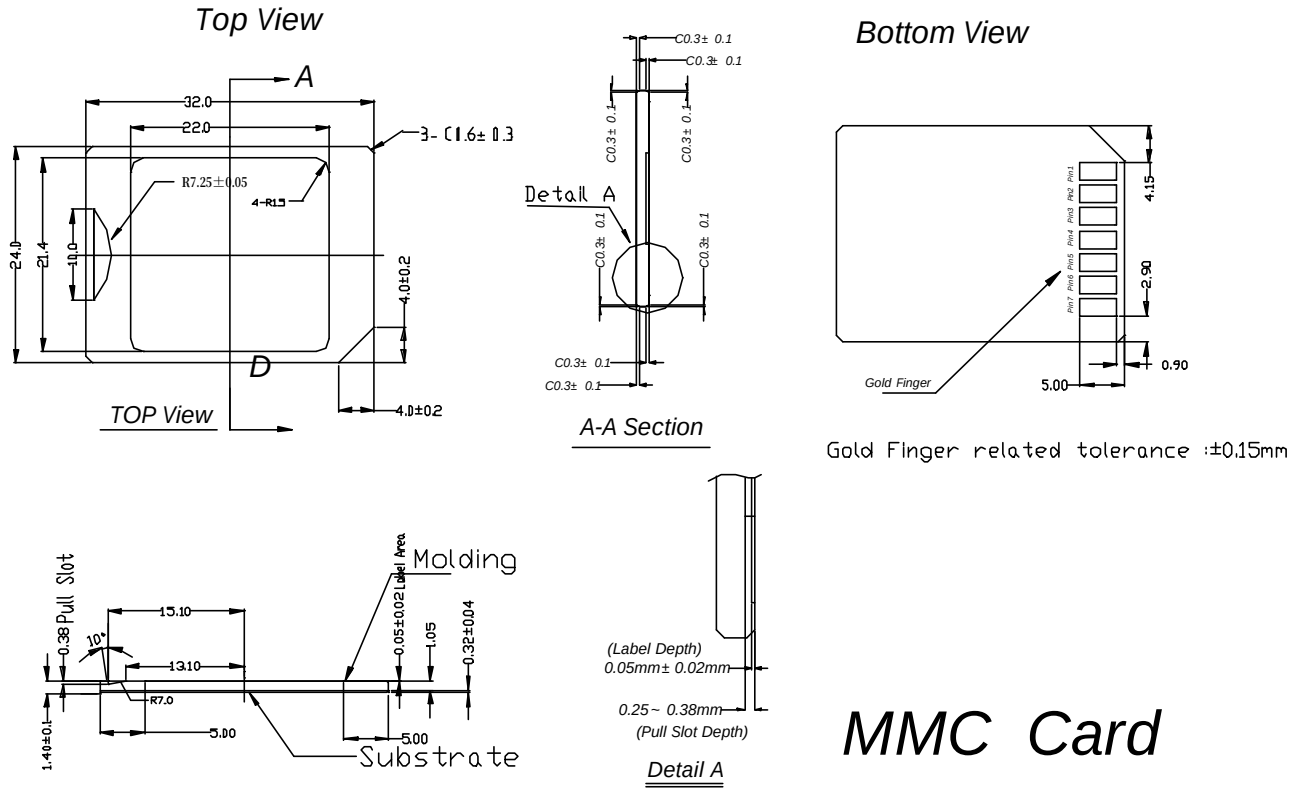
4. OS:XP with SP1

5. Software: HD Bench Ver 3.4

6. Testing Device: MMC card with USB 2.0 Card Reader(SM320T)

Capacity	Sequential Read	Sequential Write	Random Read	Random Write	Unit
32MB	3126	1368	3062	621	KB/s
64MB	3026	2228	3012	832	KB/s
128MB	3076	2918	3061	914	KB/s
256MB	2971	2741	2951	869	KB/s
512MB	2899	2685	2886	841	K/B/s
1GB	2931	2679	2919	806	K/B/s

Physical Outline Dimension



All dimension tolerances are ± 0.1mm, unless otherwise specified.