Introduction to M-LVDS (TIA/EIA-899)

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ABSTRACT

LVDS (TIA/EIA-644) devices have seen rapid incorporation into electronic designs where high speed, low power, and electromagnetic compatibility are important. LVDS devices provide a wide range of solutions for point-to-point and multidrop data transmission. A new standard has been released, Multipoint LVDS (M-LVDS), which now brings these LVDS benefits to the multipoint data transmission world. This application report summarizes the M-LVDS standard, its unique multipoint provisions, and TI's first-to-market M-LVDS devices.

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1 Introduction

Can LVDS be used in a multipoint system? Can I get more noise margin in my LVDS system? Are there any options for a higher speed, lower power version of 485? The answer to these questions is yes, as is shown in this application report.

With the introduction of the MLVD200 series single-channel transceivers, TI offers the first in a family of high-speed, low-power, true multipoint drivers and receivers that give designers the ability to realize the benefits of LVDS technology while operating in a multipoint environment. These devices comply with the requirements of TIA/EIA-899 (publication pending) providing industry standard solutions to apply to the multiple-driver multipoint problem. This application report highlights the M-LVDS standard, and introduces the TI SN65MLVD200 series multipoint devices.

2 Topologies and Technologies

TIA/EIA-899 (Electrical Characteristics of Multipoint-Low-Voltage Differential Signaling (M-LVDS)) was developed to respond to a demand for a general-purpose, high-speed, balanced interface standard for multipoint applications. A common question is often raised concerning the applicability of LVDS devices (those complying with TIA/EIA-644) to different architectural problems. *What is the difference between a point-to-point, multidrop, or multipoint system; and which devices can be applied to each system?* The following paragraphs look at various topological architectures, and the applicability of different standards to each topology.

2.1 Topologies

2.1.1 Point-to-Point

A point-to-point interface consists of a single driver and a single receiver connected by transmission media. The point-to-point connection provides the optimum configuration from a signaling quality viewpoint. Mainline stubs and other discontinuities are avoided, and the highest possible signaling rate can be expected. The point-to-point topology supports simplex communication where the data transmission is unidirectional. Figure 1 shows a differential point-to-point simplex configuration.

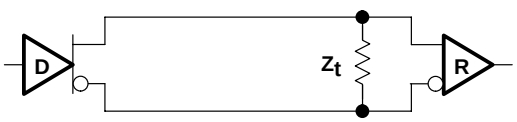

Figure 1. Point-to-Point Simplex Configuration

2.1.2 Multidrop

A second common interconnection configuration is multidrop. In a multidrop system a single driver is again used, but now multiple receivers are connected to the main transmission line. Where line termination is necessary, a single termination is located at the far end of the line from the transmitter. Like point-to-point, a multidrop connection provides unidirectional transmission. Figure 2 shows a differential multidrop interconnection.

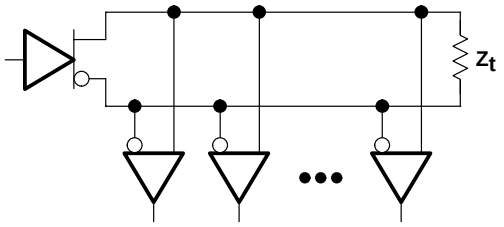

Figure 2. Multidrop Configuration

2.1.3 Multipoint

The final architecture to be discussed is multipoint. In a multipoint configuration many transmitters and many receivers can be interconnected on a single transmission line. The key difference here is the presence of two or more drivers. Such a situation creates contention issues that need not be addressed with point-to-point or multidrop systems. Multipoint operation allows for bidirectional, half-duplex communication over a single balanced media pair. To support the location of the various drivers throughout the transmission line, double termination of the transmission line is now necessary. Figure 3 shows a multipoint configuration.

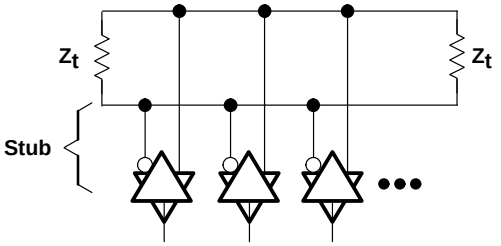

Figure 3. Multipoint Configuration

2.2 Technologies

2.2.1 TIA/EIA-644 (LVDS)

Discrete LVDS devices generally comply with the 1996 ANSI standard TIA/EIA-644, Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits. TIA/EIA-644 was conceived to provide a general-purpose electrical-layer specification for drivers and receivers connected in a point-to-point interface. Table 1 highlights some of the important LVDS specifications for drivers and receivers. LVDS drivers are specified when driving a simple 100-Ω resistive load. Figure 4 shows the driver test circuit included in the 644 standard. Receivers require ±100 mV thresholds and operation over ±1 V of ground potential difference. Table 1 shows that receivers also have a 20 μA input leakage current requirement. Since LVDS was originally specified as a point-to-point interface, this 20 μA leakage was negligible, and was therefore ignored when specifying the driver output characteristics. LVDS drivers were specified to work for point-to-point applications, but could not be assumed to work in a multidrop system.

Table 1. A Comparison of LVDS Specifications

PARAMETER	TIA/EIA-644 (LVDS)	TIA/EIA-644-A (LVDS REV A)	TIA/EIA-899 (M-LVDS)	UNIT
DRIVER CHARACTERISTICS				
Offset voltage: Vos (max)	1375	1375	2100	mV
Offset voltage: Vos (min)	1125	1125	300	mV
Differential output voltage: Vod (max)	454 (100 Ω)	454 (100 Ω)	650 (50 Ω)	mV
Differential output voltage: Vod(min)	247 (100 Ω)	247 (100 Ω)	480 (50 Ω)	mV
Offset voltage variation: Vospp	150	150	150	mV
Short circuit current: Ios	12/24	12/24	43	mA
Differential voltage change: ΔVod	50	50	50	mV
Offset voltage change: ΔVos	50	50	50	mV
Transition time: tr/tf(min)	260	260	1000	ps
RECEIVER CHARACTERISTICS				
Ground potential difference: Vgpd	+/- 1	+/- 1	+/- 1	V
Input leakage current: Iin	20	20	20	μA
Differential input leakage current: Iid	NS	6	4	μA
Input voltage range: Vin	0 to 2.4	0 to 2.4	–1.4 to 3.8	V
Input threshold: Vith	100	100	50	mV
NS: Not specified				

2.2.2 TIA/EIA-644-A (LVDS, REV A)

As discussed earlier, a multidrop application has one driver communicating with multiple receivers. The 644 receiver input leakage requirement of 20 μA has a small effect on the driver output voltage when only one receiver is connected, but this effect becomes more pronounced as the driver is loaded with additional receivers. An update to LVDS, designated TIA/EIA-644-A, was developed and released in 2001 to standardize the driver requirements for LVDS devices being used in a multidrop configuration. Devices compliant to 644-A can be easily identified by the full load test required for the driver output. Figure 5 shows this 644-A test circuit. As with 644, 644-A receivers have a 20 μA input leakage requirement, which implies a 120 kΩ input resistance. The 3.74 kΩ resistors in Figure 5 represent the worst-case parallel combination of thirty-two 644-A receivers. The V_{TEST} power supply in Figure 5 represents the possible range of bias voltages that 644-A receivers may present to the bus, when connected in a system that operates over a ±1 V ground noise environment.

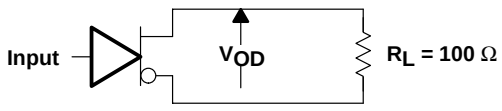

Figure 4. TIA/EIA-644 Driver Test Load

Table 1 includes significant 644-A electrical specifications alongside the 644 values. The availability of TIA/EIA-644-A compliant devices allows users to confidently choose multidrop drivers when the need arises.

2.2.3 TIA/EIA-644-A (M-LVDS)

Multipoint operation introduces a new set of problems. First, the main transmission line needs to be doubly terminated. Whereas LVDS drivers are specified for driving a 100-Ω load, a multipoint line, using 100-Ω transmission media appears as 50-Ω (or even lower depending on the capacitive loading of multiple bus transceivers). TI introduced the LVDM family of drivers in 1998, compliant to the 644 LVDS standard, with the exception of a doubling of the output current. The LVDM family does not include many of the provisions necessary when more than two drivers are expected on a multipoint bus, but provides an attractive solution when a point-to-point half-duplex (i.e., a single transceiver communicating with a second transceiver) multipoint design is needed. In a point-to-point multipoint system intermediate stubs are absent on the bus allowing the use of fast edge-rate drivers and enabling half-duplex transmissions at rates of 300-600 Mbps. LVDM devices also find use in simple point-to-point architectures when a designer is looking for additional noise margin at the receiver.

While LVDM devices provide the necessary features to address many problems, true multipoint capabilities (to include edge rate control, contention provisions, wired-Or signaling, etc.) are needed when the design involves numerous drivers and receivers connected to a bus. M-LVDS devices support these needs. Table 1 also lists M-LVDS parameters with the other standards that have already been discussed. As shown in the table, the offset voltage for M-LVDS drivers is allowed to vary over a much wider range than allowed by the previous standards discussed. This increased offset voltage range allows for the presence of multiple drivers on the bus. Table 1 shows that M-LVDS receivers are also required to operate over ±1 V of ground noise. Another noteworthy point concerns the M-LVDS specification for differential output voltage. While 644 and 644-A were specified with a 100-Ω load, the M-LVDS driver requirement is for a 50-Ω load, as would be expected for a doubly terminated multipoint driver.

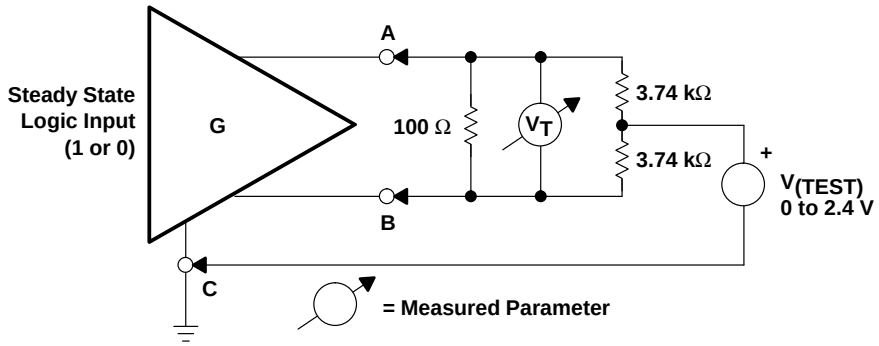

Figure 5. TIA/EIA-644-A Driver Full-Load Test Circuit

3 The M-LVDS Standard

3.1 Driver Specifications

3.1.1 Driver Offset and Differential Voltages

As mentioned above, the M-LVDS standard includes many unique features to address issues of concern when operating with multipoint communication. Figure 6 shows the test circuit for M-LVDS drivers. The similarity to the 644-A test circuit is obvious. The standard allows up to thirty-two M-LVDS circuits (driver, receiver, or transceiver) to be connected to the common transmission media. The familiar 20 μA input leakage requirement is specified for disabled drivers, disabled transceivers, or receivers. The 3.32 kΩ load resistors represent the parallel combination of any mix of thirty-two M-LVDS circuits. The test circuit power supply now ranges from –1 V to 3.4 V to accommodate the possible range of voltages that can be presented to the bus by compliant circuits. *But why is this voltage range now greater than the 0 to 2.4 V test voltage seen with 644-A?* As we see in the following paragraphs, the answer lies in the common-mode signal components and their defined voltage limits.

The common-mode voltage on a multipoint bus is the sum of the driver output and ground offset voltages. 644 and 644-A drivers are required to have an output offset voltage of 1.2 V ± 0.175 V. Since there are periods when there are no active drivers on a multipoint bus segment, the M-LVDS driver cannot be used to establish the worst-case common-mode operating point of the circuit. During this idle-bus state, the common-mode voltage is bounded by the open-circuit voltages of the attached components. In the case of TIA/EIA-899 compliant devices, this voltage is 0 V to 2.4 V and is borrowed from its 644 predecessor. Addition of a one-volt ground-noise offset added to this range gives the common-mode voltage range requirements for M-LVDS circuits of –1 V to 3.4 V as shown in Figure 6.

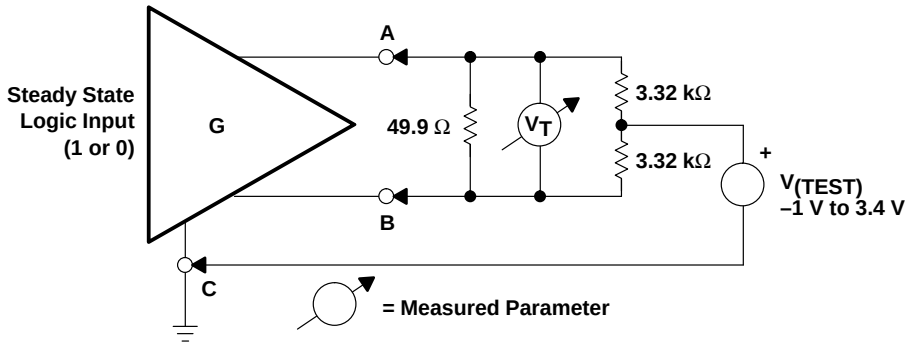

Figure 6. TIA/EIA-899 Driver Test Circuit

Figure 6 shows that the driver shunt load is ~ 50 Ω, the parallel combination of two 100-Ω ideal transmission lines, and the common-mode load is 3.32 kΩ. M-LVDS drivers provide a typical differential output signal of 565 mV into a 50-Ω test load. This means that M-LVDS drivers deliver approximately 11.3 mA when a 50-Ω load represents the actual application. M-LVDS drivers therefore, may deliver more signal to receivers in a multipoint architecture than their LVDS counterparts deliver in a point-to-point or multidrop type configuration (typical differential voltage for 644 and 644-A drivers is 350 mV). This increased, relative, drive strength is incorporated to address anticipated multipoint designs involving closely spaced nodes. While a point-to-point multipoint or widely distributed multipoint system can be expected to *look* like 50 Ω

to a driver, closely spaced nodes can easily result in capacitive loading that drops the effective load seen by the driver to 30 Ω. The 11.3 mA output ensures that M-LVDS drivers still provide greater than 300 mV under these conditions.

3.1.2 Driver Short Circuit

A second M-LVDS driver provision to address contention deals with the maximum short circuit current delivered to the multipoint bus. M-LVDS drivers are required to deliver less than 43 mA of current when driving into a short circuit as shown in Figure 7.

The power supply included in the figure is the one already seen, its range of voltage chosen to represent the maximum bus voltage due to drivers located throughout the multipoint line, and separated by up to ±1 V of ground shift. The 43-mA short circuit requirement ensures that the maximum output from any driver does not develop more than 0 to 2.4 V differential on the bus. A 50-Ω line impedance, coupled with this 43-mA current, ensures that the max differential bus voltage stays below 2.4 V in magnitude.

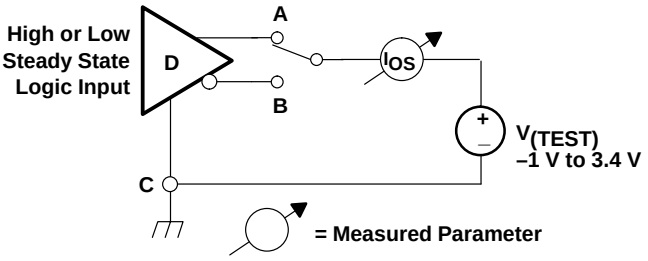

Figure 7. Driver Short-Circuit Test Circuit

3.1.3 Driver Transition Time

A final M-LVDS driver provision to address multipoint operation concerns transition time. As was shown in Table 1, 644 and 644-A allow driver transition times as fast as 260 ps. Faster transition times lead to higher signaling rates, which is one of the key benefits of LVDS. Using the rule-of-thumb below, it is seen that the 644 and 644-A allow for signaling rates up to 1.923 Gbps:

$$Max\_signaling\_rate = \frac{0.5}{tr, tf}$$

One of the drawbacks of fast transition times is that careful attention needs to be placed on the design of the interconnect to minimize impedance mismatches from stubs, connectors, and other parasitic connections to the line. General guidelines suggest that mainline stubs be kept as short as possible, with specific guidelines recommending that the propagation delay of a stub be less than 30% of the signal transition time. With 260 ps transition times, this means stubs should be less than 80 ps *long*, or approximately 0.5 inch of FR-4 PCB material.

In a multipoint system, stubs off the mainline may be the norm, rather than the exception. In order to allow for this, while also observing the 30% propagation delay recommendation, the M-LVDS standard specifies a minimum transition time of 1 ns. This 1 ns means that the maximum signaling rate expected with M-LVDS devices is 500 Mbps, but stubs can now be almost 2 inches long without violating the 30% rule.

3.2 Receiver Specifications

3.2.1 Input Impedance and Leakage Current

In a multipoint environment, active drivers provide a differential signal to receivers, as well as disabled (three-stated), inactive, drivers and transceivers. From a loading point-of-view, inactive drivers and transceivers can effect the transmitted signal in the same way that receivers can. In order to bound the impedance seen by an active driver, the M-LVDS standard specifies a common leakage requirement for disabled devices and receivers. Similar to the LVDS standard, a 20 μA leakage current is permitted over a 0 to 2.4 V input range. Since M-LVDS devices are required to operate over a wider input range than LVDS devices, additional leakage requirements are included for the wider voltage inputs, but all devices can be characterized simply as 120 kΩ, minimum, input impedance.The M-LVDS driver full-load test circuit seen earlier (Figure 6) ensures that at least thirty two compliant M-LVDS circuits can be interconnected, and comply with the electrical specifications of the standard.

3.2.2 Bus Pin Voltage

Disabled devices and M-LVDS receivers are also required to constrain their bus pin voltage. Compliant circuits are required to maintain bus-pin voltages between 0 and 2.4 V. Limiting bus pin voltage in this way ensures the bus operating voltages stay within those allowed by standard. Inactive devices and receivers are prohibited from employing simple failsafe pullup circuitry that can charge the line to more than 2.4 V or less than 0 V and result in operation outside the minimum common-mode operating voltages.

3.2.3 Input Thresholds and Type-1/Type-2 Receivers

As has been mentioned already, M-LVDS receivers are required to operate with differential inputs up to 2.4 V in magnitude. Supporting this 2.4 V input ensures that proper operation is available even under conditions of thirty-two drivers operating simultaneously. M-LVDS receivers are also required to correctly detect the input state when as little as 50 mV of signal is available. This 50-mV requirement is half the 100 mV specified for LVDS receivers. This reduction in input threshold, along with the increase in driver output (565 mV for M-LVDS vs 350 mV for LVDS drivers), provides improved noise margins when using M-LVDS devices. As in the LVDS specification, the M-LVDS threshold requirement is a steady state specification. System designers should plan on providing at least 50 mV of *overdrive* signal at the input to the receivers to provide for at-speed signaling.

The LVDS standard does not specify any requirements for receiver failsafe. Compliant receivers were simply specified to correctly detect the input state when at least 100 mV was available and receiver response to less than 100 mV differential inputs is left to the implementor. The M-LVDS standard has specified two classes of receivers to bring standardization to failsafe implementation. The standard uses the nomenclature Type-1 and Type-2 to refer to these two receiver classes.

Figure 8 shows the required response, vs input differential voltage, for Type-1 and Type-2 receivers. Type-1 receivers are similar to LVDS receivers, with improved thresholds. Type-2 receivers have an offset threshold. Bus input signals that are less than +50 mV are defined to be a low state. Greater than +150 mV results in a high state. Type-1 receivers are expected to be used for maximum speed signals such as data or clock lines. Type-2 receivers are useful for lower speed applications such as control lines.

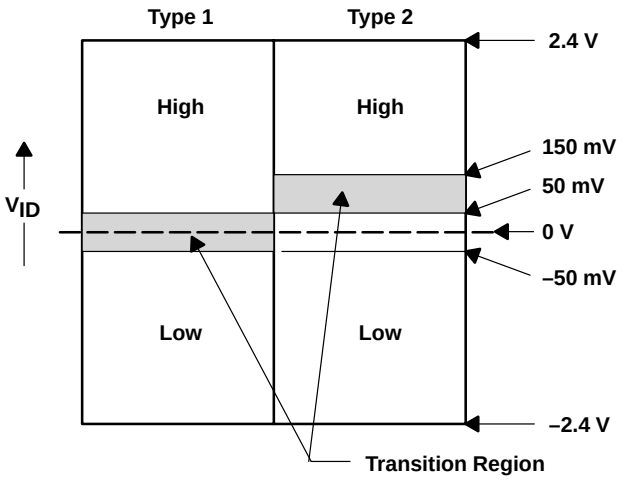

Figure 8. Receiver Differential Input Voltage Threshold Requirements

Type-2 receivers allow Wired-Or signaling with M-LVDS devices. Figure 9 shows devices connected in a Wired-Or architecture. The enable lines on the drivers are used to disable/enable the drivers. When enabled, drivers output a high state to the bus. Type-2 receivers detect a high state when one or more bus drivers are active. The receiver detects a low state when all drivers are disabled. Such a configuration might be used when sharing control lines to arbitrate for access to accompanying data lines.

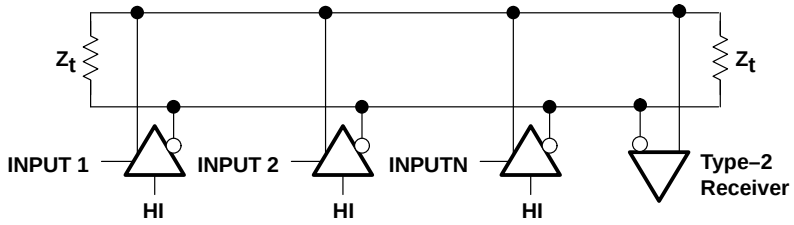

Figure 9. Wired-OR Signaling Using M-LVDS Drivers and Receivers

4 TI's MLVD200 Family

Texas Instruments' SN65MLVD200 family is the first M-LVDS compliant devices in the industry. Six devices are included in this family, providing 100/200 Mbps driver speed options, and Type-1 and Type-2 receiver options. Table 2 summarizes the available options. Details of each part are included in the product family data sheet, which is available online at www.ti.com.

Table 2. SN65MLVD200 Series Parts

PART NUMBER	NOMINAL SIGNALING RATE, Mbps	FOOTPRINT	RECEIVER TYPE
SN65MLVD200D	100	SN75176	Type 1
SN65MLVD201D	200	SN75176	Type 1
SN65MLVD202D	100	SN75ALS180	Type 1
SN65MLVD203D	200	SN75ALS180	Type 1
SN65MLVD204D	100	SN75176	Type 2
SN65MLVD205D	100	SN75ALS180	Type 2

Each of the family parts is briefly discussed below.

The ‘200, ‘202, ‘204 and ‘205 devices provide 100 Mbps signaling rates. Driver transition times are limited to 1.5 ns to 3.0 ns. Signaling rate is a function of transition time, and earlier the maximum signaling rate was defined as 50% of the inverse of the transition time. A generally accepted rule of thumb for characterizing drivers is that the useful signaling rate (that which allows for transition time degradation between driver and receiver) can be calculated using the following equation:

$$driver\_signaling\_rate = \frac{0.3}{tr, tf}$$

Using this equation and the 3.0 ns max transition time results in the 100 Mbps driver specification. The 1.5 ns minimum transition time helps bound the length of stubs off the main line, which in this case would be almost 3 inches long.

The ‘200 and ‘204 are footprint compatible with the SN75176 bidirectional bus transceiver. The ‘202 and ‘205 provide footprint replacements for devices complying with the SN75ALS180 differential driver/receiver pair. (The SN75176 and SN75ALS180 footprints are shown in Figure 10). The ‘176 is an industry standard RS-485 footprint that provides separate driver and receiver enables, allowing simultaneous *talking* and *listening* at a single node. The topology of the ‘176 footprint provides a half-duplex communication capability. The ‘180 is an industry standard RS-422/RS-485 driver/receiver pair. Full duplex communication is available with the ‘180 footprints owing to the separate driver and receiver bus lines. The ‘200 and ‘202 provide Type-1 receivers with the 100 Mbps driver circuits, while the ‘204 and ‘205 include Type-2 receivers.

The ‘201 and ‘203 devices are 200 Mbps circuits. Driver transition times on these devices are limited to 1 ns to 1.5 ns. The 1 ns lower limit allows for 2-inch stubs off the main bus line.

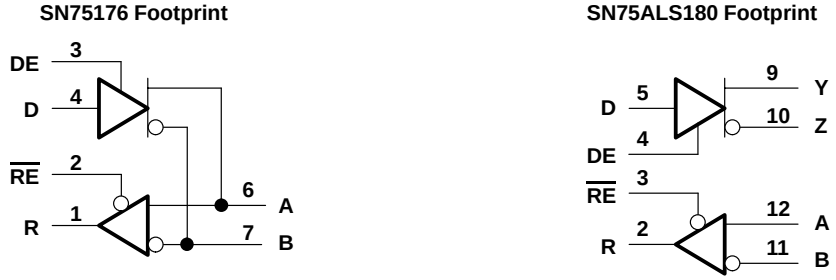

Figure 10. MLVD200 Series Footprints

5 Summary

LVDS interfacing has seen rapid acceptance by the electronics industry since its introduction in 1996. Numerous vendors offer standard and differentiated discrete interface solutions that allow signaling at rates beyond 1 Gbps, at distances of many 10’s of meters, and at fraction of the power budget required for previous generation solutions (RS-422, RS-485). LVDS technology has been successfully applied to point-to-point and multidrop applications, but has found limited application in multipoint designs. The arrival of the M-LVDS standard, as well as the introduction of the MLVD200 series of devices, brings LVDS benefits to the multipoint world. Customers can expect to see numerous component vendors support the M-LVDS standard, and a broad portfolio of solutions to enter the market in the coming years.

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