MICRON TECHNOLOGY, INC.

DRAM

MT4LC4M4E8, MT4LC4M4E9

For the latest data sheet revisions, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- Industry-standard x4 pinout, timing, functions and packages
- High-performance, low-power CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, HIDDEN and CAS#-BEFORE-RAS# (CBR)
- Optional self refresh (S) for low-power data retention
- 11 row, 11 column addresses (2K refresh) or 12 row, 10 column addresses (4K refresh)
- Extended Data-Out (EDO) PAGE MODE access

OPTIONS   MARKING

- Refresh Addressing
  2,048 (2K) rows   E8
  4,096 (4K) rows   E9

- Packages
  Plastic SOJ (300 mil)   DJ
  Plastic TSOP (300 mil)   TG

- Timing
  50ns access   -5
  60ns access   -6

- Refresh Rates
  Standard Refresh   None
  Self Refresh (128ms period)   S*

NOTE: 1. The 4 Meg x 4 EDO DRAM base number differentiates the offerings in one place - MT4LC4M4E8. The fifth field distinguishes various options: E8 designates a 2K refresh and E9 designates a 4K refresh for EDO DRAMs.
2. The "#" symbol indicates signal is active LOW.

*Contact factory for availability
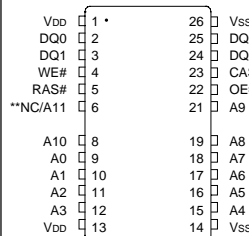
KEY TIMING PARAMETERS

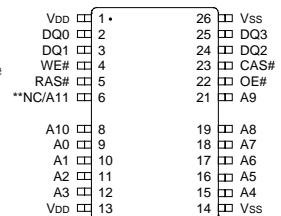| SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{CAS}
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

GENERAL DESCRIPTION

The 4 Meg x 4 DRAM is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x4 configuration. RAS# is used to latch the row address (first 11 bits for 2K and first 12 bits for 4K). Once the page has been opened by RAS#, CAS# is used to latch the column address

PIN ASSIGNMENT (Top View)

24/26-Pin SOJ

VDD	1	26	Vss
DQ0	2	25	DQ3
DQ1	3	24	DQ2
WE#	4	23	CAS#
RAS#	5	22	OE#
**NC/A11	6	21	A9
A10	8	19	A8
A0	9	18	A7
A1	10	17	A6
A2	11	16	A5
A3	12	15	A4
VDD	13	14	Vss

24/26-Pin TSOP

VDD	1	26	Vss
DQ0	2	25	DQ3
DQ1	3	24	DQ2
WE#	4	23	CAS#
RAS#	5	22	OE#
**NC/A11	6	21	A9
A10	8	19	A8
A0	9	18	A7
A1	10	17	A6
A2	11	16	A5
A3	12	15	A4
VDD	13	14	Vss

** NC on 2K refresh and A11 on 4K refresh options.

4 MEG x 4 EDO DRAM PART NUMBERS

PART NUMBER	REFRESH ADDRESSING	PACKAGE	REFRESH
MT4LC4M4E8DJ-x	2K	SOJ	Standard
MT4LC4M4E8DJ-x S	2K	SOJ	Self
MT4LC4M4E8TG-x	2K	TSOP	Standard
MT4LC4M4E8TG-x S	2K	TSOP	Self
MT4LC4M4E9DJ-x	4K	SOJ	Standard
MT4LC4M4E9DJ-x S	4K	SOJ	Self
MT4LC4M4E9TG-x	4K	TSOP	Standard
MT4LC4M4E9TG-x S	4K	TSOP	Self

x = speed

(the latter 11 bits for 2K and the latter 10 bits for 4K; address pins A10 and A11 are "Don't Care"). READ and WRITE cycles are selected with the WE# input.

A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# is taken LOW. During EARLY WRITE cycles, the data outputs (Q) will remain High-Z regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE

GENERAL DESCRIPTION (continued)

cycles, OE# must be taken HIGH to disable the data outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no WRITE will occur, and the data outputs will drive read data from the accessed location.

The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE# and OE#.

The 4 Meg x 4 DRAM must be refreshed periodically in order to retain stored data.

PAGE ACCESS

Page operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The page cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the page mode of operation, i.e., closes the page.

EDO PAGE MODE

The 4 Meg x 4 EDO DRAM provides EDO PAGE MODE, which is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# returns HIGH. EDO allows CAS# precharge time (^tCP) to occur without the output data going invalid. This elimination of CAS# output control allows pipelined READs.

FAST-PAGE-MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO-PAGE-MODE DRAMs operate like FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS# goes HIGH during READs, provided RAS# and OE# are held LOW. If OE# is pulsed while RAS# and CAS# are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE# is toggled or pulsed after CAS# goes HIGH while RAS# remains LOW, data will transition to and remain High-Z (refer to Figure 1). WE# can also perform the function of disabling the output devices under certain conditions, as shown in Figure 2.

During an application, if the DQ outputs are wire OR'd, OE# must be used to disable idle banks of DRAMs. Alterna-
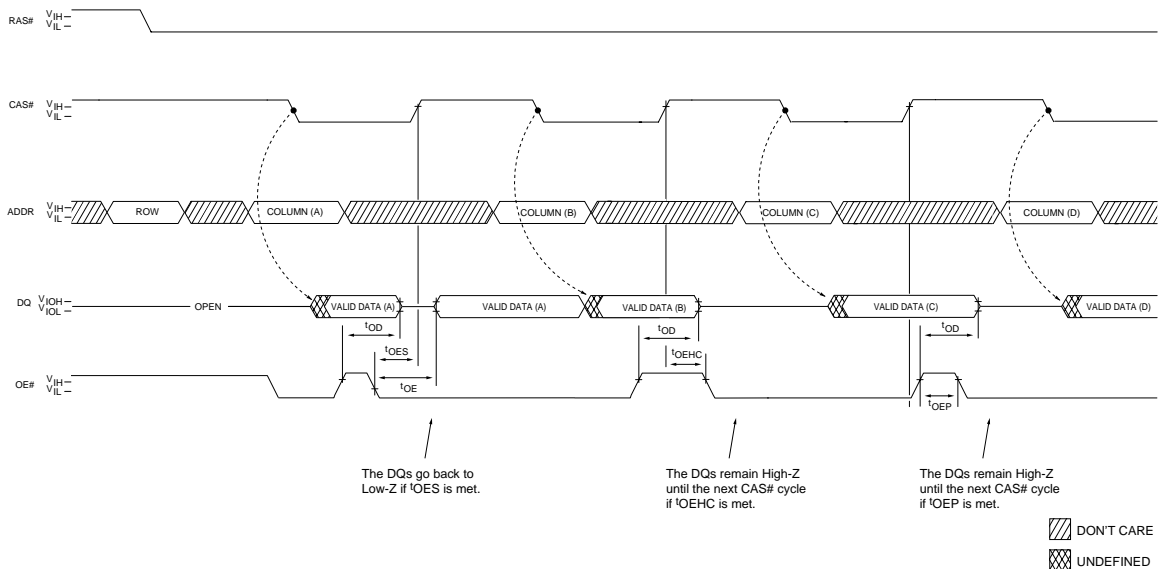

**Figure 1
OE# CONTROL OF DQs**

EDO PAGE MODE (continued)

tively, pulsing WE# to the idle banks during CAS# HIGH time will also High-Z the outputs. Independent of OE# control, the outputs will disable after ^tOFF, which is referenced from the rising edge of RAS# or CAS#, whichever occurs last.

DRAM REFRESH

Preserve correct memory cell data by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses (2,048 for 2K and 4,096 for 4K) are executed within ^tREF (MAX), regardless of sequence. The CBR and SELF REFRESH cycles will invoke the internal refresh counter for automatic RAS# addressing.
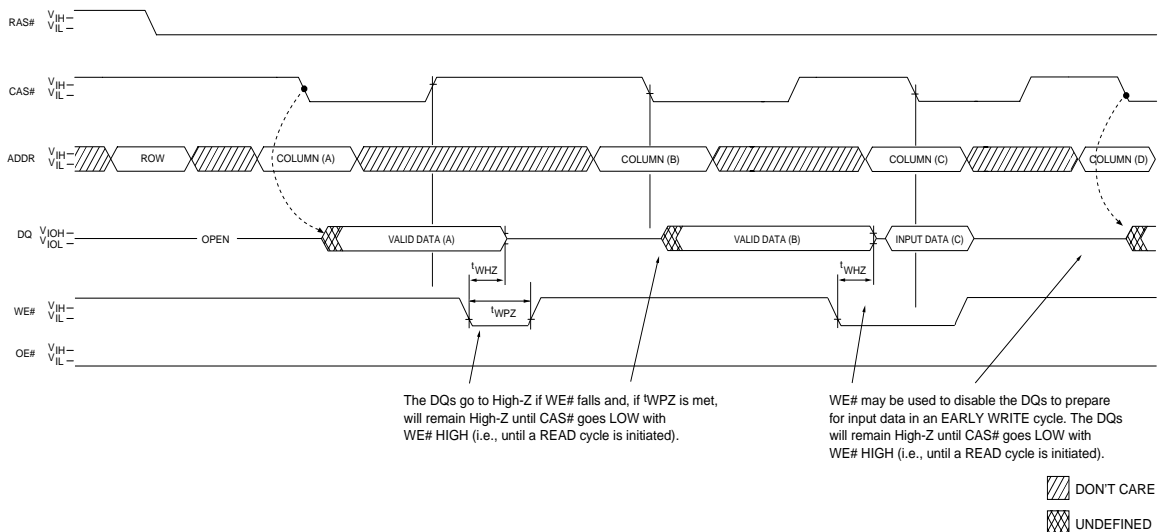
An optional self refresh mode is also available on the "S" version. The self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified ^tRASS. The "S" option allows the user the choice of a fully static, low-power data retention mode or a dynamic refresh mode at the extended refresh period of 128ms,

or 31.25µs per row for a 4K refresh and 62.5µs per row for a 2K refresh, when using a distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or battery backup mode.

The self refresh mode is terminated by driving RAS# HIGH for a minimum time of ^tRPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting self refresh. However, if the DRAM controller utilizes a RAS#-ONLY or burst refresh sequence, all rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS# HIGH time.

The DQs go to High-Z if WE# falls and, if ^tWPZ is met, will remain High-Z until CAS# goes LOW with WE# HIGH (i.e., until a READ cycle is initiated).

WE# may be used to disable the DQs to prepare for input data in an EARLY WRITE cycle. The DQs will remain High-Z until CAS# goes LOW with WE# HIGH (i.e., until a READ cycle is initiated).

DON'T CARE

UNDEFINED

Figure 2
WE# CONTROL OF DQs

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FUNCTIONAL BLOCK DIAGRAM - 2K REFRESH
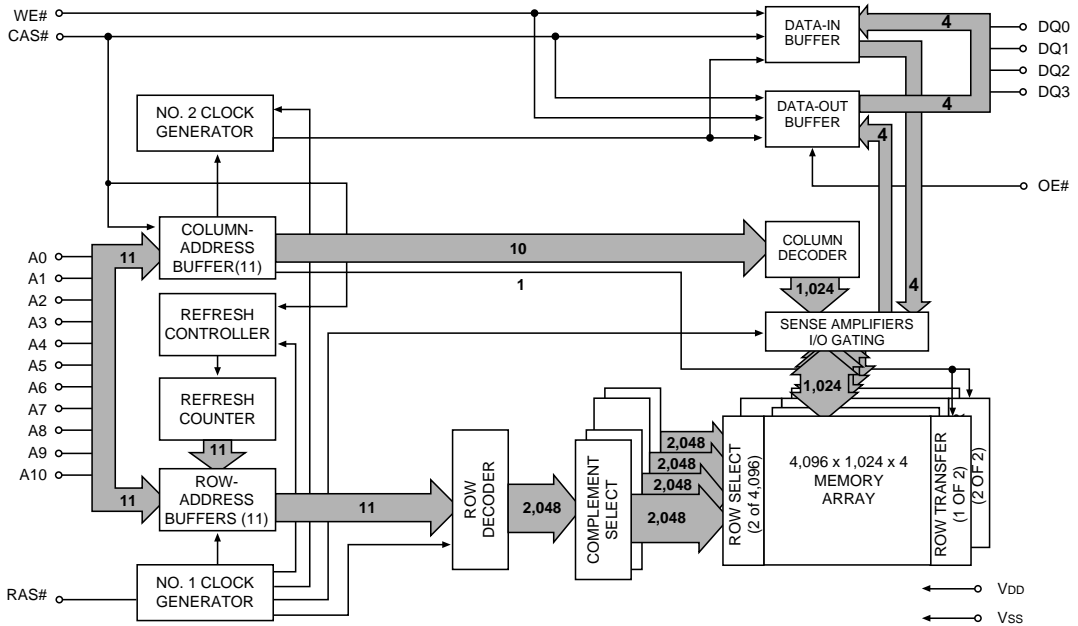
FUNCTIONAL BLOCK DIAGRAM - 4K REFRESH

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Pin Relative to V_{SS} .... -1V to +4.6V
Voltage on NC, Inputs or I/O Pins
   Relative to V_{SS} .... -1V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
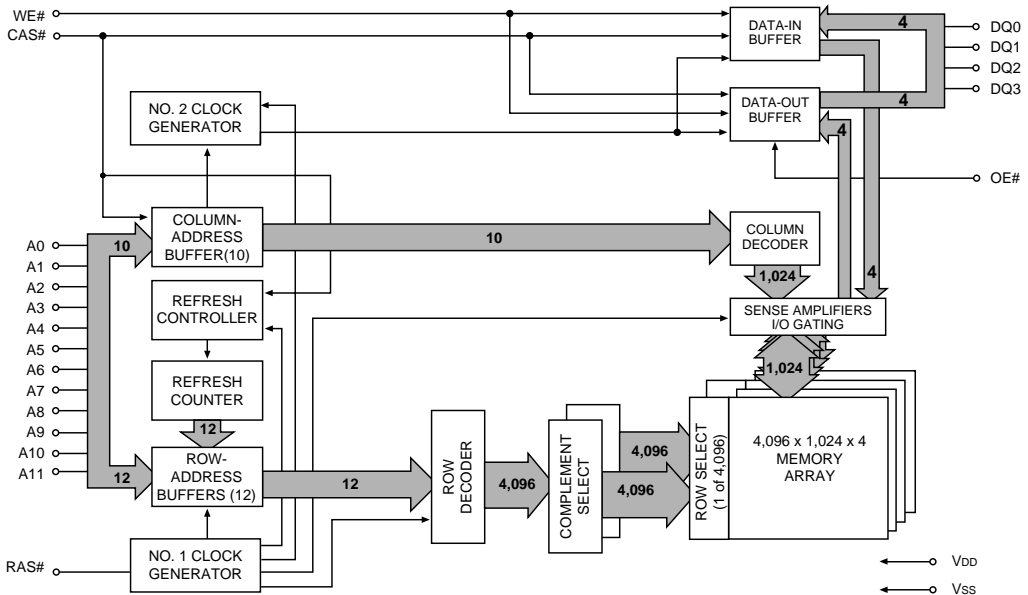Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1) (V_{DD} = +3.3V ± 0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Valid Logic 1; All inputs, I/Os and any NC	V_{IH}	2	5.5	V	26
INPUT LOW VOLTAGE: Valid Logic 0; All inputs, I/Os and any NC	V_{IL}	-0.5	0.8	V	26
INPUT LEAKAGE CURRENT: Any input at V_{IN} (0V ≤ V_{IN} ≤ V_{DD} + 0.3V); All other pins not under test = 0V	I_I	-2	2	μA	4
OUTPUT HIGH VOLTAGE: I_{OUT} = -2mA	V_{OH}	2.4	–	V	
OUTPUT LOW VOLTAGE: I_{OUT} = 2mA	V_{OL}	–	0.4	V	
OUTPUT LEAKAGE CURRENT: Any output at V_{OUT} (0V ≤ V_{OUT} ≤ V_{DD} + 0.3V); DQ is disabled and in High-Z state	I_{OZ}	-5	5	μA	

Icc OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 2, 3, 5, 8) (V_{DD} = +3.3V ± 0.3V)

PARAMETER/CONDITION	SYMBOL	SPEED	2K REFRESH	4K REFRESH	UNITS	NOTES
STANDBY CURRENT: TTL (RAS# = CAS# = V_{IH})	I_{CC1}	ALL	1	1	mA	
STANDBY CURRENT: CMOS (non-"S" version only) (RAS# = CAS# = other inputs = V_{DD} - 0.2V)	I_{CC2}	ALL	500	500	µA	
STANDBY CURRENT: CMOS ("S" version only) (RAS# = CAS# = other inputs = V_{DD} - 0.2V)	I_{CC2}	ALL	150	150	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{CC3}	-5 -6	110 100	90 80	mA	6
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^tPC = ^tPC [MIN])	I_{CC4}	-5 -6	110 100	100 90	mA	6
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	-5 -6	110 100	90 80	mA	
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{CC6}	-5 -6	110 100	90 80	mA	7, 9
REFRESH CURRENT: Extended ("S" version only) Average power supply current: CAS# = 0.2V or CBR cycling; RAS# = ^tRAS (MIN); WE# = V_{DD} - 0.2V; A0-A11, OE# and D_{IN} = V_{DD} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC7}	ALL	300	300	µA	7, 9
		^tRC	62.5	31.25	µs	25
REFRESH CURRENT: Self ("S" version only) Average power supply current: CBR with RAS# ≥ ^tRASS (MIN) and CAS# held LOW; WE# = V_{DD} - 0.2V; A0-A11, OE# and D_{IN} = V_{DD} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	ALL	300	300	µA	7, 9

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Address pins	C_{I1}	5	pF	8
Input Capacitance: RAS#, CAS#, WE#, OE#	C_{I2}	7	pF	8
Input/Output Capacitance: DQ	C_{IO}	7	pF	8

AC ELECTRICAL CHARACTERISTICS
(Notes: 2, 3, 9, 10, 11, 12) (V_{DD} = +3.3V ± 0.3V)

AC CHARACTERISTICS		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column address	^tAA		25		30	ns	
Column-address setup to CAS# precharge	^tACH	12		15		ns	
Column-address hold time (referenced to RAS#)	^tAR	38		45		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Column address to WE# delay time	^tAWD	42		49		ns	13
Access time from CAS#	^tCAC		13		15	ns	14
Column-address hold time	^tCAH	8		10		ns	
CAS# pulse width	^tCAS	8	10,000	10	10,000	ns	
CAS# LOW to "Don't Care" during Self Refresh	^tCHD	15		15		ns	
CAS# hold time (CBR Refresh)	^tCHR	8		10		ns	7
CAS# to output in Low-Z	^tCLZ	0		0		ns	
Data output hold after next CAS# LOW	^tCOH	3		3		ns	
CAS# precharge time	^tCP	8		10		ns	15
Access time from CAS# precharge	^tCPA		28		35	ns	
CAS# to RAS# precharge time	^tCRP	5		5		ns	
CAS# hold time	^tCSH	38		45		ns	
CAS# setup time (CBR Refresh)	^tCSR	5		5		ns	
CAS# to WE# delay time	^tCWD	28		35		ns	13
WRITE command to CAS# lead time	^tCWL	8		10		ns	
Data-in hold time	^tDH	8		10		ns	16
Data-in setup time	^tDS	0		0		ns	16
Output disable	^tOD	0	12	0	15	ns	
Output enable	^tOE		12		15	ns	17
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	8		10		ns	18
OE# HIGH hold from CAS# HIGH	^tOEHC	5		10		ns	18
OE# HIGH pulse width	^tOEP	5		5		ns	
OE# LOW to CAS# HIGH setup time	^tOES	4		5		ns	
Output buffer turn-off delay	^tOFF	0	12	0	15	ns	20

AC ELECTRICAL CHARACTERISTICS

(Notes: 2, 3, 9, 10, 11, 12) (V_{DD} = +3.3V ± 0.3V)

AC CHARACTERISTICS		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
OE# setup prior to RAS# during HIDDEN REFRESH cycle	^{t}ORD	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^{t}PC	20		25		ns	
EDO-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	47		56		ns	
Access time from RAS#	^{t}RAC		50		60	ns	19
RAS# to column-address delay time	^{t}RAD	9		12		ns	21
Row-address hold time	^{t}RAH	9		10		ns	
RAS# pulse width	^{t}RAS	50	10,000	60	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	^{t}RASP	50	125,000	60	125,000	ns	7
RAS# pulse width during Self Refresh	^{t}RASS	100		100		µs	
Random READ or WRITE cycle time	^{t}RC	84		104		ns	
RAS# to CAS# delay time	^{t}RCD	11		14		ns	22
READ command hold time (referenced to CAS#)	^{t}RCH	0		0		ns	23
READ command setup time	^{t}RCS	0		0		ns	
Refresh period (2,048 cycles)	^{t}REF		32		32	ms	
Refresh period (4,096 cycles)	^{t}REF		64		64	ms	
Refresh period "S" version	^{t}REF		128		128	ms	
RAS# precharge time	^{t}RP	30		40		ns	
RAS# to CAS# precharge time	^{t}RPC	5		5		ns	
RAS# precharge time exiting Self Refresh	^{t}RPS	90		105		ns	
READ command hold time (referenced to RAS#)	^{t}RRH	0		0		ns	23
RAS# hold time	^{t}RSH	13		15		ns	
READ-WRITE cycle time	^{t}RWC	116		140		ns	
RAS# to WE# delay time	^{t}RWD	67		79		ns	13
WRITE command to RAS# lead time	^{t}RWL	13		15		ns	
Transition time (rise or fall)	^{t}T	2	50	2	50	ns	
WRITE command hold time	^{t}WCH	8		10		ns	
WRITE command hold time (referenced to RAS#)	^{t}WCR	38		45		ns	
WE# command setup time	^{t}WCS	0		0		ns	13
Output disable delay from WE#	^{t}WHZ	0	12	0	15	ns	
WRITE command pulse width	^{t}WP	5		5		ns	
WE# pulse to disable at CAS# HIGH	^{t}WPZ	10		10		ns	
WE# hold time (CBR Refresh)	^{t}WRH	8		10		ns	6, 7
WE# setup time (CBR Refresh)	^{t}WRP	8		10		ns	6, 7

NOTES

1. All voltages referenced to V_{SS}.
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is ensured.
3. An initial pause of 100μs is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
4. NC pins are assumed to be left floating and are not tested for leakage.
5. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
6. Column address changed once each cycle.
7. Enables on-chip refresh and address counters.
8. This parameter is sampled. $V_{DD} = +3.3V$; $f = 1$ MHz.
9. AC characteristics assume $^tT = 2.5$ns.
10. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
11. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
12. Measured with a load equivalent to two TTL gates and 100pF; and $V_{OL} = 0.8V$ and $V_{OH} = 2V$.
13. ^tWCS, ^tRWD, ^tAWD and ^tCWD are not restrictive operating parameters. ^tWCS applies to EARLY WRITE cycles. ^tRWD, ^tAWD and ^tCWD apply to READ-MODIFY-WRITE cycles. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tWCS < {}^tWCS$ (MIN) and $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW results in a LATE WRITE (OE#-controlled) cycle. ^tWCS, ^tRWD, ^tCWD and ^tAWD are not applicable in a LATE WRITE cycle.
14. Requires that ^tAA and ^tRAC are not violated.
15. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^tCP.
16. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
17. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted. Additionally, WE# must be pulsed during CAS# HIGH time in order to place I/O buffers in High-Z.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS# remains LOW and OE# is taken back LOW after ^tOEH is met. If CAS# goes HIGH prior to OE# going back LOW, the DQs will remain open.
19. Requires that ^tAA and ^tCAC are not violated.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}. It is referenced from the rising edge of RAS# or CAS#, whichever occurs last.
21. The ^tRAD (MAX) limit is no longer specified. ^tRAD (MAX) was specified as a reference point only. If ^tRAD was greater than the specified ^tRAD (MAX) limit, then access time was controlled exclusively by ^tAA (^tRAC and ^tCAC no longer applied). With or without the ^tRAD (MAX) limit, ^tAA, ^tRAC and ^tCAC must always be met.
22. The ^tRCD (MAX) limit is no longer specified. ^tRCD (MAX) was specified as a reference point only. If ^tRCD was greater than the specified ^tRCD (MAX) limit, then access time was controlled exclusively by ^tCAC (^tRAC [MIN] no longer applied). With or without the ^tRCD limit, ^tAA and ^tCAC must always be met.
23. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# is LOW and OE# is HIGH.
25. The refresh period is extended from 32ms (2K refresh) or 64ms (4K refresh) to 128ms (both 2K and 4K refresh). For 4K refresh, $^tRC = 31.25$μs (128ms/4,096 rows = 31.25μs) and for 2K refresh, $^tRC = 62.5$μs (128ms/2,048 rows = 62.5μs).
26. V_{IH} overshoot: V_{IH} (MAX) = V_{DD} + 2V for a pulse width $\leq$ 10ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width $\leq$ 10ns, and the pulse width cannot be greater than one third of the cycle rate.

READ CYCLE

DON'T CARE

UNDEFINED

TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
t_{AA}		25		30	ns
t_{ACH}	12		15		ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAC}		13		15	ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CLZ}	0		0		ns
t_{CRP}	5		5		ns
t_{CSH}	38		45		ns
t_{OD}	0	12	0	15	ns
t_{OE}		12		15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
t_{OFF}	0	12	0	15	ns
t_{RAC}		50		60	ns
t_{RAD}	9		12		ns
t_{RAH}	9		10		ns
t_{RAS}	50	10,000	60	10,000	ns
t_{RC}	84		104		ns
t_{RCD}	11		14		ns
t_{RCH}	0		0		ns
t_{RCS}	0		0		ns
t_{RP}	30		40		ns
t_{RRH}	0		0		ns
t_{RSH}	13		15		ns

NOTE: 1. t_{OFF} is referenced from rising edge of RAS# or CAS#, whichever occurs last.

EARLY WRITE CYCLE

DON'T CARE

UNDEFINED
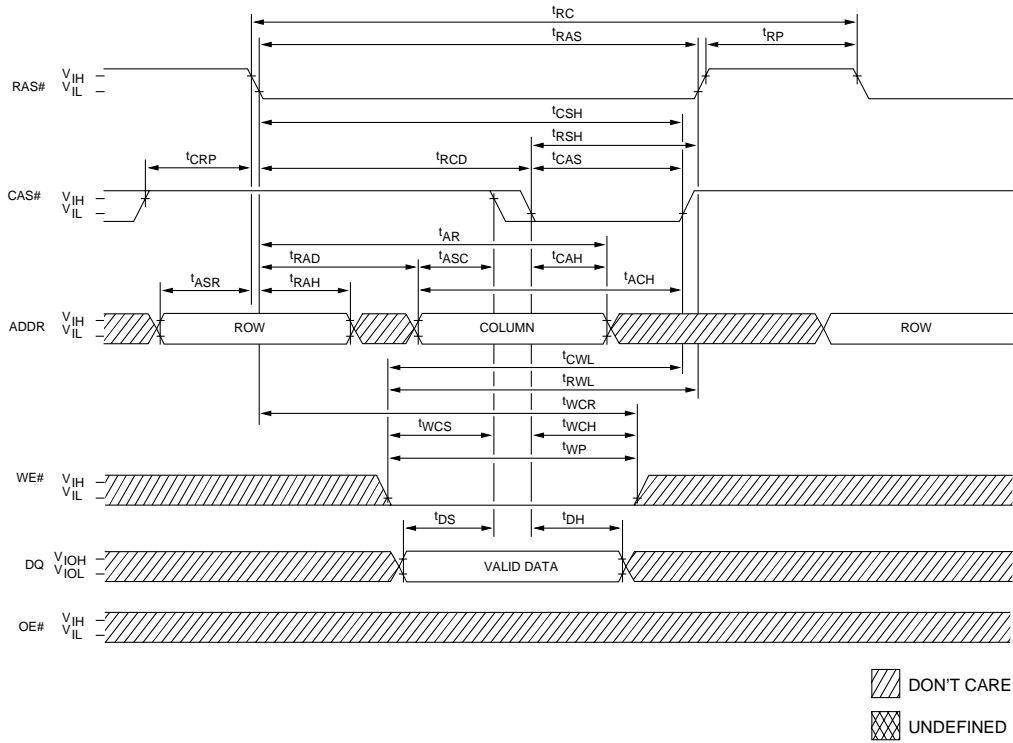
TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{ACH}	12		15		ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CRP}	5		5		ns
t_{CSH}	38		45		ns
t_{CWL}	8		10		ns
t_{DH}	8		10		ns
t_{DS}	0		0		ns
t_{RAD}	9		12		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{RAH}	9		10		ns
t_{RAS}	50	10,000	60	10,000	ns
t_{RC}	84		104		ns
t_{RCD}	11		14		ns
t_{RP}	30		40		ns
t_{RSH}	13		15		ns
t_{RWL}	13		15		ns
t_{WCH}	8		10		ns
t_{WCR}	38		45		ns
t_{WCS}	0		0		ns
t_{WP}	5		5		ns

READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
t_{AA}		25		30	ns
t_{ACH}	12		15		ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{AWD}	42		49		ns
t_{ASR}	0		0		ns
t_{CAC}		13		15	ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CLZ}	0		0		ns
t_{CRP}	5		5		ns
t_{CSH}	38		45		ns
t_{CWD}	28		35		ns
t_{CWL}	8		10		ns
t_{DH}	8		10		ns
t_{DS}	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
t_{OD}	0	12	0	15	ns
t_{OE}		12		15	ns
t_{OEH}	8		10		ns
t_{RAC}		50		60	ns
t_{RAD}	9		12		ns
t_{RAH}	9		10		ns
t_{RAS}	50	10,000	60	10,000	ns
t_{RCD}	11		14		ns
t_{RCS}	0		0		ns
t_{RP}	30		40		ns
t_{RSH}	13		15		ns
t_{RWC}	116		140		ns
t_{RWD}	67		79		ns
t_{RWL}	13		15		ns
t_{WP}	5		5		ns

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EDO-PAGE-MODE READ CYCLE

| | DON'T CARE |
| | UNDEFINED |
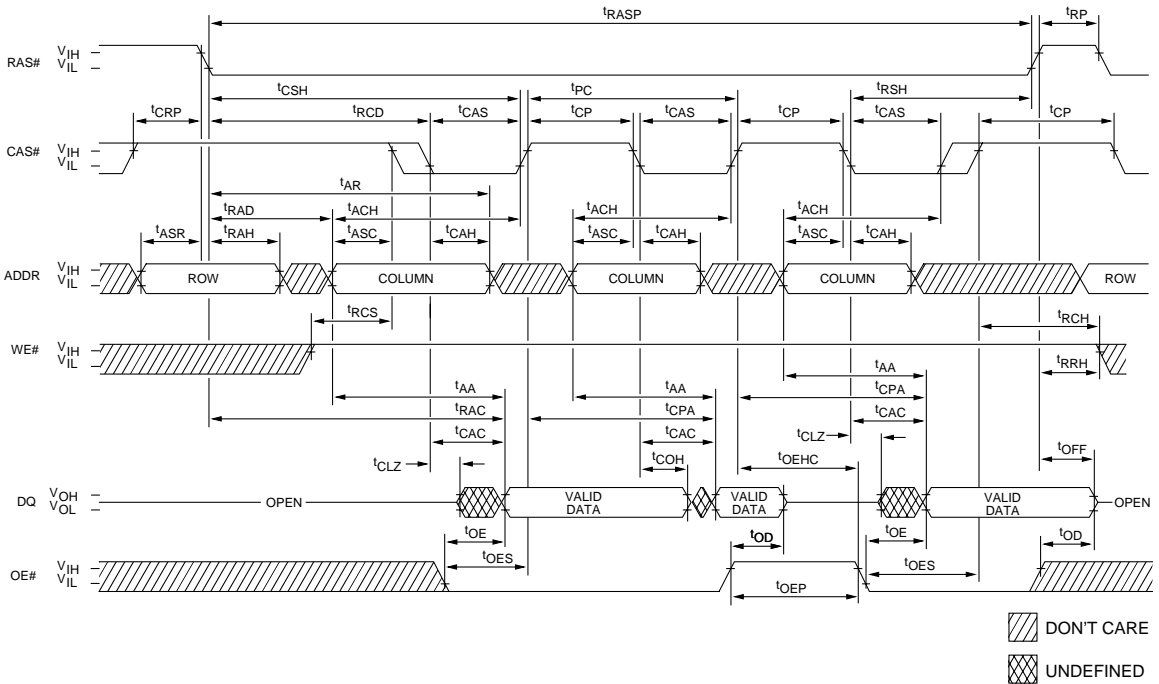
TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{AA}		25		30	ns
t_{ACH}	12		15		ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAC}		13		15	ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CLZ}	0		0		ns
t_{COH}	3		3		ns
t_{CP}	8		10		ns
t_{CPA}		28		35	ns
t_{CRP}	5		5		ns
t_{CSH}	38		45		ns
t_{OD}	0	12	0	15	ns
t_{OE}		12		15	ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{OEHC}	5		10		ns
t_{OEP}	5		5		ns
t_{OES}	4		5		ns
t_{OFF}	0	12	0	15	ns
t_{PC}	20		25		ns
t_{RAC}		50		60	ns
t_{RAD}	9		12		ns
t_{RAH}	9		10		ns
t_{RASP}	50	125,000	60	125,000	ns
t_{RCD}	11		14		ns
t_{RCH}	0		0		ns
t_{RCS}	0		0		ns
t_{RP}	30		40		ns
t_{RRH}	0		0		ns
t_{RSH}	13		15		ns

EDO-PAGE-MODE EARLY WRITE CYCLE

□ DON'T CARE

▨ UNDEFINED

TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
t_{ACH}	12		15		ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CP}	8		10		ns
t_{CRP}	5		5		ns
t_{CSH}	38		45		ns
t_{CWL}	8		10		ns
t_{DH}	8		10		ns
t_{DS}	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
t_{PC}	20		25		ns
t_{RAD}	9		12		ns
t_{RAH}	9		10		ns
t_{RASP}	50	125,000	60	125,000	ns
t_{RCD}	11		14		ns
t_{RP}	30		40		ns
t_{RSH}	13		15		ns
t_{RWL}	13		15		ns
t_{WCH}	8		10		ns
t_{WCR}	38		45		ns
t_{WCS}	0		0		ns
t_{WP}	5		5		ns

EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
t_{AA}		25		30	ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{AWD}	42		49		ns
t_{CAC}		13		15	ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CLZ}	0		0		ns
t_{CP}	8		10		ns
t_{CPA}		28		35	ns
t_{CRP}	5		5		ns
t_{CSH}	38		45		ns
t_{CWD}	28		35		ns
t_{CWL}	8		10		ns
t_{DH}	8		10		ns
t_{DS}	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
t_{OD}	0	12	0	15	ns
t_{OE}		12		15	ns
t_{OEH}	8		10		ns
t_{PC}	20		25		ns
t_{PRWC}	47		56		ns
t_{RAC}		50		60	ns
t_{RAD}	9		12		ns
t_{RAH}	9		10		ns
t_{RASP}	50	125,000	60	125,000	ns
t_{RCD}	11		14		ns
t_{RCS}	0		0		ns
t_{RP}	30		40		ns
t_{RSH}	13		15		ns
t_{RWD}	67		79		ns
t_{RWL}	13		15		ns
t_{WP}	5		5		ns

NOTE: 1. t_{PC} is for LATE WRITE cycles only.

EDO-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

▨ DON'T CARE

▨ UNDEFINED

TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
t_{AA}		25		30	ns
t_{ACH}	12		15		ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAC}		13		15	ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{COH}	3		3		ns
t_{CP}	8		10		ns
t_{CPA}		28		35	ns
t_{CRP}	5		5		ns
t_{CSH}	38		45		ns
t_{DH}	8		10		ns
t_{DS}	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
t_{OE}		12		15	ns
t_{PC}	20		25		ns
t_{RAC}		50		60	ns
t_{RAD}	9		12		ns
t_{RAH}	9		10		ns
t_{RASP}	50	125,000	60	125,000	ns
t_{RCD}	11		14		ns
t_{RCH}	0		0		ns
t_{RCS}	0		0		ns
t_{RP}	30		40		ns
t_{RSH}	13		15		ns
t_{WCH}	8		10		ns
t_{WCS}	0		0		ns
t_{WHZ}	0	12	0	15	ns

READ CYCLE
(With WE#-controlled disable)

TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
t_{AA}		25		30	ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAC}		13		15	ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CLZ}	0		0		ns
t_{CP}	8		10		ns
t_{CRP}	5		5		ns
t_{CSH}	38		45		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
t_{OD}	0	12	0	15	ns
t_{OE}		12		15	ns
t_{RAC}		50		60	ns
t_{RAD}	9		12		ns
t_{RAH}	9		10		ns
t_{RCD}	11		14		ns
t_{RCH}	0		0		ns
t_{RCS}	0		0		ns
t_{WHZ}	0	12	0	15	ns
t_{WPZ}	10		10		ns

RAS#-ONLY REFRESH CYCLE
(OE# and WE# = DON'T CARE)
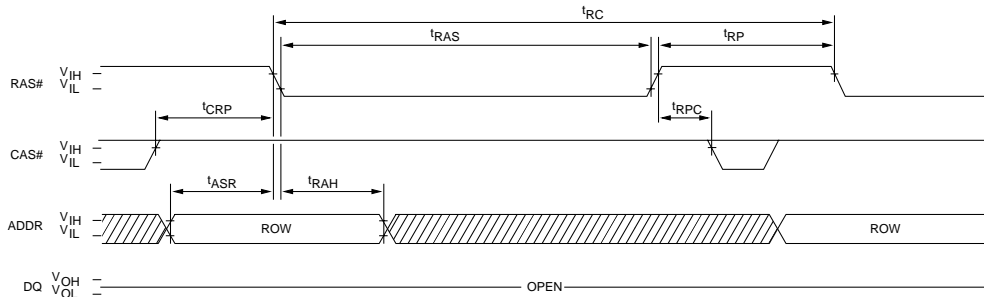
CBR REFRESH CYCLE
(Addresses and OE# = DON'T CARE)
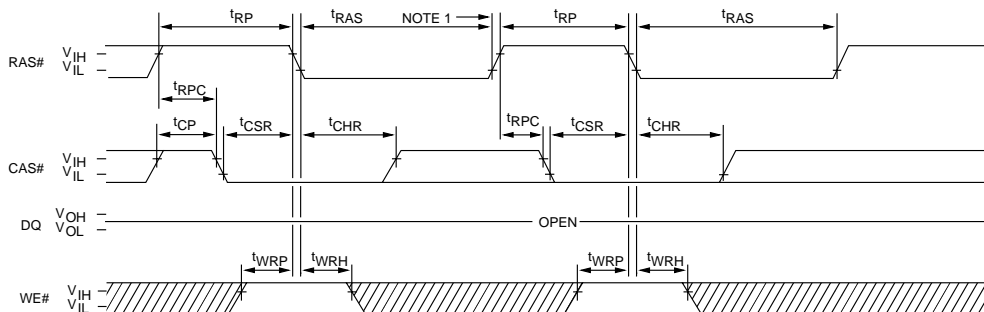
DON'T CARE

UNDEFINED
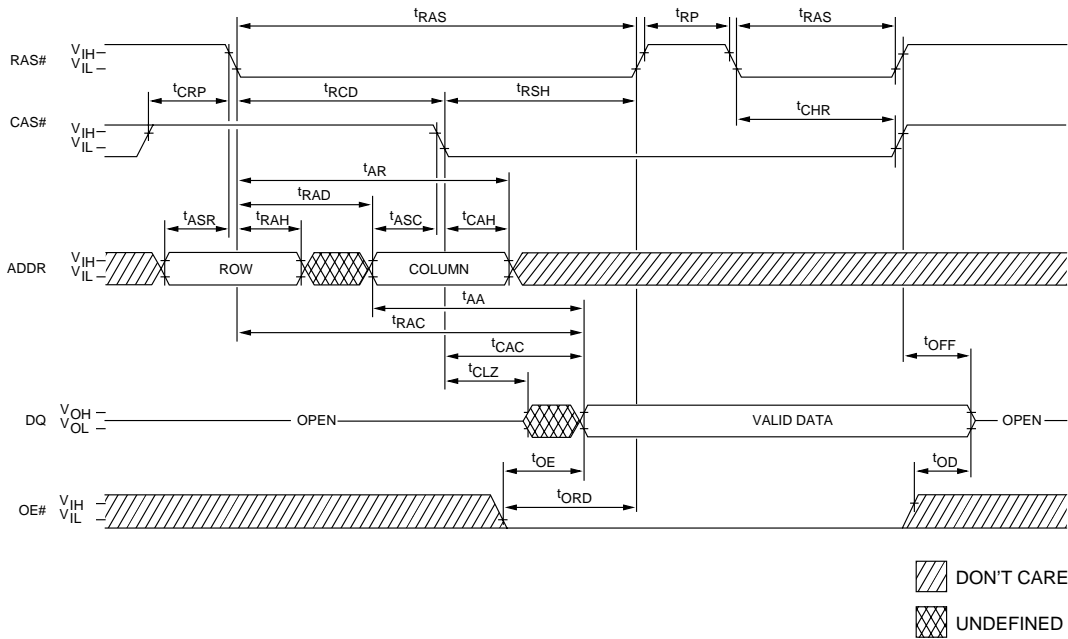
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^{t}ASR	0		0		ns
^{t}CHR	8		10		ns
^{t}CP	8		10		ns
^{t}CRP	5		5		ns
^{t}CSR	5		5		ns
^{t}RAH	9		10		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^{t}RAS	50	10,000	60	10,000	ns
^{t}RC	84		104		ns
^{t}RP	30		40		ns
^{t}RPC	5		5		ns
^{t}WRH	8		10		ns
^{t}WRP	8		10		ns

NOTE: 1. End of first CBR REFRESH cycle.

HIDDEN REFRESH CYCLE [24]
(WE# = HIGH; OE# = LOW)

DON'T CARE

UNDEFINED

TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
t_{AA}		25		30	ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAC}		13		15	ns
t_{CAH}	8		10		ns
t_{CHR}	8		10		ns
t_{CLZ}	0		0		ns
t_{CRP}	5		5		ns
t_{OD}	0	12	0	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
t_{OE}		12		15	ns
t_{OFF}	0	12	0	15	ns
t_{ORD}	0		0		ns
t_{RAC}		50		60	ns
t_{RAD}	9		12		ns
t_{RAH}	9		10		ns
t_{RAS}	50	10,000	60	10,000	ns
t_{RCD}	11		14		ns
t_{RP}	30		40		ns
t_{RSH}	13		15		ns

SELF REFRESH CYCLE
(Addresses and OE# = DON'T CARE)

DON'T CARE

UNDEFINED
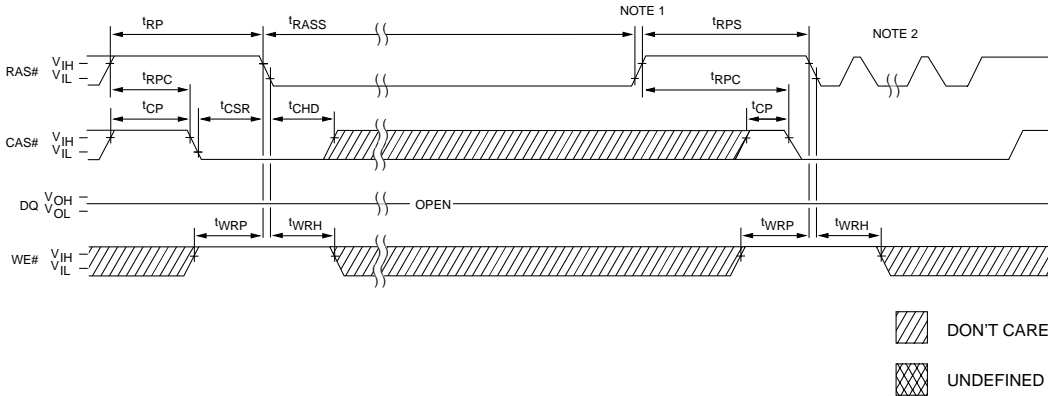
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^tCHD	15		15		ns
^tCP	8		10		ns
^tCSR	5		5		ns
^tRASS	100		100		μs
^tRP	30		40		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
^tRPC	5		5		ns
^tRPS	90		105		ns
^tWRH	8		10		ns
^tWRP	8		10		ns

NOTE: 1. Once ^tRASS (MIN) is met and RAS# remains LOW, the DRAM will enter self refresh mode.
2. Once ^tRPS is satisfied, a complete burst of all rows should be executed.

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24/26-PIN PLASTIC SOJ (300 mil)

DA-1
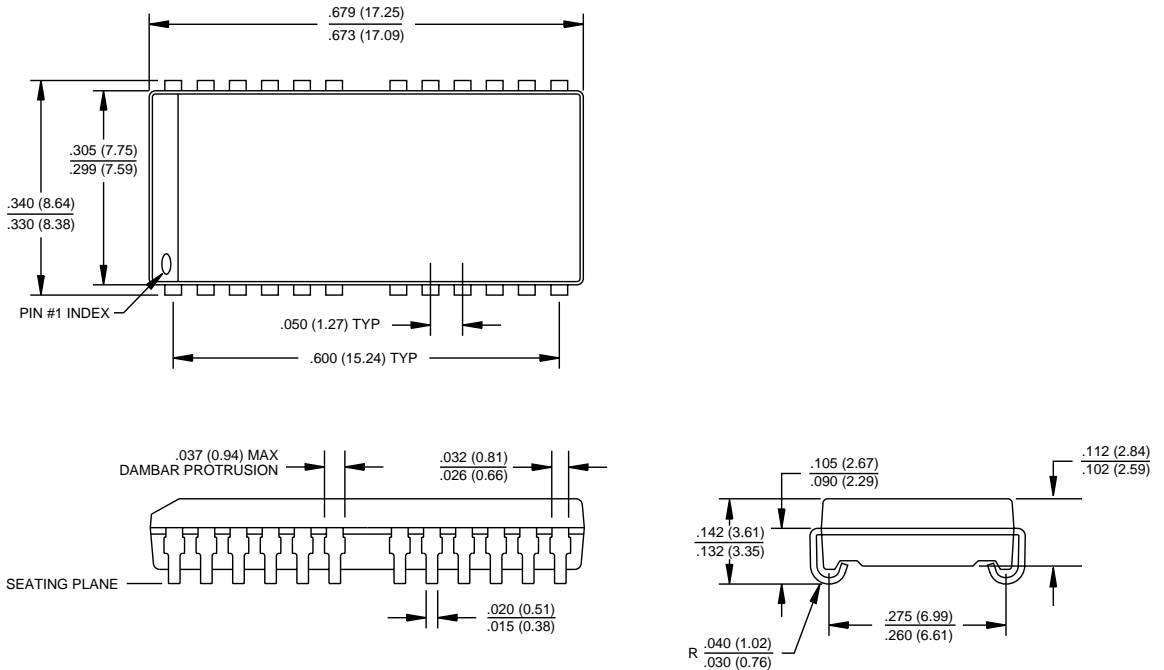
.679 (17.25)
.673 (17.09)

.305 (7.75)
.299 (7.59)

.340 (8.64)
.330 (8.38)

PIN #1 INDEX

.050 (1.27) TYP

.600 (15.24) TYP

.037 (0.94) MAX
DAMBAR PROTRUSION

.032 (0.81)
.026 (0.66)

SEATING PLANE

.020 (0.51)
.015 (0.38)

.105 (2.67)
.090 (2.29)

.112 (2.84)
.102 (2.59)

.142 (3.61)
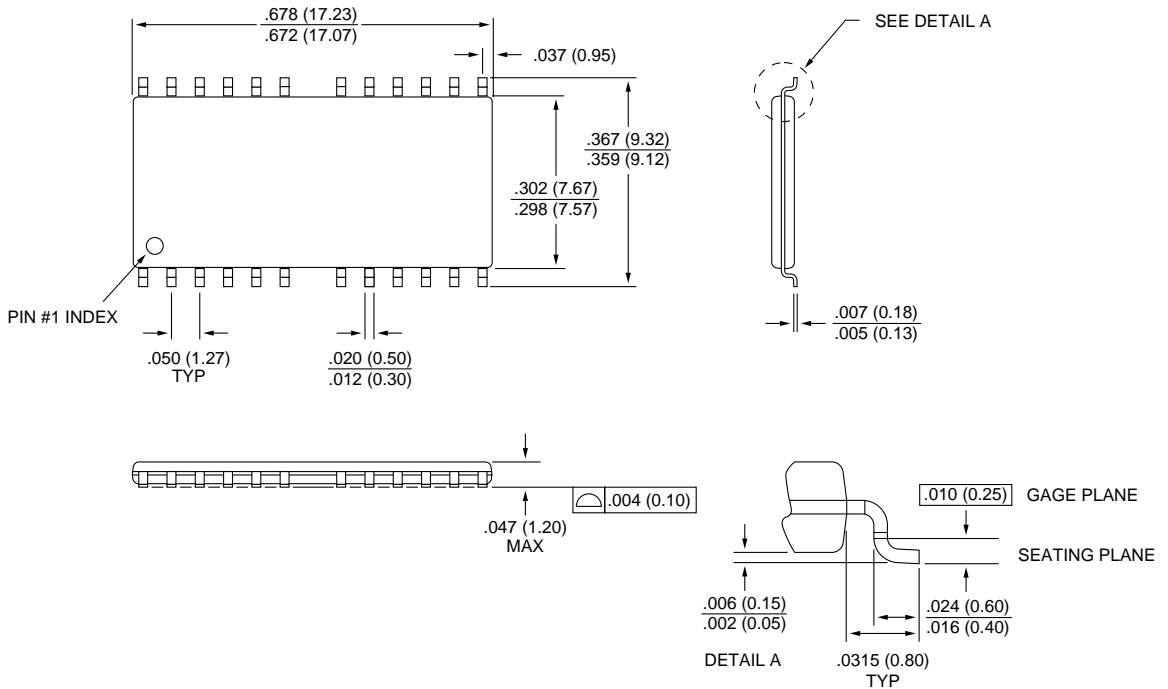.132 (3.35)

.275 (6.99)
.260 (6.61)

R .040 (1.02)
.030 (0.76)

NOTE: 1. All dimensions in inches (millimeters) $\dfrac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

MICRON
TECHNOLOGY, INC.

24/26-PIN PLASTIC TSOP (300 mil)

DB-1

.678 (17.23)
.672 (17.07)

.037 (0.95)

SEE DETAIL A

.367 (9.32)
.359 (9.12)

.302 (7.67)
.298 (7.57)

PIN #1 INDEX

.050 (1.27)
TYP

.020 (0.50)
.012 (0.30)

.007 (0.18)
.005 (0.13)

.047 (1.20)
MAX

.004 (0.10)

.010 (0.25) GAGE PLANE

SEATING PLANE

.006 (0.15)
.002 (0.05)

.024 (0.60)
.016 (0.40)

DETAIL A   .0315 (0.80)
TYP

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.