INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS 2006 UPDATE

PROCESS INTEGRATION, DEVICES, AND STRUCTURES

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SUMMARY

The 2006 PIDS chapter is mainly unchanged from the 2005 edition. There are minor updates and corrections, but major changes will await the 2007 edition. The exception is in the Logic Technology Requirements tables, where there are notable changes in the timing of the projected deployment of several key technology innovations. Specifically, for high-performance and low operating power (LOP) logic, the projected implementation of high-κ gate dielectric and metal gate electrode is delayed from 2008 (as forecasted in the 2005 ITRS) until 2010. Also, the projected implementation of fully depleted ultra-thin body (FD-UTB) silicon-on-insulator (SOI) MOSFETs for high-performance logic is delayed from 2008 (as forecasted in the 2005 ITRS) until 2010. The reason for these delays is that it now seems unlikely that the integrated circuit (IC) industry will find it feasible to deploy these innovations as early as 2008. However, for low standby power (LSTP) logic, the projected implementation of high-κ gate dielectric and metal gate electrode is in 2008, as forecasted in the 2005 ITRS. For LSTP, the relatively thick dielectric equivalent oxide thickness of 1.6 nm in 2008 and the potential use of fully silicided gate electrodes make the 2008 projected deployment more feasible than for LOP and high-performance logic.

The consequences of the delay in deploying high-κ gate dielectric and metal gate electrode were analyzed for the affected years, 2008 and 2009. The scaling of the equivalent oxide thickness of the gate dielectric is slowed in 2008 and 2009 compared to that in the 2005 PIDS tables in order to keep the gate leakage current within tolerable limits. Other consequences for those two years include increases in the source/drain leakage current and some slowing in the scaling of the transistor intrinsic delay, τ. Furthermore, $\tau = CV_{dd}/I_{d,sat}$, where C is the load capacitance, V_{dd} is the power supply voltage, and $I_{d,sat}$ is the transistor saturation drive current. Since C is inversely proportional to the equivalent oxide thickness, both C and $I_{d,sat}$ are reduced for 2008 and 2009. See the text and the updated technology requirements tables for details.

DIFFICULT CHALLENGES

Table 39a Process Integration Difficult Challenges—Near-term

Difficult Challenges ≥ 32 nm	*Summary of Issues*
1. Scaling of MOSFETs to the 32 nm technology generation	Scaling planar bulk CMOS will face significant challenges due to the high channel doping required, band-to-band tunneling across the junction and gate-induced drain leakage (GIDL), stochastic doping variations, and difficulty in adequately controlling short channel effects. Implementation into manufacturing of new structures such as ultra-thin body fully depleted silicon-on-insulator (SOI) and multiple-gate (e.g., FinFET) MOSFETs is expected. This implementation will be challenging, with numerous new and difficult issues. A particularly challenging issue is the control of the thickness and its variability for these ultra-thin MOSFETs.
2. Implementation of high-κ gate dielectric and metal gate electrode in a timely manner	High κ and metal gate electrode will be required beginning in ~2008. Timely implementation will involve dealing with numerous challenging issues, including appropriate tuning of metal gate work function, ensuring adequate channel mobility with high-κ, reducing the defects in high-κ to acceptable levels, ensuring reliability, and others.
3. Timely assurance for the reliability of multiple and rapid material, process, and structural changes	Multiple changes are projected over the next decade, such as.: Material: high-κ gate dielectric, metal gate electrodes by 2008 or so Process: elevated S/D (selective epi) and advanced annealing and doping techniques Structure: ultra-thin body (UTB) fully depleted (FD) SOI, followed by multiple-gate structures. It will be an important challenge to ensure the reliability of all these new materials, processes, and structures in a timely manner.
4. Scaling of DRAM and SRAM to the 32 nm technology generation	DRAM main issues with scaling—adequate storage capacitance for devices with reduced feature size, including difficulties in implementing high-κ storage dielectrics; access device design; holding the overall leakage to acceptably low levels; and deploying low sheet resistance materials for bit and word lines to ensure desired speed for scaled DRAMs. Also, reducing the cell area factor in a timely manner is quite challenging. (Cell area factor = a = cell area/F^2, where F=DRAM half pitch). SRAM—Difficulties with maintaining adequate noise margin and controlling key instabilities and soft error rate with scaling. Also, difficult lithography and etch issues with scaling.
5. Scaling high-density non-volatile memory to the 32 nm technology generation	Flash—Non-scalability of tunnel dielectric and interpoly dielectric. Dielectric material properties and dimensional control are key issues. FeRAM—Continued scaling of stack capacitor is quite challenging. Eventually, continued scaling in 1T1C configuration. Sensitivity to IC processing temperatures and conditions. SONOS—ONO stack dimensions and material properties, including nitride layer trap distribution in space and energy MRAM—Magnetic material properties and dimensional control. Sensitivity to IC processing temperatures and conditions

Table 39b Process Integration Difficult Challenges—Long-term

Difficult Challenges<32 nm	*Summary of Issues*
6. Implementation of advanced, non-classical CMOS with enhanced drive current and acceptable control of short channel effects for highly scaled MOSFETs	Advanced non-classical CMOS (e.g., multiple-gate MOSFETs) with ultra-thin, lightly doped body will be needed to effectively scale MOSFETs to 11 nm gate length and below. To attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced thermal velocity and injection at the source end appears to be needed. Eventually, nanowires, carbon nanotubes, or other high transport channel materials (e.g., germanium or III-V thin channels on silicon) may be needed.
7. Dealing with fluctuations and statistical process variations in sub-11 nm gate length MOSFETs	Fundamental issues of statistical fluctuations for sub-11 nm gate length MOSFETs are not completely understood, including the impact of quantum effects, line edge roughness, and width variation.
8. Identifying, selecting, and implementing new memory structures	Dense, fast, low operating voltage non-volatile memory will become highly desirable Increasing difficulty is expected in scaling DRAMs, especially scaling down the dielectric equivalent oxide thickness and attaining the very low leakage currents that will be required. All of the existing forms of nonvolatile memory face limitations based on material properties. Success will hinge on finding and developing alternative materials and/or development of alternative emerging technologies. See Emerging Research Devices section for more detail.
9. Identifying, selecting, and implementing novel interconnect schemes	Eventually, it is projected that the performance of copper/low-κ interconnect will become inadequate to meet the speed and power dissipation goals of highly scaled ICs. Solutions (optical, microwave/RF, etc,) are currently unclear. For detail, refer to ITRS Interconnect chapter.
10. Toward the end of the Roadmap or beyond, identification, selection, and implementation of advanced, beyond-CMOS devices and architectures for advanced information processing	Will drive major changes in process, materials, device physics, design, etc. Performance, power dissipation, etc., of beyond-CMOS devices need to extend well beyond CMOS limits. Beyond-CMOS devices need to integrate physically or functionally into a CMOS platform. Such integration may be difficult. See Emerging Research Devices sections for more discussion and detail.

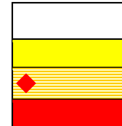
LOGIC TECHNOLOGY REQUIREMENTS

Table 40a High-Performance Logic Technology Requirements—Near-term UPDATED

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion)

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
	L_g: Physical L_{gate} for High Performance logic (nm) [1]	32	28	25	22	20	18	16	14	13
	EOT: Equivalent Oxide Thickness [2]									
IS	Extended planar bulk (Å)	12	11	11	10	9	6.5	5	5	
Delete	UTB FD (Å)				~~9~~	~~8~~	7	6	5	5
	DG (Å)							8	7	6
	Gate Poly Depletion and Inversion-Layer Thickness [3]									
IS	Extended Planar Bulk (Å)	7.3	7.4	7.4	7.0	7.0	2.7	2.5	2.5	
Delete	UTB FD (Å)				~~4~~	~~4~~	4	4	4	4
	DG (Å)							4	4	4
	EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]									
IS	Extended Planar Bulk (Å)	19.3	18.4	18.4	17.0	16.0	9.2	7.5	7.5	
Delete	UTB FD (Å)				~~13~~	~~12~~	11	10	9	9
	DG (Å)							12	11	10
	$J_{g,limit}$: Maximum gate leakage current density [5]									
IS	Extended Planar Bulk (A/cm^2)	1.88E+02	5.36E+02	8.00E+02	1.18E+03	1.10E+03	1.56E+03	2.00E+03	2.43E+03	
Delete	UTB FD (A/cm^2)				~~7.73E+02~~	~~9.50E+02~~	1.22E+03	1.38E+03	2.07E+03	2.23E+03
	DG (A/cm^2)							6.25E+02	7.86E+02	8.46E+02
	V_{dd}: Power Supply Voltage (V) [6]	1.1	1.1	1.1	1	1	1	1	0.9	0.9
	$V_{t,sat}$: Saturation Threshold Voltage [7]									
IS	Extended Planar Bulk (mV)	195	168	165	164	237	151	146	148	
Delete	UTB FD (mV)				~~169~~	~~168~~	167	170	166	167
	DG (mV)							181	184	185
	$I_{sd,leak}$: Source/Drain Subthreshold Off-State Leakage Current [8]									
IS	Extended Planar Bulk (µA/µm)	0.06	0.15	0.2	0.26	0.22	0.28	0.32	0.34	
Delete	UTB FD (µA/µm)				~~0.17~~	~~0.19~~	0.22	0.22	0.29	0.29
	DG (µA/µm)							0.1	0.11	0.11
	$I_{d,sat}$: effective NMOS Drive Current [9]									
IS	Extended Planar Bulk (µA/µm)	1.02E+03	1.13E+03	1.20E+03	1.21E+03	1.18E+03	2.05E+03	2.49E+03	2.30E+03	
Delete	UTB FD (µA/µm)				~~1486~~	~~1625~~	1815	2015	2037	2198
	DG (µA/µm)							1899	1932	2220
	Mobility Enhancement Factor for $I_{d,sat}$ [10]									
	Extended Planar Bulk	1.09	1.09	1.08	1.09	1.1	1.1	1.12	1.11	
Delete	UTB FD				~~1.06~~	~~1.06~~	1.06	1.06	1.05	1.05
	DG							1.05	1.04	1.05

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
	MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
	Effective Ballistic Enhancement Factor [11]									
	Extended Planar Bulk	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	
Delete	UTB FD				~~1~~	~~1~~	**1**	**1**	**1**	**1.1**
	DG							**1.17**	**1.25**	**1.31**
	R_{sd}: Effective Parasitic series source/drain resistance [12]									
	Extended Planar Bulk (Ω-µm)	**180**	**170**	**140**	**140**	**120**	**105**	**80**	**70**	
Delete	UTB FD (Ω-µm)				~~155~~	~~140~~	**125**	**110**	**90**	**75**
	DG (Ω-µm)							**110**	**100**	**90**
	$C_{g,ideal}$: Ideal NMOS Device Gate Capacitance [13]									
IS	Extended Planar Bulk (F/µm)	**5.73E-16**	**5.25E-16**	**4.69E-16**	**4.46E-16**	**4.31E-16**	**6.78E-16**	**7.39E-16**	**6.41E-16**	
Delete	UTB FD (F/µm)				~~5.84E-16~~	~~5.75E-16~~	**5.65E-16**	**5.52E-16**	**5.37E-16**	**4.98E-16**
	DG (F/µm)							**4.60E-16**	**4.39E-16**	**4.48E-16**
	$C_{g,total}$: Total gate capacitance for calculation of CV/I [14]									
IS	Extended Planar Bulk (F/µm)	**8.13E-16**	**7.65E-16**	**6.99E-16**	**6.56E-16**	**6.01E-16**	**8.28E-16**	**8.59E-16**	**7.51E-16**	
Delete	UTB FD (F/µm)				~~8.04E-16~~	~~7.55E-16~~	**7.35E-16**	**6.92E-16**	**6.67E-16**	**6.18E-16**
	DG (F/µm)							**6.50E-16**	**6.29E-16**	**6.28E-16**
IS	*$\tau = CV/I$: NMOSFET intrinsic delay (ps) [15]*	**0.87**	**0.74**	**0.64**	**0.54**	**0.51**	**0.4**	**0.34**	**0.29**	**0.25**
IS	*$1/\tau$: NMOSFET intrinsic switching speed (GHz) [16]*	**1149**	**1351**	**1563**	**1852**	**1961**	**2500**	**2941**	**3448**	**4000**



Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 40b High-Performance Logic Technology Requirements—Long-term

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
L_g: Physical L_{gate} for High Performance logic (nm) [1]	**11**	**10**	**9**	**8**	**7**	**6**	**5**
EOT: Equivalent Oxide Thickness [2]							
Extended planar bulk (Å)							
UTB FD (Å)	5	5					
DG (Å)	6	6	5	5	5	5	5
Gate Poly Depletion & Inversion-Layer Thickness [3]							
Extended planar bulk (Å)							
UTB FD (Å)	4	4					
DG (Å)	4	4	4	4	4	4	4
EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]							
Extended Planar Bulk (Å)							
UTB FD (Å)	9	9					
DG (Å)	10	10	9	9	9	9	9
$J_{g,limit}$: Maximum gate leakage current density [5]							
Extended Planar Bulk (A/cm^2)							
FDSOI (A/cm^2)	3.27E+03	3.70E+03					
DG (A/cm^2)	1.00E+03	1.10E+03	1.22E+03	1.38E+03	1.57E+03	1.83E+03	2.20E+03
V_{dd}: Power Supply Voltage (V) [6]	**0.9**	**0.8**	**0.8**	**0.7**	**0.7**	**0.7**	**0.7**
$V_{t,sat}$: Saturation Threshold Voltage [7]							
Extended Planar Bulk (mV)							
UTB FD (mV)	164	166					
DG (mV)	190	192	195	200	201	205	208
$I_{sd,leak}$: Source/Drain Subthreshold Off-State Leakage Current [8]							
Extended Planar Bulk (µA/µm)							
UTB FD (µA/µm)	0.36	0.37					
DG (µA/µm)	0.11	0.11	0.11	0.11	0.11	0.11	0.11
$I_{d,sat}$: effective NMOS Drive Current [9]							
Extended Planar Bulk (µA/µm)							
UTB FD (µA/µm)	2290	2188					
DG (µA/µm)	2354	2275	2713	2533	2740	2744	2981
Mobility Enhancement Factor for $I_{d,sat}$ [10]							
Extended Planar Bulk							
UTB FD	1.04	1.04					
DG	1.04	1.04	1.04	1.04	1.03	1.03	1.03
Effective Ballistic Enhancement Factor [11]							
Extended Planar Bulk							
UTB FD	1.15	1.28					
DG	1.37	1.53	1.67	1.87	1.99	1.97	2.11

Table 40b High-Performance Logic Technology Requirements—Long-term (continued)

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
R_{sd}: Effective Parasitic series source/drain resistance [12]							
Planar Bulk (Ω-µm)							
UTB FD (Ω-µm)	75	75					
DG (Ω-µm)	85	80	75	70	65	60	55
Cg,ideal: Ideal NMOS Device Gate Capacitance [13]							
Extended Planar Bulk (F/µm)							
UTB FD (F/µm)	4.22E-16	3.83E-16					
DG (F/µm)	3.80E-16	3.45E-16	3.45E-16	3.07E-16	2.68E-16	2.30E-16	1.92E-16
$C_{g,total}$: Total gate capacitance for calculation of CV/I [14]							
Extended Planar Bulk (F/µm)							
UTB FD (F/µm)	5.42E-16	5.03E-16					
DG (F/µm)	5.59E-16	5.25E-16	5.25E-16	4.87E-16	4.48E-16	4.10E-16	3.62E-16
$\tau = CV/I$: NMOSFET intrinsic delay (ps) [15]	0.210	0.180	0.150	0.130	0.110	0.100	0.080
$1/\tau$: NMOSFET intrinsic switching speed (GHz) [16]	4762	5556	6667	7692	9091	10000	12500

Manufacturable solutions exist, and are being optimized
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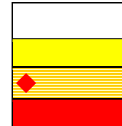
Manufacturable solutions are NOT known



Notes for Tables 40a and b:

As described in the text, MASTAR, a detailed analytical MOSFET modeling software package, has been utilized to generate the parameter values in these tables. The MASTAR modeling package and user's manual are in the backup material on the ITRS website, as well as the detailed MASTAR simulations that underlay these tables. Also note that the parameters in this table are for an NMOSFET with nominal gate length at an operating temperature of 25°C. Furthermore, although there are multiple MOSFETs in a typical logic chip, with differing threshold voltages, I_{on}, I_{off}, and oxide thickness, the transistor specified here is the transistor with the lowest threshold voltage, highest I_{on} and highest I_{off}, lowest oxide thickness, and fastest CV/I. This transistor typically constitutes a small minority of the transistors on a chip; it is used mainly in critical paths, and most of the transistors on the chip have higher threshold voltage and lower leakage current. This high speed, high leakage transistor is specified in this table because it tends to drive the technology.

IS *As explained in the text, multiple parallel options for the transistor type are included in the tables, including planar bulk CMOS extended to its practical scaling limits, ultra-thin body fully-depleted (UTB FD) SOI CMOS, also extended to its practical scaling limits, and double-gate (DG) CMOS (e.g., FinFETs). Note that the limit for planar bulk CMOS is through 2012, and for UTB FD it is through 2015, while DG continues through 2020. **In the 2006 ITRS, the projected initial implementation of UTB FD is delayed from 2008 per the 2005 ITRS until 2010 (see summary for discussion of this point).** The impact of the challenges in scaling planar bulk are clear from this table, since for planar bulk, the Source/Drain subthreshold leakage current, $I_{sd,leak}$, increases sharply for the latter years, from 0.22 μ**A**/μm in 2009 to 0.34 μ**A**/μm in 2012, and $I_{sd,leak}$ is always higher for planar bulk than for UTB FD and DG. Furthermore, both EOT and the effective parasitic series resistance, R_{sd}, are scaled more rapidly (to meet the performance target) from ~~2008~~ **2010** through 2012 for planar bulk than for UTB FD or DG. Finally, from the MASTAR modeling results, the short channel effects such as drain induced barrier lowering (DIBL) are always larger for planar bulk than for UTB FD or DG. In a similar vein, for DG, $I_{sd,leak}$ is lower than for UTB FD, while EOT and R_{sd} are scaled more slowly for DG than for UTB FD. Furthermore, from the MASTAR modeling results, short channel effects are always lower for DG. Hence, DG is the ultimate MOSFET device, continuing through the end of the Roadmap in 2020.*

For each transistor option, the scaling of the numbers in the tables reflects a particular scaling scenario in which we have attempted to optimally scale to meet the key goal for high-performance logic, 17% per year average improvement in the NMOS intrinsic switching speed, while keeping the leakage currents, the short channel effects, and other key characteristics under control. For the planar bulk CMOS option, another goal was to delay the projected need for such major innovations as metal gate electrode, high-κ gate dielectric, and novel doping and annealing techniques to reduce the value of the parasitic series source/drain resistance. However, there are numerous parameters (such as EOT, V_{dd}, $I_{sd,leak}$, etc.) that can be varied, and different scaling scenarios are possible by making different choices on the scaling of these parameters. The scenarios in this table were selected to be as representative of the industry as possible. In particular, in this table, high-κ gate dielectric and metal gate electrode are assumed to be available in 2008. See the figures and discussion in the text for why high-κ gate dielectric is required in 2008. With the EOT=0.9 nm in 2008, metal gate electrode is needed to reduce the polysilicon depletion.

[1] L_g is the physical gate length: the final, as-etched length of the bottom of the gate electrode. Values have been set by the ORTC. The gate dimensional control requirement is set by the Lithography and FEP Etch ITWGs, and is assumed to have a three-sigma value of ± 12% × L_g. It is expected that meeting this requirement will become increasingly difficult with scaling (refer to the Lithography chapter and the FEP chapter). Gate length variation is assumed to be a primary factor responsible for driving device parameter variation.

IS *[2] For a gate dielectric of thickness T_d and relative dielectric constant κ, EOT is defined by: EOT = T_d / (κ/3.9), where 3.9 is the relative dielectric constant of thermal silicon dioxide. For a MOSFET with the gate dielectric of thickness T_d, the ideal gate capacitance per unit area is the same as that of a similar MOSFET, but with a gate dielectric made up of thermal silicon dioxide with a thickness of EOT. It is projected that high-κ gate dielectric will be required by ~~2008~~ **2010** to control the gate leakage (**this is delayed from the 2008 projected deployment date in the 2005 ITRS;** see the ~~text~~ **summary** for further discussion on this point.) Note that the rate of scaling of EOT is quite slow from 2005 through ~~2007~~ **2009** to keep the gate leakage current within the specified limits while utilizing silicon oxy-nitride for the gate dielectric. However, there is a sharp EOT decrease in ~~2008~~ **2010**, when we assume that high-κ gate dielectric will be implemented. Red coloring for ~~2008~~ **2010** and beyond reflects the projected implementation of high-κ gate dielectric. The color is red because it is felt that the solutions for EOT below 1.0 nm are not understood. Measurement of EOT is complicated, and is usually done via sophisticated MOS capacitor-voltage (CV) measurements on MOS capacitors or via optical measurements.*

IS *[3] Accounts for gate electrode depletion and inversion-layer effects, including quantum effects, both of which are calculated by MASTAR. For polysilicon gate electrodes, the portion of the electrical thickness adjustment due to gate electrode depletion is dependent on the polysilicon doping. For ~~2008~~ **2010** and beyond, there is a projected inability to adequately dope polysilicon gate electrodes to meet the gate depletion thickness adjustment requirements, and hence it is assumed that metal-gate electrodes, which reduce the gate depletion effect to zero, will be introduced. The abrupt reduction in this parameter ~~for 2008~~ **in 2010** reflects the zero depletion. For ~~2008~~ **2010** and beyond, the difference between the parameter value for planar bulk versus the 4 nm value for DG and UTB FD reflects the light channel doping in the latter types of MOSFET and the heavy channel doping in planar bulk. The red color reflects the current lack of a well-known solution for metal gate electrodes with well-controlled work functions. For planar bulk CMOS, the work function needs to be near the silicon conduction band for NMOS and near the silicon valence band for PMOS to properly set the MOSFET threshold voltage, as with polysilicon gates. For UTB FD and DG MOSFETs, the channel is very thin and lightly doped, and the work function of the metal gates needs to be within a few hundred millivolts of the silicon midgap (i.e., "near silicon midgap" work function) to properly set the MOSFET's threshold voltage.*

[4] EOT_{elec} is the sum of EOT and electrical thickness adjustment (see Notes [2] and [3] above). For MOSFETs in inversion, ideal gate capacitance per unit area (see Note [13]) is εox / (EOT_{elec}), where εox is the dielectric constant of thermal silicon dioxide. The equivalent electrical oxide thickness in inversion is used in calculations of the CV/I intrinsic delay (see Note [16]). Red/yellow coloring follows that of EOT and Electrical Thickness Adjustment.

[5] $J_{g,limit}$ is the maximum allowed gate leakage current density at 25°C, and it is measured with the gate biased to V_{dd} and the source, drain, and substrate all set to ground. $J_{g,limit}$ is related to $I_{sd,leak}$, the nominal subthreshold leakage current per micron device width (see Note [8] below). Specifically, $J_{g,limit}$= [Initial Factor] x [$I_{sd,leak}$ / (physical gate length)] × [Hi T Factor] / [Circuit Factor]. Hi T Factor is set to 10, and it accounts for the high operating temperature (100°C) expected for high-performance logic, by adjusting for both the rapid increase in $I_{sd,leak}$ with temperature and the insensitivity of gate leakage current (since it is due to direct tunneling) to temperature. Circuit Factor is set to 1, and it accounts for the differences between the subthreshold leakage current and the gate leakage current in logic gates compared to single isolated transistors as specified by the $J_{g,limit}$ and $I_{sd,leak}$ parameters in this table. (The reason for these differences is the different bias conditions on the various transistors in logic gates compared to the bias conditions used to define $I_{sd,leak}$ (see Note 8) and $J_{g,limit}$ for the NMOS transistor in this table). The Initial Factor is set to 0.1, and accounts for the fact that the transistor specified in this table is the low threshold voltage transistor with high subthreshold leakage, but that the predominant transistors in typical circuits have significantly lower subthreshold leakage current. The values of Hi T Factor, Circuit Factor, and Initial Factor used here are rough estimates. The yellow and red coloring follows that of EOT (see Note [2] above).

[6] V_{dd} is the nominal power supply voltage. It has been chosen to maintain sufficient voltage over-drive [V_{dd} – saturation threshold voltage (see Note 7)] in order to meet the required saturation current drive values while still maintaining reasonable vertical gate dielectric electric field strengths. Target power supply voltage values for actual ICs may vary ± 10% (or more) from the values in this table, depending on the particular circuit design application or technology optimization.

IS

*[7] $V_{t,sat}$ is the saturation threshold voltage for a nominal gate length transistor with drain bias set equal to V_{dd}, as calculated by MASTAR. The threshold voltage values and the corresponding subthreshold leakage current values (see Note [8]) have been chosen to maintain sufficient voltage over-drive (V_{dd} – saturation threshold voltage) in order to meet the required saturation current drive values (see Note [9]). For planar bulk, the yellow color is associated with the very high substrate doping approaching or exceeding 5E18 cm^{-3} (from MASTAR) required to set the threshold voltage to the desired level and ~~to keep~~ **the difficulty in keeping** short channel effects under control. For UTB FD devices, the color is ~~yellow in 2008~~ **red in 2010** because of the challenges of controlling the very thin silicon body thickness (T_{si}) required to control $V_{t,sat}$ and short channel effects. ~~The color becomes red in 2009 when the required body thickness becomes less than ~7 nm.~~ For DG devices, the color is red right from the beginning because there are very many issues that are not understood here; in particular, defining and controlling the fin width, which is typically ~0.6 L_g, is a major challenge. The required silicon body thickness for UTB FD and the fin width for DG come from MASTAR.*

[8] $I_{sd,leak}$: subthreshold leakage current is defined as the NMOSFET source current per micron of device width, at 25°C, with the drain bias set equal to V_{dd} and with the gate, source, and substrate biases set to zero volts. Total NMOS off-state leakage current (I_{off}) is the NMOSFET drain current per micron of device width at 25°C, and is the sum of the NMOS subthreshold, gate, and junction leakage current (which includes band-to-band tunneling and gate induced drain leakage [GIDL]) components. The subthreshold leakage current is assumed to be larger than the junction leakage current component at either 25°C or high-temperature conditions, but see Note [5] for the relation between Isd,leak and gate leakage current density. The yellow and red coloring follows that of $V_{t,sat}$ (see Note 7 above) because $V_{t,sat}$ is a critical determinant of $I_{sd,leak}$. The above subthreshold, gate, and junction leakage current scaling scenario also applies to PMOS devices.

[9] $I_{d,sat}$: saturation drive current is defined as the NMOSFET drain current per micron device width with the gate bias and the drain bias set equal to V_{dd} and the source and substrate biases set to zero. The saturation drive current values have been chosen to continue the historical 17% per year device performance scaling (see Note 16 below). PMOS saturation drive current value is assumed to be (40–50)% of the NMOS saturation drive current value. Yellow and red coloring follows that of four items: the parasitic source/drain series resistance, R_{sd} (see Note 12 below), the equivalent electrical oxide thickness in inversion (see Note 4), the required mobility/transconductance improvement factor (see Note 10), and the ballistic enhancement factor (see Note [11]).

*[10] Mobility Enhancement Factor for $I_{d,sat}$: captures the improvement in the saturation drive current due to mobility enhancement. This factor is defined as [enhanced $I_{d,sat}$]/$I_{d,ref}$ = $I_{d,ratio}$, where [enhanced $I_{d,sat}$] is the actual saturation drive current including the impact of enhanced mobility and $I_{d,ref}$ is the saturation drive current in the absence of mobility enhancement. MASTAR calculates $I_{d,ratio}$ as a function of the mobility enhancement factor, μ_{ratio} = [enhanced mobility]/[reference mobility], where [enhanced mobility] is the actual mobility including the enhancement, and [reference mobility] is the mobility in the absence of enhancement. Generally, $I_{d,ratio}$ is significantly less than μ_{ratio} due to short channel effects and velocity saturation. Following the literature, the value of μ_{ratio} is limited to a maximum of 1.8[1]. Mobility enhancement was implemented in product in 2004[2] to meet the required saturation drive current, and hence the coloring for extended planar bulk is initially white. However, there are numerous approaches in the literature for mobility enhancement (including global strain using thin silicon epitaxial layers on SiGe epitaxial layers[3], different process induced strain approaches such as strained thin overlayers of SiN and selective epitaxial SiGe in the S/D, hybrid orientations, etc.**Error! Bookmark not defined.**[,4,5]), and as we continue to scale MOSFETs, it is unclear what the optimal approach(es) will be and how to integrate them into the process flow. Consequently, the row is colored yellow in 2009, when L_g=20 nm and the scaling becomes difficult enough that the doping approaches 5E18 cm^{-3} according to the MASTAR modeling. For both FD SOI and DG, the row starts out yellow (in 2008 for FD and 2011 for DG) because we don't at this point understand manufacturable solutions to mobility enhancement for these device types.*

[11] Effective Ballistic Enhancement Factor is a multiplying factor for $I_{d,sat}$, reflecting quasi-ballistic enhanced transport in highly scaled, ultra-thin body MOSFETs, both UTB FD SOI and DG MOSFETs. Planar bulk CMOS does not have ballistic enhancement because of the high doping in these devices. Values for this factor greater than 1 reflect quasi-ballistic enhancement. The value of this parameter is driven by the required saturation drive current to meet performance requirements. The initial yellow coloring reflects that quasi-ballistic enhancement is expected (and predicted by MASTAR) for undoped, very scaled UTB FD and DG MOSFETs. The later red coloring reflects the lack of known manufacturable enhanced transport solutions for transistors with gate length approaching 10 nm.

[12] R_{sd} is the maximum allowable parasitic series source plus drain resistance for a MOSFET of one micron width. The values are scaled to allow the required saturation current drive values (see Note [9]) to be met. Yellow and red coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling.

[13] $C_{g,ideal}$ is the ideal gate capacitance per micron device width, in inversion. $C_{g,ideal}$ =[εox /(EOT_{elec})] × L_g, where εox is the dielectric constant of thermal silicon dioxide, EOTelec is the equivalent electrical oxide thickness in inversion (see Note [4]), and L_g is the physical gate length (see Note [1]). The red and yellow coloring follows that of EOTelec (see Note [4]).

[14] $C_{g,total}$ is the total gate capacitance per micron device width in inversion. This is the sum of $C_{g,ideal}$ and the parasitic gate overlap/fringing capacitance per micron device width [including the Miller effect]. Red and yellow color here follows that of $C_{g,ideal}$.
[15] τ is the intrinsic transistor delay for NMOS devices at 25°C. $\tau = (C_{g,total} \times V_{dd}) / I_{d,sat}$. τ for PMOSFETs is assumed to scale similarly, but with PMOS $I_{d,sat} \sim (0.4–0.5) \times$ (NMOS $I_{d,sat}$). τ is a good metric for the intrinsic switching delay of the device, while $1/\tau$ is a good metric for the intrinsic switching speed of the device. Red and yellow coloring follows that of both saturation drive current (see Note [9]) and $C_{g,total}$ (see Note [14]).
[16] $1/\tau$ is the NMOS intrinsic switching speed. Maintenance of the historical 17% per year device performance improvement scaling trend is the key scaling goal for high-performance logic. Red and yellow coloring follows that of τ.

Table 41a Low Standby Power Technology Requirements—Near-term

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year in Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
L_g: Physical gate length for LSTP [1]									
Extended Planar Bulk and DG (nm)	65	53	45	37	32	28	25	22	20
UTB FD (nm)								22	20
EOT: Equivalent Oxide Thickness [2]									
Extended planar bulk (Å)	21	20	19	16	15	14	14	13	12
UTB FD (Å)								12	11
DG (Å)								13	12
Gate Poly Depletion and Inversion-Layer Thickness [3]									
Extended planar bulk (Å)	6.3	6.3	6.3	3.3	3.2	3.1	3.2	3.1	3.1
UTB FD (Å)								4	4
DG (Å)								4	4
EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]									
Extended planar bulk (Å)	27.3	26.3	25.3	19.3	18.2	17.1	17.2	16.1	15.1
UTB FD (Å)								16	15
DG (Å)								17	16
$J_{g,limit}$: Maximum gate leakage current density [5]									
Extended Planar Bulk (A/cm^2)	1.5E-02	1.9E-02	2.2E-02	2.7E-02	3.1E-02	3.6E-02	4.8E-02	7.3E-02	1.1E-01
UTB FD (A/cm^2)								4.5E-02	5.0E-02
DG (A/cm^2)								4.5E-02	5.0E-02
V_{dd}: Power Supply Voltage (V) [6]	1.2	1.2	1.2	1.1	1.1	1.1	1	1	1
$V_{t,sat}$: Saturation Threshold Voltage [7]									
Extended Planar Bulk (mV)	482	515	524	501	501	502	502	491	483
UTB FD (mV)								483	486
DG (mV)								441	435
$I_{sd,leak}$: Source/Drain Subthreshold Off-State Leakage Current [8]									
Extended Planar Bulk (μA/μm)	1.0E-05	1.0E-05	1.0E-05	1.0E-05	1.0E-05	1.0E-05	1.2E-05	1.6E-05	2.1E-05
UTB FD (μA/μm)								1.0E-05	1.0E-05
DG (μA/μm)								1.0E-05	1.0E-05
$I_{d,sat}$: effective NMOS Drive Current [9]									
Extended Planar Bulk (μA/μm)	497	500	519	573	612	666	580	625	684
UTB FD (μA/μm)								678	719
DG (μA/μm)								673	747

Table 41a Low Standby Power Technology Requirements—Near-term (continued)

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year in Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Mobility Enhancement Factor for $I_{d,sat}$ [10]									
Extended Planar Bulk	**1.11**	**1.11**	**1.1**	**1.1**	**1.11**	**1.15**	**1.17**	**1.16**	**1.16**
UTB FD								**1.04**	**1.05**
DG								**1**	**1.04**
Effective Ballistic Enhancement Factor [11]									
Extended Planar Bulk	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
UTB FD								**1**	**1**
DG								**1**	**1**
R_{sd}: Effective Parasitic series source/drain resistance [12]									
Extended Planar Bulk (Ω-µm)	**180**	**180**	**180**	**180**	**180**	**180**	**170**	**170**	**160**
UTB FD (Ω-µm)								**180**	**180**
DG (Ω-µm)								**180**	**180**
$C_{g,ideal}$: Ideal NMOS Device Gate Capacitance [13]									
Extended Planar Bulk (F/µm)	**8.21E-16**	**6.96E-16**	**6.14E-16**	**6.62E-16**	**6.06E-16**	**5.64E-16**	**5.01E-16**	**4.70E-16**	**4.58E-16**
UTB FD (F/µm)								**4.74E-16**	**4.60E-16**
DG (F/µm)								**4.46E-16**	**4.31E-16**
$C_{g,total}$: Total gate capacitance for calculation of CV/I [14]									
Extended Planar Bulk (F/µm)	**1.06E-15**	**9.36E-16**	**8.54E-16**	**9.02E-16**	**8.46E-16**	**8.04E-16**	**6.81E-16**	**6.40E-16**	**6.18E-16**
UTB FD (F/µm)								**6.94E-16**	**6.50E-16**
DG (F/µm)								**6.86E-16**	**6.71E-16**
$\tau = CV/I$: NMOSFET intrinsic delay (ps) [15]	**2.56**	**2.25**	**1.97**	**1.73**	**1.52**	**1.33**	**1.17**	**1.02**	**0.90**
$1/\tau$: NMOSFET intrinsic switching speed (GHz) [16]	**391**	**444**	**508**	**578**	**658**	**752**	**855**	**980**	**1111**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

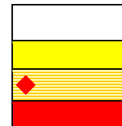


Table 41b Low Standby Power Technology Requirements—Long-term

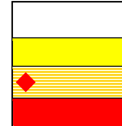
Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year in Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
L_g: Physical gate length for LSTP [1]							
Extended Planar Bulk and DG (nm)	18	16	14	13	12	11	10
UTB FD (nm)	18	17	16	15	14	13	12
EOT: Equivalent Oxide Thickness [2]							
Extended planar bulk (Å)							
UTB FD (Å)	10	9	8	8	8	8	8
DG (Å)	11	11	11	10	10	9	9
Gate Poly Depletion and Inversion-Layer Thickness [3]							
Extended planar bulk (Å)							
UTB FD (Å)	4	4	4	4	4	4	4
DG (Å)	4	4	4	4	4	4	4
EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]							
Extended planar bulk (Å)							
UTB FD (Å)	14	13	12	12	12	12	12
DG (Å)	15	15	15	14	14	13	13
$J_{g,limit}$: Maximum gate leakage current density [5]							
Extended Planar Bulk (A/cm^2)							
UTB FD (A/cm^2)	6.1E-02	6.5E-02	7.5E-02	8.0E-02	8.6E-02	1.0E-01	1.3E-01
DG (A/cm^2)	5.6E-02	6.3E-02	7.1E-02	7.7E-02	8.3E-02	9.1E-02	1.0E-01
V_{dd}: Power Supply Voltage (V) [6]	1	1	1	1	1	1	1
$V_{t,sat}$: Saturation Threshold Voltage [7]							
Extended Planar Bulk (mV)							
UTB FD (mV)	486	489	487	487	492	488	486
DG (mV)	432	434	436	438	440	443	443
$I_{sd,leak}$: Source/Drain Subthreshold Off-State Leakage Current [8]							
Extended Planar Bulk (µA/µm)							
UTB FD (µA/µm)	1.1E-05	1.1E-05	1.2E-05	1.2E-05	1.2E-05	1.30E-05	1.60E-05
DG (µA/µm)	1.0E-05	1.0E-05	1.0E-05	1.0E-05	1.0E-05	1.0E-05	1.0E-05
$I_{d,sat}$: effective NMOS Drive Current [9]							
Extended Planar Bulk (µA/µm)							
UTB FD (µA/µm)	773	882	1016	1108	1188	1289	1392
DG (µA/µm)	825	863	908	1011	1090	1192	1283
Mobility Enhancement Factor for $I_{d,sat}$ [10]							
Extended Planar Bulk							
UTB FD	1.06	1.06	1.05	1.05	1.05	1.04	1.04
DG	1.06	1.06	1.05	1.05	1.05	1.05	1.04
Effective Ballistic Enhancement Factor [11]							
Extended Planar Bulk							
UTB FD	1	1.08	1.15	1.24	1.32	1.4	1.48
DG	1	1	1.1	1.16	1.24	1.28	1.36

Table 41b Low Standby Power Technology Requirements—Long-term (continued)

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year in Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
R_{sd}: *Effective Parasitic series source/drain resistance [12]*							
Extended Planar Bulk (Ω-µm)							
UTB FD (Ω-µm)	175	170	160	155	150	145	140
DG (Ω-µm)	180	175	170	165	160	155	150
$C_{g,ideal}$: *Ideal NMOS Device Gate Capacitance [13]*							
Extended Planar Bulk (F/µm)							
UTB FD (F/µm)	4.44E-16	4.51E-16	4.60E-16	4.31E-16	4.02E-16	3.74E-16	3.45E-16
DG (F/µm)	4.14E-16	3.68E-16	3.22E-16	3.20E-16	2.96E-16	2.92E-16	2.65E-16
$C_{g,total}$: *Total gate capacitance for calculation of CV/I [14]*							
Extended Planar Bulk (F/µm)							
UTB FD (F/µm)	6.14E-16	6.11E-16	6.20E-16	5.91E-16	5.63E-16	5.34E-16	5.05E-16
DG (F/µm)	6.54E-16	5.98E-16	5.52E-16	5.40E-16	5.16E-16	4.92E-16	4.65E-16
$\tau = CV/I$: *NMOSFET intrinsic delay (ps) [15]*	0.79	0.69	0.61	0.53	0.47	0.41	0.36
$1/\tau$: *NMOSFET intrinsic switching speed (GHz) [16]*	1266	1449	1639	1887	2128	2439	2778



Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 41c Low Operating Power Technology Requirements—Near-term UPDATED

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion)..

	Year in Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
	MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
	L_g: Physical gate length for LOP (nm) [1]	**45**	**37**	**32**	**28**	**25**	**22**	**20**	**18**	**16**
	EOT: Equivalent Oxide Thickness [2]									
IS	Extended planar bulk (Å)	14	13	12	11	10	9	9	9	
	UTB FD (Å)							9	9	8
	DG (Å)							9	9	8
	Gate Poly Depletion and Inversion-Layer Thickness [3]									
IS	Extended planar bulk (Å)	6.5	6.5	6.4	6.6	6.7	3.2	3.3	3.2	
	UTB FD (Å)							4	4	4
	DG (Å)							4	4	4
	EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]									
IS	Extended planar bulk (Å)	20.5	19.5	18.4	17.6	16.7	12.2	12.3	12.2	
	UTB FD (Å)							13	13	12
	DG (Å)							13	13	12
	$J_{g,limit}$: Maximum gate leakage current density [5]									
IS	Extended Planar Bulk (A/cm^2)	3.30E+01	4.10E+01	7.80E+01	1.54E+02	1.61E+02	1.10E+02	4.50E+02	6.90E+02	
	UTB FD (A/cm^2)							2.00E+02	2.80E+02	3.10E+02
	DG (A/cm^2)							1.30E+02	1.90E+02	2.20E+02
	V_{dd}: Power Supply Voltage (V) [6]	0.9	0.9	0.8	0.8	0.8	0.7	0.7	0.7	0.6
	$V_{t,sat}$: Saturation Threshold Voltage [7]									
IS	Extended Planar Bulk (mV)	288	303	285	271	276	226	233	231	
	UTB FD (mV)							273	268	272
	DG (mV)							261	255	257
	$I_{sd,leak}$: Source/Drain Subthreshold Off-State Leakage Current [8]									
IS	Extended Planar Bulk (μA/μm)	3.00E-03	3.00E-03	5.00E-03	8.6E-03	8.0E-03	5.00E-03	1.80E-02	2.50E-02	
	UTB FD (μA/μm)							8.00E-03	1.00E-02	1.00E-02
	DG (μA/μm)							5.00E-03	7.00E-03	7.00E-03
	$I_{d,sat}$: effective NMOS Drive Current [9]									
IS	Extended Planar Bulk (μA/μm)	589	607	573	612	652	749	749	774	
	UTB FD (μA/μm)							740	765	718
	DG (μA/μm)							783	822	789
	Mobility Enhancement Factor for $I_{d,sat}$ [10]									
IS	Extended Planar Bulk	1.12	1.11	1.11	1.13	1.13	1.11	1.11	1.11	
	UTB FD							1.07	1.06	1.06
	DG							1.06	1.06	1.06
	Effective Ballistic Enhancement Factor [11]									

Year in Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
Extended Planar Bulk	1	1	1	1	1	1	1	1	
UTB FD							1	1	1.26
DG							1.12	1.14	1.37

		2005	2006	2007	2008	2009	2010	2011	2012	2013
	R_{sd}: Effective Parasitic series source/drain resistance [12]									
	Planar Bulk (Ω-µm)	180	180	180	180	180	180	170	165	
	UTB FD (Ω-µm)							145	140	135
	DG (Ω-µm)							160	155	150
	$C_{g,ideal}$: Ideal NMOS Device Gate Capacitance [13]									
IS	Extended Planar Bulk (F/µm)	7.57E-16	6.55E-16	6.00E-16	5.51E-16	5.17E-16	6.20E-16	5.63E-16	5.09E-16	
	UTB FD (F/µm)							5.31E-16	4.78E-16	4.25E-16
	DG (F/µm)							5.31E-16	4.78E-16	4.60E-16
	$C_{g,total}$: Total gate capacitance for calculation of CV/I [14]									
IS	Extended Planar Bulk (F/µm)	9.97E-16	8.95E-16	8.40E-16	7.91E-16	7.37E-16	8.40E-16	7.43E-16	6.79E-16	
	UTB FD (F/µm)							7.31E-16	6.68E-16	6.40E-16
	DG (F/µm)							7.71E-16	7.18E-16	7.00E-16
IS	$\tau = CV/I$: NMOSFET intrinsic delay (ps) [15]	1.52	1.33	1.17	1.03	0.9	0.79	0.69	0.61	0.53
IS	$1/\tau$: NMOSFET intrinsic switching speed (GHz) [16]	658	752	855	971	1111	1266	1449	1639	1887

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

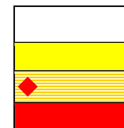


Table 41d Low Operating Power Technology Requirements—Long-term

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

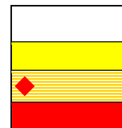
Year in Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
L_g: Physical gate length for LOP (nm) [1]	**14**	**13**	**11**	**10**	**9**	**8**	**7**
EOT: Equivalent Oxide Thickness [2]							
Extended planar bulk (Å)							
UTB FD (Å)	**8**	**8**	**7**				
DG (Å)	**8**	**8**	**7**	**7**	**7**	**7**	**7**
Gate Poly Depletion and Inversion-Layer Thickness [3]							
Extended planar bulk (Å)							
UTB FD (Å)	**4**	**4**	**4**				
DG (Å)	**4**	**4**	**4**	**4**	**4**	**4**	**4**
EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]							
Extended planar bulk (Å)							
UTB FD (Å)	**12**	**12**	**11**				
DG (Å)	**12**	**12**	**11**	**11**	**11**	**11**	**11**
$J_{g,limit}$: Maximum gate leakage current density [5]							
Extended Planar Bulk (A/cm^2)							
UTB FD (A/cm^2)	**3.6E+02**	**3.8E+02**	**1.1E+03**				
DG (A/cm^2)	**3.6E+02**	**3.8E+02**	**9.1E+02**	**1.0E+03**	**1.1E+03**	**1.3E+03**	**1.4E+03**
V_{dd}: Power Supply Voltage (V) [6]	**0.6**	**0.6**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
$V_{t,sat}$: Saturation Threshold Voltage [7]							
Extended Planar Bulk (mV)							
UTB FD (mV)	**275**	**277**	**254**				
DG (mV)	**250**	**251**	**238**	**239**	**242**	**243**	**246**
$I_{sd,leak}$: Source/Drain Subthreshold Off-State Leakage Current [8]							
Extended Planar Bulk (μA/μm)							
UTB FD (μA/μm)	**1.0E-02**	**1.0E-02**	**2.5E-02**				
DG (μA/μm)	**1.0E-02**	**1.0E-02**	**2.0E-02**	**2.0E-02**	**2.0E-02**	**2.0E-02**	**2.0E-02**
$I_{d,sat}$: effective NMOS Drive Current [9]							
Extended Planar Bulk (μA/μm)							
UTB FD (μA/μm)	**738**	**796**	**695**				
DG (μA/μm)	**829**	**892**	**760**	**820**	**873**	**929**	**931**
Mobility Enhancement Factor for $I_{d,sat}$ [10]							
Extended Planar Bulk							
UTB FD	**1.05**	**1.05**	**1.04**				
DG	**1.06**	**1.06**	**1.06**	**1.06**	**1.05**	**1.05**	**1.05**
Effective Ballistic Enhancement Factor [11]							
Extended Planar Bulk							
UTB FD	**1.28**	**1.37**	**1.39**				
DG	**1.38**	**1.47**	**1.59**	**1.7**	**1.8**	**1.9**	**1.92**

Table 41d Low Operating Power Technology Requirements—Long-term (continued)

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year in Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
R_{sd}: Effective Parasitic series source/drain resistance [12]							
Planar Bulk (Ω-µm)							
UTB FD (Ω-µm)	130	125	90				
DG (Ω-µm)	145	140	130	125	120	115	115
$C_{g,ideal}$: Ideal NMOS Device Gate Capacitance [13]							
Extended Planar Bulk (F/µm)							
UTB FD (F/µm)	4.02E-16	3.74E-16	3.45E-16				
DG (F/µm)	4.02E-16	3.74E-16	3.45E-16	3.14E-16	2.82E-16	2.51E-16	2.20E-16
$C_{g,total}$: Total gate capacitance for calculation of CV/I [14]							
Extended Planar Bulk (F/µm)							
UTB FD (F/µm)	5.83E-16	5.44E-16	5.05E-16				
DG (F/µm)	6.43E-16	6.14E-16	5.55E-16	5.24E-16	4.82E-16	4.41E-16	4.00E-16
$\tau = CV/I$: NMOSFET intrinsic delay (ps) [15]	0.47	0.41	0.36	0.32	0.28	0.24	0.21
$1/\tau$: NMOSFET intrinsic switching speed (GHz) [16]	2128	2439	2778	3125	3571	4167	4762

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 41a through 41d (LSTP and LOP):

As described in the text, MASTAR, a detailed analytical MOSFET modeling software package, has been utilized to generate the parameter values in these tables. The MASTAR modeling package and user's manual are in the backup material on the ITRS website, as well as the detailed MASTAR simulations that underlay these tables. Also note that the parameters in this table are for an NMOSFET with nominal gate length at an operating temperature of 25°C. Furthermore, although there are multiple MOSFETs in a typical logic chip, with differing threshold voltages, Ion, Ioff, and oxide thickness, for LSTP logic the transistor specified in this table is the transistor with the highest threshold voltage, lowest Ion and Ioff, highest oxide thickness, and slowest CV/I. The majority of the transistors on the chip are of this type, in order to keep the leakage and static power dissipation within tolerable limits. This transistor is specified here because it drives the technology. In contrast, for LOP logic, the transistor specified in this table is the "standard" transistor, with intermediate threshold voltage, I_{on}, and I_{off}. The majority of the transistors on the chip are of this type, because the performance requirements are critical, and standby power dissipation is less critical than for LSTP. Dynamic power dissipation is critical here, and V_{dd} is rapidly scaled to keep this within tolerable limits. This transistor is specified here because it drives the technology.

As explained in the text, multiple parallel options for the transistor type are included in the tables, including planar bulk CMOS extended to its practical scaling limits, ultra-thin body fully-depleted (UTB FD) SOI CMOS, also extended to its practical scaling limits, and double-gate (DG) CMOS (e.g., FinFETs). Note that, for LOP, the limit for planar bulk CMOS is through 2012, and for UTB FD is through 2016. UTB FD and DG start in 2011, with overlap of the three options from 2011 through 2012. In contrast, for LSTP, the limit for planar bulk CMOS is through 2013, and UTB FD continues through 2020. UTB FD and DG start in 2012, with overlap of the three options from 2012 through 2013.

For each transistor option, the scaling of the numbers in the tables reflects a particular scaling scenario in which we have attempted to optimally scale to meet the key goals while keeping the performance, short channel effects, and other key characteristics under control. For LSTP, the key goal is ultra-low leakage current, while for LOP the goal is relatively high speed and low dynamic power dissipation, along with low leakage current (but not so low as for LSTP). However, there are numerous parameters (such as EOT, V_{dd}, $I_{sd,leak}$, etc.) that can be varied, and different scaling scenarios are possible by making different choices on the scaling of these parameters. The scenarios in this table were selected to be as representative of the industry as possible. In particular, in these tables, high-κ gate dielectric and metal gate electrode are assumed to be available in 2008. See the figures and discussion in the text for why high-κ gate dielectric is required in 2008.

[1] L_g is the physical gate length: the final, as-etched length of the bottom of the gate electrode. The values here lag behind the gate length values for high- performance logic by two years (LOP) or four years (LSTP) in order to meet the stringent leakage current requirements. For UTB FD devices, late in the ITRS, L_g scaling lags slightly behind that for DG MOSFETs because of the difficulty in scaling UTB FD MOSFETs for such short devices. The gate dimensional control requirement is set by the Lithography and FEP Etch ITWGs, and is assumed to have a three-sigma value of $\pm$ 12% $\times$ L_g. It is expected that meeting this requirement will become increasingly difficult with scaling (refer to the Lithography chapter and the FEP Chapter). Gate length variation is assumed to be a primary factor responsible for driving device parameter variation.

IS

*[2] For a gate dielectric of thickness T_d and relative dielectric constant κ, EOT is defined by: EOT = T_d / (κ/3.9), where 3.9 is the relative dielectric constant of thermal silicon dioxide. For a MOSFET with the gate dielectric of thickness T_d, the ideal gate capacitance per unit area is the same as that of a similar MOSFET, but with a gate dielectric made up of thermal silicon dioxide with a thickness of EOT. Red coloring ~~from 2008-2010 on~~ reflects the projected implementation of high-κ gate dielectric, due to the inability of silicon oxy-nitride gate dielectric to meet the gate leakage current density limits for those years (**for LOP logic, this is delayed until 2010 from the 2008 projected deployment date in the 2005 ITRS, while the 2008 deployment date is retained for LSTP logic. See the summary for further discussion on this point**). The red color reflects the current lack of a well-known solution for high-κ gate dielectric with metal gate electrode~~, which is also projected for 2008-2010~~ (see Note 3). Measurement of EOT is complicated, and is usually done via sophisticated MOS capacitor-voltage (CV) measurements on MOS capacitors or via optical measurements.*

IS

*[3] Accounts for gate electrode depletion and inversion-layer effects, including quantum effects, both of which are calculated by MASTAR. For polysilicon gate electrodes, the portion of the electrical thickness adjustment due to gate electrode depletion is dependent on the polysilicon doping. For ~~2008~~ **2010** and beyond, it is assumed that metal-gate electrodes, which reduce the gate depletion effect to zero, will be introduced. **(This is delayed from the 2008 projected deployment date in the 2005 ITRS; see the text for further discussion on this point).** The abrupt reduction in this parameter for ~~2008~~ **2010** reflects the zero depletion. For ~~2008~~ **2010** and beyond, the difference between the parameter value for planar bulk versus the 4 nm value for DG and UTB FD reflects the light channel doping in the latter types of MOSFET and the heavy channel doping in planar bulk. The red color for metal gate electrodes reflects the current lack of a well-known solution for metal gate electrodes with well-controlled and tunable work functions. For planar bulk CMOS, the work function needs to be near the silicon conduction band for NMOS and near the silicon valence band for PMOS to properly set the MOSFET threshold voltage, as with polysilicon gates. For UTB FD and DG MOSFETs, the channel is very thin and lightly doped, and the work function of the metal gates needs to be within a few hundred millivolts of the silicon midgap (i.e., "near silicon midgap" work function) to properly set the MOSFET's threshold voltage.*

[4] EOT_{elec} is the sum of EOT and electrical thickness adjustment (see Notes [2] and [3] above). For MOSFETs in inversion, ideal gate capacitance per unit area (see Note [14]) is ε_{ox} / (EOT_{elec}), where ε_{ox} is the dielectric constant of thermal silicon dioxide. The equivalent electrical oxide thickness in inversion is used in calculations of the CV/I intrinsic delay (see Note [16]). Red/yellow coloring follows that of EOT and Electrical Thickness Adjustment.

[5] $J_{g,limit}$ is the maximum allowed gate leakage current density at 25°C, and it is measured with the gate biased to V_{dd} and the source, drain, and substrate all set to ground. $J_{g,limit}$ is related to $I_{sd,leak}$, the nominal subthreshold leakage current per micron device width (see Note [8] below). Specifically, $J_{g,limit}$= [$I_{sd,leak}$ / (physical gate length)] $\times$ [Hi T Factor] / [Circuit Factor]. For LOP, Hi T Factor is set to 5, and it accounts for the high operating temperature (well over room temperature, but not as high as the 100°C for high-performance logic, where Hi T Factor = 10). Hi T Factor accounts for both the rapid increase in $I_{sd,leak}$ with temperature and the insensitivity of gate leakage current (since it is due to direct tunneling) to temperature. For LSTP, where the operating temperature is expected to be room temperature, Hi T Factor = 1. The Circuit Factor is set to 1, and it accounts for the differences between the subthreshold leakage current and the gate leakage current in logic gates compared to single isolated transistors as specified by the $J_{g,limit}$ and $I_{sd,leak}$ parameters in this table. (The reason for these differences is the different bias conditions on the various transistors in logic gates compared to the bias conditions used to define $I_{sd,leak}$ (see Note 8) and $J_{g,limit}$ for the NMOS transistor in this table). The values of Hi T Factor and Circuit Factor used here are rough estimates. The yellow and red coloring follows that of EOT (see Note [2] above).

[6] V_{dd} is the nominal power supply voltage. It has been chosen to maintain sufficient voltage over-drive [V_{dd} – saturation threshold voltage (see Note 7)] in order to meet the required saturation current drive values while still maintaining reasonable vertical gate dielectric electric field strengths. Target power supply voltage values for actual ICs may vary ± 10% (or more) from the values in this table, depending on the particular circuit design application or technology optimization. Note that V_{dd} is relatively high and scales slowly for LSTP, because the saturation threshold voltage is high here to keep the subthreshold leakage current very low. On the other hand, for LOP V_{dd} scales down rapidly in order to keep the dynamic power dissipation low.

[7] $V_{t,sat}$ is the saturation threshold voltage for a nominal gate length transistor with drain bias set equal to V_{dd}, as calculated by MASTAR. The threshold voltage values and the corresponding subthreshold leakage current values (see Note [8]) have been chosen to maintain sufficient voltage over-drive (V_{dd} – saturation threshold voltage) in order to meet the required saturation current drive values (see Note [9]). For planar bulk, the yellow color is associated with the very high substrate doping approaching or exceeding 5E18 cm^{-3} (from MASTAR) required to set the threshold voltage to the desired level and to keep short channel effects under control. For UTB FD devices, the color is red from the beginning because of the challenges of controlling the very thin silicon body thickness (right from the beginning, ~7 nm for LOP and < 7 nm for LSTP) required to control $V_{t,sat}$ and short channel effects. For DG devices, the color is red right from the beginning because there are numerous issues that are not understood here; in particular, defining and controlling the fin width, which is typically ~0.6 L_g, is a major challenge.

[8] $I_{sd,leak}$: subthreshold leakage current is defined as the NMOSFET source current per micron of device width, at 25°C, with the drain bias set equal to V_{dd} and with the gate, source, and substrate biases set to zero volts. Total NMOS off-state leakage current (I_{off}) is the NMOSFET drain current per micron of device width at 25°C, and is the sum of the NMOS subthreshold, gate, and junction leakage current (which includes band-to-band tunneling and gate induced drain leakage [GIDL]) components. The subthreshold leakage current is assumed to be larger than the junction leakage current component at either 25°C or high-temperature conditions, but see Note [5] for the relation between $I_{sd,leak}$ and gate leakage current density. The yellow and red coloring follows that of the $V_{t,sat}$ (see Note 7 above) because $V_{t,sat}$ is a critical determinant of $I_{sd,leak}$. The above subthreshold, gate, and junction leakage current scaling scenario also applies to PMOS devices.

[9] $I_{d,sat}$: saturation drive current is defined as the NMOSFET drain current per micron device width with the gate bias and the drain bias set equal to V_{dd} and the source and substrate biases set to zero. The saturation drive current values have been chosen to continue the historical approximate 17% per year device performance scaling (see Note 16 below). PMOS saturation drive current value is assumed to be (40–50)% of the NMOS saturation drive current value. Yellow/red coloring follows that of four items: the parasitic source/drain series resistance, R_{sd} (see Note 12 below), the equivalent electrical oxide thickness in inversion (see Note 4), the mobility enhancement factor (see Note 10), and the ballistic enhancement factor (see Note 11).

[10] Mobility Enhancement Factor for $I_{d,sat}$: captures the improvement in the saturation drive current due to mobility enhancement. This factor is defined as [enhanced $I_{d,sat}$]/$I_{d,ref}$ = $I_{d,ratio}$, where [enhanced $I_{d,sat}$] is the actual saturation drive current including the impact of enhanced mobility and $I_{d,ref}$ is the saturation drive current in the absence of mobility enhancement. MASTAR calculates $I_{d,ratio}$ as a function of the mobility enhancement factor, μ_{ratio} = [enhanced mobility]/[reference mobility], where [enhanced mobility] is the actual mobility including the enhancement, and [reference mobility] is the mobility in the absence of enhancement. Generally, $I_{d,ratio}$ is significantly less than μ_{ratio} due to short channel effects and velocity saturation. Following the literature, the value of μ_{ratio} is limited to a maximum of 1.8.[1] Mobility enhancement was implemented in product in 2004[2] to meet the required saturation drive current, and hence the coloring for extended planar bulk is initially white. However, there are numerous approaches in the literature for mobility enhancement (including global strain using thin silicon epitaxial layers on SiGe epitaxial layers,[3] different process induced strain approaches such as strained thin overlayers of SiN and selective epitaxial SiGe in the S/D, hybrid orientations, etc.[2, 4, 5]), and as we continue to scale MOSFETs, it is unclear what the optimal approach(es) will be and how to integrate them into the process flow. Consequently, for both LSTP and LOP the row is colored yellow when L_g=20 nm and the scaling becomes difficult enough that the doping approaches 5E18 cm^{-3} according to the MASTAR modeling. This occurs in 2013 for LSTP and in 2011 for LOP. For both FD SOI and DG, the row starts out yellow because we don't at this point understand manufacturable solutions to mobility enhancement for these device types.

[11] Effective Ballistic Enhancement Factor is a multiplying factor for $I_{d,sat}$, reflecting quasi-ballistic enhanced transport in highly scaled, ultra-thin body MOSFETs, both UTB FD SOI and DG MOSFETs. Planar bulk CMOS does not have ballistic enhancement because of the high doping in these devices. Values for this factor greater than 1 reflect quasi-ballistic enhancement. The value of this parameter is driven by the required saturation drive current to meet performance requirements. The initial yellow coloring reflects that quasi-ballistic enhancement is expected (and predicted by MASTAR) for undoped, very scaled UTB FD and DG MOSFETs. The later red coloring reflects the lack of known manufacturable enhanced transport solutions for transistors with gate length approaching 10nm.

[12] R_{sd} is the maximum allowable parasitic series source plus drain resistance for a MOSFET of one micron width. The values are scaled to allow the required saturation current drive values (see Note [9]) to be met. Yellow/red coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling.

[13] $C_{g,ideal}$ is the ideal gate capacitance per micron device width, in inversion. $C_{g,ideal} = [\varepsilon_{ox} /(EOT_{elec})] \times L_g$, where ε_{ox} is the dielectric constant of thermal silicon dioxide, EOTelec is the equivalent electrical oxide thickness in inversion (see Note [4]), and L_g is the physical gate length (see Note [1]). The red/yellow coloring follows that of EOTelec (see Note [4]).

[14] $C_{g,total}$ is the total gate capacitance per micron device width in inversion. This is the sum of $C_{g,ideal}$ and the parasitic gate overlap/fringing capacitance per micron device width [including the Miller effect]. Red/yellow color here follows that of $C_{g,ideal}$.

[15] τ is the intrinsic transistor delay for NMOS devices at 25°C. $\tau = (C_{g,total} \times V_{dd}) / I_{d,sat}$. τ for PMOSFETs is assumed to scale similarly, but with PMOS $I_{d,sat} \sim (0.4–0.5) \times$ (NMOS $I_{d,sat}$). τ is a good metric for the intrinsic switching delay of the device, while $1/\tau$ is a good metric for the intrinsic switching speed of the device. Red/yellow coloring follows that of both saturation drive current (see Note [9]) and Cg,total (see Note [14]).

[16] $1/\tau$ is the NMOS intrinsic switching speed. Red/yellow coloring follows that of τ.

MEMORY TECHNOLOGY REQUIREMENTS

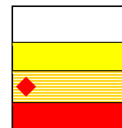
Table 42a DRAM Technology Requirements—Near-term

Year in Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) [1]	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*35*	*32*
DRAM cell size (μm²) [2]	**0.0514**	**0.0408**	**0.0324**	**0.0193**	**0.0153**	**0.0122**	**0.0096**	**0.0077**	**0.0061**
DRAM storage node cell capacitor dielectric: equivalent oxide thickness EOT (nm) [3]	**1.8**	**1.4**	**1.1**	**0.9**	**0.8**	**0.6**	**0.6**	**0.5**	**0.5**
DRAM storage node cell capacitor voltage (V) [4]	**1.5**	**1.4**	**1.3**	**1.2**	**1.1**	**1.1**	**1.1**	**1**	**1**
Electric field of capacitor dielectric, (MV/cm) [5]	**8**	**10**	**12**	**13**	**14**	**18**	**18**	**20**	**20**
DRAM cell FET dielectric: equivalent oxide thickness, EOT (nm) [6]	**5.5**	**5**	**5**	**4.5**	**4**	**4**	**4**	**4**	**4**
Maximum Wordline (WL) level (V) [7]	**3.5**	**3.3**	**3.3**	**3**	**2.7**	**2.7**	**2.7**	**2.6**	**2.6**
Electric field of cell FET device dielectric (MV/cm) [8]	**6.4**	**6.6**	**6.6**	**6.7**	**6.8**	**6.8**	**6.8**	**6.5**	**6.5**
Cell Size Factor: a [9]	**8**	**8**	**8**	**6**	**6**	**6**	**6**	**6**	**6**
Array Area Efficiency [10]	**0.63**	**0.63**	**0.63**	**0.56**	**0.56**	**0.56**	**0.56**	**0.56**	**0.56**
Minimum DRAM retention time (ms) [11]	**64**	**64**	**64**	**64**	**64**	**64**	**64**	**64**	**64**
DRAM soft error rate (fits) [12]	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**

Table 42b DRAM Technology Requirements—Long-term

Year in Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) [1]	*28*	*25*	*22*	*20*	*18*	*16*	*14*
DRAM cell size (μm²) [2]	**0.0048**	**0.0038**	**0.0030**	**0.0024**	**0.0019**	**0.0015**	**0.0012**
DRAM storage node cell dielectric: equivalent physical thickness EOT (nm) [3]	**0.45**	**0.4**	**0.4**	**0.3**	**0.25**	**0.2**	**0.15**
DRAM storage node capacitor voltage (V) [4]	**1**	**0.9**	**0.9**	**0.7**	**0.7**	**0.7**	**0.7**
Electric field of capacitor dielectric, (MV/cm) [5]	**22**	**23**	**23**	**23**	**28**	**35**	**47**
DRAM cell FET dielectric: equivalent oxide thickness, EOT (nm) [6]	**4**	**3.5**	**3.5**	**3.5**	**3**	**3**	**3**
Maximum Wordline (WL) level (V)1 [7]	**2.6**	**2.3**	**2.3**	**2.3**	**2**	**2**	**2**
Electric field of cell FET device dielectric (MV/cm) [8]	**6.5**	**6.6**	**6.6**	**6.6**	**6.7**	**6.7**	**6.7**
Cell Size Factor: a [9]	**6**	**6**	**6**	**6**	**6**	**6**	**6**
Array Area Efficiency [10]	**0.56**	**0.56**	**0.56**	**0.56**	**0.56**	**0.56**	**0.56**
Minimum DRAM retention time (ms) [11]	**64**	**64**	**64**	**64**	**64**	**64**	**64**
DRAM soft error rate (fits) [12]	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**	**1000**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 42a and b:

[1] From ORTC (Overall Roadmap Technology Characteristics) Table 1a and b. These DRAM half pitch numbers are the same as those in the 2004 ITRS due to no further speed up in the pace of DRAM half pitch scaling during 2004.

[2] The DRAM cell size is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Process chapter. The capacity and chip size numbers are based on the ORTC Tables 1a and 1b. Since the DRAM capacity and chip size numbers are quite aggressive, the cell size must also be scaled aggressively. The difficulty will lie in reducing the value of the cell size factor "a", where "a" equals (cell size /F^2) and F is the DRAM half pitch. The required values of "a" are 8 for DRAM ½ pitch of 80- 65 nm and 6 for 57 nm and beyond,

[3] Storage node cell dielectric EOT is defined as (dielectric physical thickness / [k/3.9]), where k is the relative dielectric constant of the storage node cell dielectric and 3.9 is the relative dielectric constant of thermal SiO_2. The value of EOT is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Process chapter. The capacity and the chip size numbers used by FEP are from the ORTC Tables 1a and 1b. Since the values of DRAM capacity and chip size from FEP are quite aggressive, the EOT must also be scaled very aggressively. Up to the 65 nm technology generation in 2007, the dielectric material is based on Al_2O_3 or Ta_2O_5 with MIS structure, and hence the color is white. Beyond2007, breakthroughs such as MIM structure and higher k material are needed, so the color is yellow. Finally, for the 45 nm technology generation and beyond, there are no known solutions with demonstrated credibility, and hence the color is red. The actual EOT required for each year also depends on other factors such as cell height and/or 3D structure, film leakage current and contact formation. Trench capacitors have other requirements for the cell dielectric material.

[4] The DRAM storage node capacitor voltage is driven by two opposing needs. In conjunction with the storage node capacitance, which is inversely dependent on EOT (see note [3]), this voltage should be large enough that the stored charge is tolerably large. On the other hand, the voltage must be low enough that the resulting electric field in the dielectric (see Note [5]) is within acceptable limits.

[5] The electric field in the capacitor dielectric is (DRAM storage node capacitor voltage / DRAM storage node dielectric equivalent oxide thickness, EOT). Due to the sharp increase in the field with scaling, the color turns yellow in 2008, when the electric field is 13 MV/cm, and red in 2010, when the field becomes 18 MV/cm.

[6] DRAM cell FET dielectric EOT is defined as (dielectric physical thickness / [k/3.9]), where k is the relative dielectric constant of the DRAM cell FET dielectric and 3.9 is the relative dielectric constant of thermal SiO_2. The EOT values here are large, mainly because of the high word line voltage levels (see Note 7) and the need to keep the electric field in the dielectric within tolerable limits (see Note 8)

[7] Maximum wordline level is the (highly boosted) gate voltage for cell FET devices. The high gate voltage is required to get enough device drive current with high threshold voltage due to back gate voltage at the operating condition.

[8] The electric field in the cell FET device dielectric is (maximum wordline level / DRAM cell FET dielectric equivalent oxide thickness, EOT).

[9] Cell size factor = a = (DRAM cell size/F^2), where F is the DRAM ½ pitch. The required values of a are 8 for DRAM ½ pitch of 80–65 nm and 6 for 57 nm and beyond. In contrast to previous versions, the 2005 version of the DRAM table doesn't have a = 4 because a $4F^2$ cell structure is considered to be unrealistic.

[10] Array area efficiency is the ratio of cell array area to total chip area. Hence, array area efficiency = 1 / (1 + [peripheral circuit area]/NaF^2), where N is the DRAM capacity (number of bits per chip), F is the DRAM ½ pitch, and a is the cell size factor (see Note 9). For a = 8, array area efficiency is estimated to be 0.63, so when a is decreased to 6 after 2007, the array area efficiency is decreased to 0.56, assuming the same relative peripheral circuit area.

[11] Retention time is defined at 85°C, and is the minimum time during which the data from memory can still be sensed correctly without refreshing a row bit line. The 64 ms specified here is the value needed for PC applications. The retention time depends on the combined interaction of device leakage current, signal strength and signal sensing circuit sensitivity, and also depends on operational frequency and temperature.

[12] This is a typical FIT rate and depends on cycle time and the quality of cell capacitor and sensing circuits.

NON-VOLATILE MEMORY TECHNOLOGY REQUIREMENTS

Table 43a Non-Volatile Memory Technology Requirements—Near-term

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Flash technology NOR/NAND – F (nm) [1]	**80/76**	**70/64**	**65/57**	**57/51**	**50/45**	**45/40**	**40/36**	**35/32**	**32/28**
Flash NOR cell size – area factor a in multiples of F^2 [2], [3], [4], [5]	**9–11**	**9–11**	**9–11**	**9–12**	**10–12**	**9–12**	**9–12**	**10–12**	**10–12**
Flash NAND cell size – area factor a in multiples of F^2 SLC/MLC [6]	**4.0/2.0**	**4.0/2.0**	**4.0/2.0**	**4.0/2.0**	**4.0/2.0**	**4.0/1.0**	**4.0/1.0**	**4.0/1.0**	**4.0/1.0**
Flash NOR typical cell size (μm^2) [7], [8]	**0.064**	**0.049**	**0.042**	**0.034**	**0.028**	**0.021**	**0.017**	**0.013**	**0.011**
Flash NOR L_g-stack (physical – µm) [8], [9]	**0.14**	**0.135**	**0.13**	**0.12**	**0.12**	**0.11**	**0.11**	**0.1**	**0.1**
Flash NOR highest W/E voltage (V) [10], [11]	**7-9**	**7-9**	**7-9**	**7-9**	**7-9**	**6-8**	**6-8**	**6-8**	**6-8**
Flash NAND highest W/E voltage (V) [12]	**17–19**	**17–19**	**15–17**	**15–17**	**15–17**	**15–17**	**15-17**	**15–17**	**15–17**
Flash NOR I_{read} (µA) [13]	**29–37**	**28–36**	**27–35**	**26–34**	**25–33**	**27–33**	**27–33**	**26–32**	**25–31**
Flash coupling ratio [14]	**0.65–0.75**	**0.6–0.7**	**0.6–0.7**	**0.6–0.7**	**0.6–0.7**	**0.6–0.7**	**0.6–0.7**	**0.6–0.7**	**0.6–0.7**
Flash NOR tunnel oxide thickness EOT (nm) [15]	**8–9**	**8–9**	**8–9**	**8–9**	**8–9**	**8**	**8**	**8**	**8**
Flash NAND tunnel oxide thickness EOT (nm) [16]	**7–8**	**7-8**	**6–7**	**6–7**	**6–7**	**6–7**	**6–7**	**6–7**	**6–7**
Flash NOR interpoly dielectric thickness EOT (nm) [17]	**13-15**	**13-15**	**13-15**	**13-15**	**13-15**	**10-12**	**10-12**	**10-12**	**10-12**
Flash NAND interpoly dielectric thickness (nm) [18]	**13–15**	**13–15**	**10–13**	**10–13**	**10–13**	**10–13**	**10–13**	**10–13**	**9–10**
Flash endurance (erase/write cycles) [19]	**1.00E+05**	**1.00E+05**	**1.00E+05**	**1.00E+05**	**1.00E+05**	**1.00E+06**	**1.00E+06**	**1.00E+06**	**1.00E+06**
Flash nonvolatile data retention (years) [20]	**10–20**	**10–20**	**10–20**	**10–20**	**10–20**	**10–20**	**10–20**	**10–20**	**20**
Flash maximum number of bits per cell (MLC) [21]	**2**	**2**	**2**	**2**	**2**	**4**	**4**	**4**	**4**
FeRAM technology – F (nm) [22]	**130**	**110**	**100**	**90**	**80**	**65**	**57**	**50**	**45**
FeRAM cell size – area factor a in multiples of F^2 [23]	**34**	**34**	**30**	**30**	**30**	**24**	**24**	**24**	**20**
FeRAM cell size (μm^2) [24]	**0.575**	**0.411**	**0.300**	**0.243**	**0.192**	**0.101**	**0.078**	**0.060**	**0.041**
FeRAM cell structure [25]	**1T1C**	**1T1C**	**1T1C**	**1T1C**	**1T1C**	**1T1C**	**1T1C**	**1T1C**	**1T1C**
FeRAM capacitor structure [26]	**stack**	**stack**	**stack**	**stack**	**stack**	**3D**	**3D**	**3D**	**3D**
FeRAM capacitor footprint (μm^2) [27]	**0.32**	**0.23**	**0.158**	**0.128**	**0.101**	**0.049**	**0.038**	**0.029**	**0.018**
FeRAM capacitor active area (μm^2) [28]	**0.32**	**0.23**	**0.158**	**0.128**	**0.101**	**0.076**	**0.069**	**0.064**	**0.059**
FeRAM cap active area/footprint ratio [29]	**1**	**1**	**1**	**1**	**1**	**1.55**	**1.85**	**2.2**	**3.31**

Table 43a Non-Volatile Memory Technology Requirements—Near-term (continued)

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Ferro capacitor voltage (V) [30]	**1.5**	**1.5**	**1.2**	**1.2**	**1.2**	**1**	**1**	**1**	**0.7**
FeRAM minimum switching charge density (μC/cm^2) [31]	**11.4**	**14.2**	**19**	**22**	**26**	**30**	**30**	**30**	**30**
FeRAM endurance (read/write cycles) [32]	**1.0E+13**	**1.0E+14**	**1.0E+15**	**>1.0E16**	**>1.0E16**	**>1.0E16**	**>1.0E16**	**>1.0E16**	**>1.0E16**
FeRAM nonvolatile data retention (years) [33]	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**	**10**
SONOS/NROM technology – F (nm) [34]	**100**	**90**	**70**	**65**	**55**	**50**	**45**	**40**	**35**
SONOS/NROM cell size – area factor a in multiples of F^2 [35]	**5.5**	**5.5**	**6**	**6**	**6**	**6**	**6**	**6**	**6.5**
SONOS/NROM typical cell size (μm^2) [36]	**0.055**	**0.045**	**0.029**	**0.025**	**0.018**	**0.015**	**0.012**	**0.01**	**0.008**
SONOS/NROM maximum number of bits per cell ((physical 2-bit/cell) x MLC) [37]	**2**	**2**	**2**	**2**	**2**	**4**	**4**	**4**	**4**
SONOS/NROM area per bit (μm^2) [38]	**0.028**	**0.022**	**0.015**	**0.013**	**0.009**	**0.0038**	**0.003**	**0.0024**	**0.002**
SONOS L_g-stack (physical – μm) [39]	**0.17**	**0.17**	**0.16**	**0.16**	**0.16**	**0.16**	**0.16**	**0.16**	**0.15**
SONOS highest W/E voltage (V) [40]	**5.0–6.0**	**5.0–6.0**	**5.0–5.5**	**5.0–5.5**	**5.0–5.5**	**5.0–5.5**	**5.0–5.5**	**5.0–5.5**	**5.0–5.5**
SONOS/NROM I_{read} (μA) [41]	**31–41**	**29–39**	**27–37**	**25–35**	**25–35**	**25–35**	**25–35**	**24–34**	**23–33**
SONOS/NROM tunnel oxide thickness (nm) [42]	**4.5**	**4**	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**	**3**
SONOS/NROM nitride dielectric thickness (nm) [43]	**5**	**4.5**	**4**	**4**	**4**	**4**	**4**	**4**	**4**
SONOS/NROM blocking (top) oxide or dielectric thickness (nm) [44]	**4.5**	**4.5**	**4**	**6**	**6**	**6**	**6**	**6**	**6**
SONOS/NROM endurance (erase/write cycles) [45]	**1.00E+07**	**1.00E+07**	**1.00E+07**	**1.00E+07**	**1.00E+07**	**1.00E+08**	**1.00E+08**	**1.00E+08**	**1.00E+08**
SONOS/NROM nonvolatile data retention (years) [46]	**10–20**	**10–20**	**10–20**	**10–20**	**10–20**	**10–20**	**10–20**	**10–20**	**10–20**
MRAM technology F (nm) [47]	**180**	**90**	**90**	**65**	**65**	**45**	**45**	**45**	**32**
MRAM cell size area factor a in multiples of F^2 [48]	**25**	**23**	**20**	**22**	**19**	**20**	**18**	**18**	**19**
MRAM typical cell size (μm^2) [49]	**0.81**	**0.19**	**0.16**	**0.09**	**0.08**	**0.041**	**0.036**	**0.036**	**0.019**
MRAM switching field (Oe) [50]	**35**	**35**	**35**	**35**	**35**	**35**	**35**	**35**	**35**
MRAM write energy (pJ/bit) [51]	**150**	**100**	**70**	**35**	**35**	**25**	**25**	**25**	**20**
MRAM active area per cell (μm^2) [52]	**0.11**	**0.05**	**0.05**	**0.025**	**0.025**	**0.013**	**0.013**	**0.013**	**0.009**
MRAM resistance-area product (Kohm-(μm^2) [53]	**4**	**2**	**2**	**1.1**	**1**	**0.8**	**0.8**	**0.8**	**0.6**
MRAM magnetoresistance ratio (%) [54]	**40**	**70**	**70**	**70**	**70**	**70**	**70**	**70**	**70**
MRAM nonvolatile data retention (years) [55]	**>10**	**>10**	**>10**	**>10**	**>10**	**>10**	**>10**	**>10**	**>10**
MRAM write endurance (read/write cycles) [56]	**>3e16**	**>3e16**	**>3e16**	**>3e16**	**>3e16**	**>3e16**	**>3e16**	**>3e16**	**>3e16**
MRAM endurance – tunnel junction reliability (years at bias) [57]	**>10**	**>10**	**>10**	**>10**	**>10**	**>10**	**>10**	**>10**	**>10**

Table 43a Non-Volatile Memory Technology Requirements—Near-term (continued)

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
PCRAM technology F (nm) [58]	90	70	65	57	50	45	40	35	32
PCRAM cell size area factor a in multiples of F^2 (BJT access device) [59]	7.2	7.0	6.4	5.6	5.8	5.8	5.8	6.1	5.8
PCRAM cell size area factor a in multiples of F^2 (nMOSFET access device) [60]	17.0	14.9	12.8	11.8	11.6	11.0	10.5	10.1	9.5
PCRAM typical cell size (μm^2) (BJT access device) [61]	0.059	0.034	0.027	0.018	0.015	0.012	0.0092	0.0074	0.0059
PCRAM typical cell size (μm^2) (nMOSFET access device) [62]	0.14	0.073	0.054	0.038	0.029	0.022	0.017	0.012	0.0097
PCRAM number of bits per cell (MLC) [63]	1	1	2	2	2	4	4	4	4
PCRAM typical cell area per bit size (μm^2) (BJT access device) [64]	0.059	0.034	0.014	0.009	0.008	0.003	0.0023	0.0018	0.0015
PCRAM typical cell area per bit size (μm^2) (nMOSFET access device) [65]	0.14	0.073	0.027	0.019	0.015	0.006	0.004	0.003	0.0025
PCRAM storage element CD (nm) [66]	32	25	23	21	18	16	14	13	12
PCRAM phase change volume (nm^3) [67]	17,157	8,181	6,371	4,849	3,054	2,145	1,437	1,150	905
PCRAM reset current (µA) [68]	270	191	170	150	121	102	85	77	68
PCRAM set resistance (Kohm) [69]	2.5	3.4	3.7	4.3	5.0	5.7	6.5	7.6	8.5
PCRAM BJT current density (A/cm^2) [70]	4.3E+6	5.0E+6	5.1E+6	5.9E+6	6.2E+6	6.5E+6	6.8E+6	8.0E+6	8.5E+6
PCRAM BJT emitter area (μm^2) [71]	0.0064	0.0039	0.0033	0.0026	0.0020	0.0016	0.0013	0.00096	0.00080
PCRAM nMOSFET current density for reset (µA/µm) [72]	643	689	802	896	842	853	849	924	987
PCRAM nMOSFET device width (µm) [73]	0.42	0.28	0.21	0.17	0.14	0.12	0.10	0.083	0.069
PCRAM nonvolatile data retention (years) [74]	>10	>10	>10	>10	>10	>10	>10	>10	>10
PCRAM write endurance (read/write cycles) [75]	1.0E+12	1.0E+12	1.0E+12	1.0E+12	1.0E+12	1.0E+13	1.0E+13	1.0E+13	1.0E+14

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

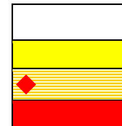


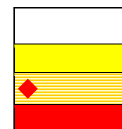
Table 43b Non-Volatile Memory Technology Requirements—Long-term

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Flash technology NOR/NAND – F (nm) [1]	28/25	25/23	22/20	20/18	18/16	16/14	14/13
Flash NOR cell size – area factor a in multiples of F^2 [2], [3], [4], [5]	10–12	10–13	10–-13	11–14	11–14	12–14	12–14
Flash NAND cell size – area factor a in multiples of F^2 SLC/MLC [6]	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0
Flash NOR typical cell size (μm^2) [7], [8]	0.0086	0.0073	0.0057	0.005	0.004	0.0034	0.0026
Flash NOR L_g-stack (physical – µm) [8], [9]	0.09	0.09	0.08	0.08	0.07	0.07	0.06
Flash NOR highest W/E voltage (V) [10], [11]	6–8	6–8	6–8	6–8	6–8	6–8	6–8
Flash NAND highest W/E voltage (V) [12]	15–17	15–17	15–17	15-17	15–17	15–17	15–17
Flash NOR I_{read} (µA) [13]	24–30	23–29	22–28	21–27	20–26	19–25	18–24
Flash coupling ratio [14]	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6-0.7	0.6-0.7
Flash NOR tunnel oxide thickness EOT (nm) [15]	7 – 8	7 – 8	7 – 8	7 – 8	7 – 8	7 – 8	7 – 8
Flash NAND tunnel oxide thickness EOT (nm) [16]	6–7	6–7	6–7	6–7	6–7	6–7	6–7
Flash NOR interpoly dielectric thickness EOT (nm) [17]	8–10	8–10	8–10	8–10	7–9	6–8	6–8
Flash NAND interpoly dielectric thickness (nm) [18]	9–10	9–10	9–10	9–10	9–10	9–10	9–10
Flash endurance (erase/write cycles) [19]	1.00E+06	1.00E+06	1.00E+07	1.00E+07	1.00E+07	1.00E+07	1.00E+07
Flash nonvolatile data retention (years) [20]	20	20	20	20	20	20	20
Flash maximum number of bits per cell (MLC) [21]	4	4	4	4	4	4	4
FeRAM technology – F (nm) [22]	40	35	32	28	25	22	20
FeRAM cell size – area factor a in multiples of F^2 [23]	20	20	16	16	16	14	14
FeRAM cell size (μm^2) [24]	0.032	0.025	0.016	0.013	0.010	0.007	0.006
FeRAM cell structure [25]	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C
FeRAM capacitor structure [26]	3D	3D	3D	3D	3D	3D	3D
FeRAM capacitor footprint (μm^2) [27]	0.014	0.011	0.0064	0.0049	0.0039	0.0024	0.002
FeRAM capacitor active area (μm^2) [28]	0.055	0.05	0.047	0.043	0.04	0.037	0.035
FeRAM cap active area/footprint ratio [29]	3.88	4.63	7.38	8.81	10.25	15.12	17.17
Ferro capacitor voltage (V) [30]	0.7	0.7	0.7	0.7	0.7	0.7	0.7
FeRAM minimum switching charge density ($\mu C/cm^2$) [31]	30	30	30	30	30	30	30
FeRAM endurance (read/write cycles) [32]	>1.0E16	>1.0E16	>1.0E16	>1.0E16	>1.0E16	>1.0E16	>1.0E16
FeRAM nonvolatile data retention (years) [33]	10	10	10	10	10	11	12
SONOS/NROM technology – F (nm) [34]	32	28	25	23	20	19	18
SONOS/NROM cell size – area factor a in multiples of F^2 [35]	6.5	6.5	7	7	7	7	7
SONOS/NROM typical cell size (μm^2) [36]	0.007	0.005	0.004	0.0037	0.003	0.0025	0.002
SONOS/NROM maximum number of bits per cell ((physical 2-bit/cell) x MLC) [37]	4	4	4	4	4	4	4
SONOS/NROM area per bit (μm^2) [38]	0.0018	0.0013	0.0011	0.0009	0.0007	0.0006	0.0005
SONOS L_g-stack (physical – µm) [39]	0.15	0.15	0.14	0.14	0.14	0.13	0.13
SONOS highest W/E voltage (V) [40]	5.0–5.5	5.0–5.5	4.5–5.0	4.5–5.0	4.0–4.5	4.0–4.5	4.0–4.5
SONOS/NROM I_{read} (µA) [41]	23–33	22–32	21–31	21–31	20–30	20–30	20–30

Table 43b Non-Volatile Memory Technology Requirements—Long-term (continued)

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
SONOS/NROM tunnel oxide thickness (nm) [42]	**3**	**3**	**2.5**	**2.5**	**2.5**	**2**	**2**
SONOS/NROM nitride dielectric thickness (nm) [43]	**4**	**4**	**4**	**4**	**4**	**4**	**4**
SONOS/NROM blocking (top) oxide or dielectric thickness (nm) [44]	**6**	**6**	**5**	**5**	**5**	**5**	**5**
SONOS/NROM endurance (erase/write cycles) [45]	**1.00E+08**	**1.00E+08**	**1.00E+09**	**1.00E+09**	**1.00E+09**	**1.00E+09**	**1.00E+09**
SONOS/NROM nonvolatile data retention (years) [46]	**10–20**	**10–20**	**10–20**	**10–20**	**10–20**	**10–20**	**10–20**
MRAM technology F (nm) [47]	**32**	**32**	**22**	**22**	**22**	**16**	**16**
MRAM cell size area factor a in multiples of F^2 [48]	**17**	**17**	**18**	**16**	**16**	**17**	**16**
MRAM typical cell size (μm^2) [49]	**0.017**	**0.017**	**0.009**	**0.0077**	**0.0077**	**0.0044**	**0.0041**
MRAM switching field (Oe) [50]	**35**	**35**	**35**	**35**	**35**	**35**	**35**
MRAM write energy (pJ/bit) [51]	**20**	**20**	**20**	**20**	**20**	**20**	**20**
MRAM active area per cell (μm^2) [52]	**0.009**	**0.009**	**0.007**	**0.007**	**0.007**	**0.005**	**0.005**
MRAM resistance-area product (Kohm-(μm^2) [53]	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**
MRAM magnetoresistance ratio (%) [54]	**70**	**70**	**70**	**70**	**70**	**70**	**70**
MRAM nonvolatile data retention (years) [55]	**>10**	**>10**	**>10**	**>10**	**>10**	**>10**	**>10**
MRAM write endurance (read/write cycles) [56]	**>3e16**	**>3e16**	**>3e16**	**>3e16**	**>3e16**	**>3e16**	**>3e16**
MRAM endurance – tunnel junction reliability (years at bias) [57]	**>10**	**>10**	**>10**	**>10**	**>10**	**>10**	**>10**
PCRAM technology F (nm) [58]	**28**	**25**	**22**	**20**	**18**	**16**	**14**
PCRAM cell size area factor a in multiples of F^2 (BJT access device) [59]	**5.9**	**5.9**	**5.0**	**4.8**	**4.7**	**4.7**	**4.7**
PCRAM cell size area factor a in multiples of F^2 (nMOSFET access device) [60]	**8.7**	**8.2**	**7.4**	**6.8**	**6.3**	**5.8**	**5.4**
PCRAM typical cell size (μm^2) (BJT access device) [61]	**0.0046**	**0.0037**	**0.0024**	**0.0019**	**0.0015**	**0.0012**	**0.0009**
PCRAM typical cell size (μm^2) (nMOSFET access device) [62]	**0.0068**	**0.0051**	**0.0036**	**0.0027**	**0.0020**	**0.0015**	**0.0011**
PCRAM number of bits per cell (MLC) [63]	**4**	**4**	**4**	**4**	**4**	**4**	**4**
PCRAM typical cell area per bit size (μm^2) (BJT access device) [64]	**0.0012**	**0.0009**	**0.0006**	**0.0005**	**0.0004**	**0.0003**	**0.0002**
PCRAM typical cell area per bit size (μm^2) (nMOSFET access device) [65]	**0.0017**	**0.0013**	**0.0009**	**0.0007**	**0.0005**	**0.0004**	**0.0003**
PCRAM storage element CD (nm) [66]	**10**	**9**	**7.9**	**7.2**	**6.5**	**5.8**	**5.0**
PCRAM phase change volume (nm^3) [67]	**524**	**382**	**268**	**180**	**113**	**102**	**65**
PCRAM reset current (μA) [68]	**53**	**46**	**39**	**32**	**26**	**21**	**16**
PCRAM set resistance (Kohm) [69]	**9.9**	**11.3**	**13.2**	**14.7**	**16.7**	**18.7**	**21.7**
PCRAM BJT current density (A/cm^2) [70]	**8.6E+6**	**9.3E+6**	**1.0E+7**	**1.0E+7**	**1.0E+7**	**1.0E+7**	**1.0E+7**
PCRAM BJT emitter area (μm^2) [71]	**0.00062**	**0.00049**	**0.00038**	**0.00031**	**0.00026**	**0.00020**	**0.00015**
PCRAM nMOSFET current density for reset (μA/μm) [72]	**997**	**1,056**	**1,202**	**1,270**	**1,310**	**1,320**	**1,340**
PCRAM nMOSFET device width (μm) [73]	**0.053**	**0.043**	**0.032**	**0.025**	**0.020**	**0.016**	**0.012**
PCRAM nonvolatile data retention (years) [74]	**>10**	**>10**	**>10**	**>10**	**>10**	**>10**	**>10**
PCRAM write endurance (read/write cycles) [75]	**1.0E+14**	**1.0E+14**	**1.0E+15**	**1.0E+15**	**1.0E+15**	**1.0E+15**	**1.0E+15**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Table 43a and b:

[1] In the past Flash devices tended to lag behind the current CMOS technology's feature size, F, but that delay no longer exists. This entry provides the F value for designs in the indicated time period.

[2] The area factor "a" = cell area/F^2, so this entry presents the expected range for Flash NOR cell area in multiples of the implementation technology's F^2. Note the slowly increasing trend that reflects the difficulty of scaling the gate length when the tunnel oxide thickness is fixed.

[3] High-κ interpoly dielectric is projected at the 45 nm technology generation and beyond, and gate coupling ratio of >0.7 can be achieved which helps to maintain the cell size.[6] This helps to slow down the increase in the area factor.

[4] Although virtual ground array may significantly decrease the cell size in the near term [7]this effect has not been included in the current table.

[5] Although non-planar devices (such as FinFET) are being developed for future Flash scaling, their impact has not been included in the current table. The deployment of high κ in interpoly may help to reduce the Lg somewhat.

[6] The area factor "a" = cell area/F^2, so this entry presents the Flash NAND cell area in multiples of F^2 of the implementation technology. Flash NAND enjoys a small cell size because much of the cell structure is shared among a group of cells. (SLC = single level cell, MLC = multilevel cell; see Note 21 below for more detail.)

[7] A typical Flash NOR cell size in micrometers squared is estimated using the midrange area factor "a."

[8] Both the cell size and the gate length for NOR Flash have been more aggressively scaled recently.[8, 9, 10]

[9] This is the physical length of the control gate of Flash NOR devices.

[10, 12] This is the highest voltage relative to ground seen in the cell array. It is not usually an external supply.

[11] The introduction of high-κ interpoly dielectric will help to reduce the erase voltage.

*[13] The current reduces with scaling at a rate higher than W/(L*Cox) to reduce the voltage overdrive factor.*

[14] The coupling ratio is the (control gate to floating gate capacitance)/(total floating gate to source, drain and substrate capacitance).

[15, 16] Tunnel oxides must be thick enough to assure retention but thin enough to allow ease of erase/write. This difficult trade off problem hinders scaling. Tunnel oxides less than 7 nm seem to pose fundamental problems for retention reliability.

[17, 18] Interpoly dielectric must be thick enough to assure retention but thin enough to assure an almost constant coupling ratio. Charge retention when the dielectric is scaled downward is the major issue. High-κ interpoly will help reducing the interpoly EOT and maintain constant coupling ratio without losing retention.

[19] E/W endurance requirements vary with the specifics of an application, but 1E5 cycles have been accepted as the historical minimum acceptable level for a useful product. It is expected that emerging technology will allow both tradeoffs of endurance for retention as well as increases in the specified minimum endurance capability as device design options.

[20] Retention is a defect related parameter rather than an intrinsic device characteristic. Improvement in defect control and accumulation of device history is expected to eventually allow specification of 20 years retention. Also, it should become possible to accept a reduced retention specification as a tradeoff for increased E/W endurance.

[21] Cell read out distinguishes between four levels of charge storage to provide two storage bits. Progression to 16 levels is anticipated but maintaining reasonable V_t, read speed and array efficiency beyond 2-bit/cell are challenging. (MLC multilevel cell).

[22] This entry is the critical dimension "F" within the FeRAM cell for stand-alone memory devices (not embedded devices).

[23] This is the area factor "a" = cell size/F^2. FeRAM cell size is presented in terms of multiples of the FeRAM implementation technology's F^2

[24] FeRAM cell size is presented in terms of micrometers squared. It is the product "a"xF^2.

[25] FeRAM cell structures have migrated to one transistor, one capacitor (1T1C) formats.[11,12] Other alternative configurations are under investigation such as Chain-FeRAM.[13, 14]

[26] The geometry of the capacitor is a key factor in determining cell size. Stacked planar films are expected to be replaced by more efficient 3D structures.

[27] This is the footprint of the capacitor in micrometers squared. It is this area that constitutes the capacitor area contribution to the cell size. For 2005–2006 ~19F^2, for 2007 - 2009 ~16F^2, and for 2010–2020 ~ 10F^2 or less (3D capacitor) are assumed.

[28] This is the actual effective area of the capacitor. It is larger than the footprint for 3D capacitor because of the utilization of area in the third dimension.

[29] This ratio of the effective area to the footprint gives a measure of the impact of utilization of the third dimension.

[30] This is the operating voltage (V_{op}) applied to the capacitor. Low voltage operation is a difficult key design issue. Generally the ferroelectric film thickness needs to be decreased in order to reduce the V_{op}, with great technological challenges.[15]

[31] The minimum switching charge density in μC/cm^2 is a useful design parameter. It is equal to the cell minimum switching charge divided by the capacitor actual effective area. The capacitor voltage is taken as V_{op}.

[32] FeRAM is a destructive read-out technology, so every read is accompanied by a write to restore the data. Endurance cycles are taken as the sum of all read and all write cycles. For FeRAM to compete with DRAM and SRAM the cycle endurance should be about 1E15. Test time is a serious concern. Note that operation at 100 MHz for 10 years would accumulate 1E16 cycles.

[33] This is the data retention requirement while the device is disconnected from power. It is usually specified at 85 ºC.

[34] SONOS/NROM devices have recently been introduced into the commercial market and will tend to lag the feature size of the current CMOS technology by one year. This entry provides the F value for designs in the indicated time period.

[35] The area factor "a" = cell area/F^2. This entry depicts the expected SONOS/NROM NOR cell area in multiples of the implementation technology's F^2. SONOS/NROM device stores two physical bits of data per device. This area factor "a" is per cell, not per bit.

[36] The expected "typical" SONOS/NROM NOR cell size is presented in terms of micrometers squared. Again, this cell size is per cell, not per physical or MLC bit.

[37] MBC signifies "multiple bit storage," while MLC signifies "multiple level storage." The SONOS/NROM cell stores charge in two distinct locations – in the nitride over the source and drain junctions. Thus, in the simplest case there are two distinct bits within each cell; however, each charge location may be partitioned into multiple levels (MLC), thereby, increasing the bit storage per cell.

[38] The expected SONOS/NROM NOR area per bit is presented in terms of micrometers squared. The stored bit includes both physical 2-bit/device and MLC.

[39] This is the physical length of the gate of SONOS/NROM devices in micrometers as there is only a single gate, similar to a MOSFET.

[40] This is the highest voltage relative to ground seen in the cell array. It is not usually an external supply.

*[41] Reduction rate is higher than (W/L)*Cox) to reduce the voltage overdrive factor.*

[42] Tunnel oxides must be thick enough to assure retention but thin enough to allow ease of erase/write at low voltage. This offers a challenge to scaling.
[43] The nitride dielectric provides the charge storage medium and its thickness is a compromise between program/erase voltages, erase/write window, retention, process control and endurance. This offers a challenge to scaling.
[44] The blocking (top) oxide thickness isolates the charge storage region (nitride) from the gate electrode. Its thickness is a compromise between program/erase voltages and retention. This offers a challenge to scaling. With the advent of high-κ dielectrics, such as aluminum oxide, and advanced deposition techniques, such as atomic layer deposition (ALD), the thickness of the blocking (top) insulator may be increased to prevent gate injection, while maintaining program speed and long-term retention. This technology will probably mature in the year 2008 and beyond. High-κ dielectrics also ease the requirements on scaling the nitride and tunnel oxide since the electric fields may be preserved in the latter.
[45] E/W endurance (erase/write cycles) requirements vary with the specifics of an application, but 1E5 cycles has been accepted as the historical minimum acceptable level for a useful product. It is expected that emerging technology will allow both tradeoffs of endurance for retention as well as increases in the specified minimum endurance capability as device design options.
[46] SONOS/NROM retention follows a stretched exponential curve and saturates and becomes time independent afterwards. Thus the charge loss affects the V_t programming window but is not a long-term reliability issue. As long as the programming window is sufficiently designed retention by itself is not a concern. However, charge loss mechanisms and retention models are still being improved and further modifications are possible in the future[16,17].
[47] MRAM devices are expected to lag the feature size of the CMOS current technology until 2010. This entry provides the F value for designs in the indicated time period.
[48] The area factor "a" = cell area/F^2. This entry is the expected MRAM cell area in multiples of the implementation technology's F^2.
[49] The expected "typical" MRAM cell size is presented in micrometers squared.
[50] The MRAM switching field is the magnetic intensity H required to change the direction of magnetization of the cell.
*[51] MRAM switching energy per bit is calculated as (write current * power supply voltage * write time). It is preferred to use the median value of switching energy measured on a multi-megabit array. A good estimate of power drain is (switching energy * number of writes per second).*
*[52] MRAM active bit area is the area of the magnetic material stack within the cell. It represents the "A" in the R*A product.*
*[53] MRAM resistance-area product (i.e., the R*A product) is an intrinsic property of the magnetic material stack that provides a convenient basis for comparing cells of different sizes. The R*A product can be computed by measuring the effective low state resistance (R_{low}) of the magnetic tunnel junction and multiply it by the active bit area of the magnetic stack.*
[54] MRAM magnetoresistive ratio is calculated as $100*(R_{high} – R_{low})/R_{low}$. This ratio summarizes the difference between a logic ONE and a logic ZERO, and as such it represents the intrinsic capability of the magnetic stack. The magnetic tunnel junction resistance values are to be measured at low currents.
[55] MRAM devices are required to retain data while unpowered. This entry states the retention requirement in years.
[56] This entry is the required number of read/write cycles that an MRAM device must be able to endure without degradation that impacts the ability of the device to pass all operating specifications.
[57] An MRAM device is required to meet this minimum life requirement when the magnetic material stack is continuously under bias.
[58] PCRAM devices are expected to follow the feature size of the current CMOS technology. This entry provides the F value for designs in the indicated time period.
[59] The area factor "a" = cell area/F^2. This entry is the expected PCRAM cell area in multiples of the implementation technology's F^2. PCRAM requires significant reset current to change the phase-change element from crystalline to amorphous. A BJT transistor is capable of providing more current per unit area compared to a MOSFET, thus helps to reduce the cell size. Both BJT and nMOSFET access device cells are represented in this table. PCRAM is capable of MLC multi-bit per cell. This area factor is per cell, not per bit.
[60] The area factor "a" = cell area/F^2. This entry is the expected PCRAM cell area in multiples of the implementation technology's F^2. PCRAM requires significant reset current to change the phase-change element from crystalline to amorphous. A BJT transistor is capable of providing more current per unit area compared to a MOSFET, thus helps to reduce the cell size. An nMOSFET transistor has larger cell size in the near term years, but offers simple process and low voltage operation. Both BJT and nMOSFET access device cells are represented in this table. PCRAM is capable of MLC multi-bit per cell. This area factor is per cell, not per bit.
[61] The expected "typical" PCRAM cell size with BJT access device is presented in micrometers squared.
[62] The expected "typical" PCRAM cell size with nMOSFET access device is presented in micrometers squared.
[63] PCRAM is capable of MLC multi-bit/cell operation since the resistance ratio between amorphous and crystalline state is typically 100–1,000. This entry is the expected number of MLC bits per cell.
[64] The expected cell size per MLC bit for the PCRAM with BJT cell. It is the physical cell size divided by the number of MLC bits per cell.
[65] The expected cell size per MLC bit for the PCRAM with nMOSFET cell. It is the physical cell size divided by the number of MLC bits per cell.
[66] PCRAM phase change element must be substantially smaller than the technology's feature size, F, to have efficiency reset operation with reasonable current. This entry is the expected dimension for the phase change element in nanometers.
[67] PCRAM phase change volume is a key factor for device design and peak power requirement. This entry is the expected phase change volume in nanometer cubed.
[68] This entry is the expected reset current for PCRAM in microamperes.
[69] The set resistance is a key design factor for PCRAM read speed.
[70] This entry is the expected current density output from the BJT access device required to reset the PCRAM cell (from crystalline to amorphous state). It is a compromise between larger area BJT (which causes larger cell size) and higher output current (which requires higher operation voltage).
[71] This entry is the expected BJT emitter area that can provide the needed reset current, assuming the BJT current density is met.
[72] This entry is the expected current density output from the nMOSFET access device required to reset the PCRAM cell (from crystalline to amorphous state). It is a compromise between larger width nMOSFET (which causes larger cell size) and higher output current (which requires higher operation voltage or less reliable device).
[73] This entry is the expected nMOSFET gate width that can provide the needed reset current, assuming the MOSFET output current density is met.
[74] This entry is the expected PCRAM data retention that will allow it to be used as a nonvolatile memory. Data retention mechanism for PCRAM is not yet thoroughly studied. Recent published data indicate >10 years of retention at elevated temperatures.[18, 19]
[75] This entry is the expected PCRAM W/E cycling endurance. Recent published data indicate cycling endurance from 1E+9 to 1E+13.[20, 21]

RELIABILITY

Table 44 Reliability Difficult Challenges

Difficult Challenges ≥ 32 nm	*Summary of Issues*
High-κ gate dielectrics with metal gate electrodes	Dielectric breakdown characteristics (hard and soft breakdown) Transistor stability (charge trapping, work function stability, metal ion drift or diffusion) Impact of implantation Metal gate thermomechanical issues (coefficient of thermal expansion mismatch)
Copper/Low-κ interconnects	Stress migration of Cu vias and lines Cu via and line electromigration performance Impact of degradation of properties with lowering k (strength, adhesion, thermal conductivity, coefficient of thermal expansion) Time Dependent Dielectric Breakdown of the Cu/low-κ system Impact of packaging
Packaging	Impact of increasing Coefficient of Thermal Expansion (CTE) mismatch between low-κ, silicon and organic packages Increasing use of multi-chip packages and heterogeneous integration (e.g., CMOS plus MEMs or Sensor) Electromigration in package traces, vias and bumps Impact of assembly and packaging on on-chip failure mechanisms (cracking, stack delamination) Ability of bumps to withstand thermal and mechanical stresses while providing sufficient current carrying capability
Design and test for reliability	Simulation tools for concurrent optimization of circuit performance and reliability Tools to simulate electromigration, thermal-mechanical stress and process induced charging Soft error detection and correction at chip and system level, including random logic faults Screens for resistive and capacitively coupled interconnect defects Alternative screens for decreasing burn-in effectiveness
Negative bias temperature instability	Degradation of p channel current Dependence on scaling and nitrogen in gate insulator Impact on burn-in
Difficult Challenges<32 nm	*Summary of Issues*
Reliability of novel devices, structures, materials and applications	Need to identify and model failure modes, develop acceleration techniques and qualify Post-Cu interconnect solutions (e.g., optical, robust thermal solution, superconductors) Non-CMOS transistors and memory elements New packaging paradigms Novel applications

RELIABILITY REQUIREMENTS

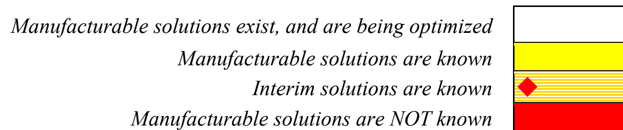
Table 45a Reliability Technology Requirements—Near-term

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013	
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32	
MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13	
Early failures (ppm) (First 4000 operating hours)** [1]	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	
Long term reliability (FITS = failures in 1E9 hours) [2]	10-100	10-100	50–2000	10–100	10–100	10–100	10–100	10–100	10–100	
Soft error rate (FITs)	1000	1000	1000	1000	1000	1000	1000	1000	1000	
Relative failure rate per transistor (normalized to2005 value) [3]	1.00	0.79	0.63	0.50	0.40	0.32	0.25	0.20	0.16	Number of transistors
Relative failure rate per m of interconnect (normalized to2005 value) [4]	1.00	0.84	0.71	0.59	0.51	0.47	0.41	0.37	0.33	Customer needs; J11 length of interconnect

Table 45b Reliability Technology Requirements—Long-term

Year of Production	2014	2015	2016	2017	2018	2019	2020	
DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14	
MPU Physical Gate Length (nm)	11	10	9	8	7	6	6	
Early failures (ppm) (First 4000 operating hours)** [1]	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	
Long term reliability (FITS = failures in 1E9 hours) [2]	10–100	10–100	10–100	10–100	10–100	10–100	10–100	
Soft error rate (FITs)	1000	1000	1000	1000	1000	1000	1000	
Relative failure rate per transistor (normalized to2005 value) [3]	0.13	0.10	0.08	0.06	0.05	0.04	0.03	Number of transistors
Relative failure rate per m of interconnect (normalized to2005 value) [4]	0.29	0.27	0.22	0.20	0.18	0.16	0.14	Customer needs; J11 length of interconnect

Please note that in the above Long-term table, the "Relative failure rate per transistor" value for 2019–2020 is not entered, because there is not projection in the ORTC tables for the number of transistors per chip in those years.



Notes for Table 45a and b:

Reliability requirements vary with different applications. For many mainstream customers it will be sufficient to hold current reliability levels steady during this period of rapid technological change. However, other customers would like reliability levels to be improved. Degradation of current reliability levels is not acceptable. Reliability requirements are for the packaged device and include both chip and package related failure modes.

A reliability qualification can always be attempted with available knowledge. The better the knowledge the less risk in the qualification and vice versa. Yellow coloring indicates some risk. Striped indicates a greater risk (due to changed and possible new failure modes). Finally, red indicates an unspecified solution (e.g., what technology will be used for post-Cu) for which the reliability risk cannot be assessed until details about the solution are provided.

[1] Failures during the first 4000 hours of operation (~1 year's use at 50% duty cycle). Early failures are associated with defects.

[2] Long term reliability rate applies for the specified lifetime of the IC.

[3] While the overall IC failure rate does not change with time, as the number of transistors per chip increases [from ORTC], the relative failure rate per transistor must decrease

[4] As the length of interconnect per chip increases [from Interconnect Technology Requirements Tables], the failure rate per m of interconnect must decrease. Even more important for reliability is the increase in the number of vias.

REFERENCES

[1] S. Takagi et al., "Channel Structure Design, Fabrication and Carrier Transport Properties of Strained-Si/SiGe-On-Insulator (Strained-SOI) MOSFETs," *Technical Digest of IEEE International Electron Devices Meeting*, pp. 57‾60, December 2003.

[2]T. Ghani et al., "A 90 nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate length Strained Silicon CMOS transistors," *Technical Digest of IEEE International Electron Devices Meeting* pp. 978‾980, December 2003.

[3] K. Rim et al., "Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs," *Symposium on VLSI Technology*, pp. 98‾99, June 2002.

[4] C. D. Sheraw et al., "Dual Stress Liner Enhancement in Hybrid Orientation Technology," *Symposium on VLSI Technology*, pp. 12‾13, June 2005.

[5] B. Doris et al., "A Simplified Hybrid Orientation Technology (SHOT) for High Performance CMOS," *Symposium on VLSI Technology*, pp. 86‾87, June 2004.

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[6] E. S. Cho, et al., "Hf-silicate Inter-Poly Dielectric Technology for sub 70 nm Body Tied FinFET Flash Memory", *Symposium on VLSI Technology*, pp. 208-209, June 2005.

[7] R. Koval, et al. "Flash ETOX Virtual Ground Architecture: A Future Scaling Direction", *Symposium on VLSI Technology*, pp. 204–205, June 2005.

[8] "A 90nm 512Mb 166 MHz Multilevel Cell Flash Memory with 1.5MBytes/s Programming", *International Solid State Circuits Conference,* pp. 54–55, February 2005.

[9] "Highly Manufacturable 90 nm NOR Flash Technology with 0.081 μm^2 Cell Size", *Symposium on VLSI Technology*, pp. 91–92, June 2003.

[10] "A 70 nm NOR Flash Technology with 0.049 μm^2 Cell Size", *Symposium on VLSI Technology*, pp. 238–239, June 2004.

[11] J.H. Park, et al., "Fully Logic Compatible (1.6V Vcc, 2 Additional FRAM Masks) Highly Reliable Sub $10F^2$ Embedded FRAM with Advanced Direct Via Technology and Robust 100 nm thick MOCVD PZT Technology", *Technical Digest of IEEE International Electron Devices Meeting,* pp. 591–594, December 2004.

[12] Y. M. Kang et al., "Sub-1.2V Operational, 0.15 µm/$12F^2$ Cell FRAM Technologies for Next Generation SoC Applications", *Symposium on VLSI Technology*, pp. 102–103, June 2005.

[13] H. Kanaya et al., "A 0.602 μm^2 Nestled Chain Cell Structure Formed by One Mask Etching Process for 64 Mbit FeRAM", *Symposium on VLSI Technology*, pp. 150–151, June 2004.

[14] N. Nagel et al., ""New Highly Scalable 3 Dimensional Chain FeRAM Cell with Vertical Capacitor", *Symposium on VLSI Technology*, pp. 146–147, June 2004.

[15] D. C. Yoo et al., "Highly Reliable 50 nm-thick PZT Capacitor and Low Voltage FRAM Device Using Ir/$SrRuO_2$/MOCVD PZT Capacitor Technology", *Symposium on VLSI Technology*, pp. 100–101, June 2005.

[16] M. Janai and B. Eitan, "The Kinetics of Degradation of Data Retention of Post-cycled NROM Non-Volatile Memory Products", *IEEE International Reliability Physics Symposium Proceedings*, pp. 175–180, 2005.

[17] T. Wang et al., "Reliability Models of Data Retention and Read-disturb in 2-bit Nitride Storage Flash Memory Cells", *Technical Digest of IEEE International Electron Devices Meeting*, pp. 169–172, December 2003.

[18] S. J. Ahn et al., "Highly Manufacturable High Density Phase Change Memory of 64 Mb and Beyond", *Technical Digest of IEEE International Electron Devices Meeting*, pp. 907–910, December 2004

[19] A. L. Lacaita et al., "Electrothermal and Phase Change Dynamics in Chalcogenide-Based Materials", *Technical Digest of IEEE International Electron Devices Meeting*, pp. 911–914, December 2004.

---

[20] S.J. Ahn et al., "Highly Manufacturable High Density Phase Change Memory of 64 Mb and Beyond", *Technical Digest of IEEE International Electron Devices Meeting*, pp. 907–910, December 2004.

[21] S. Lai et al., "Current Status of Phase Change Memory and Its Future", *Technical Digest of IEEE International Electron Devices Meeting*, pp. 255–258, December 2003.