VRenderZERO+

DATA SHEET

Release Version 1.31

Document Release
2003/08/21

Document Revision History

The following table provides the revision history for this manual. This history includes technical content revisions only and not stylistic or grammatical changes.

VRenderZERO+Reference Manual Revision History Rev. 1.2,

	Revision Location	Revision
1.	Introduction	PERIPHRALS - 27 channel priority interrupt controller / - 4Ch. 16Bit counter for timer
2.1	Package Dimention	Location move
3.2.2	Configuration Register	Add Table Description
3.2.5	Watch Dog Timer Count Register	Add Table Description
3.5.3	Interrupt sources	Table Edit
3.5.4.3	Interrupt Enable Register	Add Text
3.5.4.4	Interrupt Status Register	Add Text
3.6.2	UART Channel 0/1 Status Register	Table Edit
3.7.2	Timer Count Register	Add Text
3.7.6	PWM Period Register	Add Text
3.11.13	CRT Display Start Address 0 Register	Table Edit
3.11.17	Light Pen 0Y Register	Table Edit
3.11.19	Light Pen 1Y Register	TABLE EDIT
3.13.2	PLL Program Register	Add Text
3.14.1	TMEM/FMEM Type Control Register	Table Edit
3.14.2	FMEM Timing Control Register	Table Edit
3.14.3	TMEM Timing Control Register	Table Edit
4.	BOUNDARY SCAN FOR VRenderZERO+	Add Chapter

VRenderZERO+Reference Manual Revision History Rev. 1.21,

3.11.20	Light Pen Input Control Register (LIGHTC)	Error Edit
3.4.2.1	DMA0 Control Register(DMAC0)	Hold -> Direction
3.4.2.5	DMA1 Control Register(DMAC1)	Hold –> Direction

VRenderZERO+Reference Manual Revision History Rev. 1.30,

3.5.3	Interrupt Sources Register	Table Edit
3.5.4.1	Interrupt Mode Register	Table Edit
3.5.4.3	Interrupt Enable Register	Table Edit
3.5.4.4	Interrupt Status Register	Table Edit
3.11.2	Timing Control Register	Table Edit
3.11.5	Horizontal Sync From Porch Register	Table Edit
3.11.12	CRT Display Start Address 0 Register	Table Edit
3.11.13	CRT Display Start Address 1 Register	Table Edit
3.11.16	Light Pen 0 Y Register	Table Edit
3.11.18	Light Pen 1 Y Register	Table Edit
3.16.3.1	Master Command Register	Add Description
3.16.3.2	Status Register	Add Description
3.16.3.3	Invalidate Cache without Copy Back Register	Add Description
3.16.3.4	Memory Bank Data Register	Add Description

VRenderZERO+Reference Manual Revision History Rev. 1.31,

3.5.3	Interrupt Sources Register	Table Edit
3.5.4.3	Interrupt Enable Register	Table Edit
3.5.4.4	Interrupt Status Register	Table Edit

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1. Introduction

MagicEyes's VRenderZERO+ chip is designed to provide a cost-effective and high performance 2D rendering solution for game and entertainment market. VRenderZERO+ chip integrates 32bit EISC(SE3208) microprocessor, high-performance 2D graphic accelerator, Wavetable synthesizer, peripheral functions. So you can make cost-effective and powerful game and entertainment machine by using VRenderZERO+, memory and little more parts. VRenderZERO+ BD1 includes the all most of game system, RTC (Real time Clock), battery backed memory, light pen interface, joystick interface, stereo audio amp, etc.

CPU
- High performance EISC core SE3208
- 4KByte unified cache
- Normal operation speed 40MHz

GRAPHIC CONTROLLER
- Frame buffer color format : 16bit
- Peak performance : 80MPixel/sec with zoom/shadow/texture
- Drawing performance 1100 objects/sec @80MHz, 320x240 resolution, 256x256 texture size
- Enhanced graphic function
- Zoom in/out, rotation, alpha-blending compatible with MS-DirectX
- 2x2/4x4 ordered dither functions
- Normal operation speed 80MHz

DISPLAY CONTROLLER
- Support standard video format : NTSC, PAL
- Support interaced / non-interaced format
- Support internal video display mode and external video & overlay mode
- Support external sync detection
- Resolution up to 1024 pixel horizontally.

Audio Processing
- Output format : 16bit, ~44.1KHz, stereo PCM
- 32 output channel.
- Individual volume control
- Individual panning control
- Individual 4 stage envelope control (Attack, decay, sustain, release)
- Wave format
  8bit : u-Law compressed format,
  8/16bit PCM
- Supports programmable reverb effects.

MEMORY MANAGEMENT
- RAM : SRAM, Sync DRAM support for main memory
- ROM : 8/16 bit support for system program
- External Chip Selection with flexible data bus width and access time
- Individual panning control

PERIPHRALS
- 2 channel DMA
- 27 channel priority interrupt controller
- 4Ch. 16Bit counter for timer
- 1Ch. SIO
- 2Ch. UART with 16*8bit FIFO
- 32 PIO (Peripheral Input Output)
- 1Ch. PWM
- 2Ch. light pen interface

INTEGRATION
- Embedded triple DAC
- Embedded PLL

PROCESS
- 0.35um CMOS VLSI
- 3.3Volt operation
- 208 Pin QFP package

2. Block Diagram & Pin Description

2.1 Package Dimension

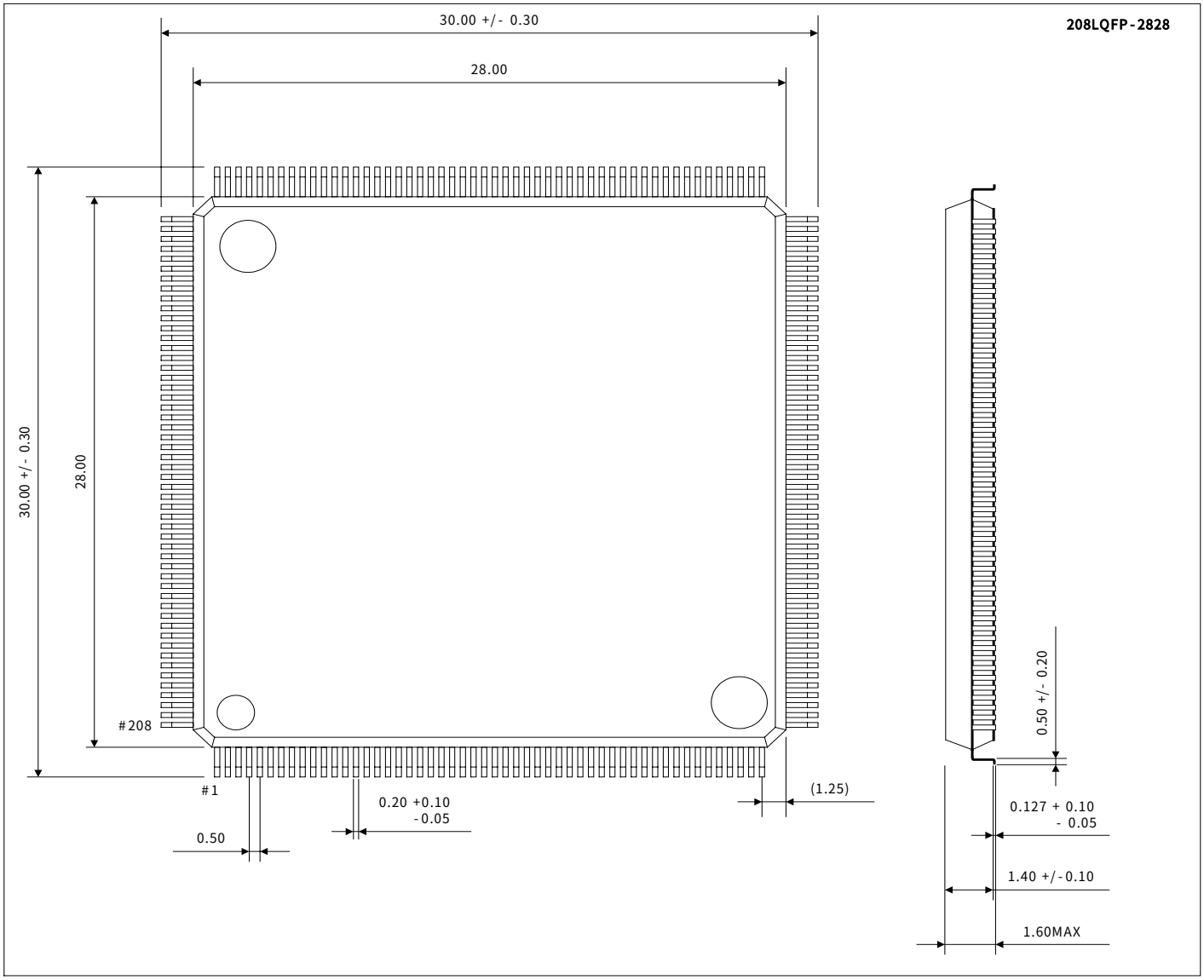


Figure 2.1-1 Package Dimension

2.2 Package Diagram

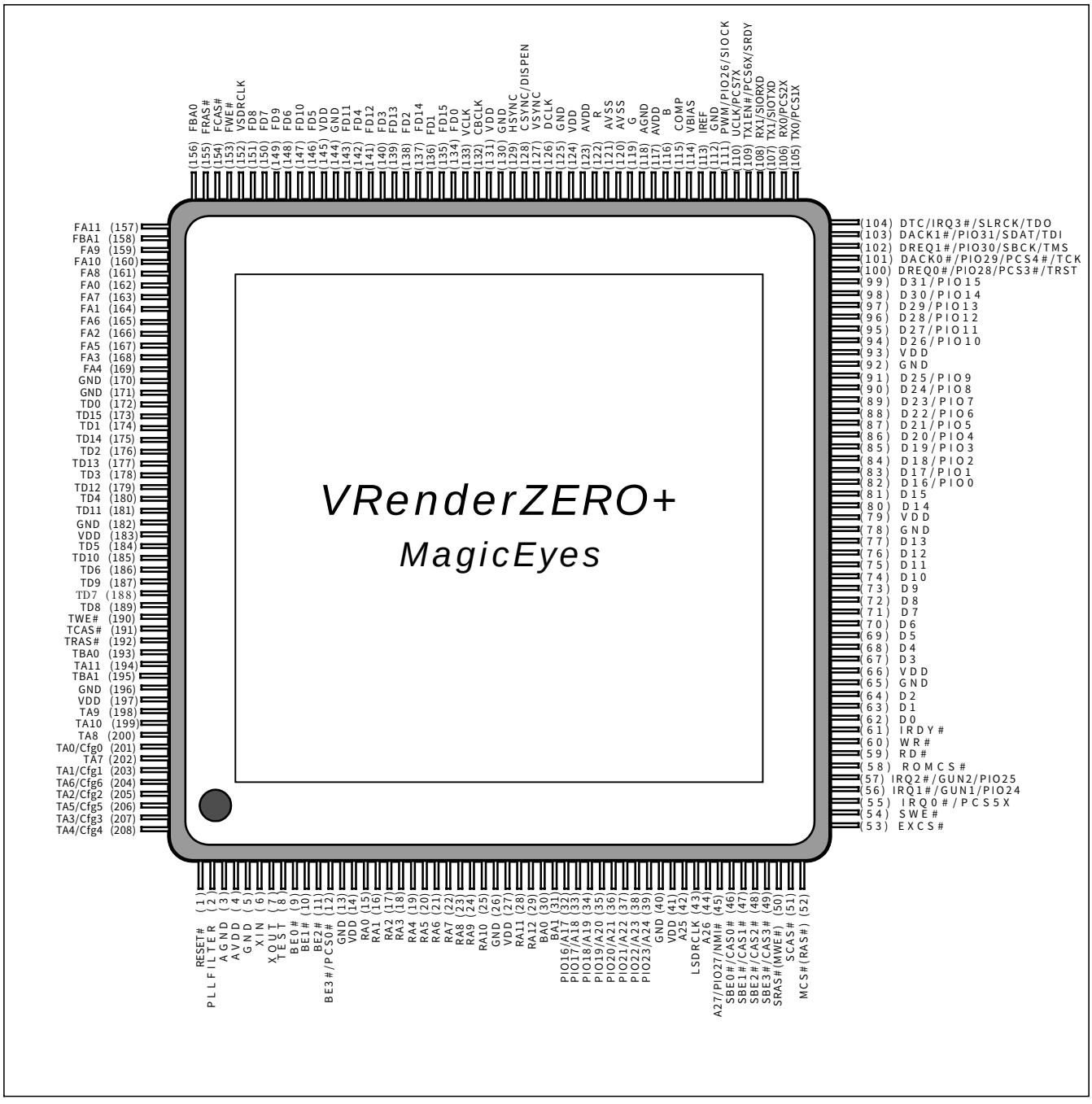


Figure 2.2-1 Pin Diagram

2.3 Pin Information

Bottom		RIGHT		TOP		LEFT	
No	Pin Name	No	Pin Name	No	Pin Name	No	Pin Name
1(I)	RESETX(t,s)	53(O)	EXCSX/HALTX (j)	105(O)	TX0/PCS1X(j)	157(O)	FA11
2(O)	PLLFILTER	54(B)	SWEX/INTX (t,j)	106(B)	RX0/PCS2X(t,j)	158(O)	FBA1
3	AGND(VSSA,VBBA)	55(B)	IRQ0X/INTAX/PCS5X (t,s,u,j)	107(O)	TX1/SIOTXD(j)	159(O)	FA9
4	AVDD(VDDD,VDDA)	56(B)	IRQ1X/GUN1/PIO24 (t,s,u,j)	108(I)	RX1/SIORXD(t,j)	160(O)	FA10
5	GND(VSSD)	57(B)	IRQ2X/GUN2/PIO25 (t,s,u,j)	109(B)	TX1EN/PCS6X/SRDY(t,j)	161(O)	FA8
6(I)	XIN	58(O)	ROMCSX /AC_OUT (j)	110(B)	UCLK/PCS7X(t,j)	162(O)	FA0
7(O)	XOUT	59(O)	RDX / DC_OUT (j)	111(B)	PWM/PIO26/SCK(t,j)	163(O)	FA7
8(I)	TEST(t)	60(O)	WRX / cmpout (j)	112	GND(VSSO)	164(O)	FA1
9(O)	BE0X(A0) (j)	61(I)	IRDYX(t,j)	113(I)	IREF	165(O)	FA6
10(O)	BE1X (j)	62(B)	D0(t,j)	114(I)	VBIAS	166(O)	FA2
11(O)	BE2X(A1) (j)	63(B)	D1(t,j)	115(O)	COMP	167(O)	FA5
12(O)	BE3X/PCS0X (j)	64(B)	D2(t,j)	116(O)	Blue	168(O)	FA3
13	GND	65	GND	117	AVDD(VDDA)	169(O)	FA4
14	VDDO	66	VDDI	118	AGND(VSSA)	170	GND(VSSO)
15(O)	RA0(A2)	67(B)	D3(t,j)	119(O)	Green	171	GND(VSSO)
16(O)	RA1(A3) (j)	68(B)	D4(t,j)	120	AGND(VBBA)	172(B)	TD0/dactdr0
17(O)	RA2(A4) (j)	69(B)	D5(t,j)	121	AGND(VSSA)	173(B)	TD15/dactdg7
18(O)	RA3(A5) (j)	70(B)	D6(t,j)	122(O)	Red	174(B)	TD1/dactdr1
19(O)	RA4(A6) (j)	71(B)	D7(t,j)	123	AVDD(VDDA)	175(B)	TD14/dactdg6
20(O)	RA5(A7) (j)	72(B)	D8(t,j)	124	VDD(VDDD)	176(B)	TD2/dactdr2
21(O)	RA6(A8) (j)	73(B)	D9(t,j)	125	GND(VSSD)	177(B)	TD13/dactdg5
22(O)	RA7(A9) (j)	74(B)	D10(t,j)	126(O)	DCLK	178(B)	TD3/dactdr3
23(O)	RA8(A10) (j)	75(B)	D11(t,j)	127(O)	VSYNC	179(B)	TD12/dactdg4
24(O)	RA9(A11) (j)	76(B)	D12(t,j)	128(O)	CSYNC/DISPEN	180(B)	TD4/dactdr4
25(O)	RA10(A12) (j)	77(B)	D13(t,j)	129(O)	HSYNC	181(B)	TD11/dactdg3
26	GND	78	GND	130	GND	182	GND
27	VDDP	79	VDDI	131	VDDP	183	VDDO
28(O)	RA11(A13) (j)	80(B)	D14(t,j)	132(O)	CBCLK	184(B)	TD5/dactdr5
29(O)	RA12(A14) (j)	81(B)	D15(t,j)	133(I)	VCLK (t)	185(B)	TD10/dactdg2
30(O)	BA0(A15) (j)	82(B)	D16 /PIO0/pixel0(t,j)	134(B)	FD0/dactdb0	186(B)	TD6/dactdr6
31(O)	BA1(A16) (j)	83(B)	D17 /PIO1/pixel1(t,j)	135(B)	FD15	187(B)	TD9/dactdg1
32(B)	A17/PIO16/cta0 (t,j)	84(B)	D18 /PIO2/pixel2(t,j)	136(B)	FD1/dactdb1	188(B)	TD7/dactdr7
33(B)	A18/PIO17/cta1 (t,j)	85(B)	D19 /PIO3/pixel3(t,j)	137(B)	FD14	189(B)	TD8/dactdg0
34(B)	A19/PIO18/cta2 (t,j)	86(B)	D20 /PIO4/pixel4(t,j)	138(B)	FD2/dactdb2	190(O)	TWEX
35(B)	A20/PIO19/cta3 (t,j)	87(B)	D21 /PIO5/pixel5(t,j)	139(B)	FD13	191(O)	TCASX
36(B)	A21/PIO20/cta4 (t,j)	88(B)	D22 /PIO6/pixel6(t,j)	140(B)	FD3/dactdb3	192(O)	TRASX
37(B)	A22/PIO21/cta5 (t,j)	89(B)	D23 /PIO7/pixel7(t,j)	141(B)	FD12	193(O)	TBA0
38(B)	A23/PIO22/cta6 (t,j)	90(B)	D24 /PIO8/pixel8(t,j)	142(B)	FD4/dactdb4	194(O)	TA11
39(B)	A24/PIO23/cta7 (t,j)	91(B)	D25 /PIO9/pixel9(t,j)	143(B)	FD11	195(O)	TBA1
40	GND	92	GND	144	GND	196	GND
41	VDDO	93	VDDO	145	VDDO	197	VDDI
42(B)	A25/cta8 (t,j)	94(B)	D26 /PIO10/pixel10(t,j)	146(B)	FD5/dactdb5	198(O)	TA9
43(O)	LSDRCLK (j)	95(B)	D27 /PIO11/pixel11(t,j)	147(B)	FD10	199(O)	TA10
44(B)	A26/cta9 (t,j) = ctwrx	96(B)	D28 /PIO12/pixel12(t,j)	148(B)	FD6/dactdb6	200(O)	TA8
45(B)	A27/PIO27/ctrdx/NMIX (t,j)	97(B)	D29 /PIO13/pixel13(t,j)	149(B)	FD9/dactclk	201(B)	TA0/Cfg0
46(O)	A28/DQM0(SBE0X)/CAS0X (j)	98(B)	D30 /PIO14/pixel14(t,j)	150(B)	FD7/dactdb7	202(O)	TA7
47(O)	A29/DQM1(SBE1X)/CAS1X (j)	99(B)	D31 /PIO15/pixel15(t,j)	151(B)	FD8/dactpd	203(B)	TA1/Cfg1
48(O)	A30/DQM2(SBE2X)/CAS2X (j)	100(B)	DREQ0X/PIO28/PCS3X/TRST (t,s)	152(O)	VSDRCLK	204(B)	TA6/Cfg6
49(O)	A31/DQM3(SBE3X)/CAS3X (j)	101(B)	DACK0X/PIO29/PCS4X/TCK(t)	153(O)	FWEX	205(B)	TA2/Cfg2
50(B)	SRASX(MWE0X)/HOLDX (t,j)	102(B)	DREQ1X/PIO30/SBCK/TMS(t, s)	154(O)	FCASX	206(B)	TA5/Cfg5
51(O)	SCASX/HLDAX (j)	103(B)	DACK1X/PIO31/SDAT/TDI(t)	155(O)	FRASX	207(B)	TA3/Cfg3
52(O)	MCS0X(RASX) (j)	104(B)	DTC/IRQ3X/SLRCK/TDO(t,s)	156(O)	FBA0	208(B)	TA4/Cfg4

Nand Tree Test : IRDYX (start point) -->IRQ2X(end point) -->RDX (DC_OUT monitor) , ROMCSX(AC_OUT monitor)
Index (s) is Schmitt PAD
Index (u) is Pull-up PAD
Index (J) is a pin which can use JTAG

I : input pin O : Output pin B : Bi-directional pin P : VDD pin G : VSS pin TTLS : TTL type Schmitt Od : Open Drain type

Pkg pin No.	PIN Name	I/O	Entity name	Output drive current	Pull up/down	I/O interface
1	RESETX	I	PTIS	-	Null	TTLS
2	PLLFILTER	O	POAR50_BB		Null	Analog
3	GND	G	VSSA,VBBA	-	-	-
4	VDD	P	VDDD,VDDA	-	-	-
5	GND	G	VSSD	-	-	-
6	XIN	I	PSOSCM2		Null	Oscillator Pad
7	XOUT	O	PSOSCM2		Null	Oscillator Pad
8	TEST	I	PTIC	-	Null	TTL
9	A1_0[0] / BE[0]	O	POB4	4mA	Null	TTL
10	BEX1 / BE[1]	O	POB4	4mA	Null	TTL
11	A1_0[1]/ BE[2]	O	POB4	4mA	Null	TTL
12	PCS0X / BE[3]	O	POB4	4mA	Null	TTL
13	GND	G	VSSO			
14	VDD	P	VDD3O			
15	RA12_0[0]	O	POB4	4mA	Null	TTL
16	RA12_0[1]	O	POB4	4mA	Null	TTL
17	RA12_0[2]	O	POB4	4mA	Null	TTL
18	RA12_0[3]	O	POB4	4mA	Null	TTL
19	RA12_0[4]	O	POB4	4mA	Null	TTL
20	RA12_0[5]	O	POB4	4mA	Null	TTL
21	RA12_0[6]	O	POB4	4mA	Null	TTL
22	RA12_0[7]	O	POB4	4mA	Null	TTL
23	RA12_0[8]	O	POB4	4mA	Null	TTL
24	RA12_0[9]	O	POB4	4mA	Null	TTL
25	RA12_0[10]	O	POB4	4mA	Null	TTL
26	GND	G	VSSP	-	-	-
27	VDD	P	VDD3P	-	-	-
28	RA12_0[11]	O	POB4	4mA	Null	TTL
29	RA12_0[12]	O	POB4	4mA	Null	TTL
30	BA1_0[0]	O	POB4	4mA	Null	TTL
31	BA1_0[1]	O	POB4	4mA	Null	TTL
32	PIO16 / A17	B	PTBCT4	4mA	Null	TTL
33	PIO17 / A18	B	PTBCT4	4mA	Null	TTL
34	PIO18 / A19	B	PTBCT4	4mA	Null	TTL
35	PIO19 / A20	B	PTBCT4	4mA	Null	TTL
36	PIO20 / A21	B	PTBCT4	4mA	Null	TTL
37	PIO21 / A22	B	PTBCT4	4mA	Null	TTL
38	PIO22 / A23	B	PTBCT4	4mA	Null	TTL
39	PIO23 / A24	B	PTBCT4	4mA	Null	TTL
40	GND	G	VSSO	-	-	-
41	VDD	P	VDD3O	-	-	-
42	A25	B	PTBCT4	4mA	Null	TTL
43	LSDRCLK	O	POB4	4mA	Null	TTL
44	A26	B	PTBCT4	4mA	Null	TTL
45	A27 / PIO27/NMI#	B	PTBCT4	4mA	Null	TTL
46	A28/DQM0(SBE0#)/CAS0#	O	POB4	4mA	Null	TTL
47	A29/DQM1(SBE1#)/CAS1#	O	POB4	4mA	Null	TTL
48	A30/DQM2(SBE2#)/CAS2#	O	POB4	4mA	Null	TTL
49	A31/DQM3(SBE3#)/CAS3#	O	POB4	4mA	Null	TTL
50	SRAS# / MWE# (HOLD#)	B	PTBCT4	4mA	Null	TTL
51	SCAS# (HLDA#)	O	POB4	4mA	Null	TTL
52	MCS# / RAS#	O	POB4	4mA	Null	TTL
53	EXCS# (HALT#)	O	POB4	4mA	Null	TTL
54	SWE# (INT#)	B	PTBCT4	4mA	Null	TTL
55	IRQ0# / PCS5# (INTA#)	B	PTBSUT4	4mA	Null	TTLS,Up
56	IRQ1# / GUN1 / PIO24	B	PTBSUT4	4mA	Null	TTLS,Up
57	IRQ2# / GUN2 / PIO25	B	PTBSUT4	4mA	Null	TTLS,UP
58	ROMCS#	O	POB4	4mA	Null	TTL
59	RD#	O	POB4	4mA	Null	TTL
60	WR#	O	POB4	4mA	Null	TTL
61	IRDY#	I	PITC	-	Null	TTL
62	D[0]	B	PTBCT4	4mA	Null	TTL

63	D[1]	B	PTBCT4	4mA	Null	TTL
64	D[2]	B	PTBCT4	4mA	Null	TTL
65	GND	G	VSSI	-	-	-
66	VDD	P	VDDI	-	-	-
67	D[3]	B	PTBCT4	4mA	Null	TTL
68	D[4]	B	PTBCT4	4mA	Null	TTL
69	D[5]	B	PTBCT4	4mA	Null	TTL
70	D[6]	B	PTBCT4	4mA	Null	TTL
71	D[7]	B	PTBCT4	4mA	Null	TTL
72	D[8]	B	PTBCT4	4mA	Null	TTL
73	D[9]	B	PTBCT4	4mA	Null	TTL
74	D[10]	B	PTBCT4	4mA	Null	TTL
75	D[11]	B	PTBCT4	4mA	Null	TTL
76	D[12]	B	PTBCT4	4mA	Null	TTL
77	D[13]	B	PTBCT4	4mA	Null	TTL
78	GND	G	VSSI	-	-	-
79	VDD	P	VDD3I	-	-	-
80	D[14]	B	PTBCT4	4mA	Null	TTL
81	D[15]	B	PTBCT4	4mA	Null	TTL
82	D[16] / PIO0	B	PTBCT4	4mA	Null	TTL
83	D[17] / PIO1	B	PTBCT4	4mA	Null	TTL
84	D[18]/PIO2	B	PTBCT4	4mA	Null	TTL
85	D[19]/PIO3	B	PTBCT4	-	-	-
86	D[20]/PIO4	B	PTBCT4	4mA	Null	TTL
87	D[21]/PIO5	B	PTBCT4	-	-	-
88	D[22]/PIO6	B	PTBCT4	4mA	Null	TTL
89	D[23]/PIO7	B	PTBCT4	4mA	Null	TTL
90	D[24]/PIO8	B	PTBCT4	4mA	Null	TTL
91	D[25]/PIO9	B	PTBCT4		Null	TTL
92	GND	G	VSSO	-	-	-
93	VDD	P	VDD3O	-	-	-
94	D[26]/PIO10	B	PTBCT4	4mA	Null	TTL
95	D[27]/PIO11	B	PTBCT4	4mA	Null	TTL
96	D[28]/PIO12	B	PTBCT4	4mA	Null	TTL
97	D[29]/PIO13	B	PTBCT4	4mA	Null	TTL
98	D[30]/PIO14	B	PTBCT4	4mA	Null	TTL
99	D[31]/PIO15	B	PTBCT4	4mA	Null	TTL
100	DREQ0# / PIO28 / PCS3#/TRST	B	PTBST4	4mA	Null	TTLS
101	DACK0# / PIO29 / PCS4# / TCK	B	PTBCT4	4mA	Null	TTL
102	DREQ1# / PIO30 / SBCK / TMS	B	PTBST4	4mA	Null	TTLS
103	DACK1# / PIO31 / SDAT / TDI	B	PTBCT4	4mA	Null	TTL
104	DTC / IRQ3 / SLRCK /TDO	B	PTBST4	4mA	Null	TTLS
105	TX0 / PCS1#	O	POB4	4mA	Null	TTL
106	RX0 / PCS2#	B	PTBCT4	4mA-	Null	TTL
107	TX1 / SIOTXD	O	POB4	4mA	Null	TTL
108	RX1 / SIORXD	I	PTIC	-	Null	TTL
109	TX1EN# / PCS6# / SRDY	B	PTBCT4	4mA	Null	TTL
110	UCLK / PCS7#	B	PTBCT4	4mA	Null	TTL
111	PWM / PIO26/SCK	B	PTBCT4	4mA	Null	TTL
112	GND	G	VSSO	-	-	-
113	IREF	I	PIA_BB	-	-	Analog
114	VBIAS	I	PIA_BB	-	-	Analog
115	COMP	O	POA_BB	-	-	Analog
116	B	O	POA_BB	-	-	Analog
117	VDD	P	VDDA	-	-	Analog Power
118	GND	G	VSSA	-	-	Analog GND
119	G	O	POA_BB	-	-	Analog
120	GND	G	VBBA	-	-	Analog GND
121	GND	G	VSSA	-	-	Analog GND
122	R	O	POA_BB	-	-	Analog
123	VDD	P	VDDA	-	-	Analog Power
124	VDD	P	VDDD	-	-	Digital Power
125	GND	G	VSSD	-	-	Digital GND

126	DCLK	B	POB4	4mA	Null	TTL
127	VSYNC	O	POB4	4mA	Null	TTL
128	CSYNC/DISPEN	O	POB4	4mA	Null	TTL
129	HSYNC	O	POB4	4mA	Null	TTL
130	GND	G	VSSP	-	-	-
131	VDD	P	VDD3P	-	-	-
132	CBCLK	O	POB4	4mA	Null	TTL
133	VCLK	I	PTIC	-	Null	TTL
134	FD[0]	B	PBCT4	4mA	Null	TTL
135	FD[15]	B	PBCT4	4mA	Null	TTL
136	FD[1]	B	PBCT4	4mA	Null	TTL
137	FD[14]	B	PBCT4	4mA	Null	TTL
138	FD[2]	B	PBCT4	4mA	Null	TTL
139	FD[13]	B	PBCT4	4mA	Null	TTL
140	FD[3]	B	PBCT4	4mA	Null	TTL
141	FD[12]	B	PBCT4	4mA	Null;	TTL
142	FD[4]	B	PBCT4	4mA	Null	TTL
143	FD[11]	B	PBCT4	4mA	Null	TTL
144	GND	G	VSSO	-	-	-
145	VDD	P	VDD3O	-	-	-
146	FD[5]	B	PBCT4	4mA	Null	TTL
147	FD[10]	B	PBCT4	4mA	Null	TTL
148	FD[6]	B	PBCT4	4mA	Null	TTL
149	FD[9]	B	PBCT4	4mA	Null	TTL
150	FD[7]	B	PBCT4	4mA	Null	TTL
151	FD[8]	B	PBCT4	4mA	Null	TTL
152	VSDRCLK	O	POB4	4mA	Null	TTL
153	FWEX	O	POB4	4mA	Null	TTL
154	FCASX	O	POB4	4mA	Null	TTL
155	FRASX	O	POB4	4mA	Null	TTL
156	FBA[0]	O	POB4	4mA	Null	TTL
157	FA[11]	O	POB4	4mA	Null	TTL
158	FBA[1]	O	POB4	4mA	Null	TTL
159	FA[9]	O	POB4	4mA	Null	TTL
160	FA[10]	O	POB4	4mA	Null	TTL
161	FA[8]	O	POB4	4mA	Null	TTL
162	FA[0]	O	POB4	4mA	Null	TTL
163	FA[7]	O	POB4	4mA	Null	TTL
164	FA[1]	O	POB4	4mA	Null	TTL
165	FA[6]	O	POB4	4mA	Null	TTL
166	FA[2]	O	POB4	4mA	Null	TTL
167	FA[5]	O	POB4	4mA	Null	TTL
168	FA[3]	O	POB4	4mA	Null	TTL
169	FA[4]	O	POB4	4mA	Null	TTL
170	GND	G	VSSO	-	-	-
171	GND	G	VSSO	-	-	-
172	TD[0]	B	PBCT4	4mA	Null	TTL
173	TD[15]	B	PBCT4	4mA	Null	TTL
174	TD[1]	B	PBCT4	4mA	Null	TTL
175	TD[14]	B	PBCT4	4mA	Null	TTL
176	TD[2]	B	PBCT4	4mA	-	-
177	TD[13]	B	PBCT4	4mA	Null	TTL
178	TD[3]	B	PBCT4	4mA	Null	TTL
179	TD[12]	B	PBCT4	4mA	Null	TTL
180	TD[4]	B	PBCT4	4mA	Null	TTL
181	TD[11]	B	PBCT4	4mA	Null	TTL
182	GND	G	VSSO	-	-	-
183	VDD	P	VDD3O	-	-	-
184	TD[5]	B	PBCT4	4mA	Null	TTL
185	TD[10]	B	PBCT4	4mA	Null	TTL
186	TD[6]	B	PBCT4	4mA	Null	TTL
187	TD[9]	B	PBCT4	4mA	Null	TTL
188	TD[7]	B	PBCT4	4mA	Null	TTL
189	TD[8]	B	PBCT4	4mA	Null	TTL
190	TWEX	O	POB4	4mA	Null	TTL
191	TCASX	O	POB4	4mA	Null	TTL

192	TRASX	O	POB4	4mA	Null	TTL
193	TBA[0]	O	POB4	4mA	Null	TTL
194	TA[11]	O	POB4	4mA	Null	TTL
195	TBA[1]	O	POB4	4mA	Null	TTL
196	GND	G	VSSI	-	-	-
197	VDD	P	VDD3I	-	-	-
198	TA[9]	O	POB4	4mA	Null	TTL
199	TA[10]	O	POB4	4mA	Null	TTL
200	TA[8]	O	POB4	4mA	Null	TTL
201	TA[0]/Cfg0	B	PBCT4	4mA	Null	TTL
202	TA[7]	O	POB4	4mA	Null	TTL
203	TA[1]/Cfg1	B	PBCT4	4mA	Null	TTL
204	TA[6]/Cfg6	B	PBCT4	4mA	Null	TTL
205	TA[2]/Cfg2	B	PBCT4	4mA	Null	TTL
206	TA[5]/Cfg5	B	PBCT4	4mA	Null	TTL
207	TA[3]/Cfg3	B	PBCT4	4mA	Null	TTL
208	TA[4]/Cfg4	B	PBCT4	4mA	Null	TTL

2.4 Pin Description

Pin name	I/O	Pin No.	Description
RESET#	I	1	System reset. Low active signal.
PLLFILTER	O	2	Internal PLL'' filter output
XIN	I	6	Source of Internal/External Clock. When Internal PLL is used, 14.318MHz is entered. When External Clock is used 2 times the frequency of CPU Clock is entered.
XOUT	O	7	OSC Cell's Output. XIN is output right after going through feedback at OSC PAD
TEST	I	8	It is always connected to Ground. It makes Test Mode enable/disable. This signal is used for chip test and is normally tied to ground and executed as Normal mode. If it is to be used as Test Mode, TEST PIN must be High and is controlled by other Configuration Pin's Pullup/Pulldown..
BE0# (A0)	O	9	CPU byte enable bit 0. If ROM or IO's data bus width is 8bit, it means system address bit 0. If ROM or IO's data bus width is 16/32 bit, it means byte enable [0] .
BE1#	O	10	CPU byte enable bit 1.
BE2# (A1)	O	11	CPU byte enable bit 2. If ROM or IO's data bus width is 16bit or 8bit, it means system address bit 1. Or those are 32bit , it means byte enable 2.
BE3# / PCS0#	O	12	CPU byte enable bit 3 or Peripheral chip select 0. We can select it by altering the Pin mux control register bit 3.
A[16:2] (BA[1:0], RA[12:0])	O	31~28, 25~15	Local address bit[16:2] BA[1:0] is used a Bank select address for SDRAM. RA[12:0] is used as address bits for DRAM,
A[24:17] / PIO[23:16]	B	39~32	Local address bits [24:17] or Peripheral IO port. Users can determine the function of the pin by programming the corresponding bit of Pin mux control register.
A[26:25]	O	44, 42	Local address bit [26:25]
A[27] / PIO[27]/ NMI#	B	45	Local address bit [27] or Peripheral IO port bit 27 or CPU's Non-maskable Interrupt Users can determine the function of the pin by programming the corresponding bit of Pin mux control register.
D[15:0]	B	81~80, 77~67, 64~62	Local data bus lower 16 bit
D[31:16] / PIO[15:0]	B	99~94, 91~82	CPU data bus upper 16 bits or Programmable IO port. When this pin is used as a bit of IO port for external device, local memory data bus width cannot be 32-bit bus to avoid data conflict. Local memory bus width is set as 16bit by power on configuration , these pins' PIO[15:0]function are automatically changed.
EXCS#	O	53	Chip select signal for the external expansion ROM. It can be active between Address 0x0500_0000 and 0x0fff_ffff
MCS# (RAS#)/	O	52	If Local memory is SDRAM/SRAM mode, this pin is used as memory chip select. And if Local memory is edo-DRAM mode, this pin is used as row address strobe signal.
SBE[3:0]# (DQM[3:0]#) (CAS[3:0]#)	O	49~46	If users use SRAM mode as Local memory, this pin is used as SRAM data byte enable signal. In SDRAM mode, these operate as DQM signals. In edo-DRAM mode, these operate as column address strobe signal.
SRAS# (MWE#)	O	50	If users use SDRAM mode as Local memory, this pin is used as row address strobe signal. And if users use EDO-DRAM mode as Local memory, this pin is used as memory write enable signal.

SCAS#	O	51	If users used SDRAM as Local memory, this pin is used as column address strobe signal.
SWE#	O	54	If users use SDRAM as Local memory, this pin is used memory write enable signal
LSDRCLK	O	43	Local memory SDRAM clock.
ROMCS#	O	58	Local boot ROM chip select.
IRQ0# / PCS5#	B	55	Used Peripheral chip select 5 , Can be changed by Pin mux control register bit 3 External Interrupt request 0 from external devices.
IRQ1# / GUN1/ PIO[24]	B	56	External interrupt request0 signal come from external device Strobe input signal in order to obtain Light Pen 1. Can be used as a Peripheral IO port bit 24
IRQ2# / GUN2/ PIO[25]	B	57	External interrupt request1signal com from external device. Strobe input signal in order to obtain Light Pen 2 Can be used as a Peripheral IO port bit 25
RD#	O	59	CPU read command signal.
WR#	O	60	CPU write command signal.
IRDY#	I	61	CPU ready signal. It informs the end of RD# or WR# command execution. CPU is in wait state until this signal is activated after those commands.
DREQ0# / PIO[28] / PCS3#/ TRST	B	100	DMA channel request signal for 0 VRenderZERO+can receive 2 channel, DMA request form outside. among them. It is Request for DMA 1 channel. Can be used as peripheral IO port bit 28 Peripheral chip select signal . Can be controlled by Pin mux control register When It is JTAG Mode It is a TRST Using JTAG for high speed download This time, It is not controlled by pin mux control register
DACK0# / PIO[29] / PCS4#/ TCK	B	101	DMA channel 0 acknowledge Signal It is used as a Peripheral IO port bit 29 Peripheral chip select signal. Controlled by Pin mux control register When It is JTAG Mode It is a TCK Using JTAG for high speed download This time, It is not controlled by pin mux control register
DREQ1# / PIO[30] / SBCK/ TMS	B	102	It is request signal for DMA channel 1 Used as a Peripheral IO port bit 30 Serial DAC interface signal for sound. Controlled by Pin mux control register When It is JTAG Mode It is a TMS Using JTAG for high speed download This time, It is not controlled by pin mux control register.
DACK1# / PIO[31] / SDAT/ TDI	B	103	DMA channel 1 acknowledge signal Used as a Peripheral IO port bit 31 Serial DAC interface signal for sound. Controlled by Pin mux control register When It is JTAG Mode It is a TDI Using JTAG for high speed download This time, It is not controlled by pin mux control register
DTC / IRQ[3] / SLRCK/ TDO	B	104	As a DMA terminal count signal, after DMA data was transferred completely, come to active. As programming each bit of Pin mux control register It is used as a External interrupt request is a signal which come from external device Serial DAC interface signal for sound. When It is JTAG Mode, It is a TDO Using JTAG for high speed download This time, It is not controlled by pin mux control register
TX0 / PCS1#	O	105	UART channel 0 transmit data or Peripheral chip select signal . Controlled by Pin mux control register.
RX0 / PCS2#	B	106	UART channel 0 receive data or Peripheral chip select signal. Controlled by Pin mux control register
TX1 / SIOTXD	O	107	Can be used as a UART channel 1 transmit data or Synchrous IO's Transmit Data , controlled by Pin mux control register

RX1 / SIORXD	I	108	Can be used as a UART channel 1 receive data or Synchrous IO's Receive Data. Controlled by Pin mux control register
TX1EN# / PCS6# / SRDY	B	109	UART channel 1 transmit data enable. While Data is transferred , come to active Can be used as a External interrupt request, It is signal which come from External device Controlled by Pin mux control register
UCLK / PCS[7]#	B	110	The external UART clock input. Users can used internal UART's operation clock by receiving from external devices. It is a Peripheral chip select signal and can be controlled by Pin mux control register.
PWM / PIO[26]/ SIOCK	B	111	Can be used as a Pulse width modulation output signal. Used as a Peripheral IO port bit 26. and Clock signal of Synchrous IO Clock signal. Controlled by Pin mux control register
FD[15:0]	B	135,137, 139,141, 143,147, 149,151, 150,148, 146,142, 140,138, 136,134	Video/Graphic frame memory data bus.
FBA[1:0]	O	158,156	SDRAM bank address for Frame memory
FA[11:0]	O	157,160, 159,161, 163,165, 167,169, 168,166, 164,162	SDRAM address bus for Frame memory
FRAS#	O	155	SDRAM row address strobe signal for Frame memory
FCAS#	O	154	SDRAM column address strobe signal for Frame memory
FWE#	O	153	SDRAM write enable signal for Frame memory
TD[15:0]	B	173,175, 177,179, 181,185, 187,189, 188,186, 184,180, 178,176, 174,172	Video/Graphic texture memory data bus.
TBA[1:0]	O	195,193	SDRAM bank address for Texture memory
TA[11:7]	O	194,199, 198,200, 202	SDRAM address bit[11:7] for Texture memory
TA[6:0] (CFG[6:0])	B	204,206, 208,207, 205,203, 201	SDRAM address bit[6:0] for Texture memory These pins are pulled up or pulled down to set configuration register. When power on reset signal이 becomes inactive, pull-up / pull-down values are latched in configuration register. Texture memory를 위한 SDRAM address bus.
TRAS#	O	192	SDRAM row address strobe signal for Texture memory
TCAS#	O	191	SDRAM column address strobe signal for Texture memory
TWE#	O	190	SDRAM write enable signal for Texture memory
VSDRCLK	O	152	SDRAM clock for Texture/Frame memory
DCLK	O	126	Dot Clock for Video Output
VSYNC	O	127	Vertical Sync output

CSYNC/ DISPEN	O	128	Composite Sync Video data is displayed on screen according to this sync signal. When using TFT LCD on outside, Dispen is used as a Data Enable signal to LCD Controller .In fact, Dispen is faster to become active high about 2 pixel than displayed pixel .
HSYNC	O	129	Horizontal Sync It is horizontal sync signal of video data. When this signal happens, new lines start to be displayed from the left hand side of the screen
CBCLK	O	132	Color Burst Clock. It is Color sync signal of Video data. If Color sync is not fitted, color changes when the two video signals are overlaid
VCLK	I	133	It is a basic Clock, which displays Video Data on screen as a Video Clock.
R	O	122	DAC Analog Red Data
G	O	119	DAC Analog Green Data
B	O	116	DAC Analog Blue Data
IREF	I	113	DAC Reference Voltage.
VBIAS	I	114	DAC Bias Voltage
COMP	I	115	DAC Compare Output
AVDD	P	4,117 123	Analog Power
AGND	G	3,118 120,121	Analog Ground
VDD	P	14,27,41 ,66,79, 93,124, 131,145, 183,197	Power
GND	G	5,13,26, 40,65,78 ,92,112, 125,130, 144,170, 171,182, 196	Ground

* Remark : (B) is pin direction in case of external CPU mode.

3. Register Description

3.1 Memory Map

The SE3208 CPU Core of VRenderZERO+ has 32bit address and can access up to 4Gbytes address region.

VRenderZERO+ memory area is allocated like the table shown below.

Address Range	Description	Remark
0000 0000h ~ 00FF FFFFh	Local ROM	ROMCS#
0100 0000h ~ 01FF FFFFh	Peripheral Device & Registers	
0100 0000h ~ 010F FFFFh	Peripheral Device 0	PCS0#
0110 0000h ~ 011F FFFFh	Peripheral Device 1	PCS1#
0120 0000h ~ 012F FFFFh	Peripheral Device 2	PCS2#
0130 0000h ~ 013F FFFFh	Peripheral Device 3	PCS3#
0140 0000h ~ 014F FFFFh	Peripheral Device 4	PCS4#
0150 0000h ~ 015F FFFFh	Peripheral Device 5	PCS5#
0160 0000h ~ 016F FFFFh	Peripheral Device 6	PCS6#
0170 0000h ~ 017F FFFFh	Peripheral Device 7	PCS7#
0180 0000h ~ 01FF FFFFh	Internal Register	Below Table
0200 0000h ~ 02FF FFFFh	Local DRAM/SRAM	
0300 0000h ~ 037F FFFFh	Graphic/MISC Controller Region	16bit access only
0380 0000h ~ 03FF FFFFh	Texture Buffer Memory	Max. 8Mbytes Texture Mem.
0400 0000h ~ 047F FFFFh	Frame Buffer Memory	Max. 8Mbytes Frame Mem
0480 0000h ~ 04FF FFFFh	Sound Engine Registers	16bit access only
0500 0000h ~ 05FF FFFFh	Expansion ROM	EXCS#
1000 0000h ~ 0FFF FFFFh	Reserved for Feature Use	

Table 3-1 VRenderZERO+ Memory Map

The Register Region at 01800000h is allocated to 1Kbyte per 1 block. The CPU accesses its region with memory mapped I/O as below.

Offset Address	Internal Peripheral	Remark
0180 0000h	System / General	
0180 0400h	Local Memory Controller	ROM, DRAM, SRAM
0180 0800h	DMA	2 Channel
0180 0C00h	Interrupt Controller	27 Channel
0180 1000h	UART	2 Channel
0180 1400h	Timer & Counter	4 Channel
0180 1800h	Pulse Width Modulation	1 Channel
0180 1C00h	Reserved	
0180 2000h	PIO (PORT)	32 PORT
0180 2400h	Peripheral Chip Select	8 Chip Select
0180 2800h	SIO	1 Channel
0180 2C00h	Reserved	
0180 3000h	Reserved	
0180 3400h	CRT Controller	
0180 3800h	Reserved	
0180 3C00h	Reserved	
0180 4000h	RAMDAC & PLL	3 DAC
0180 4400h	Reserved	Built in Memory Addressing
0180 FFFFh	Reserved	

Table 3-2. Internal Peripheral Register Map

The address boundary is 400h(1024Byte).

3.2 System / General Register

OVERVIEW

Determine the register value which is used for main clock, local ROM, watch dog timer, and PIO pin. Each value can be configured by hardware to meet various system configuration.

Configuration Register(CFGR)

Select configuration of Main clock, Local ROM data bus width, and Local memory bus width. The data bus width of Local ROM should be set to one of 8-bit, 16-bit, 32-bit. Because the Local ROM is booting ROM, the bus width of Local ROM must be determined before the first ROM access. The mode of Main clock should be set to one of 2'b00, 2'b01, 2'b10, 2'b11.The logic level of TA[7:0] is determined by the pull-up/pull-down register tied to Vcc or GND.

System Control Register(SYSCON)

Select configuration of Expansion ROM data bus width, Flame memory internal command wait cycle, register internal command wait cycle, external read/write command wait cycle.

Watch-DOG Timer

VRenderZERO+ watch-dog timer is used to resume the controller operation when it is disturbed by malfunctions such as noise and system errors.

Pin Mux Control Register

According to setting of local memory bus width of configuration register, D[31:16] of external data bus pin can be used as PIO pin. That is, only in case of using 16bit as local memory data bus, PIO0~PIO15 will be used.

3.2.1 System ID Register (SYSID)

Address : 0180 0000h

Bit	R/W	Description	Default Value
31:16	R	Reserved.	00h
15: 8	R	Device ID	0ah
7 : 0	R	Revision Number	00h

3.2.2 Configuration Register (CFGR)

Address : 0180 0004h

Bit	R/W	Description	Default Value
31: 7	R	Reserved.	-
6	R	Main Clock Select 0 : External Clock (Disable PLL) 1 : Internal PLL Clock	TA[6]
5 : 3	R	Reserved for Chip Test Mode : Normally you have to pull down. Select Test Mode (When TEST pin is active state.) JTAG test mode is a high speed download mode and is not support boundary scan. That is, Frame/texture memory I/F pin don't make as a JTAG 000 : CPU Stand Alone 100 : Counter Test mode 001 : Cache Tag Memory 101 : pll test mode (50Mhz output) 010 : Internal DAC 11x : JTAG Mode 011 : Cache data Momory	TA[5:3]
2 : 1	R	Local ROM Data Bus Width 00 : 8Bit 01 : 16Bit 1x : 32bit	TA[2:1
0	R	Local Memory Bus Width . 0 : 16Bit 1 : 32Bit	TA[0]

3.2.3 System Control Register (SYSCON)

Address : 0180 0008h

Bit	R/W	Description	Default Value
31 : 10	R	Reserved	000h
9 : 8	RW	Expansion ROM Data Bus Width 00 : 8Bit 01 : 16Bit 1x : 32bit	00b
7 : 6	RW	Frame Memory Internal Command Cycle Wait Control 00 : 2 Clk 01 : 3 Clk 10 : 4 Clk 11 : 5 Clk	11b
5 : 4	RW	Register Internal Command Cycle Wait Control 00 : 2 Clk 01 : 3 Clk 10 : 4 Clk 11 : 5 Clk	11b
3	R	Reserved	0
2 : 0	RW	External Read/Write Command Cycle Wait Control (Pin RD# / WR#) 000 : 2 Clk 100 : 10 Clk 001 : 4 Clk 101 : 12 Clk 010 : 6 Clk 110 : 14 Clk 011 : 8 Clk 111 : 16 Clk	111b

3.2.4 Watch Dog Timer Control Register (WDCON)

Address : 0180 0010h

Bit	R/W	Description	Default Value
31 : 4	R	Reserved.	0000h
4	R	Watch Dog Reset Status. When CPU reads WDCON, WDCNT is cleared. 0 : Normal 1 : Watch Dog Reset	0
3 : 1	RW	Pre-scale Factor Selection 000 : 128 cycle 001 : 256 cycle 010 : 512 cycle 011 : 1024 cycle 100 : 2048 cycle 101 : 4096 cycle 110 : 8192 cycle 111 : 16384 cycle It can select the clock which is divided by Pre-scaler counter's standard Cycle. It is a clock which has the maximum 256 Cycle and it can count WDCNT	111b
0	RW	Watch Dog Timer Enable / Disable 0 : Disable Timer 1 : Enable Timer	0

3.2.5 Watch Dog Timer Count Register (WDCNT)

Address : 0180 0014h

Bit	R/W	Description	Default Value
31:16	R	Reserved.	0000h
15: 0	RW	Watch Dog Timer Count Value. Watch dog timer can down from the value expressed hear. And when it reaches 0, it causes Reset. This register value shows the watchdog counter value, so users can know the current count value. The pulse width of reset signal generated by the watch dog depends on the Presale Factor Selection Value.	FFFFh

3.2.6 Pin Mux Control Register 1

Address : 0180 0018h

Bit	R/W	Description	Default Value
31 : 21	RW	Reserved.	0
20		0 : A24 1 : PIO23	
19		0 : A23 1 : PIO22	
18		0 : A22 1 : PIO21	
17		0 : A21 1 : PIO20	
16		0 : A20 1 : PIO19	
15		0 : A19 1 : PIO18	
14		0 : A18 1 : PIO17	
13		0 : A17 1 : PIO16	
12		Reserved	
11:10		00 : A27 01 : PIO27 1x : NMIX	
9:8		00 : PCS3# 01 : PIO28 1x : DREQ0	
7:6		00 : PCS4# 01 : PIO29 1x : DACK0	
5:4		00 : SBCK 01 : PIO30 1x : DREQ1	
3:2		00 : SDAT 01 : PIO31 1x : DACK1	
1:0		00 : SLRCK 01 : IRQ3 1x : DTC	

Data Bus pin or D[31:16] can be used as PIO by setting local memory bus width of configuration register. That is, when only lower 16bit of local memory data bus is used, D[31:16] is replaced with PIO0~PIO15.

3.2.7 Pin Mux Control Register 2

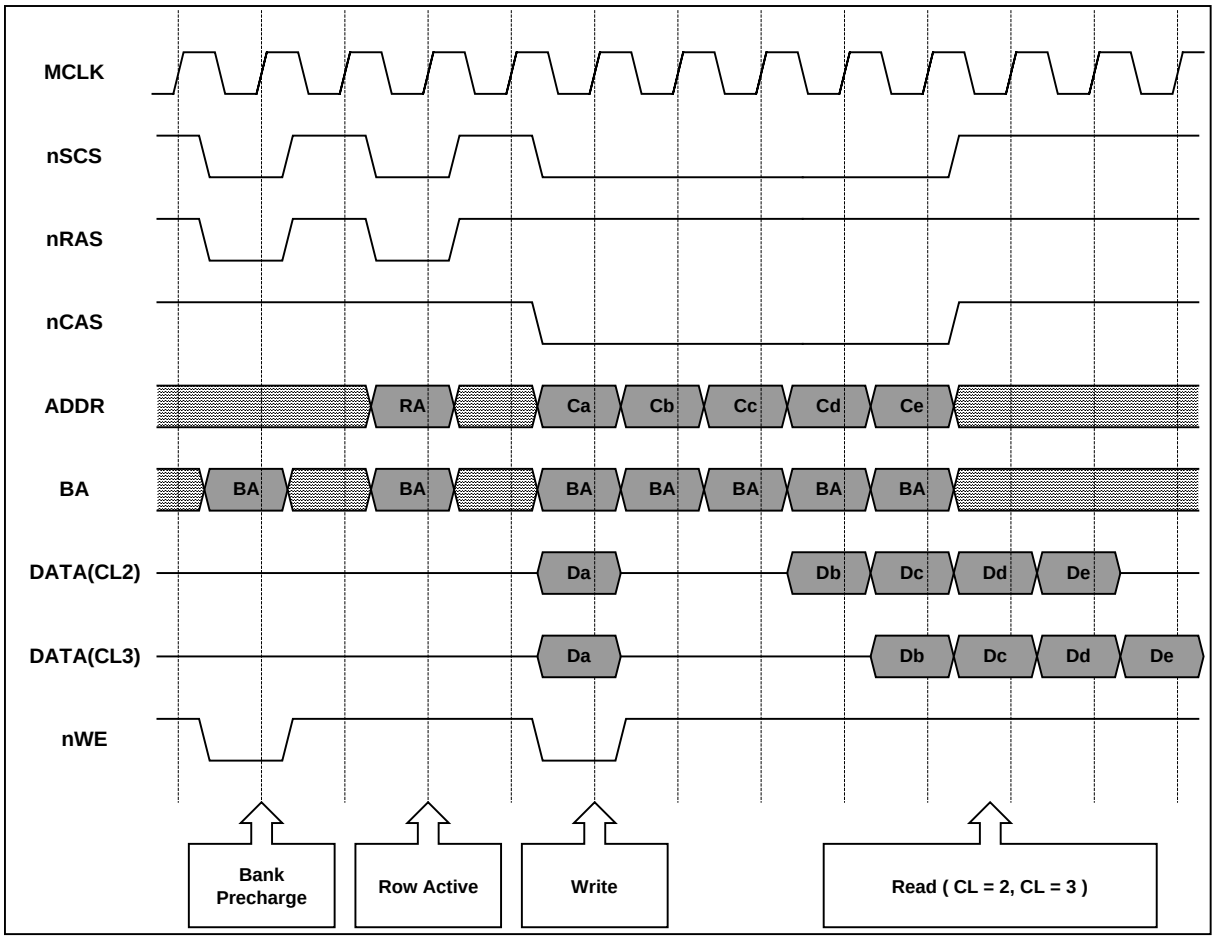
Address : 0180 001Ch

Bit	R/W	Description	Default Value
31 : 22	RW	Reserved.	0
21		0 : MWE#(SRAS#), SCAS# / 1 : HOLD# HLDA#	
20		Reserved	
19		0 : SWE# / 1 : INT#	
18:17		00 : PCS5# / 01 : INTA / 1x : IRQ0#	
16		0 : EXCS# / 1 : HALT#	
15:14		Reserved / Reserved	
13:12		00 : PWM / 01 : PIO26 / 1x : SIOCK	
11:10		00 : IRQ1 / 01 : PIO24 / 1x : GUN1	
9:8		00 : IRQ2 / 01 : PIO25 / 1x : GUN2	
7		0 : TX0 / 1 : PCS1#	
6		0 : RX0 / 1 : PCS2#	
5		0 : TX1 / 1 : SIOTX	
4		0 : RX1 / 1 : SIORX	
3:2		00 : TX1EN / 01 : PCS6# / 1x : SRDY	
1		0: UCLK / 1 : PCS7#	
0		0 : BE3# / 1 : PCS0#	

3.3 Local Memory Control Registers

OVERVIEW

Set up parameters relevant to local ROM and local DRAM. The following <Figure 3.3-1> is the case of using SDRAM with local DRAM. At the below figure, RAS pre-charge time and RAS to CAS delay time are all each 2 cycles. In case of SDRAM, writing is made immediately but reading is made after delay of set CAS latency(CL). In case of DATA(CL2), data comes after the delay of 3 cycles.



<Figure 3.3-1 VRenderZERO+ SDRAM Timing Diagram>

3.3.1 Local ROM Control Register (LROMC)

Address : 0180 0400h

Bit	R/W	Description	Default Value
31:16	R	Reserved.	0
15:12	RW	Local Memory SDRAM Clock Control (LSDRCLK) 0000 : clk1x 0001 : clk1x + 2ns 0010 : clk1x + 4ns 0011 : clk1x + 6ns 0100 : clk1x + 8ns 0101 : clk1x + 10ns 0110 : clk1x + 12ns 0111 : clk1x + 14ns 1000 : Inverted clk1x 1001 : Inverted clk1x + 2ns 1010 : Inverted clk1x + 4ns 1011 : Inverted clk1x + 6ns 1100 : Inverted clk1x + 8ns 1101 : Inverted clk1x + 10ns 1110 : Inverted clk1x + 12ns 1111 : Inverted clk1x + 14ns	0000
11:8	RW	Frame/Texture Memory SDRAM Clock Control(VSDRCLK) 0000 : clk2x 0001 : clk2x + 1ns 0010 : clk2x + 2ns 0011 : clk2x + 3ns 0100 : clk2x + 4ns 0101 : clk2x + 5ns 0110 : clk2x + 6ns 0111 : clk2x + 7ns 1000 : Inverted clk2x 1001 : Inverted clk2x + 1ns 1010 : Inverted clk2x + 2ns 1011 : Inverted clk2x + 3ns 1100 : Inverted clk2x + 4ns 1101 : Inverted clk2x + 5ns 1110 : Inverted clk2x + 6ns 1111 : Inverted clk2x + 7ns	0000
7	RW	Select the decode method of LROMCS Pin. 0 : Decode address and RD# 1 : Decode address only	1
6 : 3	R	Reserved.	0
2:0	RW	LROMCS wait state 000 : 2 Clk 001 : 4 Clk 010 : 6 Clk 011 : 8 Clk 100 : 10 Clk 101 : 12 Clk 110 : 14 Clk 111 : 16 Clk	111b

3.3.2 Local DRAM Control Register (LDCON)

Address : 0180 0408h

Bit	R/W	Description	Default Value
31 : 25	R	Reserved	0000h
24	RW	Local Memory Control Reset 0 : Active 1 : Software Reset While this bit is 1, memory state machine is reset, When it becomes active, there happens mode setting cycle in case of SDRAM	0
23 : 20	R	Reserved.	
19 : 18	RW	Row Address Line Number (SDRAM Only) 00 : 11 01 : 12 10 : 13 11 : Reserved.	00b
17 : 16	RW	Column Address Line Number (FP,EDO DRAM / SDRAM) 00 : 8 01 : 9 10 : 10 11 : 11 SDRAM Mode : 2'b11 is invalid.	00b
15 : 14	R	Reserved.	0
13	RW	Internal Read Data Latch Timing Control for FP DRAM 0 : Normal 1 : 1 Clk Delay	0
12 : 11	RW	RAS to CAS Delay. 00 : 1 Clk 01 : 2 Clk 1x : 3 Clk	01b
10 : 9	RW	RAS Pre-charge Time 00 : 1 Clk 01 : 2 Clk 10 : 3 Clk 11 : 4 Clk	11b
8	RW	*SDRAM Mode* : CAS Latency 0 : 2 Clk 1 : 3 Clk *EDO/FP DRAM Mode* : CAS Pre-charge Time 0 : 1 Clk 1 : 2 Clk	1
7 : 6	RW	*EDO/FP DRAM Mode* : CAS Active Pulse Width Time 0x : 1 Clk 1x : 2 Clk *SRAM Mode* : SRAM Command Width Time 00 : 1 Clk 01 : 2 Clk 10 : 3 Clk 11 : 4 Clk	11b
5 : 4	RW	*SDRAM Mode* : RAS Cycle Time after Auto-refresh Command 00 : 3 Clk 01 : 4 Clk 10 : 5 Clk 11 : 6 Clk *EDO/FP DRAM Mode* : RAS Pulse Width for CBR Refresh 00 : 2 Clk 01 : 3 Clk 10 : 4 Clk 11 : 5 Clk	11b
3	RW	Refresh Cycle Period 0 : 15.6 usec 1 : 31.2 usec	0
2	RW	Number of Refresh Cycle / Period 0 : 1 Cycle 1 : 2 Cycle	1
1 : 0	RW	Local Memory Type. 00 : SRAM 01 : EDO DRAM 10 : Fast Page DRAM 11 : Sync DRAM	00b

3.4 DMA

3.4.1 OVERVIEW

The VRenderZERO+ has 2 channel DMA Controllers. The each channel can transfer data to and from main memory in response to requests generated by I/O device or software.

(Caution) Because texture and frame memory support only 16bits/32bits Interface, texture and frame memory do not support 8bits transfer mode when using DMA. If using 8bits transfer mode, the transferred data is not be guaranteed.

If memory address at where data to transfer is saved is assigned to DMASA (Source Address), memory address to be transferred is assigned to DMADA(Destination Address) and the number of times to transfer data is assigned to DMATC (DMA Transfer Count), one DMA transfer is executed and DMATC value decreases by 1 whenever DMA request happens on the outside. Accordingly, as CPU reads DMATC value, you can check success of whole DMA transfer. Furthermore, if you set up interrupt controller, you can run appropriate interrupt service routine.

In case of memory to memory transfer, please pull-up or pull-down external DMA request pin according to the status of DMAPOL to make it active always.

3.4.2 Registers

3.4.2.1 DMA0 Control Register (DMAC0)

***Address* : 0x0180 0800**

Bit	R/W	Description	Default Value
31:11	R	Reserved.	0b
10	R/W	**DMAEN0 :** DMA0 Enable 0: Disable 1: Enable DMA Operation	0b
9	R/W	**DMAPOL0** : DMA0 Request Polarity 0: Active High 1: Active Low	0b
8	R/W	**DMAWREN0** : DMASA0, DMADA0 Register and Internal Counter Simultaneous Write Enable 0: Register Only 1: Register and Counter	1b
7:6	R/W	**DMAMODE0** : DMA Transfer Mode 0x:: Single Transfer 10:: Repeat Data Transfer with Counter Reloading 11: Repeat Data Transfer with Counter and Address Reloading	00b
5	R/W	**DMASHOLD0** : Source Address Hold 0: Increase/Decrease Address 1: Fix Address	0b
4	R/W	**SMASDIR0** : Source Address Direction 0: Increase Address 1: Decrease Address	0b
3	R/W	**DMADHOLD0** : Destination Address Hold 0: Increase/Decrease Address 1: Fix Address	0b
2	R/W	**DMADIR0** : Destination Address Direction 0: Increase Address 1: Decrease Address	0b
1:0	R/W	**DMATRWIDTH0** : Data Transfer Width 00: 8bit, 01:16bit 1x:32bit	00b

DMA0EN controls DMA channel on/off

DMA0POL determines whether DMA controller runs at low DMA request signal input from DMA controller or runs at high. In case of memory to memory transfer, if external DMAREQ pin is pulled up, DMAPOL should be set to active high.

DMA0WREN

DMAMODE determines DMA operation method. After single transfer mode is transferred at the same number of times with that of set transferring times into DMATC (DMA Transfer Counter Register), single transfer mode is the mode to complete DMA operation. When DMATC becomes to 0 in case of 10b (Repeat Data Transfer with Counter Reloading) Setting, it makes to reload automatically to the first DMATC loading data and to transfer continuously. When the transfer is completed to the number of times same to that of set transferring times into DMATC value in case of 11b (Repeat Data Transfer with Counter and Address Reloading), it makes to load the first set address and counter value

DMASHOLD decides whether to increase/decrease source address or keep it whenever one DMA transfer is completed.

DMASDIR decides the increased/decreased direction of source address.

DMDHOLD decides whether to increase/decrease source address or keep it whenever one DMA transfer is completed..

DMASDIR decides the increased/decreased direction of source address.

DMATRWIDTH determines to transfer at which bit when transferring through DMA.

3.4.2.2 DMA0 Source Address Register (DMASA0)

***Address* : 0x0180 0804**

Bit	R/W	Description	Default Value
31:0	R/W	**DMASA0 :** DMA0 Source Address A[31:0]	00000000h

DMASA determines source address to save data to be transferred through DMA. When specifying source address, if DMATRWIDTH is 32bits, DMASA[1:0] is disregarded. If DMATRWIDTH is 16bits, DMASA[0] is disregarded internally

3.4.2.3 DMA0 Destination Address Register (DMADA0)

Address : **0x0180 0808**

Bit	R/W	Description	Default Value
31:0	R/W	**DMADA0 :** DMA0 Destination Address A[31:0]	00000000h

DMADA specifies destination address to save data to be transferred through DMA. When specifying destination address, if DMATRWIDTH is 32bits, DMASA[1:0] is disregarded. If DMATRWIDTH is 16bits, DMASA[0] is disregarded internally

3.4.2.4 DMA0 Transfer Count Register (DMATC0)

Address : **0x0180 080C**

Bit	R/W	Description	Default Value
31:24	R	Reserved.	0b
23:0	R/W	**DMATC0 :** DMA0 Transfer Count Register The Value is decrease by 1 every DMA transfer – one read and write. Data transfer width makes no difference.	00000h

DMATC specifies the number of DMA transfer times DMA and is decreased by 1 whenever DMA transfer is completed regardless of DMATRWIDTH. So, this value is not the number of byte to be transferred but the number of DMA transfer times

3.4.2.5 DMA1 Control Register (DMAC1)

Address : 0x0180 0810

Bit	R/W	Description	Default Value
31:11	R	Reserved.	0
10	R/W	**DMAEN1** : DMA1 Enable 0: Disable 1: Enable DMA Operation	0
9	R/W	**DMAPOL1** : DMA1 Request Polarity 0: Active High 1: Active Low	0
8	R/W	**DMAWREN1** : DMASA1, DMADA1 Register and Internal Counter Simultaneous Write Enable 0: Register Only 1: Register and Counter	1b
7:6	R/W	**DMAMODE1** : DMA Transfer Mode 0x:: Single Transfer 10:: Repeat Data Transfer with Counter Reloading 11: Repeat Data Transfer with Counter and Address Reloading	00b
5	R/W	**DMASHOLD1** : Source Address Hold 0: Increase/Decrease Address 1: Fix Address	0b
4	R/W	**SMASDIR1** : Source Address Direction 0: Increase Address 1: Decrease Address	0b
3	R/W	**DMADHOLD1** : Destination Address Hold 0: Increase/Decrease Address 1: Fix Address	0b
2	R/W	**DMADDIR1** : Destination Address Direction 0: Increase Address 1: Decrease Address	0b
1:0	R/W	**DMAWIDTH1** : Data Transfer Width 00: 8bit, 01:16bit 1x:32bit	00b

3.4.2.6 DMA1 Source Address Register (DMASA1)

Address : 0x0180 0814

Bit	R/W	Description	Default Value
31:0	R/W	**DMASA1 :** DMA1 Source Address A[31:0]	00000000h

3.4.2.7 DMA1 Destination Address Register (DMADA1)

Address : 0x0180 0818

Bit	R/W	Description	Default Value
31:0	R/W	**DMADA1 :** DMA1 Destination Address A[31:0]	00000000h

3.4.2.8 DMA1 Transfer Count Register (DMATC1)

Address : 0x0180 081C

Bit	R/W	Description	Default Value
31:24	R	Reserved.	0
23:0	R/W	**DMATC1 :** DMA1 Transfer Count Register The Value is decrease by 1 every DMA transfer – one read and write. Data transfer width makes no difference	00000h

3.5 Interrupt Controller

3.5.1 OVERVIEW

The interrupt controller in VRenderZERO+ receives 27 interrupts source. Among them, 20 sources are provided from internal peripherals like the DMA, Display controller, UART, etc.

The role of interrupt controller is to ask for the IRQ interrupt request to the EISC Core after making the arbitration process when there are multiple interrupt requests from internal peripherals and external interrupt request pins.

3.5.2 Operation

First, you set the corresponding enable bit in interrupt enable register to indicate the interrupt to be enabled. If an interrupt enable bit of INTEN is 1, the interrupt will be serviced normally.

After that, when the interrupt occurs, the corresponding interrupt service routine will wake up. Its service routine gets information containing which devices generate interrupt by reading INTST. To handle next interrupt event, you must set an interrupt clear vector value of INTVEC to clear interrupt pending registers.

3.5.3 Interrupt Sources

Among 27 interrupt sources, 20 sources are provided form interrupt controller. Eight interrupts request are provided form external pins. Vector 0 is the highest priority like below.

Vector No.	Description	Remar
26	PWM Interrupt (Lower Priority)	Interrupt is accepted by the order of the priorities. And the value of Vector is issued by Data Bus in the active range of CPU's INTA#
25	Reserved	
24	Video Vertical Blank Interrupt	
23	Reserved	
22	Reserved	
21	Reserved	
20	Reserved	
19	Reserved	
18	UART Channel 1 Transmit Interrupt	
17	UART Channel 1 Receive Interrupt	
16	UART Channel 1 Error Interrupt	
15	UART Channel 0 Transmit Interrupt	
14	UART Channel 0 Receive Interrupt	
13	UART Channel 0 Error Interrupt	
12	External IRQ3	
11	External IRQ2	
10	Timer 3 Interrupt	
9	Timer 2 Interrupt	
8	DMA 1 Interrupt	
7	DMA 0 Interrupt	
6	External IRQ1	
5	External IRQ0	
4	Reserved	
3	SIO Interrupt	
2	Wavetable Synthesizer interrupt	
1	Timer 1 Interrupt	
0	Timer 0 Interrupt (Highest Priority)	

3.5.4 REGISTER

3.5.4.1 Interrupt Mode Register (INTMODE)

Address : 0x0180 0C00

Bit	R/W	Description	Default Value
31:16	R	Reserved.	0
15:12	RW	Reserved.	Fh
11:8	R/W	**EINTTRIG** : External IRQ3~IRQ0 Trigger Mode 0: Level Trigger 1: Edge Trigger	Fh
7:4	R/W	Reserved.	Fh
3:0	R/W	**EINTPOL** : External IRQ7~IRQ0 Active State 0: Active Low 1: Active high	FFh

EINTTRIG decides trigger mode of external interrupt pin. If EINTTRIG is set to 0 and IRQPin is changed to the level decided by EINTPOL, interrupt happens. If IRQPin is kept to the level that interrupt happens, the next interrupt will happen though clearing interrupt pending register by INTCLR and finishing interrupt service routine.

EINTPOL decides polarity of external interrupt pin.

EINTPOL=1, EINTTRIG=1 : Interrupt happens when IRQPin is on rising-edge (From low to high).

EINTPOL=1, EINTTRIG=0 : Interrupt happens when IRQPin is on high.

3.5.4.2 Interrupt Vector Register (INTVEC)

Address : 0x0180 0C04

Bit	R/W	Description	Default Value
31:11	R	Reserved.	0
10:8	R/W	**INTVMSB** : interrupt Vector High 3 Bit, Programmable Bits.	000b
7:5	R	Reserved.	0
4:0	W	**INTCLR** : Interrupt Clear Vector Value By writing the vector number of each interrupt at the end of service routine, the latched interrupt request is cleared and CPU can accept next interrupt request.	0

I**NTCLR** carries out the function to clear interrupt pending register. You can clear the value by writing the number of interrupt you desire to clear.

3.5.4.3 Interrupt Enable Register (INTEN)

These are the mask bits for interrupt sources and perform interrupt enable/disable function. When the mask bit is 0, interrupt becomes disable and interrupt becomes enable when the mask bit is 1.

Address : 0x0180 0C08

Bit	R/W	Description	Default Value
31:27	R	Reserved	00000000h
26	R/W	PWM Interrupt (Lower Priority)	
25	R/W	Reserved	
24	R/W	Video Vertical Blank Interrupt	
23	R/W	Reserved	
22	R/W	Reserved	
21	R/W	Reserved	
20	R/W	Reserved	
19	R/W	Reserved	
18	R/W	UART Channel 1 Transmit Interrupt	
17	R/W	UART Channel 1 Receive Interrupt	
16	R/W	UART Channel 1 Error Interrupt	
15	R/W	UART Channel 0 Transmit Interrupt	
14	R/W	UART Channel 0 Receive Interrupt	
13	R/W	UART Channel 0 Error Interrupt	
12	R/W	External IRQ3	
11	R/W	External IRQ2	
10	R/W	Timer 3 Interrupt	
9	R/W	Timer 2 Interrupt	
8	R/W	DMA 1 Interrupt	
7	R/W	DMA 0 Interrupt	
6	R/W	External IRQ1	
5	R/W	External IRQ0	
4	R/W	Reserved	
3	R/W	SIO Interrupt	
2	R/W	Wavetable Synthesizer interrupt	
1	R/W	Timer 1 Interrupt	
0	R/W	Timer 0 Interrupt (Highest Priority)	

Interrupt enable register is used as mask bit over interrupt source and carries out interrupt enable/disable function. If bit of appropriate interrupt is set to 1, interrupt becomes enable and If it is set to 0, interrupt becomes disable.

3.5.4.4 Interrupt Status Register (INTST)

This register shows the interrupt request status. The status bit becomes high when interrupt is occurred, and goes low when interrupt clear vector is written. In external CPU mode, this register informs which interrupts are being requested.

Address : 0x0180 0C0C

Bit	R/W	Description	Default Value
31:27	R	Reserved	00000000h
26	R/W	PWM Interrupt (Lower Priority)	
25	R/W	Reserved	
24	R/W	Video Vertical Blank Interrupt	
23	R/W	Reserved	
22	R/W	Reserved	
21	R/W	Reserved	
20	R/W	Reserved	
19	R/W	Reserved	
18	R/W	UART Channel 1 Transmit Interrupt	
17	R/W	UART Channel 1 Receive Interrupt	
16	R/W	UART Channel 1 Error Interrupt	
15	R/W	UART Channel 0 Transmit Interrupt	
14	R/W	UART Channel 0 Receive Interrupt	
13	R/W	UART Channel 0 Error Interrupt	
12	R/W	External IRQ3	
11	R/W	External IRQ2	
10	R/W	Timer 3 Interrupt	
9	R/W	Timer 2 Interrupt	
8	R/W	DMA 1 Interrupt	
7	R/W	DMA 0 Interrupt	
6	R/W	External IRQ1	
5	R/W	External IRQ0	
4	R/W	Reserved	
3	R/W	SIO Interrupt	
2	R/W	Wavetable Synthesizer interrupt	
1	R/W	Timer 1 Interrupt	
0	R/W	Timer 0 Interrupt (Highest Priority)	

This is a status register to check whether interrupt is on pending status or not. As CPU accesses register, you can check which device to make interrupt.

To clear this value, you can write appropriate vector number to INTCLR bit of INTVEC.

3.6 UART

OVERVIEW

VRenderZERO+ UART(Universal Asynchronous Receiver and Transmitter) unit provides two independent asynchronous serial I/O(SIO) ports, each of which can operate in interrupt-based mode. In other words, UART can generate an interrupt request to transfer data between CPU and UART.

The VRenderZERO+ UART includes programmable baud-rates, one or two stop bit insertion, 7-bit or 8-bit data width and parity checking.

UART OPERATION

The following sections describe the UART operations that include data transmission, data reception.

Data Transmission

The data frame for transmission is programmable. It consists of a start bit, 7 or 8 data bits, an optional parity bit and 1-2 stop bits, which can be specified by UART Channel Control Register(UCONn). Check the value of USTATn[5], and if Tx buffer is empty input the TX data to UTXBn.

Data Reception

Like the transmission, the data frame for reception is also programmable. It consists of a start bit, 7 or 8 data bits, an optional parity bit and 1-2 stop bits, which can be specified by UART Channel Control Register(UCONn).

Baud Rate Divisor Value

TX/RX Baud Rate is calculated to following formula. Clock Source becomes internal or external clock (UCLK).

*Baud Rate = Clock Source / ((Divisor Value+1) * 16)*

Example 1) If the baud rate is 38400 bps and UCLK is 3.5795MHz, Baud Rate Divisor Value is :

Baud Rate Divisor Value = 3579500 / (38400*16) – 1 $\approx 4.8260 \approx 5$

Example 2) If the baud rate is 38400 bps and UCLK is 1.8432MHz, Baud Rate Divisor Value is :

Baud Rate Divisor Value = 1843200 / (38400*16) – 1 = 2

3.6.1 UART Channel 0/1 Control Register (UCON0 / UCON1)

Address : 0180 1000h / 0180 1020h

Bit	R/W	Description	Default Value
31: 9	R	Reserved.	0
8	RW	UART Enable 0: Disable 1: Enable	0
7	RW	Loop Back Test. 0 : Normal 1 : Loop-back Mode for Test	0
6	RW	Send Break. Break means to generate transmit data output continuously more than one frame duration at low level. 0 : Not Send Break 1 : Send Break	0
5	RW	Enable Receive Status Interrupt. Enable or disable interrupt occurrence about break or error happened during data transmit. 0 : Do not generate receive status interrupt 1 : Generate receive status interrupt	0
4	RW	Serial Clock Selection. 0 : Internal Clock 1 : External Clock (UCLK)	0
3 : 2	RW	Parity Mode. 0x : No Parity 10 : Even Parity 11 : Odd Parity	0
1	RW	Number of Stop Bit. 0 : 1 Bit per Frame 1 : 2 Bit per Frame	0
0	RW	Word Length. The number of data bit to be transmitted or received per frame. 0 : 7 Bit 1 : 8 Bit	1

3.6.2 UART Channel 0/1 Status Register (USTAT0 / USTAT1)

Address : 0180 1004h / 0180 1024h

Bit	R/W	Description	Default Value
31 : 12	R	Reserved.	0
11 : 8	R	Receive-FIFO Level. 16 Level FIFO. Receive Interrupt happens whenever the half of receive FIFO is half-empty.	0
7	R	Reserved	0
6	R	Transmitter Empty. This bit is cleared to 0 when there is no data to transmit to transmit buffer and Tx shift register is empty. 0 : Transmitter is empty. 1 : Transmitter has some data. Tx is in progress.	0
5	R	Transmit FIFO Holding Data. This bit is set automatically by writing to UTXB0(UTXB1) register. 0 : Tx Buffer is Empty. 1 : Tx Buffer has some data.	0
4	R	Receive FIFO Data Ready. This bit is cleared when FIFO is empty by reading URXB0(URXB1) register. 0 : Receive FIFO is empty. 1 : Receive FIFO has some data.	0

Bit	R/W	Description	Default Value
3	R	Break Detect. This bit is cleared automatically when reading USTAT0(USTAT1) register. 0 : Normal Operation 1 : Break Sequence Detection	0
2	R	Frame Error. This bit is cleared automatically when reading USTAT0(USTAT1) register. 0 : No Error 1 : Error	0
1	R	Parity Error. This bit is cleared automatically when reading USTAT0(USTAT1) register. 0 : No Error 1 : Error	0
0	R	Overrun Error. This bit is cleared automatically when reading USTAT0(USTAT1) register. 0 : No Error 1 : Error	0

3.6.3 UART Channel 0/1 Transmit Buffer Register (UTXB0 / UTXB1)

Address : 0180 1008h / 0180 1028h

Bit	R/W	Description	Default Value
31: 8	W	Reserved.	0
7 : 0	W	Transmit Data for UART0 / 1	

3.6.4 UART Channel 0/1 Receive Buffer Register (URXB0 / UBDR1)

Address : 0180 100Ch / 0180 102Ch

Bit	R/W	Description	Default Value
31: 8	W	Reserved.	0
7 : 0	W	Receive Data for UART0 / 1	

3.6.5 UART Channel 0/1 Baud Rate Divisor Register (UBDR0 / UBDR1)

Address : 0180 1010h / 0180 1030h

Bit	R/W	Description	Default Value
31: 16	R	Reserved.	0
15 : 0	RW	Baud Rate Divisor Value.	01

TX/RX baud rate is calculated as follows. Clock Source is internal(system clock/2) or external clock(UCLK)

*Baud Rate = Clock Source / (Divisor Value * 16)*

3.7 Timer

OVERVIEW

The VRenderZERO+ has four 16-bit timers. Each timer has its own 16-bit up-counter which is driven by the timer clock. When the up-counter reaches Timer Count Value of Timer Count Register, the timer interrupt request is generated to inform the CPU that the timer operation is completed.

FEATURE

- Four 16-bit timers
- Four 8-bit prescalers
- Support 2 mode : Continuous mode(Periodic count) or Single mode(One shot count)

Continuous mode

If timer enabled, internal counter starts up-count from 0. When count value reaches to Timer Count Value set at Timer Count Register, timer interrupt request happens. After that, it starts counting from 0 again and reiterates above process.

Single mode

If timer enabled, internal counter starts up-count from 0. When count value reaches to Timer Count Value set at Timer Count Register, timer interrupt request happens. But different from continuous mode, it does not reiterate above process.

3.7.1 Timer Control Register

Register Name	Address	Description
TMCON0	0180 1400h	Timer 0 Control Register
TMCON1	0180 1408h	Timer 1 Control Register
TMCON2	0180 1410h	Timer 2 Control Register
TMCON3	0180 1418h	Timer 3 Control Register

Bit	R/W	Description	Default Value
31 : 16	R	Reserved.	0
15 : 8	RW	Timer *n* Pre-scaler Divide Count Value This value should be more than 1.	FFh
7 : 5	R	Reserved for test mode.	0
4 : 2	R	Reserved.	0
1	RW	Timer *n* Operation Mode 0 : Single (One Shot Count) 1 : Continuous (Periodic Count)	0
0	RW	Timer *n* Enable 0 : Stop 1 : Run	0

3.7.2 Timer Count Register

Register Name	Address	Description
TMCNT0	0180 1404h	Timer 0 Count Register
TMCNT1	0180 140Ch	Timer 1 Count Register
TMCNT2	0180 1414h	Timer 2 Count Register
TMCNT3	0180 141Ch	Timer 3 Count Register

Bit	R/W	Description	Default Value
31 : 16	R	Reserved.	0
15 : 0	RW	Timer Count Value.(TCV) Timer up-counter value is compared to this register value.	000Fh

Expect Frequency (Hz) = Bus_Clock / ((PD+1)*(TCV+1))

3.7.3 Pulse Width Modulation

OVERVIEW

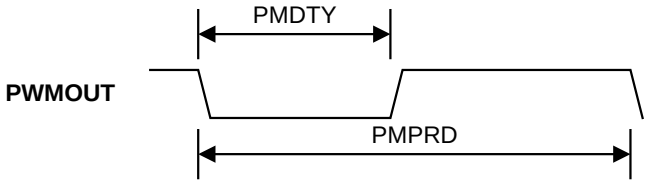
The VRenderZERO+ contains one pulse width modulator (PWM). PWM is controlled by its own set of registers, and provides a pulse width modulated signal on an external pin.

FEATURES

- Enhanced , period control through 8bit Clock divider and 16bit Period counter.
- 16bit pulse control

OPERATION

The PWM output is derived from writing the PWM Period Register (PMPRD).



PWM Up-counter value is compared to PMDTY at first. Accordingly, when counter value reaches to register value, Internal output becomes 1. This decides duty of low pulse. The value of PMPRD is applicable to total cycle and internal output becomes 0 when counter value reaches to register value. The polarity of final output is decided by PMCON Bit1

3.7.4 PWM Control Register (PMCON)

Address : 0180 1800h

Bit	R/W	Description	Default Value
31 : 16	R	Reserved.	0
15 : 8	RW	PWM Pre-scaler Divide Count 8 Bit Value	FFh
7 : 2		Reserved	
1	RW	PWM Output Polarity 0 : Negative (Start Level is High) 1 : Positive (Start Level is Low)	0
0	RW	PWM Enable 0 : Stop 1 : Run	0

3.7.5 PWM Duty Register (PMDTY)

Address : 0180 1804h

Bit	R/W	Description	Default Value
31 : 16	R	Reserved.	0
15 : 0	RW	PWM Count Value A. PWM Up-counter value is compared to register value at first. Accordingly, when counter value reaches to register value, internal output becomes 1. This decides duty of low pulse.	000Fh

3.7.6 PWM Period Register (PMPRD)

Address : 0180 1808h

Bit	R/W	Description	Default Value
31 : 16	R	Reserved.	0
15 : 0	RW	PWM Count Value B.(PCNT) PWM Up-counter value is compared to register value. This value is applicable to total cycle and internal output becomes 0 when counter value reaches to register value. Polarity of final output is decided by PMCON Bit1.	000Fh

Expect frequency (Hz) = Bus_Clock / ((PD+1)*(PCNT+1))

3.7.7 Pulse Count Register (PULCNT)

Address : 0180 180Ch

Bit	R/W	Description	Default Value
31 : 16	R	Reserved.	0
15 : 0	RW	Number of Pulse – 1	000Fh

3.8 Synchronous Serial I/O

3.8.1 SIO Control Register (SIOCON)

Address : 0180 2800h

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	0
7	RW	SIO Controller Enable 0 : Disable 1 : Enable	0
6	R	Reserved.	0
5	RW	Master / Slave Mode Select When work on as a master mode, transferring clock is generated in internal. When slave mode, clock come from master mode. 0 : Slave Mode 1 : Master Mode	
4	RW	SIO Data Transfer mode When work on DMA mode, If DTC signal come from DMA, reset happen. 0 : SIO Interrupt 1 : DMA	0
3	RW	SIO Shift operation 0 : Auto Run mode 1 : Hand-shaking Mode	0
2	RW	TX/RX Selection 0: Receive only mode 1 : Transmit/Receive mode	0
1	RW	Clock edge selection 0 : Rising Edge Clock 1 : Falling Edge Clock	0
0	RW	Data Shift Direction This bit controls whether MSB is transmitted first or LSB is transmitted first 0 : MSB First 1 : LSB First	0

3.8.2 SIO Data Register (SIODAT)

Address : 0180 2804h

Bit	R/W	Description	Default Value
31:8	R	Reserved.	0
7:0	RW	This register contains the data to be transmitted or received over the SIO	0

3.8.3 SIO Baud Rate Prescaler Register (SIOBDR)

Address : 0180 2808h

Bit	R/W	Description	Default Value
31:8	R	Reserved.	0
7:0	RW	SIO Baud Rate Prescale Value	0

Baud Rate = BCLK / (2 * SIOBDR + 2)

BCLK is a internal Bus Clock and 1/2 of PLL output. Therefore, If internal PLL frequency is 80Mhz, BCLK is 40Mhz

3.8.4 SIO Interval Count Register (SIOCNT)

Address : 0180 280Ch

Bit	R/W	Description	Default Value
31:8	R	Reserved.	0
7:0	RW	SIO Interval Counter Value	0

At Master work on as a Auto run mode, It set delay time for reception or transmission of next data

Interval Time(between 8-bit data) = BCLK / (SIOCNT + 1)

3.8.5 SIO Status Register (SIOSTAT)

Address : 0180 2810h

Bit	R/W	Description	Default Value
31 : 5	R	Reserved.	0
4	R	Present end of transfer 0 : On transfer 1 : End of transfer	0
3	R	Ready signal which come from outside device (Hand Shaking) 0 : On condition of outside device is ready 1 : On condition of outside device isn't ready	1
2	R	Transmission buffer is empty 0 : Full 1 : Empty	1
1	R	Reserved	0
0	R	If Reception buffer is full, It became set. 0 : Empty 1 : Full	0

3.9 PIO

OVERVIEW

VRenderZERO+ has 32 multi-functional input/output port pins. Each port can be easily configured by software to meet various system configuration and design requirements. If the multiplexed functions on a pin are not used, the pin can be configured as I/O ports. You must set pin mux control register before using PIO pin.

3.9.1 PIO Mode Register (PIOMOD)

In case PIO port is used as input port, it can be used as input always by setting (open collector output mode) mode control register to 1 and setting port bit of PIOLDAT register to 0.
As PIO port 0 ~ 15 shares with system data bus D[31:16], the usage is limited according to system configuration pin setting. Only in case local memory bus width is set to 16bit, Pin D[31:16] can be used as PIO.

Address : 0180 2000h

Bit	R/W	Description	Default Value
31	R / W	PIO 31 Pin Mode Control	00000000 h
30		PIO 30 Pin Mode Control	
29		PIO 29 Pin Mode Control	
28		PIO 28 Pin Mode Control	
27		PIO 27 Pin Mode Control	
26		PIO 26 Pin Mode Control	
25		PIO 25 Pin Mode Control	
24		PIO 24 Pin Mode Control	
23		PIO 23 Pin Mode Control	
22		PIO 22 Pin Mode Control	
21		PIO 21 Pin Mode Control	
20		PIO 20 Pin Mode Control	
19		PIO 19 Pin Mode Control	
18		PIO 18 Pin Mode Control	
17		PIO 17 Pin Mode Control	
16		PIO 16 Pin Mode Control	
15		PIO 15 Pin Mode Control	
14		PIO 14 Pin Mode Control	
13		PIO 13 Pin Mode Control	
12		PIO 12 Pin Mode Control	
11		PIO 11 Pin Mode Control	
10		PIO 10 Pin Mode Control	
9		PIO 9 Pin Mode Control	
8		PIO 8 Pin Mode Control	
7		PIO 7 Pin Mode Control	
6		PIO 6 Pin Mode Control	
5		PIO 5 Pin Mode Control	
4		PIO 4 Pin Mode Control	
3		PIO 3 Pin Mode Control	
2		PIO 2 Pin Mode Control	
1		PIO 1 Pin Mode Control	
0		PIO 0 Pin Mode Control 0 : Totempole Output Mode 1 : Open Collector Output Mode	

If you are willing to use PIO only as input ports, you should set Mode Control Register bits (Open Collector Output Mode), and reset the corresponding bits of PIOLDAT register. Then those ports act as input.
Because PIO0~15 are shared with system data bus D[31:16], the use of them is limited by the setting of system configuration pin. When local memory bus width is set as 16bit, pin D[31:16] can be used as PIO

3.9.2 PIO Latched Output Data Register (PIOLDAT)

Address : 0180 2004h

Bit	R/W	Description	Default Value
31 : 0	RW	PIO31 ~ PIO0 It means data to be output to external side when output mode. When open collector output mode, 0 is at output disable status and generates high-z status. 1 generates 0 at output enable status. The written value becomes to be latched and data to be written when reading this register cab be read.	0

3.9.3 PIO External Data Register (PIOEDAT)

Address : 0180 2008h

Bit	R/W	Description	Default Value
31 : 0	R	PIO31 ~ PIO0 Data to be input from PIO pin.	x

3.10 Peripheral Device Chip Select

OVERVIEW

VRenderZERO+ may has 8 peripheral devices containing 1Mbyte's address range and each range is appeared at 3.1 Memory Map (Refer to Table 3-1). To access each address range, set the value of PCS Control Register matching to address.

FEATURE

- To select the time of wait cycle (0 – 31 times)
- To select data bus width (8bit, 16bit, 32bit)
- To supply decode mode

3.10.1 PCS Control Register

Register Name	Address	Description	Pin Name
CS0CON	0180 2400h	PCS0 Control Register	
CS1CON	0180 2404h	PCS1 Control Register	
CS2CON	0180 2408h	PCS2 Control Register	
CS3CON	0180 240Ch	PCS3 Control Register	
CS4CON	0180 2410h	PCS4 Control Register	
CS5CON	0180 2414h	PCS5 Control Register	
CS6CON	0180 2418h	PCS6 Control Register	
CS7CON	0180 241Ch	PCS7 Control Register	

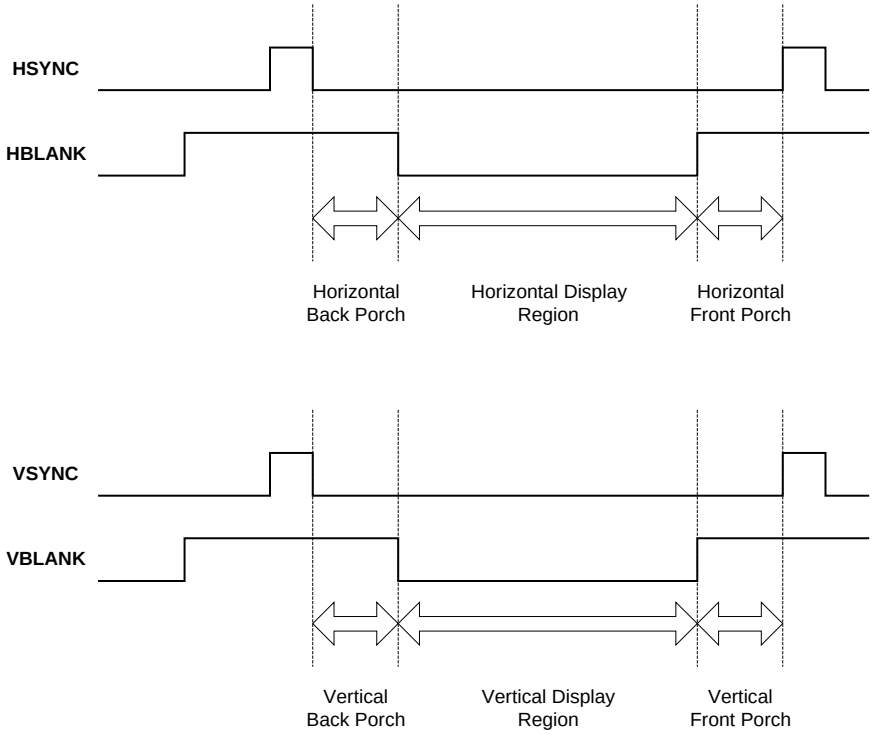
Bit	R/W	Description	Default Value
31 : 16	R	Reserved.	0
15	RW	External Ready Enable 0 : Not Use External Ready 1 : Use External Ready	0
14 : 13	R	Reserved.	0
12 : 8	RW	The Number of Wait State You can control pulse width of chip select by adding wait state from 0 to 31 cycles.	10000b
7	RW	PCSx Enable 0 : Disable 1 : Enable	0
6 : 4	R	Reserved.	0
3 : 2	RW	Data Bus Width 00 : 8Bit 01 : 16Bit 1x : 32Bit	00b
1 : 0	RW	Decode Mode 0x : Decode Address Only 10 : Decode with RD# 11 : Decode with WR#	00b

3.11 CRT Controller

OVERVIEW

Sets up various kind of basic registers which are needed to display graphic on the screen. It has parameters such as Horizontal (Vertical) sync, Horizontal (Vertical) Back Porch, Horizontal (Vertical) Front Porch, Interlace (Non-Interlace) mode, Active Display Region, Display start address, Transparency Color and Light Pen.

<Figure 3.13-1> shows video timing. The area you can draw graphic actually is Horizontal (Vertical) Display Region and register relevant to sync and blank can be set at HSWBP, HDISP, HSFP,VSBP and VDISP. Because, in case of interlace mode, it needs two times of scanning line comparing to non-Interlace mode, you have to arrange frame like skipping each one frame to play video at the same speed. That is, if 60 frames per one second at non-interlace mode, 30 frames per one second at interlace mode. This can be set at VDISP and VTOT.

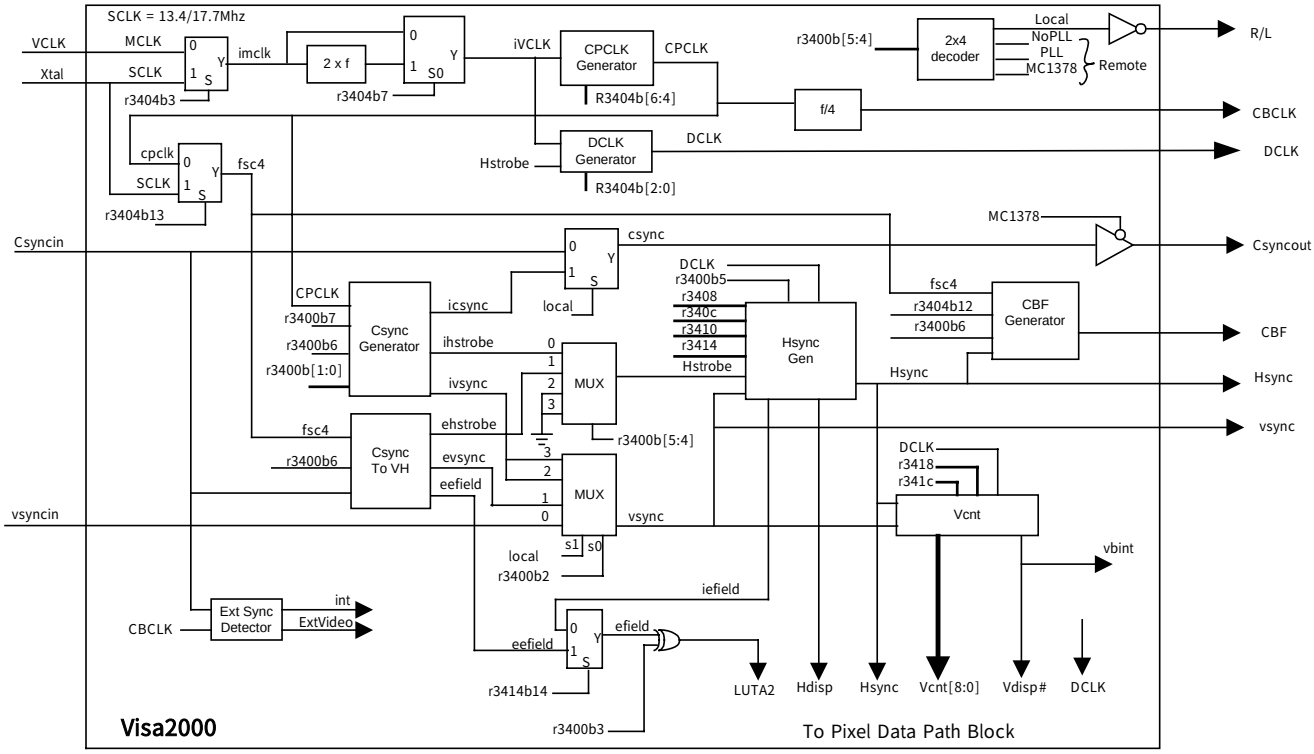


<Figure 3.13-1. Video Timing Parameters>

To draw graphic on screen, it needs to read data from memory. At this time, start address which reads data is not accessed optionally but accessed by 1Kbyte. That means, address 0, address 1024 and address 2048 can be accessed but address2, address3, …….address512 can not be used as start address. If horizontal resolution is less than 512 and is non-interlace mode, start address is [22:10]. And if horizontal resolution is more than 512 and is interlace mode, start address is [22:11]. This is related with STADn register and can set us overlay ON/OFF and Vertical Flip ON/OFF. In case of overlay on, external sync of the outside is used as sync and make graphic overlay possible. AT this time, the self sync is not used. Vertical flip is the function to turn over graphic vertically. You have to be careful that start address read from memory is start address of the last line different from the original start address. Light pen is to transmit data by reading the value of coordinate of screen and is the structure used at gun-shooting game. At 2 players mode, there are LIGHTnX to save horizontal position and LIGHTnY to save vertical position.

CLOCK, SYNC

Following is the internal block diagram CRT controller.



* CLK which makes CSYNC is CPCLK.
* Clock to make HLINE(HW+HBP+HDISP+HFP) and pixel clock use DCLK.
* Register related with CSYNC is HTOT and VTOT Register. In case of HTOT[10] =1, the value of HTOT will be amended. And in case of VTOT[11]=1, the value of VTOT can be changed.

Formula of determining the number of vertical total line :
In case CRTMOD[7:6]=00 and VTOT[11]=1,
vertical total line = 9 + (VTOT[10:0]+1)/2.
And in case the value of VTOT[10:0] is even number, it becomes interlaced. In case of odd number, it becomes non-interlaced.

Formula of determining the number of Hline total length : (Unit= cpclk)
In case CRTMOD[10]=1,
Hline total length = (HTOT[9:0]+1)*2.

Example 1 > 320*240 non-interlace, Horizontal frequency : 15.7Khz, Vertical frequency : 60Hz

In case XIn=14.3182Mhz, Hline_Length=910cpclk , vertical total line = 262, Vertical Frequency = 60Hz

At first, set to CPCLK =14.3182 Mhz. And set to DCLK=7.159 Mhz.

Consider the following process.

1. Fivclk = (CRTTIM[3]==1) ? Fxin_pin : Fvclk_pin => Which pin we will use as clock source ?
2. Fiivclk = (CRTTIM[7]==1) ? Fivclk * 2 : Fivclk => Decide to whether multiply Fivclk by 2 or not.
3. Fcpclk = Fiivclk / (CRTTIM[6:4] + 1) => Divide Fivclk by CRTTIM[6:4].
4. Fcbclk_pin = Fcpclk / 4 => 3.58Mhz appears.
5. Fdclk = Fiivclk / (CRTTIM[2:0] + 1) => Dividing by CTRTIM[2:0], make DCLK.
6. Fsc4clk = (CRTTIM[13]==1) ? Fxin_pin : Fcpclk => Use at Csync2VH & CBF_generate block

Based on above process, you can get the following value.

1. Supposing that we use 14.3182 Mhz from Xin. CRTTIM[3]=1
2. To multiply 2, set to CRTTIM[7]=1.
3. To make to CPCLK=14.3182Mhz, set to CRTTIM[6:4]=1.
4. To make DCLK=7.159Mhz, set to CRTTIM[2:0]=3. Accordingly, it becomes CRTTIM[7:0]=00011011=0x1B

Vertical total line is CRTMOD[7:6]=00 and in case of VTOT[11]=1, vertical total line = 262 = 9 + (VTOT[10:0]+1)/2.
Extracting the above formula, it becomes VTOT[10:0]=505. => Because of odd number, it becomes non interlaced.

In case Hline total length is HTOT[10]=1, it becomes Hline total length = 910 cpclk = (HTOT[9:0]+1)*2.
Extracting the above numeric formula, it becomes HTOT[9:0]=454.

Hline parameter (HW+HBP+HDISP+HFP) is fit to DCLK unit.

HW=4.7us * 7.159=>34-1=33
HBP=4.7us* 7.159=>34-1=33
HDISP=320-1=319
In local mode, no need to set HFP.

Example 2 > VGA 640 x 480, 60Hz setting

Actually, VGA 640 x 480 mode is clk=25.175Mhz, Hline_Length=800clk and vertical total line = 525.
First, set to CPCLK =DCLK=21.175 Mhz. (In case of DCLK, no problem to set any frequency)

Consider the following process.

1. Fivclk = (CRTTIM[3]==1) ? Fxin_pin : Fvclk_pin => Which pin you will use as clock source?
2. Fiivclk = (CRTTIM[7]==1) ? Fivclk * 2 : Fivclk => Decide to whether multiply Fivclk by 2 or not.
3. Fcpclk = Fiivclk / (CRTTIM[6:4] + 1) => Divide Fivclk by CRTTIM[6:4].
4. Fcbclk_pin = Fcpclk / 4 => 3.58Mhz appears.
5. Fdclk = Fiivclk / (CRTTIM[2:0] + 1) => Dividing by CTRTIM[2:0], make DCLK.
6. Fsc4clk = (CRTTIM[13]==1) ? Fxin_pin : Fcpclk => Use at Csync2VH & CBF_generate block

Based on the above process, you can get the below value.

1. If you use 21.175 Mhz from Xin, no need to use VCLK. But in this case, because PLL setting becomes complicated, connect 21.175 Mhz OSC to VCLK pin. CRTTIM[3]=0
2. To multiply this by 2, set to CRTTIM[7]=0.
3. To do CPCLK=21.175Mhz, set to CRTTIM[6:4]=1.
4. To do DCLK=21.175Mhz, set to CRTTIM[2:0]=1. So, CRTTIM[7:0]=00010001=0x11

In case vertical total line is CRTMOD[7:6]=00 and VTOT[11]=1, it becomes vertical total line = 525 = 9 + (R3424[10:0]+1)/2.
Extracting the above numeric formula, it becomes VTOT[10:0]=1031. => Because of odd number, it becomes non-interlaced.

In case Hline total length is HTOT[10]=1, it becomes Hline total length = 800 cpclk = (HTOT[9:0]+1)*2.
Extracting the above numeric formula, it becomes HTOT[9:0]=399.

Hline parameter (HW+HBP+HDISP+HFP) is fit according to VGA spec. => Unit DCLK

3.11.1 CRTC Status / Mode Register (CRTMOD)

Address : 0180 3400h

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	00h
15	R	Horizontal Sync. Status. It is read as 0 in Sync active block.	-
14	R	Vertical Display Enable Status It is read as 1 in vertical display enable block.	-
13	R	Horizontal & Vertical Blank Period. It is read as 0 in blank block.	-
12	R	External Video Signal Status 0 : Invalid State 1 : Valid State	-
11 : 10	R	Reserved.	0
9	RW	Screen Blank Enable 0 : Normal 1 : Blank Screen	0
8	RW	Protect to write CRTC Registers 0x01803404~0x01803424 0 : Possible to write . 1 : Impossible to write.	0
7	RW	Horizontal Scan Line Number 0 : 525 Line 1 : 625 Line	0
6	RW	Color Burst Frequency 0 : 3.58 MHz 1 : 4.43 MHz	0
5 : 4	R	Reserved	00
3	RW	Select Display Start Field in the Interlace mode 0 : Odd Field (NTSC), Even Field (PAL) 1 : Even Field (NTSC), Odd Field (PAL)	0
2	R	Reserved	0
1 : 0	RW	Vertical Sync Width Generation 00 : Serration Only 01 : Pre-equalization and Serration 10 : Post-equalization and Serration 11 : Pre/Post-equalization and Serration	0

3.11.2 Timing Control Register (CRTTIM)

Address : 0180 3404h

Bit	R/W	Description	Default Value
31 : 14	R	Reserved	00h
13	RW	Fsc4clk Select. 0 : CPCLK Pin 1 : 14.318Mhz(External clock Xin)	0
12	RW	CBF Output Polarity 0 : Low Active Signal 1 : High Active Signal	0
11:8	RW	Reserved	0
7	RW	Set the speed of ivclk 0 : Normal 1 : Double(ivclk=2*video clock)	0
6 : 4	RW	It generates CBCLK and de-multiplies video clock which is input from video encoder to 3.58MHz. The available frequencies to be input externally are as below. CBCLK = ivclk/ (this value + 1)*4 000 : No use 001 ~ 111 : Divided by 2~8	010b
3	RW	VCLK (Video Clock) Select. 0 : VCLK Pin 1 : 14.318Mhz	0
2 : 0	RW	It generates DCLK and de-multiplies video clock which is input from video encoder to generate dot clock. DCLK = ivclk / (this value + 1) 000 : Reserved 001 ~ 111 : Divided by 2~8	010b

3.11.3 Horizontal Sync Width / Back Porch Register (HSWBP)

Address : 0180 3408h

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	00h
15 : 8	RW	HBP: Horizontal Back Porch - 1	0
7 : 0	RW	HW : Horizontal Sync Width - 1	0

3.11.4 Horizontal Display Total Register (HDISP)

Address : 0180 340Ch

Bit	R/W	Description	Default Value
31 : 10	R	Reserved	00h
9 : 0	RW	HDISP : Horizontal Display Total - 1	0

3.11.5 Horizontal Sync Front Porch Register (HSFP)

Address : 0180 3410h

Bit	R/W	Description	Default Value
31 : 9	R	Reserved	00h
7 : 0	RW	Reserved	0

3.11.6 Field Window Bound Register (FWINB)

Address : 0180 3414h

Bit	R/W	Description	Default Value
31 : 15	R	Reserved	00h
14	RW	Even Field Select 0 : From Hsync block 1 : From CynvToVH	0
13 : 8	RW	Odd/Even Field Window Upper Bound by 16 pixel	0
7 : 6	R	Reserved.	0
5 : 0	RW	Odd/Even Field Window Lower Bound by 16 pixel	0

3.11.7 Vertical Sync Back Porch Register (VSBP)

Address : 0180 3418h

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	00h
7 : 0	RW	VBP : Vertical Sync Back Porch -1	0

3.11.8 Vertical Display Total Register (VDISP)

Address : 0180 341Ch

Bit	R/W	Description	Default Value
31 : 9	R	Reserved	00h
8 : 0	RW	VDISP : (Vertical Display Total /2)-1 (Interlace mode) Vertical Display Total –1 (non-Interlace mode)	0

At this point, vertical display total is the number of frame line. Accordingly, it is to combine the number of display line of even/odd field.

3.11.9 Horizontal Total Register (HTOT)

Address : 0180 3420h

Bit	R/W	Description	Default Value
31 : 13	R	Reserved	00h
12	RW	Csync width is 2cpclk for test.	0
10	RW	Enable this register bit[9:0] programming.	0
9 : 0	RW	Horizontal Total Pixel (Horizontal Total / 2) - 1	00h

3.11.10 Vertical Total Register (VTOT)

Address : 0180 3424h

Bit	R/W	Description	Default Value
31 : 12	R	Reserved	00h
11	RW	Enable this register bit[10:0] programming.	0
10 : 0	RW	Vertical Total Line NTSC : (Vertical Total – 9) * 2 (Interlace mode) ((Vertical Total – 9) *2) –1 (non-Interlace Mode) PAL : (Vertical Total – 9) * 2 – 1 (Interlace Mode) ((Vertical Total – 9) *2 (non-Interlace mode)	00h

* There is no need to program HTOT and VTOT register in ordinary case. It becomes automatic setting automatically .

* At this point, vertical total means the number of total line between vsync and vsync. That is, the number of interlace line is half of non-interlace line.

3.11.11 Horizontal Line Back Porch Register (HLBP)

Address : 0180 3428h

Bit	R/W	Description	Default Value
31 : 10	R	Reserved	00h
9 : 0	RW	Horizontal Display Start Position Control Register	00h

3.11.12 CRT Display Start Address 0 Register (STAD0)

Address : 0180 342Ch

Bit	R/W	Description	Default Value
31 : 15	R	Reserved	00h
14 : 2	RW	*When Horizontal resolution is less than 512 pixels in interlace mode or any pixels in non-interlace mode* - These bits are the CRT display start address bits [22:10] of 1st Bank. *When horizontal resolution is more than 511 pixels in interlace mode* - Bits [13:2] are the CRT display start address bits [22:11] of 1st Bank. - Bit[14] is reserved. The start address is basically the address of every 1024 bytes (512pixels).	00h
1	R	Reserved	0
0	RW	Vertical Flip Enable Display Current Upside Down Screen Image . To make screen upside down, this bit and display start address of STAD0 and STAD1should be reprogrammed with start address of last line in normal screen.	0

3.11.13 CRT Display Start Address 1 Register (STAD1)

Address : 0180 3430h

Bit	R/W	Description	Default Value
31 : 15	R	Reserved	00h
14 : 2	RW	*When Horizontal resolution is less than 512 pixels in interlace mode or any pixels in non-interlace mode* - These bits are the CRT display start address bits [22:10] of 2nd Bank. *When horizontal resolution is more than 511 pixels in interlace mode* - Bits [13:2] are the CRT display start address bits [22:11] of 1st Bank. - Bit[14] is reserved. The start address is basically the address of every 1024 bytes (512pixels).	0
1	RW	Select Current Display Frame for Double Buffering at Interlace Mode 0 : Even Frame 1 : Odd Frame	0
0	RW	Select Non-interlace mode 0 : Interlace Mode 1 : Non-Interlace Mode	0

3.11.14 Transparency Color Register (TCOL)

***Address :* 0180 3434h**

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	00h
15 : 0	RW	Transparency Color bit If 16bit color to be displayed is same to register value, it generates overlay signal to generate background image(Video).	00h

3.11.15 Light Pen 0 X Register (LIGHT0X)

Address : 0180 3438h

Bit	R/W	Description	Default Value
31 : 11	R	Reserved	00h
10 : 0	R	Light Pen 0 Current Horizontal Position	x

3.11.16 Light Pen 0 Y Register (LIGHT0Y)

Address : 0180 343Ch

Bit	R/W	Description	Default Value
31 : 9	R	Reserved	00h
8 : 0	R	Light Pen 0 Current Vertical Position	x

3.11.17 Light Pen 1 X Register (LIGHT1X)

***Address* : 0180 3440h**

Bit	R/W	Description	Default Value
31 : 11	R	Reserved	00h
10 : 0	R	Light Pen 1 Current Horizontal Position	x

3.11.18 Light Pen 1 Y Register (LIGHT1Y)

Address : 0180 3444h

Bit	R/W	Description	Default Value
31 : 9	R	Reserved	00h
8 : 0	R	Light Pen 1 Current Vertical Position	x

3.11.19 Light Pen Input Control Register (LIGHTC)

Address : 0180 3448h

Bit	R/W	Description	Default Value
31 : 2	R	Reserved	00h
1	RW	Light Pen 1 Input Polarity 0 : High Active Strobe 1 : Low Active Strobe	0
0	RW	Light Pen 0 Input Polarity 0 : High Active Strobe 1 : Low Active Strobe	0

3.12 Frequency Synthesizer

OVERVIEW

The power consumption in VRenderZERO+ is reduced by software control. The power management has two power down modes: Power Saving mode for DAC, Power Saving mode for PLL.

PLL(Phase Locked Loop)

PLL is the circuit that synchronizes an output signal with a reference or input signal in frequency as well as in phase.

Frequency Equation : Fout = ((M + 8) * Fin) / ((P + 2) * 2^S)
Reference input frequency : Fin = 14.318MHz
Example : M = 3Eh, P = 001000b, S = 01b (50MHz)
Default frequency output is 20MHz.

3.12.1 PLL Control Register (DPCON)

Address : 0180 4000h

Bit	R/W	Description	Default Value
31 : 10	R	Reserved	00h
9	RW	Power Saving Mode for DAC 0 : Normal 1 : Power Saving Enable	0
8 : 3	R	Reserved.	0
2	RW	Write Protect PLL Program Register (PLPGM) 0 : Possible to write 1 : Impossible to write	0
1	RW	16Bit RGB Output 0 : Normal Mode 1 : Output to PIO[15:0] If this bit is set to 1, the output of 16bit Pixel Data R[4:0], G[5:0], B[4:0] is generates to PIO pin [15:0]. Accordingly, local memory should be run with 16bit interface.	0
0	RW	Power Saving Mode for PLL 0 : Normal 1 : Power Saving Enable In case of direct usage of external clock, internal PLL goes to power saving mode automatically.	0

3.12.2 PLL Program Register (PLPGM)

Address : 0180 4004h

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	000h
15 : 8	RW	Main Divider 8 Bit (M)	57h
7 : 2	RW	Pre-divider 6 Bit (P)	001111b
1 : 0	RW	Post Scaler 2 Bit (S)	10b

Frequency Equation : Fout = ((M+8)*Fin) / ((P+2)*2^S)

Reference input frequency : Fin = 14.318MHz

Example : M = 3Eh, P = 001000b, S = 01b (50MHz)

Default frequency output is 20MHz

OUTPUT FREQUENCY EQUATION & TABLE

Frequency Equation: $$F_{OUT} = \frac{(m+8)}{(p+2) \times 2^{s}} \times F_{IN}$$

Table 1. Example of Divider Ratio

M[7]	M[6]	M[5]	M[4]	M[3]	M[2]	M[1]	M[0]	m	M (m+8)	P[6]	P[5]	P[4]	P[3]	P[2]	P[1]	P[0]	p	P (p+2)	S[1]	S[0]	2^S
0	1	0	1	0	1	0	1	85	93	0	1	0	1	0	0	1	41	43	0	0	1

Table 2. Sample Frequency Coefficient(Reference Input Frequency=14.318MHz)

Fout	P	M	S	Fout	P	M	S	Fout	P	M	S	Fout	P	M	S	Fout	P	M	S
10	15	87	3	41.6	19	144	1	69	9	98	1	100.76	25	182	0	137	5	59	0
14.318	8	72	3	42	13	80	1	70	16	80	0	101	17	126	0	138	23	233	0
15	19	168	3	43	8	52	1	71	22	111	0	102	22	163	0	139	22	225	0
16	15	68	2	44	25	158	1	72	18	93	0	103	19	143	0	140	7	80	0
17	10	49	2	44.3	14	91	1	73	18	94	0	104	17	140	0	141	11	120	0
18	27	138	2	44.74	10	67	1	74	10	54	0	105	10	80	0	142	10	111	0
19	11	61	2	44.9	9	61	1	75	15	81	0	106	8	66	0	143.18	7	82	0
20	15	87	2	45.5	12	81	1	76	11	61	0	107	17	134	0	144	15	163	0
21	13	80	2	46	24	159	1	77	14	78	0	108	22	173	0	145	6	73	0
22	12	78	2	47	21	143	1	77.25	21	116	0	109	16	129	0	146	3	43	0
23	24	159	2	48	15	106	1	78	18	101	0	110	20	161	0	147	13	146	0
24	25	173	2	49	11	81	1	79	27	152	0	111	14	116	0	148	1	23	0
25.175	23	168	2	49.2	22	157	1	80	15	87	0	112	15	125	0	149	20	221	0
25.5	14	106	2	49.5	10	75	1	81	30	173	0	113	17	142	0	150	19	212	0
26	17	130	2	50	8	62	1	82	9	55	0	114	22	183	0	151	9	108	0
27	22	173	2	50.35	23	168	1	83.04	13	79	0	115	22	185	0	152	11	130	0
28.322	21	174	2	51	22	163	1	84	13	80	0	116	8	73	0	153	17	195	0
29	8	73	2	52	17	130	1	85	14	87	0	117	21	180	0	154	2	35	0
30	19	168	2	53	8	66	1	86	8	52	0	118	23	198	0	155	21	241	0
30.25	18	161	2	54	9	75	1	87	11	71	0	119	14	125	0	156	17	199	0
31	7	70	2	55	20	161	1	88	25	158	0	120	19	168	0	157	22	255	0
31.5	8	80	2	56	15	125	1	89	12	79	0	121	18	161	0	158.12	21	246	0
32	15	144	2	56.644	21	174	1	89.8	9	61	0	122	21	188	0	159	17	203	0
32.514	17	79	1	57	22	183	1	91	12	81	0	123	20	181	0	160	21	249	0
33	21	98	1	58	8	73	1	92	24	159	0	124	7	70	0	161	2	37	0
34	10	49	1	59	19	165	1	93	8	57	0	125	9	88	0	162	17	207	0
35	36	80	1	60	19	168	1	93.4	17	116	0	126	8	80	0	163	11	140	0
35.5	22	111	1	61	21	188	1	94.5	8	58	0	127	13	125	0	164	9	118	0
36	18	93	1	62	13	122	1	95	9	65	0	128	14	135	0	165	19	234	0
37	10	54	1	62.5	9	88	1	95.5	7	52	0	129	8	82	0	166	20	247	0
37.5	15	81	1	63	8	80	1	96	15	106	0	130	11	110	0	167	7	97	0
38	11	61	1	64	15	144	1	97	20	141	0	131	18	175	0	168	13	168	0
39	27	150	1	65	11	110	1	98	11	181	0	132	7	75	0	169	13	169	0
39.5	27	152	1	66	12	121	1	99	21	151	0	133	19	187	0	170	6	127	0
40	15	87	1	66.6	12	123	1	99.7	25	180	0	134	12	123	0				
41	9	55	1	68	12	125	1	100.	8	62	0	135	12	124	0				

[Note] If you want to used anyother divider ratios, Please you contact to SEC engineers

Table 3-3 Frequency table of P,M,S value of PLL(AL2007LA)

3.13 Graphic Controller

3.13.1 Graphic Packet Format

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PD[0]/ PH	R	E6	E5	E4	E3	E2	E1	E0	7	6	5	4	3	2	1	0
PD[1]	Reserved						Dx									
PD[2]	Reserved							Dy								
PD[3]	Reserved						EndX									
PD[4]	Reserved							EndY								
PD[5]	Tx[15:0]															
PD[6]	Reserved											Tx[20:16]				
PD[7]	Ty[15:0]															
PD[8]	Reserved											Ty[20:16]				
PD[9]	dTxdx[15:0]															
PD[10]	Reserved											dTxdx[20:16]				
PD[11]	dTydx[15:0]															
PD[12]	Reserved											dTydx[20:16]				
PD[13]	dTxdy[15:0]															
PD[14]	Reserved											dTxdy[20:16]				
PD[15]	dTydy[15:0]															
PD[16]	Reserved											dTydy[20:16]				
PD[17]	SrcAlphaColor[15:0]															
PD[18]	Reserved		SrcBlendFunc[5:0]						SrcAlphaColor[23:16]							
PD[19]	DestAlphaColor[15:0]															
PD[20]	Reserved		DestBlendFunc[5:0]						DestAlphaColor[23:16]							
PD[21]	ShadeColor[15:0]															
PD[22]	Reserved								ShadeColor[23:16]							
PD[23]	TransparencyColor[15:0]															
PD[24]	Reserved								TransprarencyColor[23:16]							
PD[25]	TileOffset															
PD[26]	FontOffset															
PD[27]	PaletteOffset													Reserved		
PD[28]	Reserved			9	PaletteBankSelect				8		THeight			TWidth		

0 : FlipFlag
1 : AlphaEnable
2 : TransparencyEnable
3 : TextureEnable
4 : ShadeEnable
5 : DrawType
6 : PaletteUpdateFlag
7 : AsyncFlipFlag
8 : PixelFormat
9 : TextureMode

E0~E6

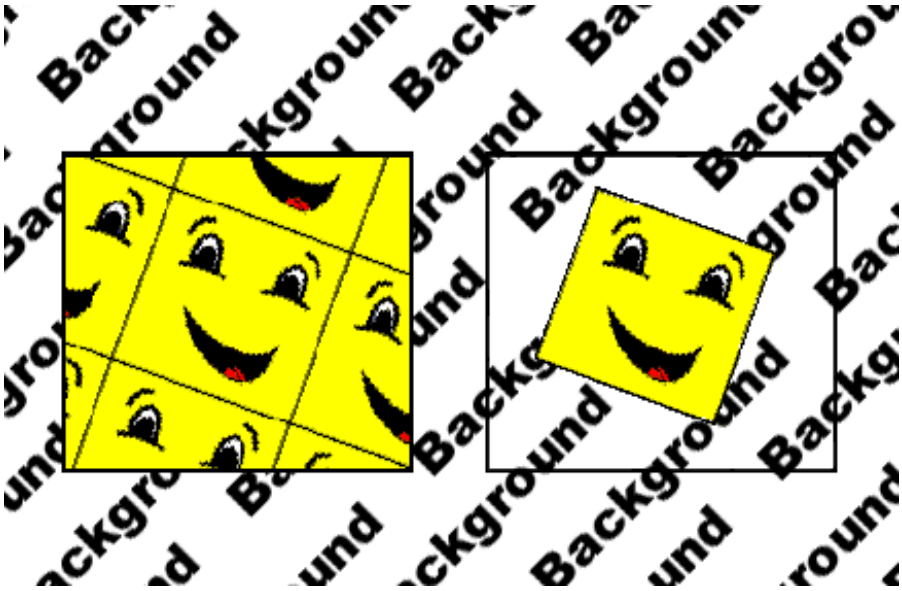
Indicates the validity of each parameter group.
There are 7 groups of commands and each group has its own parameters except control parameter. This is to reduce CPU load in transmitting parameters.

If this bit is 1, corresponding group uses the contents of the packet. If 0, it uses initial value or re-uses the previous value.(This is defined group by group)

Group	Parameter	if(En == 1)	if(En == 0)
E0	Dx, Endx Dy, Endy	To draw box.	Do not execure rendering
E1	Tx, Ty	Tx = PD[5~6] Ty = PD[7~8]	Tx = 0 Ty = 0
E2	dTxdx, dTydx dTxdy, dTydy	dTxdx = PD[9~10] dTydx = PD[11~12] dTxdy = PD[13~14] dTydy = PD[15~16]	dTxdx = (1<<9) dTydx = 0 dTxdy = 0 dTydy = (1<<9)
E3	SrcAlphaColor, DestAlphaColor	SrcAlphaColor = PD[17~18] SrcAlphaFunc = PD[18] DestAlphaColor = PD[19~20] DestAlphaFunc = PD[20]	To keep register value
E4	ShadeColor	ShadeColor = PD[21~22]	
E5	TransparencyColor	TransparencyColor = PD[23~24]	
E6	TileOffset FontOffset PaletteOffset PaletteBankSelect PixelFormat TWidth, Theight TextureMode	TileOffset = PD[25] FontOffset = PD[26] PaletteOffset = PD[27] PaletteBankSelect = PD[28] PixelFormat = PD[28] TWidth, Theight = PD[28] TextureMode = PD[28]	

3.13.1.1 Draw Information Flag

- **FlipFlag** :
  Indicates the current command is flipping command. If this value is 1, all other parameters are disregarded. FlipFlag executes flipping only after vertical recurrence.
- **AsyncFlipFlag** :
  Indicates the current command is asynchronous flipping. If this value is 1, all other parameters are disregarded. But ASyncFlipFlag executes flipping immediately, not waiting for vertical recurrence.
- **AlphaEnable** :
  Alpha blending enable.
  Executes blending by using alpha blending register (Group E3).
- **TransparencyEnable** :
  Transparency color check enable.
  If the value is 1, the color like transparency color among texture colors is not rendered.
- **TextureEnable** :
  Texture mapping enable.
  0: Texture color = White
  1: Texture color = ReadTexture(tx,ty)
- **ShadeEnable** :
  Shade enable.
  0: Shade color = White
  1: Shade color = ShadeColor register
- **DrawType** :
  Sprite enable.
  When the texture coordinate (tx,ty) goes off texture size, if the value is 0, it is repeat and if the value is 1, it is clipping.



< In case RegDrawType is 0 (Left) & 1 (Right) >

- **PaletteUpdateFlag** :
  This is the flag meaning to update new palette.
  VRenderZERO+has 256pcs of 24bit RGB color tables inside.
  If the value is 1, fill color table with memory contents indicated by PaletteOffset.
  If E0 = 1, update color table and execute rendering.

3.13.1.2 Coordinate Information

[9 : 0] Dx, Endx
[8 : 0] Dy, Endy

Screen coordinates to do rendering (Dx, Dy)-(Endx, Endy)
unsigned integer (Unit:Pixel)

[20 : 0] Tx, Ty :

Texture coordinates to be mapped at the beginning point of rendering.
fixed point [s.11.9]. (Unit:Texel)

[20 : 0] dTxdx, dTydx, dTxdy, dTydy :

dTxdx : Increased value of texture x coordinates according to a increase of 1 in screen x coordinates.
dTydx : Increased value of texture y coordinates according to a increase of 1 in screen x coordinates.
dTxdy : Increased value of texture x coordinates according to a increase of 1 in screen y coordinates.
dTydy : Increased value of texture y coordinates according to a increase of 1 in screen y coordinates.
fixed point [s.11.9]. (unit:Texel/Pixel)

3.13.1.3 Color Processing Information

[23 : 0] SrcAlphaColor, DestAlphaColor :

Alpha blending color.
{ R[7:0], G[7:0], B[7:0] }

[5 : 0] SrcBlendFunc, DestBlendFunc :

Blend function select

Number	Blend function
000001 (0x01)	Zero
000010 (0x02)	Source Alpha
000100 (0x04)	Source Color
001000 (0x08)	Destination Alpha
010000 (0x10)	Destination Color
100001 (0x21)	One
100010 (0x22)	Inverse Source Alpha
100100 (0x24)	Inverse Source Color
101000 (0x28)	Inverse Destination Alpha
110000 (0x30)	Inverse Destination Color

Source Alpha : SrcAlphaColor register value
Source Color : Texture color x Shade color
Destination Alpha : DestAlphaColor register value
Destination Color : Render target buffer의 pixel color

Result color = Source Color x [SrcBlendFunc] + Destination Color x [DestBlendFunc]

[23 : 0] ShadeColor :

{ R[7:0], G[7:0], B[7:0] }

[23 : 0] TransparencyColor :

{ R[7:0], G[7:0], B[7:0] }

[15 : 0] TileOffset :

Tile index-map offset
TileOffset = offset>>7, offset = address-03800000h
Offset : The other address of texture memory base address(03800000h)..
Address : Located at index-map address and texture memory, not overlapped with command queue field and must be multiple of 128.

[15 : 0] FontOffset :

Pixel data offset
FontOffset = offset>>7, offset = address-03800000h
Offset : The other address of texture memory base address(03800000h).
Address : Locates at pixel data address and texture memory, not overlapped with command queue field and must be a multiple of 128.

[21 : 9] PaletteOffset :

Palette offset
PaletteOffset = (offset>>7)&0xfff8, offset = address-03800000h
Offset : The other address of texture memory base address(03800000h).
Aaddress : Locates at palette data address and texture memory, not overlapped with command queue field and must be a multiple of 1024..

[3 : 0] PaletteBankSelect :

Palette bank select for 4bpp(16color)
VRenderZERO+has 256kinds of 24bit RGB color tables internally. If 4bpp mode is used, 256pcs of 24bit

RGB color tables are divided into 16kinds of 16color tables and one of them is used. The one used at this time is palette bank select.

[1 : 0] PixelFormat :

To select pixel format of fontOffset indicated by pixel data.

00: 4bit indexed mode (16color)
01: 8bit indexed mode (256color)
1x: 16bit RGB565 mode (65536color)

[2 : 0] TWidth, Theight :

Texture size
TWidth = $\log_2$(Texture_width)-3 , 8 ≤ Texture_width ≤ 1024 (pixel)
THeight = $\log_2$(Texture_height)-3 , 8 ≤ Texture_height ≤ 1024 (pixel)

TextureMode :

0: Image texture
if 16bpp, Texel=(unsined short*)address(FontOffset) [ty * (8<< TWidth) + tx]
1: Tile indexed texture
if 16bpp, Texel=(unsined short*)address(FontOffset)[(index<<6) + ((ty&7)<<3) + (tx&7)]

where:

Index = (unsined short*)address(TileOffset)[(ty>>3) * (1<< TWidth) + (tx>>3)]
address(A) = 03800000h + (A*128)

3.13.2 Registers

3.13.2.1 Command queue front pointer register

Address : 0300 0080h

Bit	R/W	Description	Default Value
15:11	R	Reserved.	xxh
10: 0	R/W	CmdQueueFront Front pointer.of Command Queue Command queue : Arranged to 0380 0000h ~ 0381 FFFFh field. 64byte x 2048 depth	00h

3.13.2.2 Command queue rear pointer register

Address : 0300 0082h

Bit	R/W	Description	Default Value
15:11	R	Reserved.	xx
10: 0	R	CmdQueueRear Rear pointer of command queue. Rear pointer is increased automatically until the same with font pointer. (Until command is processed)	000h

3.13.2.3 Rendering engine control register

Address : 0300 008ch

Bit	R/W	Description	Default Value
15: 8	R	Reserved.	xx
7	R/W	Rendering Buffer Select 0 : render to Back buffer (~ Current display bank) 1 : render to Front buffer (Current display bank)	0b
6 : 5	R	Reserved.	x

Bit	R/W	Description	Default Value
3	R/W	Engine Reset To initialize all rendering pipelines. To initialize pipeline only, not video register.	0b
2	R/W	Engine Start Engine reset and engine start should not be 1 at the same time. If the value is 1, the contents of command queue start to proceed. Until engine reset becomes 1, the processing will not be stopped..	0b
1 : 0	R/W	Dither Mode 00 : 2x2 01 : 4x4 1x : Disable	10b

3.13.2.4 Display bank register

Address : 0300 008eh

Bit	R/W	Description	Default Value
15: 1	R	Reserved.	xx
0	R	Current display bank	0

3.13.2.5 Rendering bank1 address select register

***Address* : 0300 0090h**

Bit	R/W	Description	Default Value
15	R/W	Rendering bank1 address select 0 : Bank1 address = 0410 0000h 1 : Bank1 address = 0440 0000h Rendering bank0 address is fixed. (Bank0 address = 0400 0000h) Because bank1 is set to 0410 0000h, the system becomes slower. 0440 0000h is recommended.	00
14: 0	R	Reserved	xxxx

3.13.2.6 Flip command count register

Address : 0300 00a6h

Bit	R/W	Description	Default Value
15: 8	R	Reserved.	xx
7 : 0	R/W	Flip Count Automatically decreased counter whenever flipping happens. Read : counter value. Write 0 : reset flip counter Write 1 : increase flip count	00

3.14 Misc. Register

3.14.1 TMEM/FMEM Type Control Register (TFCTRL)

Address : 0300 0100h

Bit	R/W	Description	Default Value
15	R/W	nMRST : Reset Memory Controller for Tmem/FMEM. After setting 1, The Initial cycle and mode parameter cycle for each SDRAM is inserted automatically. 0 : Tmem/Fmem Reset 1 : Active	0
14:4	R	Reserved	
3:2	RW	CfgTMEMType : SDRAM Type Select 00 ; 16Mbit SDRAM 10 : 64Mbit SDRAM	00
1:0	RW	CfgFMEMType : SDRAM Type Select 00 ; 16Mbit SDRAM 10 : 64Mbit SDRAM	00

After power-on-reset or system reset, the memory controller for T/FMEM do not operate. So. You must set nMRST bit before you access TMEM or FMEM.

VRenderZERO+ supports only 2 Type SDRAM, 16Mbit, 2Banks and 64Mbit, 4Banks for F/TMEM. T/FDRAMType deciding the memory type of each memory should be set before you set nMRST.

3.14.2 FMEM Timing Control Register (FTIMCON)

Address : 0300 0106h

Bit	R/W	Description	Default Value
15:12	R	Reserved	0
11:9	R/W	FtRP : FMEM tRP Parameter	101
8:6	RW	FtRCD : RAS-to-CAS Delay	011
5:3	RW	FtRC : tRC	110
2:0	RW	FtCL : FMEM CAS Latency	010

3.14.3 TMEM Timing Control Register (TTIMCON)

Address : 0300 0108h

Bit	R/W	Description	Default Value
15:12	R	Reserved	0
11:9	R/W	FtRP : TMEM tRP Parameter	101
8:6	RW	TtRCD : RAS-to-CAS Delay	011
5:3	RW	FtRC : tRC	110
2:0	RW	FtCL : TMEM CAS Latency	010

3.15 Wavetable Synthesizer

OVERVIEW

VRenderZERO+ has Wavetable synthesizer to support 32 poly and each 32 sound channel designates volume, panning, envelope and wave to generate individually.

Wave format VRenderZERO+ supports is signed 8bit PCM, signed 16bit PCM and 8bit u-law and each wave data is to exist on frame buffer or texture buffer respectively.

Each channel has channel parameter register composed of 32half-words. Channel parameter register designates address of frame memory or texture memory which saves sample and saves volume, envelope control parameter and increased value to generate wave at desired frequency.

It has sound control register to control whole Wavetable synthesizer. This sound control register has function to start or stop operation of each channel according to channel parameter register value and function to control existing operation status and interrupt control.

3.15.1 Channel Parameter Register (WP0~31)

***Address* : 0x0480_0000 ~ 0x0480_03FF**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	CurSAddr[15:0]															
0x02	CurSAddr[31:16]															
0x04	EnvVol[15:0]															
0x06	R	1	1	LD	EnvStage				EnvVol[23:16]							
0x08	dSAddr[15:0]															
0x0A	R	Modes							Reserved							
0x0C	LoopBegin[15:0]															
0x0E	R	LChnVol							Reserved		LoopBegin[21:16]					
0x10	LoopEnd[15:0]															
0x12	R	RChnVol							Reserved		LoopEnd[21:16]					
0x14	EnvRate0[15:0]															
0x16	EnvRate1[15:0]															
0x18	EnvRate2[15:0]															
0x1A	EnvRate3[15:0]															
0x1C	EnvRate1[16]	EnvTarget1							EnvRate0[16]	EnvTarget0						
0x1E	EnvRate3[16]	EnvTarget3							EnvRate2[16]	EnvTarget2						

3.15.1.1 Sample Address Control

- ***CurSAddr (Current Sample Address)***

Fixed Point : 22.10 ***Default Value : unknown***

This value saves address of texture/frame memory which saves wave sample to generate. By reading the value, you can monitor the processed status of cuirrent channel.

- ***dSAddr (Delta Sample Address)***

Fixed Point : 6.10 ***Default Value : unknown***

It designates increased value of CurSAddr. Whenever one sample data is generated, this value is added to CurSAddr. By changing the value, each wave frequency will be changed.

3.15.1.2 Loop Control

- ***LoopBegin, LoopEnd***

Fixed Point : 22 ***Default Value : unknown***

The beginning and end of sample loop are set to LoopBegin and LoopEnd. Although you do not want looping, LoopEnd should be set. By setting modes, user can run looping and pingpong. Like CurSAddr, user must set word-type offset from memory into LoopBegin and LoopEnd.

- ***LD (Loop Direction)***

Bits : 1 ***Recommend Value : 1***

LD (Loop Direction) can set beginning direction of play when setting wave loop.

0 : Inverse Direction : Decreases CurSAddr value and brings the value.
1 : Normal Direction : Increases CurSAddr value and brings the value

3.15.1.3 Envelope Control

- ***EnvVolume (Envelope Volume)***

Fixed Point : S.7.6 ***Default Value : unknown***

Designates the value of existing envelope volume and reads the value of existing envelope volume to be processed.

- ***EnvStage (Envelope Stage)***

Bits :4 ***Recommend Value : 4'b0001***

Saves status of current envelope. Wavetable synthesizer of VRenderZERO+ can have total 4 envelope stages and have the following values.

Bit 0 : Attack Stage
Bit 1 : Decay Stage
Bit 2 : Sustain Stage
Bit 3 : Release Stage

- ***EnvTarget0~3 (Envelope Target)***

Unsigned : 0~127 ***Default Value : unknown***

Designates target volume value per envelope stage. Envelope stage moves to next stage when interpolated envelope volume value accords with EnvTarget.

- ***EnvRate0~3 (Envelope Rate)***

Fixed Point : S.16 ***Default Value : unknown***

Assign increased value of EnvVol by EnvStage.

3.15.1.4 Mode Control

- ***Modes (Modes)***

Bits : 6 ***Default Value : unknown***

Designates increased value to interpolate envelope volume value.

Designates loop, envelope and wave format of each channel.

Bit 0 : **Looping** : Plays from LoopBegin to LoopEnd repetitiously when wave output.
Bit 1 : **Sustain** : Runs sustain block from LoopBegin to LoopEnd until note-off happens on envelope mode.

Bit 2 : **Envelope** : Decides whether to run envelope control or not.
Bit 3 : **Pingpong** : Decides to run normal direction and inverse direction repetitiously on loop mode.
Bit 4 : **u-Law** : Decides wave data to be 8 bit u-law.
Bit 5 : **8-bit** : Decides wave data to be 8bit/16bit PCM.
1 : 8bit PCM, 0 : 16bit PCM
This value is meaningless if wave data is 8bit u-law.
Bit 6 : **Texture** : Decides where wave data is.

1 : Texture memory 0 : Frame memory

3.15.1.5 Channel Volume Control

- ***LChnVolume (Left Channel Volume)***

Unsigned : 0~127 ***Default Value : unknown***
Assign size of left volume.

- ***RChnVolume (Right Channel Volume)***

Unsigned : 0~127 ***Default Value : unknown***
Assign size of right volume.

3.15.2 Sound Control Registers (0x04800404 ~ 0x04800602)

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x04800404(R)	Status(Low) : Channel 15 – 0															
0x04800406(R)	Status(High) : Channel 31-16															
0x04800404/6(W)	S	Reserved												ChnNum for Status		
0x04800408(R)	NoteOn(Low) : Channel 15 – 0															
0x0480040A(R)	NoteOn(High) : Channel 31-16															
0x04800408/A(W)	S	Reserved												ChnNum for Note		
0x04800410(R/W)	Reserved											RevFactor				
0x04800412(R/W)	Reserved											BufferSAddr				
0x04800420(R/W)	Reserved						BufferSize0									
0x04800422(R/W)	Reserved						BufferSize1									
0x04800440(R/W)	Reserved						BufferSize2									
0x04800442(R/W)	Reserved						BufferSize3									
0x04800480(R/W)	IntMask(Low) : Channel 15 – 0															
0x04800482(R/W)	IntMask(High) : Channel 31-16															
0x04800500(R/W)	IntPend(Low) : Channel 15 – 0															
0x04800502(R/W)	IntPend(High) : Channel 31-16															
0x04800600(R/W)	Reserved						MaxChn					ChnClkNum				
0x04800602(R/W)	RS	Reserved									TM	RE	R	CW	AW	MW

Caution) Do not write at other address besides Sound Control Register from 0x04800400 till 0x048007FF.

3.15.2.1 Status Control Register(Address bit 2)

0 : Idle
1 : Busy

Read : Read status of each channel.
Write : Set up “S” in channel status which ChnNum for Status assigned .

3.15.2.2 Note Control Register(Address bit 3)

0 : Note Off
1 : Note On

Read : Return note status of each channel.
Write : Set up “S” in channel note which ChnNum for Note assigned.

3.15.2.3 Reverberation Control Registers (Address bit 4, 5, 6)

BufferSAddr : Reverb Buffer Start Address

Save top 7 bit of start address (22 bit) for Reverb Buffer.(32k word align)

21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	BufferSAddr						BufferSelector			Buffer Pointer											

RevFactor

Assign reverberation size.

BufferSize0, 1, 2, 3

Fix buffer size which will be used at reverberation.

Be sure to make clear before enabling reverb to total 8 including left & right channel of make buffer.

BufferSize = RevFactor * sound_frequency / 1000

4000 < sound frequency < 65000

BufferSize <= 4K words

3.15.3 Interrupt Control (Address Bit 7,8)

- ***Interrupt Mask Register***

Bits :1 ***Default Value : unknown***
Enable or disable interrupt of each channel

0 : enable
1 : disable

- ***Interrupt Pend Register***

Bits :1 ***Default Value : unknown***
Read : To be set at channel where interrupt happens.
Write : Clear pending of channel which bit is set.

3.15.4 Sound Core Control Register (Address Bit 9)

- ***RS : Run Sound***

Bits :1 ***Default Value : 0***
Play or stop sound..

- ***TM : Texture Memory Select***

Bits :1 ***Default Value : Unknown***
Select memory to used as reserve buffer.

1 : Texture Memory
0 : Frame Memory

- ***RE : Reverberation Enable***

Bits :1 ***Default Value : 0***
Enable or disable reverberation effect.

- ***CW : 32bit Adder Wait***

Bits :1 ***Default Value : 0***
Enable or disable wait at 32bit adder among ALU.

- ***AW : 16bit Adder Wait***

  Bits :1 ***Default Value : 0***

  Enable or disable wait at 16bit adder among ALU..

- ***MW : Multiplier Wait***

  Bits :1 ***Default Value : 0***

  Enable or disable wait at multiplier among ALU..

- ***MaxChn : Max Channel***

  Bits :5 ***Default Value : 0***

  Select –1, the total number of channel to synthesize.(0 ~ 31)

- ***ChnClkNum*** : Clock Number per Channel

  Bits :7 ***Default Value : 0***

  Select the number of clock by each channel.

$$\text{ChnClkNum} = \frac{\text{Clock frequency}}{\text{Sound frequency} * 64} - 1$$

3.16 E3208 System Co-processor

3.16.1 General Descriptions

Co-processor spec to be applied to embedded 32bit EISC (Extendable Instruction Set Computer) is based on CP32 version 0.21 (VRenderZERO+ only) as below.

CP32 Version 0.21

Cache Feature

4Kbyte Unified 2 Way Set Associative Cache
Write Through / Write Back
16 Byte / Line
LRU Replacement
Invalidated by Hardware

Memory Map for Caching

0000_0000h ~ 00FF_FFFFh : Local ROM Area
0200_0000h ~ 02FF_FFFFh : Local DRAM, SRAM Area
0500_0000h ~ 07FF_FFFFh : Expansion ROM Area

4 Word Deep Write Buffer (FIFO)

3.16.2 Write-through or Write-Back caches

When a cache hit occurs for a data store access, the cache line containing the data is updated to contain its new value. As this cache line will eventually be re-allocated to another address, the main memory location for the data aloes needs to have the new value written to it. There two common techniques for handling this:

- In a *write-through* cache, the new data is also immediately written to the main memory location. (This is usually done though a write buffer, to avoid slowing down the processor)
- In a *write-back* cache, the cache line is marked as dirty, which means that it contains data values which are more up-to-date than those in main memory. Whenever a dirty cache line is selected to be re-allocated to another address, the data currently in the cache line is written back to main memory. Writing back the contents of the cache line in this manner is known as cleaning the cache line.

The main disadvantage of write-through caches is that if the processor speed becomes high enough relative to that of main memory, it generates data stores faster than they can be processed by the write buffer. The result is that the processor is slowed down by having to wait for the write buffer to be able to accept more data.

Because a write-back cache only stores to main memory once when a cache line is re-allocated, even if many stores have occurred to the cache line, write-back caches normally generate fewer stores to main memory. However, write-back caches have a number of drawbacks.

3.16.3 System Co-processor Register Descriptions

3.16.3.1 Master Command Register

Co-processor #0 – R7

Bit	R/W	Description	Default Value
31 : 13	R	Reserved	0
12	R	Always 1.	1
11	W	Local ROM, Local RAM Function Unit Control 0 : Disable Cache Unit 1 : Enable Cache Unit	0
10	R	Expansion ROM Function Unit Control 0 : Disable Cache Unit 1 : Enable Cache Unit	0
9 : 8	R	Function Unit (Cache)	01b
7 : 1	R	Reserved.	0
0	R/W	Co-processor wait option 0: normal(1clock) 1: 1 Wait (2clock)	

Cache usage for local memory (ROM/RAM) and expansion ROM can be set by using Coprocessor Register %R7's bit 11 and bit 10, respectively. Also, by using bit 0 of the same register, the access time for cache read hit case can be set either at 1 cycle (normal mode) or 2 cycles (wait mode.) For 1 cycle access, performance (IPC) improves at the penalty of slower clock frequency, whereas for 2 cycle access, clock frequency improves at the expense of lower performance (IPC.)

3.16.3.2 Status Register

Co-processor #0 – R6

Bit	R/W	Description	Default Value
31	R	Privileged co-processor.	1
30 : 28	R	Type	000b
27 : 25	R	Sub type	000b
23	R	Cache Status 0 : Disable 1 : Enable	0
22	R	Reserved.	0
21	R	Write Buffer (FiFo) Enable	1
20	R	Invalid Status 0 : Not Invalidate Processing 1 : Invalidate Processing	0
19 : 16	R	Reserved.	0
15 : 14	R	Debugger Configuration 2 Channel Debugger, Break only at Instruction Fetch.	01b
13 : 12	R	Reserved. (No TLB)	0
11	R	Write Buffer Configuration 4 Word Deep Write Buffer	1
10 : 8	R	Cache Configuration Unified 4Kbyte, 2 Way Set Associative, Write Through/Write Back	011b
7 : 1	R	Reserved.	0
0	R	Always 1	1

Coprocessor Register %R6 contains cache states. Bit 20 is indicates whether cache is in invalidating phase at cache initialization during which all valid and dirty bits are cleared.

3.16.3.3 Invalidate Cache without Copy Back Register

Co-processor #0 – R5

Bit	R/W	Description	Default Value
31	R	Cache Type 0 : Unified Cache	0
30 : 1	R	Reserved.	0
0	W	It sets cache tag status to all invalidate status. 0 : Disable Invalid (No Action) 1 : Enable Invalid It is useful only in case cache is disable in R7 master command register.	0

Coprocessor Register %R5 controls cache initialization. If bit 0 is set, all valid and dirty bits are cleared.

3.16.3.4 Memory Bank Data Register

Co-processor #0 – R3

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	0
7	R	Always 1.	1
6	RW	It sets cache configuration of memory bank (Local ROM / RAM, expansion ROM). 0 : Write Through Cache 1 : Write Back Cache	0
5 : 0	R	Reserved.	0

Coprocessor Register %R3 is used to set write-through and write-back modes for local ROM/RAM and expansion ROM.

4. BOUNDARY SCAN FOR VRENDER ZERO+

• Boundary scan of VRenderZERO+ is not designed for testing board but designed for flash download. Analog, POC and Frame/Texture memory pins are not connected to boundary scan register.
• JTAG of VRenderZERO+ is not entirely compatible to IEEE1149.1. Because test pins are shared with other function, these can be used as JTAG test pin after switched to JTAG test mode. POC configuration for jtag test mode is as follow.

Pin name	Pin number	Value
TEST	8	1
TA[5]	206	1
TA[4]	208	1
TA[3]	207	X

Table 4-1. POC Configuration for JTAG test mode

• After switched to JTAG test mode, PCS3X, PCS4X, SBCK, SDAT are changed to input and SLRCK is changed to tri-state output.

Test	Pin Pin Mapping(pin number)
TRST	PCS3X (100)
TCK	PCS4X (101)
TMS	SBCK (102)
TDI	SDAT (103)
TDO	SLRCK (104)

Table 4-2. JTAG Test Port

4.1 TAP Controller

4.1.1 TAP controller interface

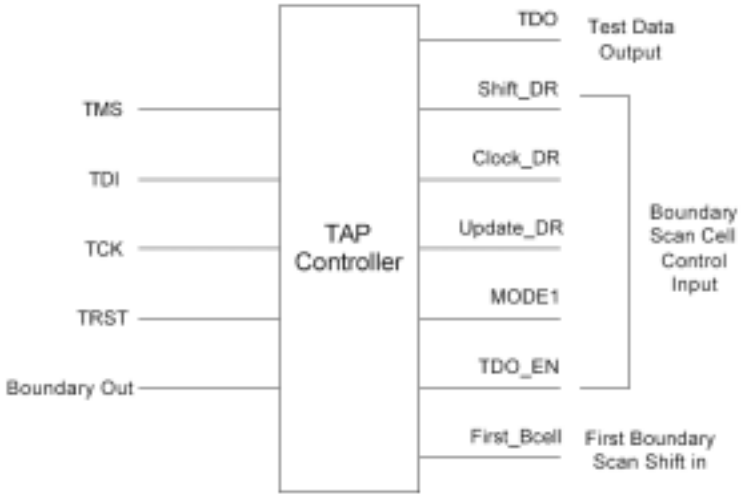


Figure 4.1-1 IN/OUT of TAP Controller

First_Bcell of the above figure is connected to TDI and input data is applied from TDI to first boundary scan. Boundary Out is connected to TDO and output data is observed in TDO. Shift_DR/Clock_DR/Update_DR/MODE1 is control signals of boundary scan cell.

4.1.2 State machine

State machine with 16-state largely consists of four operation RESET, RUN-TEST, SCAN-DR, SCANIR and SCAN-DR/SCAN-IR consist of three main state CAPTURE, SHIFT, UPDATE.
State transition occurs at rising edge of TCK according to TMS.
Instruction Register is controlled at right side of state diagram (SCAN-IR). Input data is applied to TDI at SHIFT-IR state and applied data can be outputted to normal output at UPDATE-IR state and default instruction register (4'b0001) is captured at CAPTURE-IR Control of Data Register (Bypass register or Boundary Scan Chain Register) is same as control of Instruction Register.

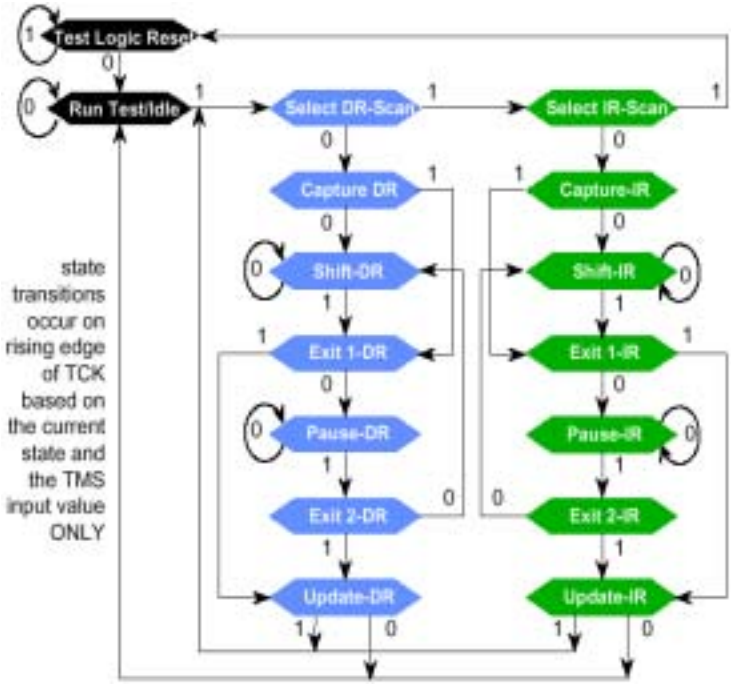


Figure 4.1-2 State diagram of TAP Controller

4.1.3 Boundary Scan Cell

Boundary scan cell is controlled by signals generated from TAP controller and these signals are varied according to state. Boundary scan cell at following figure can be used at input, output, and control pin.

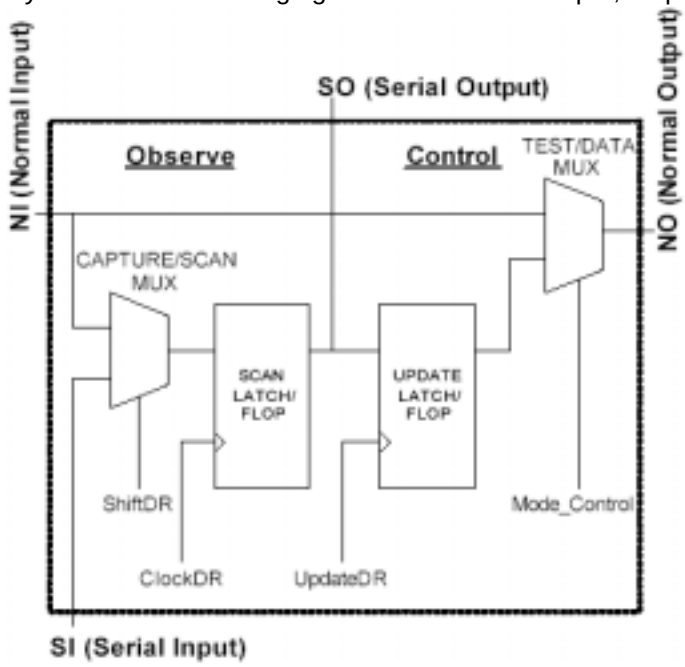


Figure 4.2-1 Boundary Scan cell for observe/control

4.1.4 Instruction Register

Instruction register has commands to control data register and is determined at SHIFT-IR of SCAN-IR.
If you know detail information of each instruction, refer IEEE 1149.1
Instructions that VRenderZERO+ supports and data register according to those are as follow.

Instruction	Binary	Hex	Selected Data Register
EXTEST	0000	0x0	**Boundary Scan Chain Register**
BYPASS	1111	0xF	Bypass Register
SAMPLE/PRELOAD	1011	0xB	Boundary Scan Chain Register
CLAMP	0011	0x3	Bypass Register

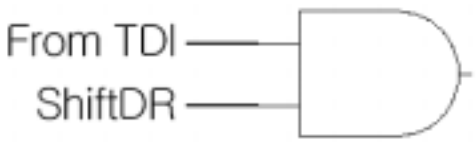
Table 4-3. JTAG Instruction

4.1.5 Data Register

4.1.5.1 Bypass Register

This register is selected by instruction BYPASS/CLAMP and is purposed to skip test of one among several chips.

This register is one-bit shift register



4.1.5.2 Boundary Scan Register

Information about configuration of Boundary scan chain is indicated at VRenderZERO+ bsd. Input/output pin have a boundary scan cell and Bi-directional pin has three boundary scan cells at Input/Output/Control. Bidirectional pin is input when control pin is 0, output when control pin is 1

Following tables show boundary scan register pin map.

Bit	Pin Name and Number			Bit	Pin Name and Number		
1	TX0/PCS1X	Output(1)	105	26	A17/PIO16	Input(34) Output(35) Control(36)	32
2	RX0/PCS2X	Input(2) Output(3) Control(4)	106	27	A18/PIO17	Input(37) Output(38) Control(39)	33
3	TX1/SIOTXD	Output(5)	107	28	A19/PIO18	Input(40) Output(41) Control(42)	34
4	RX1/SIORXD	Input(6)	108	29	A20/PIO19	Input(43) Output(44) Control(45)	35
5	TX1EN/PCS6X	Input(7) Output(8) Control(9)	109	30	A21/PIO20	Input(46) Output(47) Control(48)	36
6	UCLK/PCS7X	Input(10) Output(11) Control(12)	110	31	A22/PIO21	Input(49) Output(50) Control(51)	37
7	PWM/PIO26	Input(13) Output(14) Control(15)	111	32	A23/PIO22	Input(52) Output(53) Control(54)	38
8	BE0X(A0)	Output(16)	9	33	A24/PIO23	Input(55) Output(56) Control(57)	39
9	BE1X	Output(17)	10	34	A25	Input(58) Output(59) Control(60)	42
10	BE2X(A1)	Output(18)	11	35	LSDRCLK	Output(61)	43
11	BE3X/PCS0X	Output(19)	12	36	A26	Input(62) Output(63)	44
12	RA1(A3)	Output(20)	16	37	A27/PIO27	Input(64) Output(65) Control(66)	45
13	RA2(A4)	Output(21)	17	38	A28/SBE0X	Output(67)	46
14	RA3(A5)	Output(22)	18	39	A29/SBE1X	Output(68)	47
15	RA4(A6)	Output(23)	19	40	A30/SBE2X	Output(69)	48
16	RA5(A7)	Output(24)	20	41	A31/SBE3X	Output(70)	49
17	RA6(A8)	Output(25)	21	42	SRASX	Input(71) Output(72) Control(73)	50
18	RA7(A9)	Output(26)	22	43	SCASX	Output(74)	51
19	RA8(A10)	Output(27)	23	44	MCS0X	Output(75)	52
20	RA9(A11)	Output(28)	24	45	EXCSX	Output(76)	53
21	RA10(A12)	Output(29)	25	46	SWEX	Input(77) Output(78) Control(79)	54
22	RA11(A13)	Output(30)	28	47	IRQ0X/PCS5X	Input(80) Output(81) Control(82)	55
23	RA12(A14)	Output(31)	29	48	IRQ1X/PIO24	Input(83) Output(84) Control(85)	56
24	BA0(A15)	Output(32)	30	49	IRQ2X/PIO25	Input(86) Output(87) Control(88)	57
25	BA1(A16)	Output(33)	31	50	ROMCSX	Output(89)	58

Table 4-4. Boundary-scan Register Pin Map (Sheet 1 of 2)

Bit	Pin Name and Number			Bit	Pin Name and Number		
51	RDX	Output(90)	59	69	D15	Input(124) Output(125)	81
52	WRX	Output(91)	60	70	D16	Input(126) Output(127) Control(128)	82
53	IRDYX	Input(92)	61	71	D17	Input(129) Output(130) Control(131)	83
54	D0	Input(93) Output(94) Control(95)	62	72	D18	Input(132) Output(133) Control(134)	84
55	D1	Input(96) Output(97)	63	73	D19	Input(135) Output(136) Control(137)	85
56	D2	Input(98) Output(99)	64	74	D20	Input(138) Output(139) Control(140)	86
57	D3	Input(100) Output(101)	67	75	D21	Input(141) Output(142) Control(143)	87
58	D4	Input(102) Output(103)	68	76	D22	Input(144) Output(145) Control(146)	88
59	D5	Input(104) Output(105)	69	77	D23	Input(147) Output(148) Control(149)	89
60	D6	Input(106) Output(107)	70	78	D24	Input(150) Output(151) Control(152)	90
61	D7	Input(108) Output(109)	71	79	D25	Input(153) Output(154) Control(155)	91
62	D8	Input(110) Output(111)	72	80	D26	Input(156) Output(157) Control(158)	92
63	D9	Input(112) Output(113)	73	81	D27	Input(159) Output(160) Control(161)	93
64	D10	Input(114) Output(115)	74	82	D28	Input(162) Output(163) Control(164)	94
65	D11	Input(116) Output(117)	75	83	D29	Input(165) Output(166) Control(167)	95
	D12	Input(118) Output(119)	76	84	D30	Input(168) Output(169) Control(170)	96
67	D13	Input(120) Output(121)	77	85	D31	Input(171) Output(172) Control(173)	97
68	D14	Input(122) Output(123)	80				

Table 4-5. Boundary-scan Register Pin Map (Sheet 2 of 2)

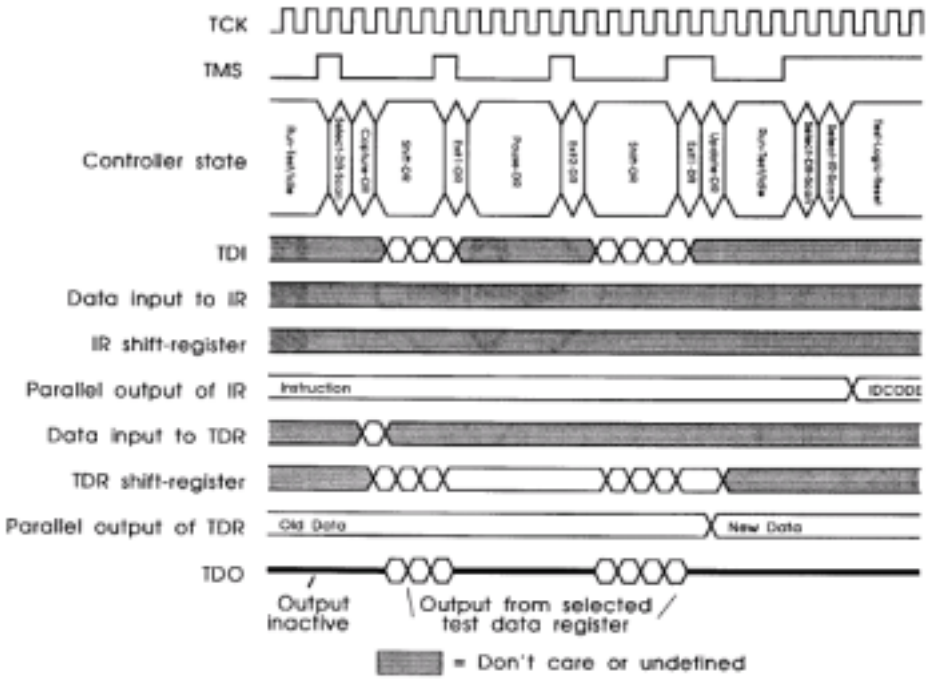
D31 pin is adjacent **to TDI and TX0/PCS1 pin** is adjacent **to TDO.** When data is shift to TDI, data of TX0/PCS1 must be applied first of all.

D0 ~ D15 pins share each control pin and these pins have only input/output boundary scan register. Control pin of D0 determine direction and shared.

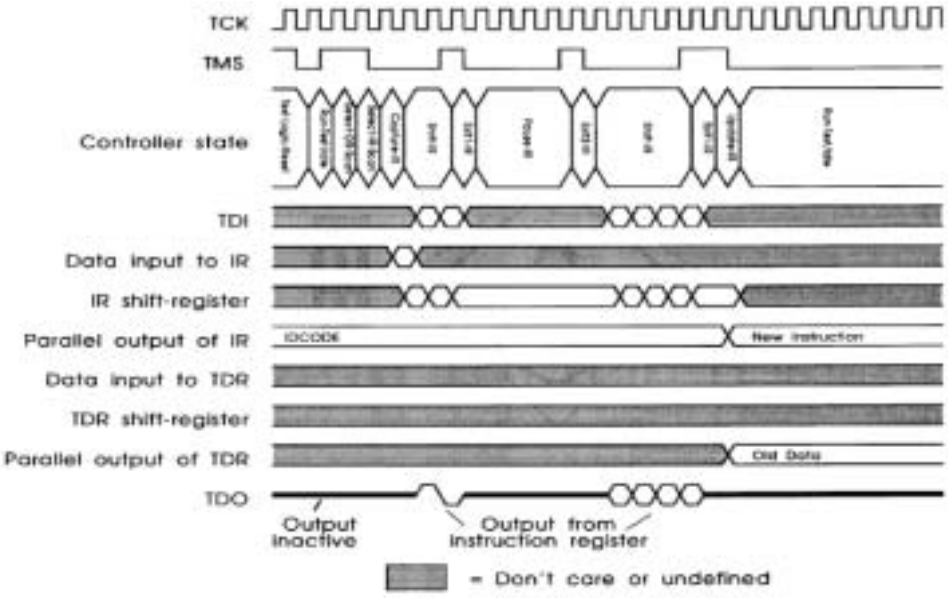
4.1.6 JTAG Operation Sequence

A. Configure POC to switch JTAG Test mode.
B. Apply data to Instruction Register

Apply data to TCK, TMS, and TDI to determine JTAG Instruction. At shift-IR state, apply jtag instruction sequence.
Timing diagram to enter instruction EXTEST is followed.
At SHIFT-IR state, 4'b0000 is applied to TDI during 4 cycles of TCK.



C. Apply Data to Data Register



After instruction register is set to 4'b0000, data register is determined to boundary scan chain register and TAP controller generates signals for controlling Boundary Scan Cell. To apply data to boundary scan cell, state must be switched to SHIFT-DR.
You can apply data to TDI serially to set boundary scan register according to order of Boundary-scan Register Pin Map.

5. Electrical Characteristics

5.1 Absolute Maximum Rating

Parameter	Symbol	Rating		Units
Supply Voltage	V_{DD}/V_{DDA}	– 0.3 to 3.8		V
DC input Voltage	V_{IN}	3.3 V I/O	– 0.3 to V_{DD} + 0.3	V
		5 V-tolerant	– 0.3 to 5.5	
DC input current	I_{IN}	± 10		mA
Operating temperature	T_{OPR}	0 to 70		ºC
Storage temperature	T_{STG}	– 40 to 125		ºC

Table 5-1. Absolute Maximum Rating

5.2 DC Characteristics

Parameter	Symbol	Rating	Units
Supply Voltage	V_{DD}/V_{DDA}	3.0 to 3.6	V
Oscillator frequency	f_{OSC}	10 to 40	MHz
External Loop Filter Capacitance	L_F	820	pF
Commercial temperature	T_A	0 to 70	ºC

Table 5-2. DC Characteristics

NOTES

- ✓ It is strongly recommended that all the supply pins (VDD/VDDA) be powered from the same source to avoid power latch-up.

5.3 DC Electrical Characteristics

VDD=3.3V+/-0.3V, VEXT = 5+/-0.25V, TA=0 to 70 Centigrade (In case of 5V-tolerant I/O)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	LVCMOS interface	V_{IH} (1)	–	2.0	–	–	V
Low level input voltage	LVCMOS interface	V_{IL} (1)	–	–	–	0.8	V
Switching threshold		VT	LVCMOS	–	1.4	–	V
Schmitt trigger positive-going threshold		VT+	LVCMOS	–	–	2.0	–
Schmitt trigger negative-going threshold		VT–	LVCMOS	0.8	–	–	–
High level input current	Input buffer	I_{IH}	$V_{IN} = V_{DD}$	– 10	–	10	µA
	Input buffer with pull-up			10	30	60	
Low level input current	Input buffer	I_{LH}	$V_{IN} = V_{SS}$	– 10	–	10	µA
	Input buffer with pull-up			– 60	– 30	– 10	
High level output voltage	Type B1 to B16 (2)	V_{OH}	I_{OH} = – 1uA	V_{DD} – 0.05	–	–	V
	Type B1		I_{OH} = – 1 mA	2.4			
	Type B2		I_{OH} = – 2 mA				
	Type B4		I_{OH} = – 4 mA				
	Type B6		I_{OH} = – 6 mA				
Low level output voltage	Type B1 to B16 (2)	V_{OL}	I_{OL} = – 1uA			0.05	V
	Type B1		I_{OL} = – 1 mA			0.4	
	Type B2		I_{OL} = – 2 mA				
	Type B4		I_{OL} = – 4 mA				
	Type B6		I_{OL} = – 6 mA				
Tri-state output leakage current		I_{OZ}	$V_{OUT} = V_{SS}$ or V_{DD}	– 10		10	µA
Maximum operating current		I_{DD}	V_{DD} = 3.3 V, f_{MCLK} = 40MHz				mA

Table 5-3. DC Electrical Characteristics

NOTES:
1. All 5V-tolerant input have less than 0.2V hysterisis.
2. Type B1 means 1mA output driver cells, and Type B6/B24 means 6mA/24mA output driver cells.

5.4 AC Electrical Characteristics

(Ta = 0 to +70 Centigrade, Vdd = 3.0V to 3.6V, LSDRCLK = 40MHz)

Signal Name	Description	Min	Typ	Max	Unit
f_{EXTCLK}	EXTCLK input frequency when not using PLL	0		80	MHz
f_{PLLIN}	EXTCLK input frequency for PLL		14.318		
t_{ADDR}	Address delay time			6.1	ns
t_{NCS}	ROM/SRAM or external I/O bank chip select delay time			4.3	
t_{NOE}	ROM/SRAM or external I/O bank output enable delay			2.5	
t_{NWE}	ROM/SRAM or external I/O bank write enable delay			2.6	
t_{RDh}	Read data hold time	3.0			
t_{WD}	Write data delay time (SRAM or external I/O)			6.8	
t_{WS}	WAITX sampling setup time	0			
t_{WH}	WAITX sampling hold time	3.0			
T_{NRASD}	DRAM row address strobe active delay			2.8	
t_{NCASD}	DRAM column address strobe active delay			3.0	
t_{NDWE}	DRAM bank write enable delay time			2.0	
t_{WDD}	DRAM write data delay time (DRAM)			4.1	

Table 5-1. Local BUS Timing Characteristics

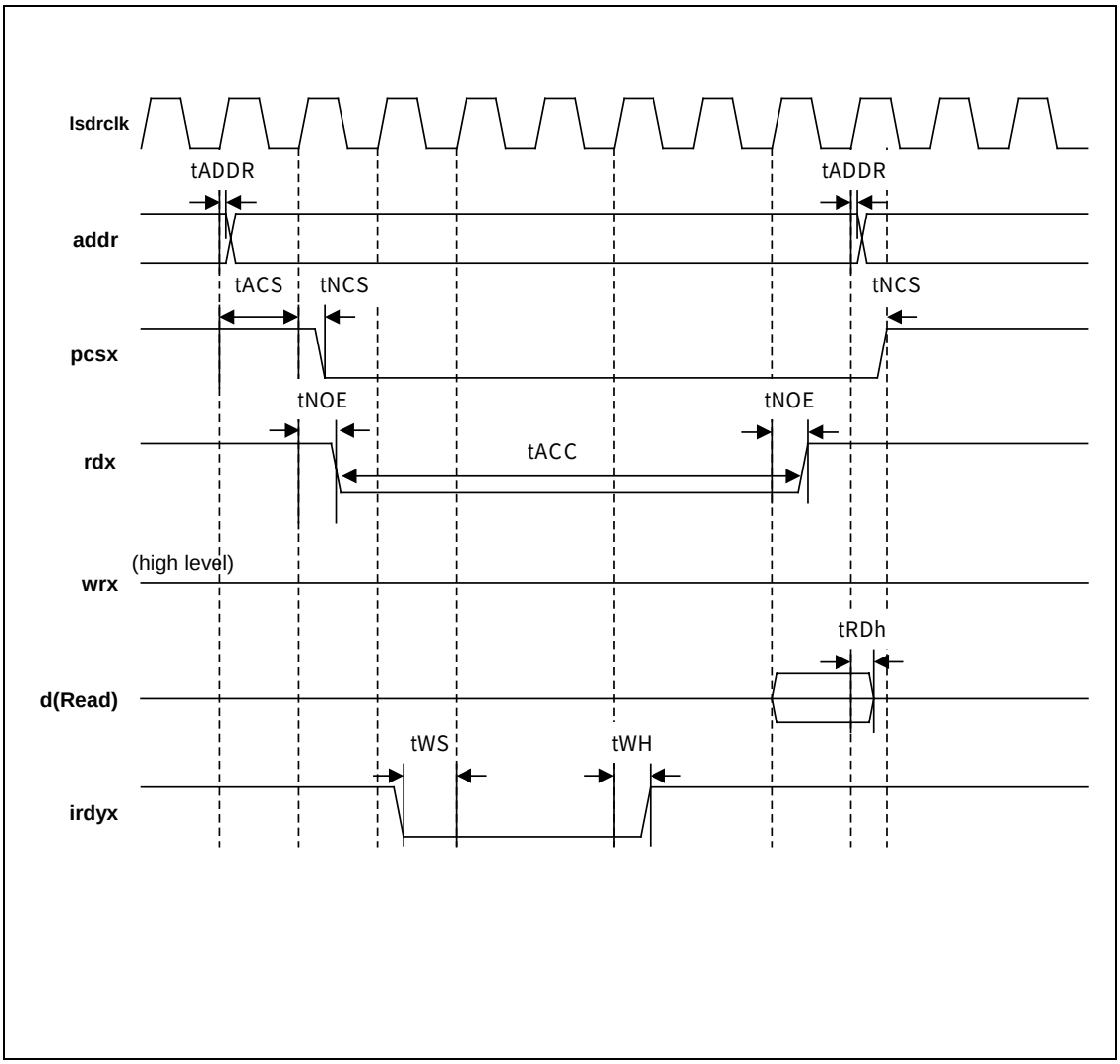


Figure 5.4-1 External I/O, ROM Read Timing with Wait (irdyx) (t_{ACC} = programmable, t_{ACS} = 1)

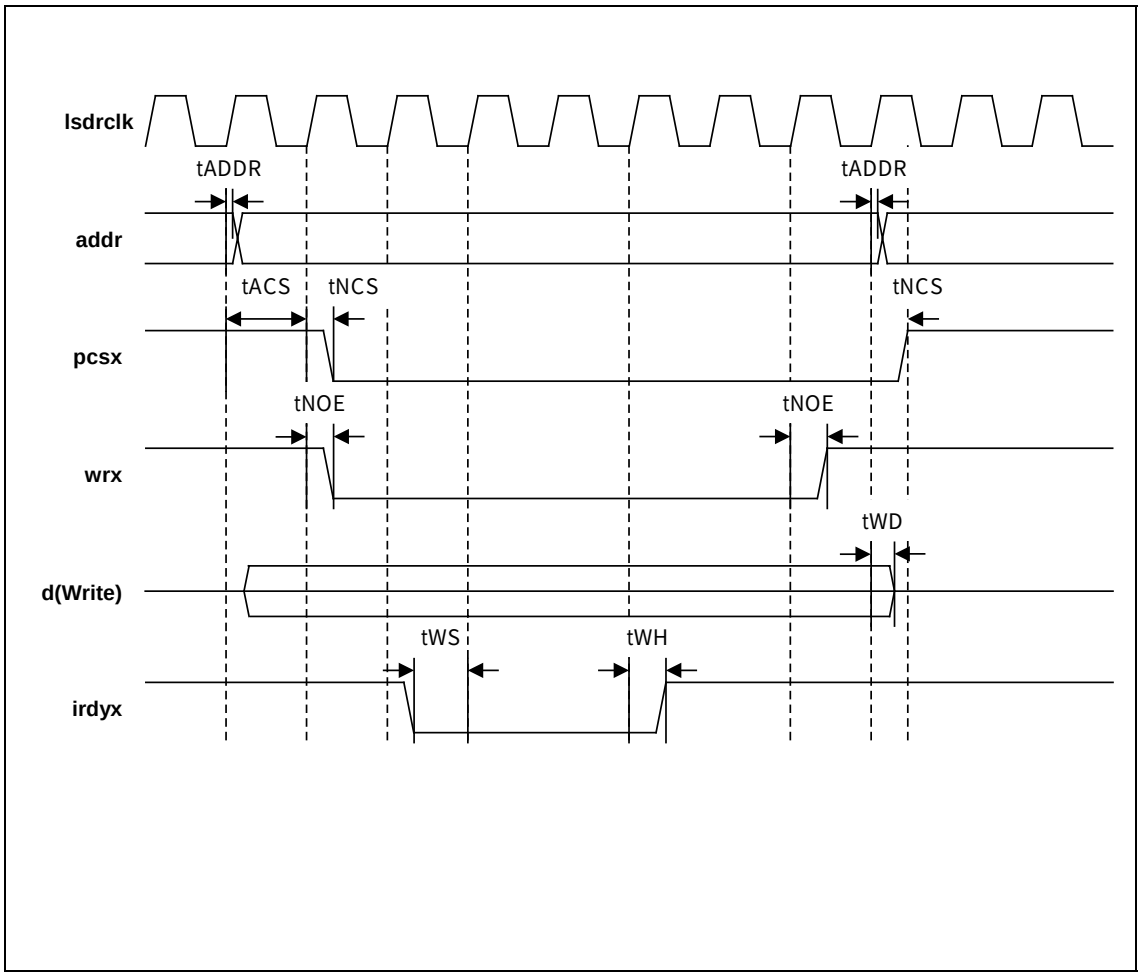


Figure 5.4-2 External I/O, ROM Write Timing with Wait (irdyx) : (t_{ACC} = programmable, t_{ACS} = 1)

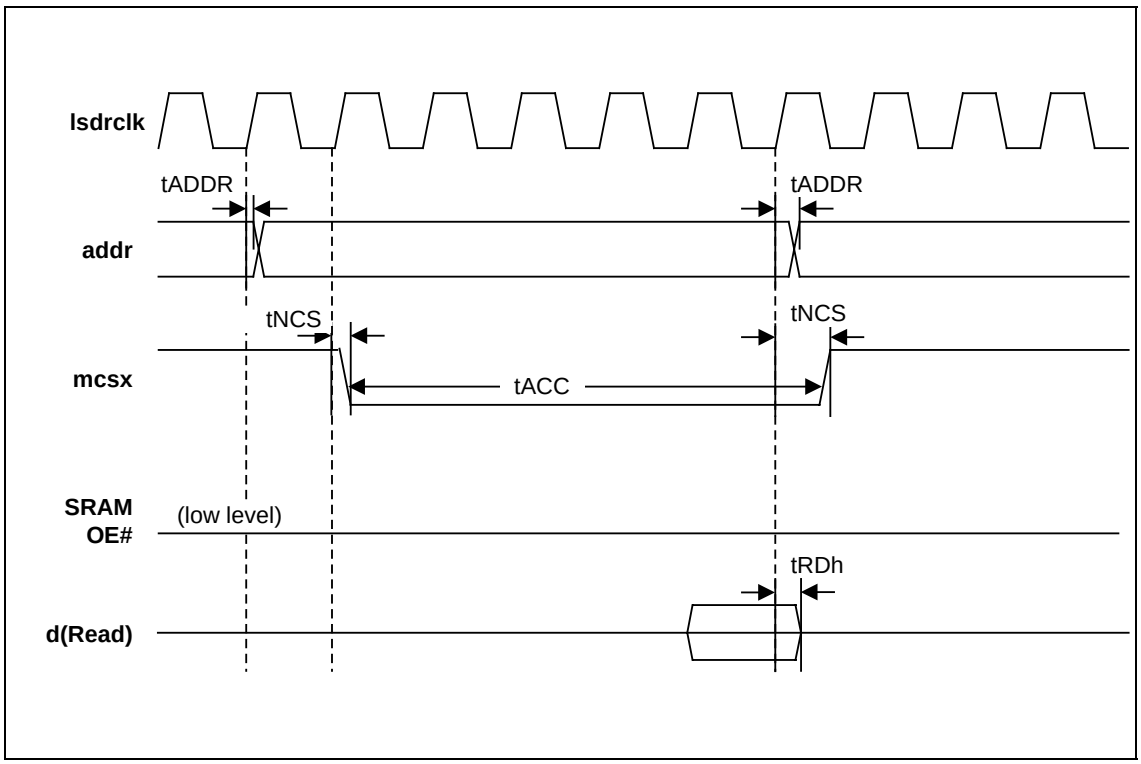


Figure 5.4-3 SRAM Read Access Timing (t_{ACC} = programmable)

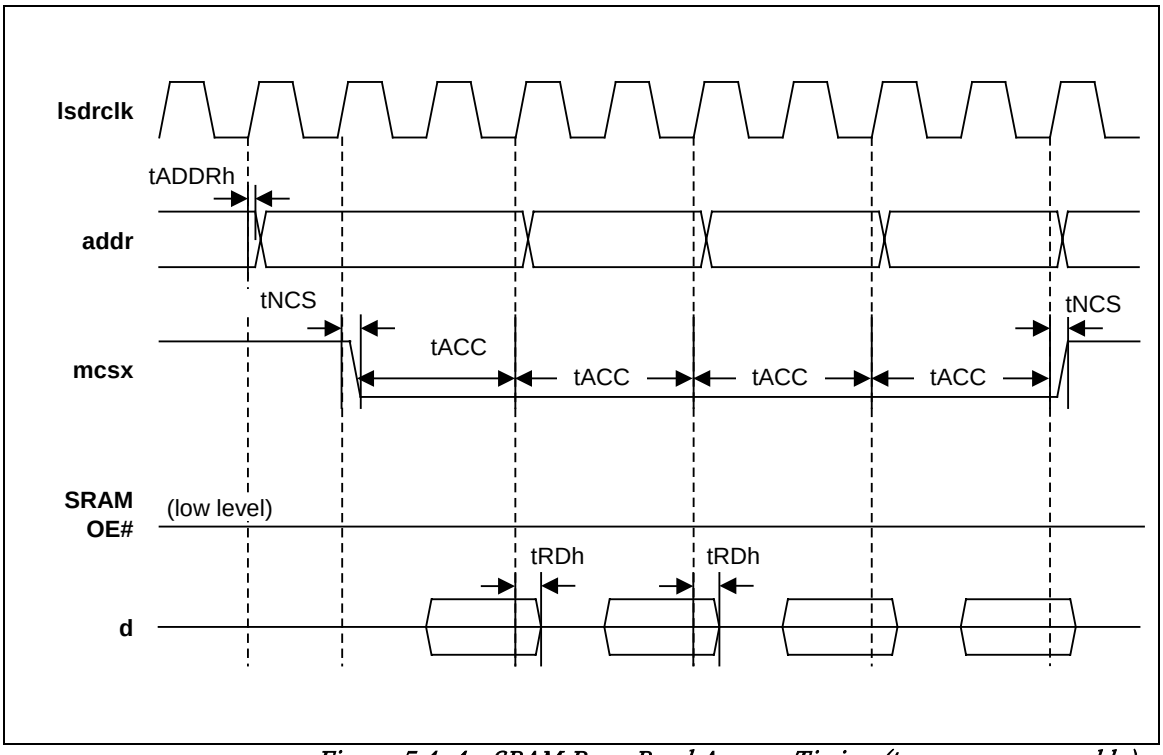


Figure 5.4-4 SRAM Page Read Access Timing (t_{ACC} = programmable)

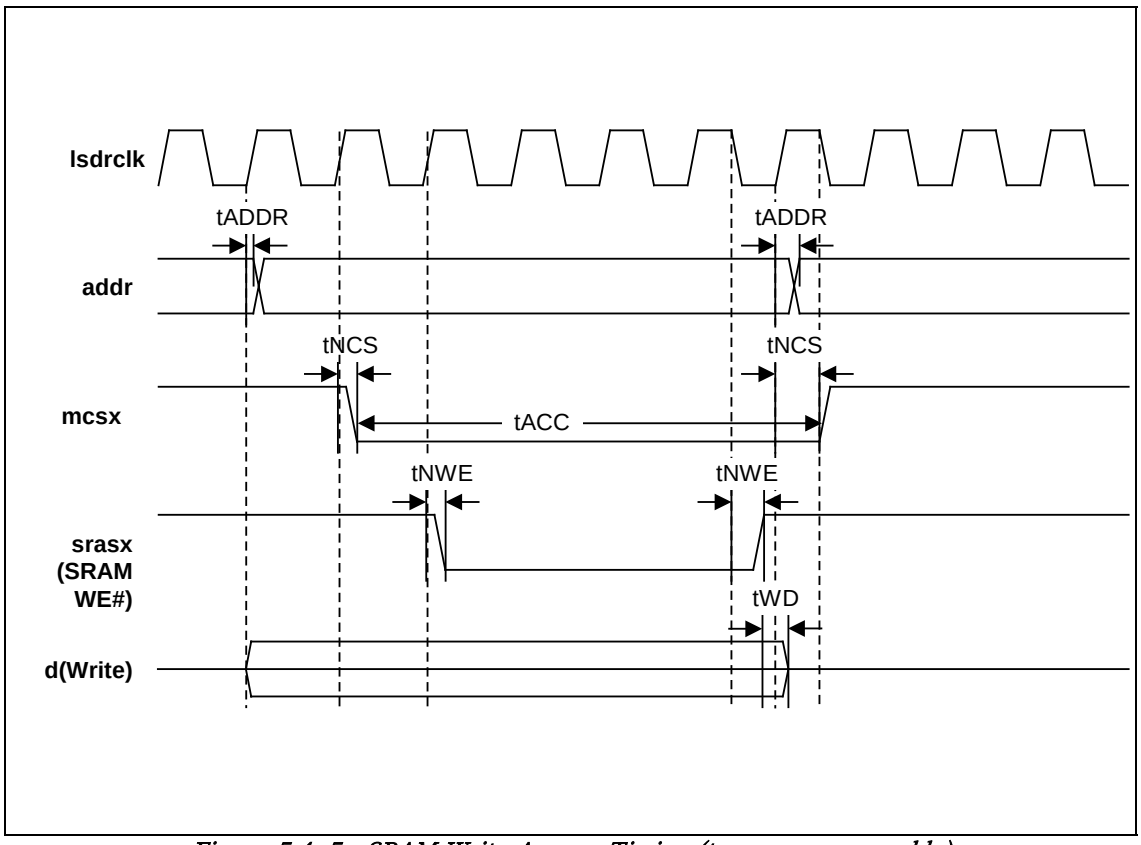


Figure 5.4-5 SRAM Write Access Timing (t_{ACC} = programmable)

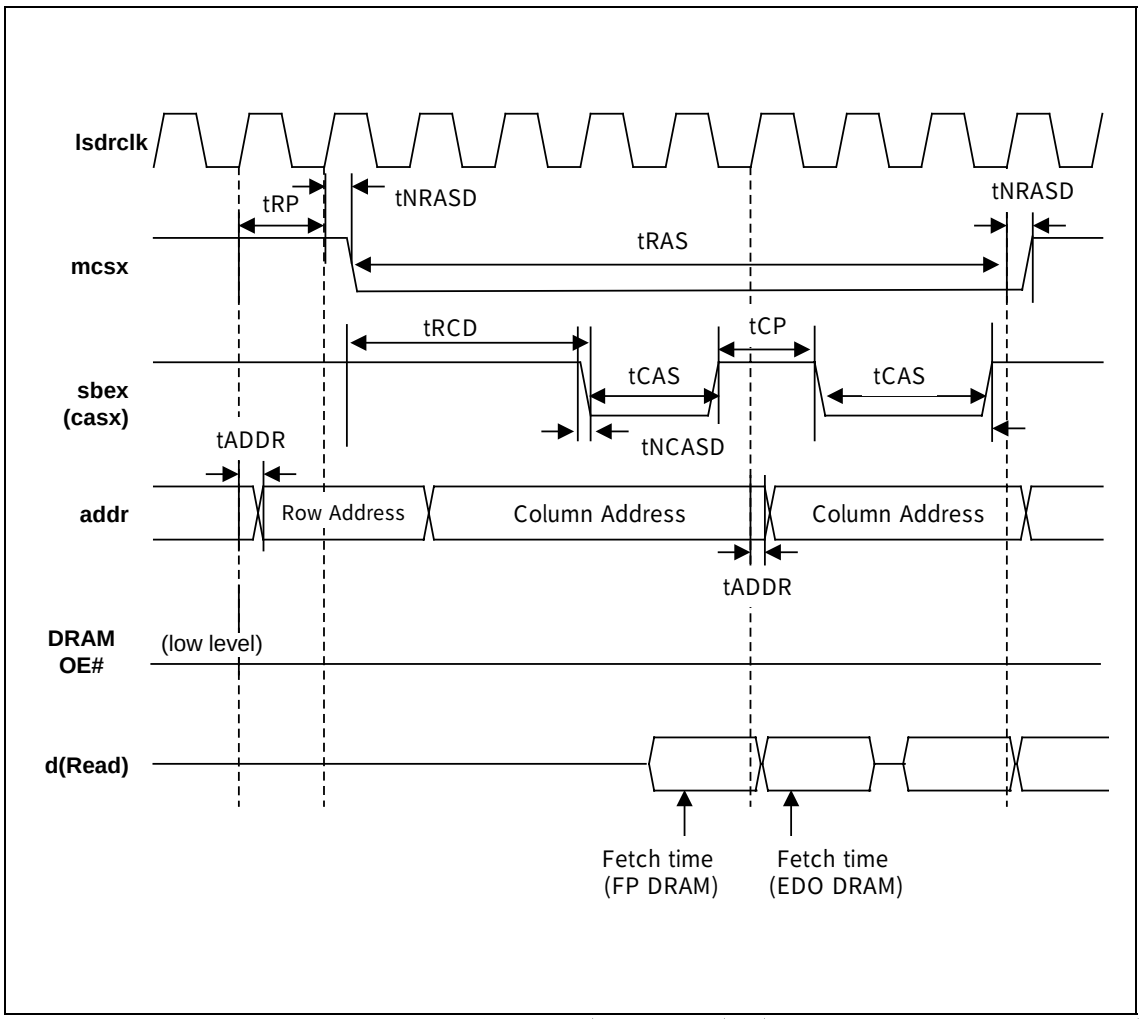


Figure 5.4-6 EDO/FP DRAM Bank Read Timing (Page Mode) : (t_{RAS}, t_{RP}, t_{CAS}, t_{CP} = programmable)

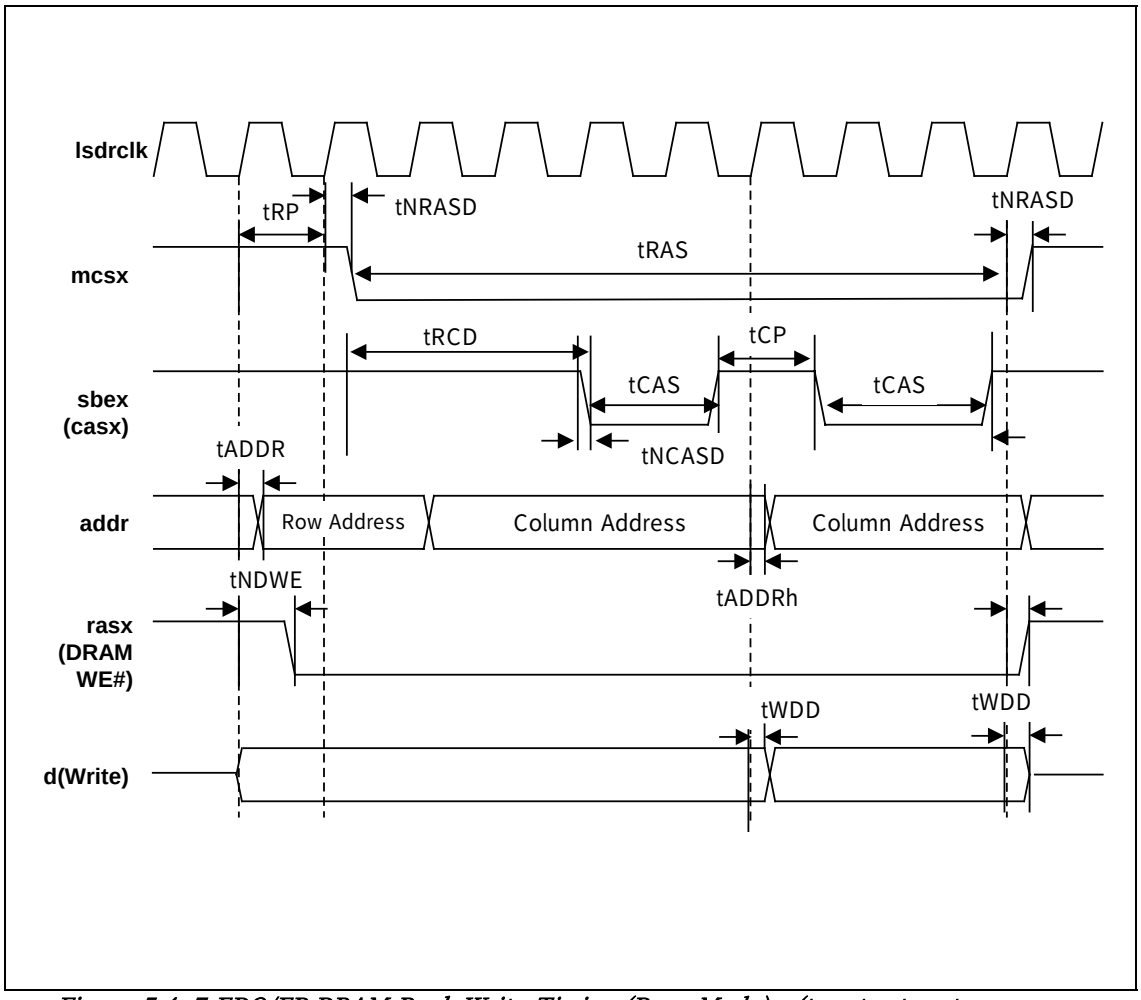
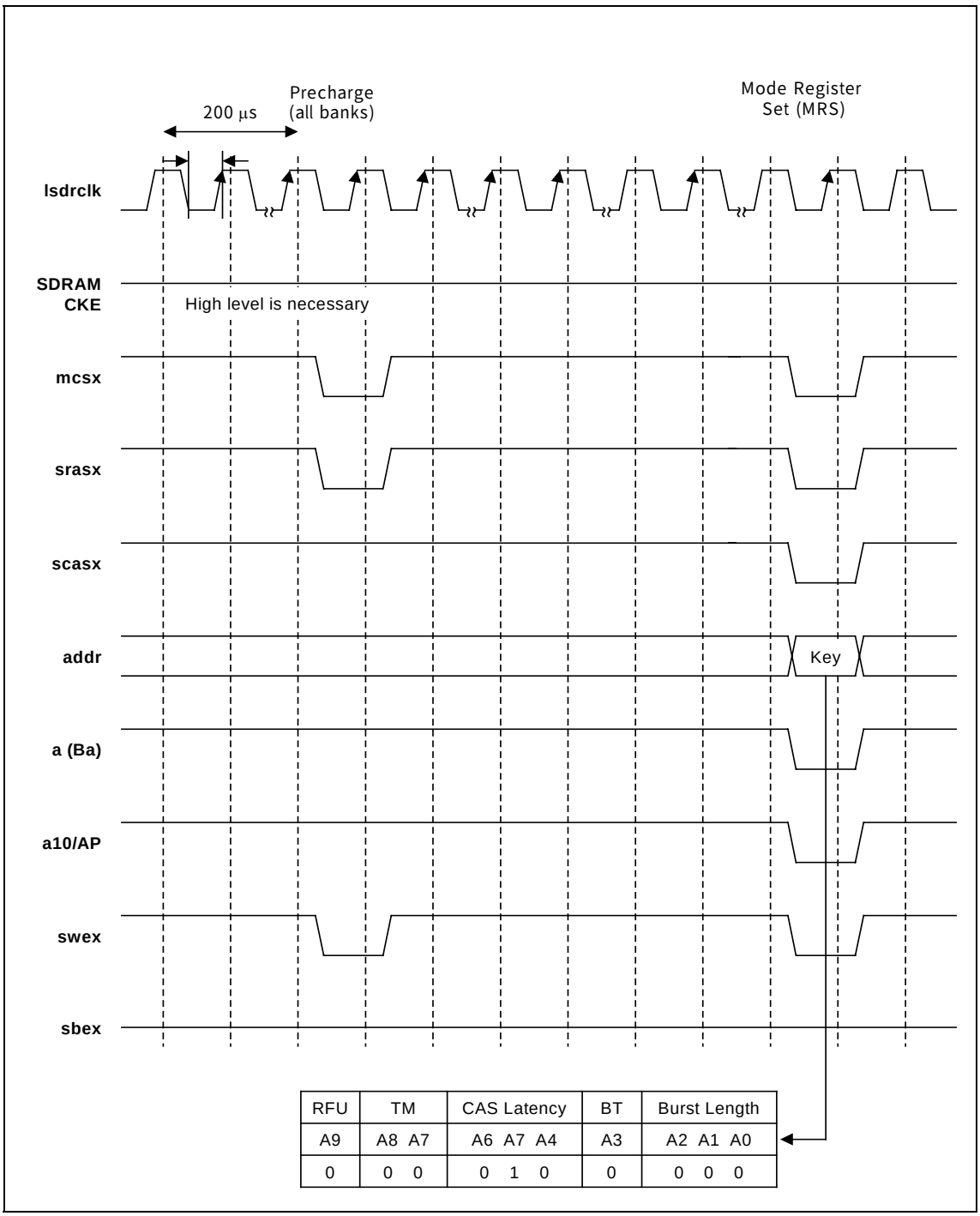


Figure 5.4-7 EDO/FP DRAM Bank Write Timing (Page Mode) : (t_{RAS}, t_{RP}, t_{CAS}, t_{CP} = programmable)



RFU	TM	CAS Latency	BT	Burst Length
A9	A8 A7	A6 A7 A4	A3	A2 A1 A0
0	0 0	0 1 0	0	0 0 0

Figure 5.4-8 SDRAM Power-up Sequence

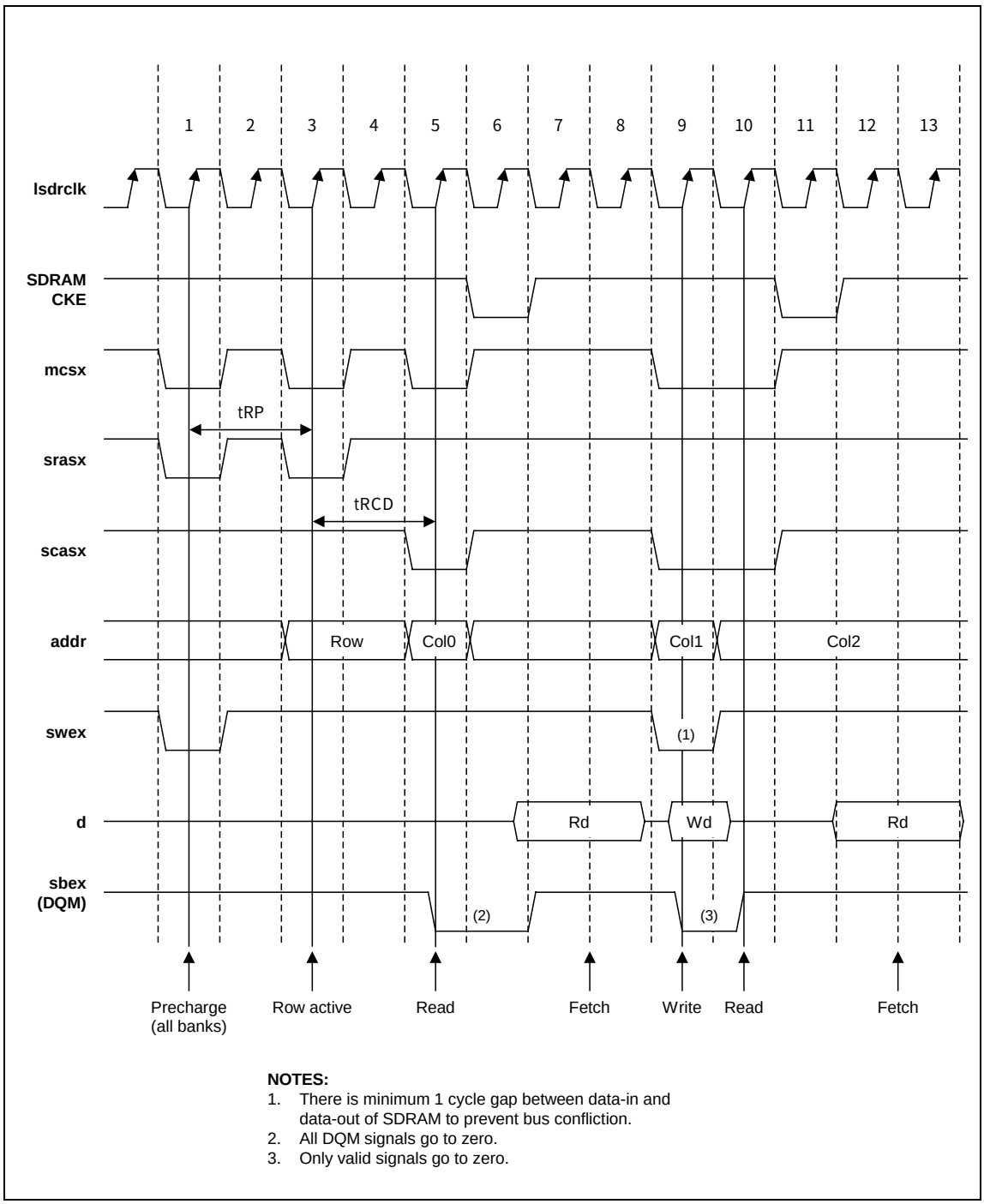


Figure 5.4-9 Non-burst, Read-Write-Read Cycles @CAS Latency = 2, Burst Length = 1 (t_{RP}, t_{RCD} = programmable)

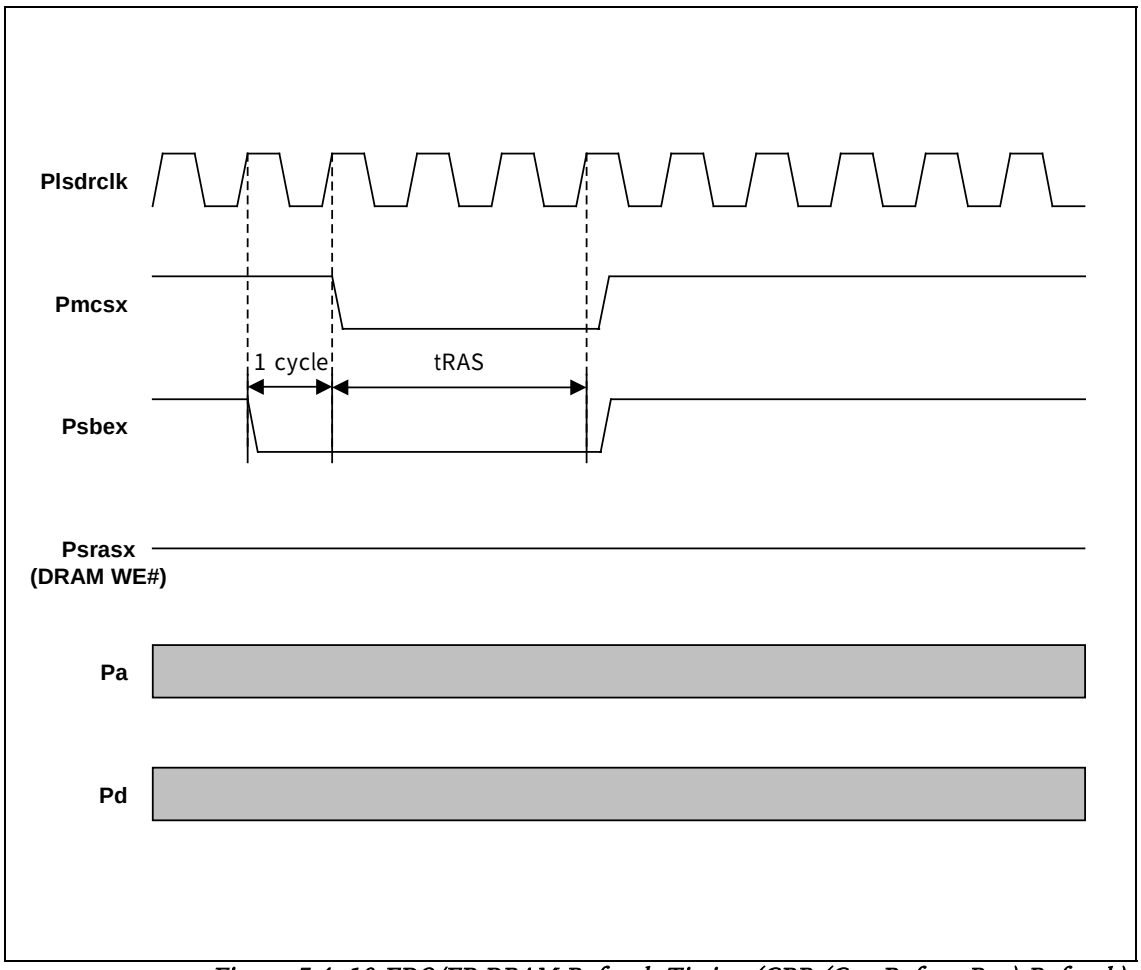


Figure 5.4-10 EDO/FP DRAM Refresh Timing (CBR (Cas Before Ras) Refresh)

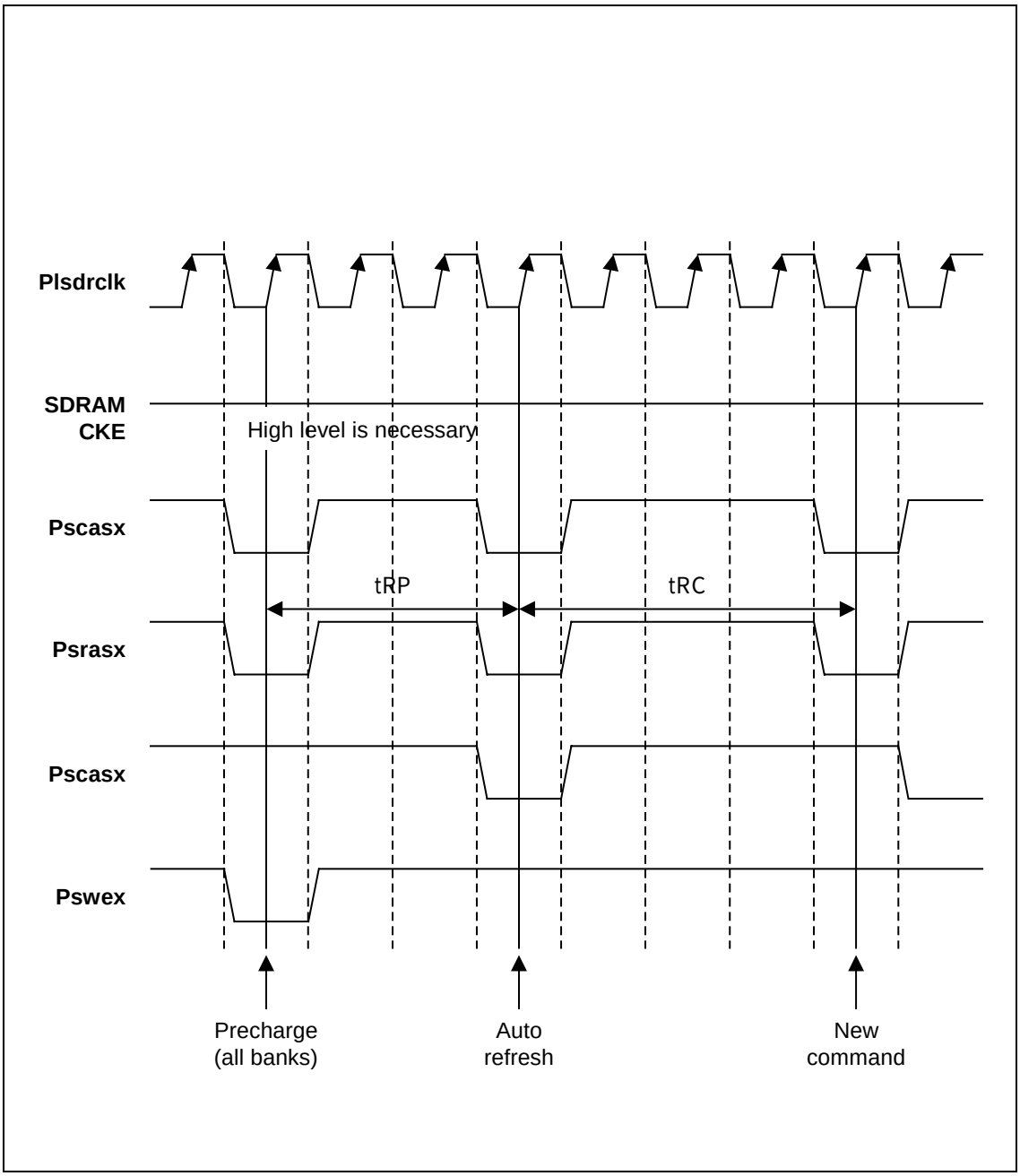


Figure 5.4-11 Auto Refresh Cycle of SDRAM (t_{RP}, t_{RCD} = programmable)