Low Temperature Single Grain Thin Film Transistor (LTSG-TFT) with SOI Performance Using CMP-Flattened μ-Czochralski Process

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Abstract

We succeeded in fabricating low temperature single grain thin film transistor (LTSG-TFT) devices with excellent characteristics by using the CMP-flattened μ-Czochralski process for 3-D integrated circuits application. The LTSG-TFT devices demonstrated high drivability comparable to that of SOI-MOSFETs and an excellent gate delay time of 65psec was obtained despite the use of fully low temperature processing.

Introduction

High-performance thin film transistors (TFTs) have long been recommended for 3-dimensional (3-D) integrated circuits [1-6]. Such 3-D circuits provide revolutionary improvements in circuit performance and compactness by using shortened vertical connections [7,8]. The most difficult challenge faced in developing this 3-D technology is the formation of high quality single crystalline silicon film on an insulating material. On the other hand, we should consider that fully low temperature processing is crucial for realizing truly 3-D devices due to difficulties in controlling the thermal budget at all semiconductor layers and interconnect electrodes, especially in scaled MOSFETs.

In this work, we have developed a scaled low temperature single grain thin film transistor (LTSG-TFT) by using position-controlled single grain growth using the μ-Czochralski grain filter process, which realizes mobility exceeding 500cm^2/Vsec [9]. In addition, chemical mechanical polishing (CMP) was used on the laser-crystallized silicon film to adjust it to the desired thickness and obtain a perfectly flat surface for quarter-μm scaling. The LTSG-TFT devices exhibit excellent characteristics comparable to those of SOI devices, despite the fully low temperature processing. Therefore, we believe that this technology can be used to realize high performance 3-D integrated circuits, as well as scaled TFTs on glass substrates for LCD projectors.

Experiments

First of all, a thick TEOS-SiO_2 layer was deposited on a 6-inch Si wafer. Semiconductor film was then formed on the SiO_2 layer. In this experiment, a relatively thick (~150nm) amorphous silicon (a-Si) film was deposited at 550˚C, followed by formation of 0.1μm holes in the thick SiO_2 layer, the holes serving as a grain filter. After that, the a-Si film was crystallized by a XeCl excimer laser (308nm) with an energy density of 1.6J/cm^2 at a substrate temperature of 400˚C. As a result, a filtered single grain can be grown to more than 5μm in diameter. This procedure for forming crystalline Si (c-Si) film is called the μ-Czochralski (grain filter) process [9](Fig. 1). As shown in Fig. 2, the surface morphology of the crystallized Si film was very rough due to a difference in volume density between the a-Si and c-Si. The surface roughness needs to be minimized to maintain high mobility in a high electric field region [10]. Furthermore, it is well known that the thickness of the Si film needs to be adjusted (thinned) to avoid punch-through [11]. Therefore we tried to adopt a CMP process with an optical end-point detecting system for use with the crystallized Si film. A thin gate oxide was prepared by radical oxidation, the oxidizing rate of which is not dependent on the Si surface orientation, using a high density microwave excited plasma of krypton and oxygen at 400˚C [12]. A low resistive Tantalum (Ta) and Tantalum Nitride (TaNx) multi layer system as a metal gate electrode was sputtered by using Xenon or Xenon/Nitrogen gases to suppress plasma-induced damage [13]. Then, highly selective etching of Ta/ TaNx gate films to thin gate oxide using NF_3 and $SiCl_4$ gas mixture plasma was

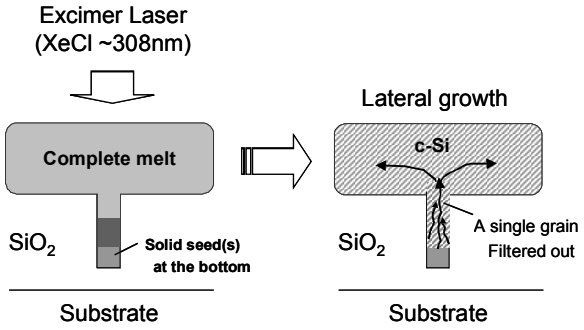

Fig. 1 Schematic of μ-Czochralski grain filter process

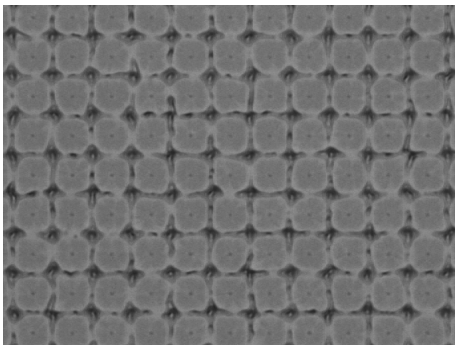

Fig. 2 Photograph of crystallized Si film formed by μ-Czochralski process with a tiled array of grain filter at intervals of 5μm.

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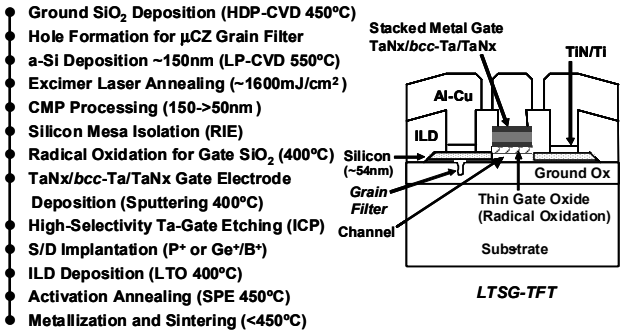


Fig. 3 Process flow of the LTSG-TFT device using fully low-temperature processing

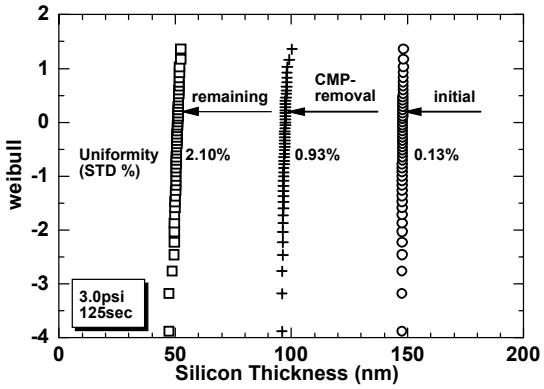
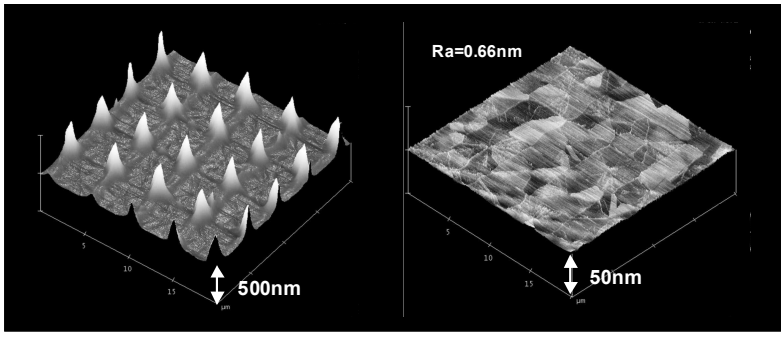


Fig. 4 Uniformity of a-Si film using optimized CMP flattening process with end-point detecting system

performed [14]. Finally, the source/drain region was formed by ion implantation and annealing at 450°C using the solid phase epitaxy (SPE) method [15]. Fig. 3 shows a process flow of the LTSG-TFT devices using fully low temperature processing.

Results and Discussions

We have confirmed that the surface roughness of the crystallized silicon film can be improved dramatically by CMP processing with mildly alkaline slurry for final polishing of a silicon wafer. Moreover the end-point at a desired thickness can be successfully detected by optical wavelength signals, even though only a very thin layer of silicon film was removed. This optimization produced an a-Si film with a thickness of 50±2.6nm, as shown in Fig. 4. Fig. 5 shows atomic force microscope (AFM) images of the crystallized Si film surface before and after CMP processing. We can see that the surface roughness has been dramatically improved, resulting in Ra of 0.66nm. Fig. 6 shows an electron back-scatter diffraction (EBSD) analysis of the crystallized Si film after CMP processing with a tiled array of grain filter at intervals of 5µm. No random grain boundaries have been observed within the single grains. Fig. 7 shows an SEM image of an LTSG-TFT with L/W of 0.25/0.50µm. We can see that a single grain covers the entire channel area of the TFT. Fig. 8 (a) and (b) compare the subthreshold characteristics of nMOS and pMOS transistors (L/W=0.25/0.50µm, Tox=5nm, Si film=54nm), respectively, between the fabricated LTSG-TFT and a low temperature SOI MOSFET (LT-SOI) fabricated with the same procedure except for a silicon film preparation. In the nMOS graph, a conventional low temperature polysilicon (LTPS) TFT using a line-beam excimer laser annealing with an energy density of 500mJ/cm^2 are also described for comparison. A significant improvement was observed in the LTSG-TFT, which is comparable to the LT-SOI. Fig. 9 compares the output characteristics of the LTSG-TFT and the LT-SOI. Excellent current drivability was observed, including gm=300mS/mm and Idsat=350µA/µm at Vg-Vth=1.3V for nMOS, which is comparable to the performance of a conventional SOI-MOSFET and much better than other reported LTPS-TFTs. Fig. 10 shows the subthreshold characteristics of a long channel LTSG-nTFT device with a linear array of grain filter at



(a) Before CMP process (b) After CMP process

Fig. 5 Atomic Force Microscope (AFM) images of the crystallized Si film surface

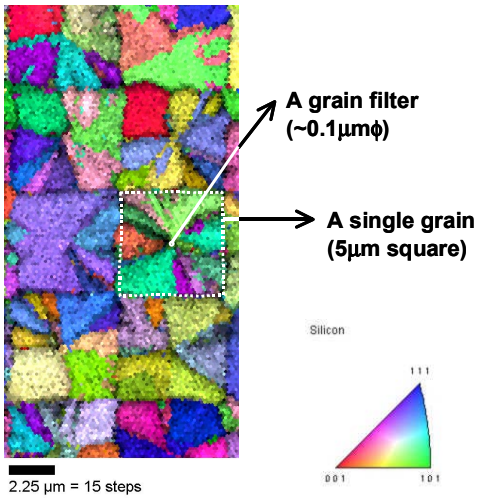


Fig. 6 EBSD analysis of crystallized Si film after CMP processing.
No random grain boundaries have been observed within an each grain.

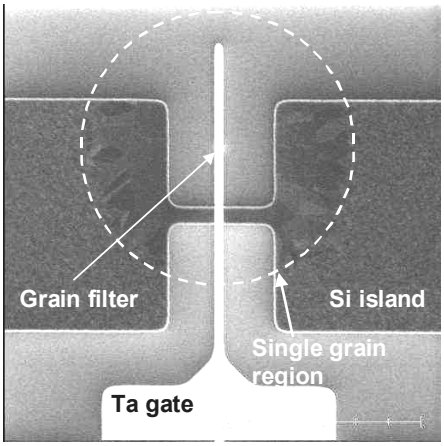


Fig. 7 SEM image of LTSG-TFT with L/W of 0.25/0.50μm

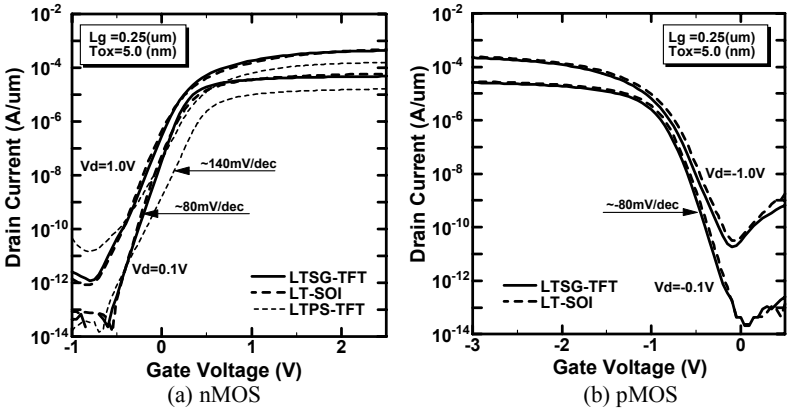


Fig. 8 Subthreshold characteristics of transistors between fabricated LTSG-TFT and LT-SOI MOSFET. In the nMOS graph, characteristics of conventional LTPS-TFT are also described.

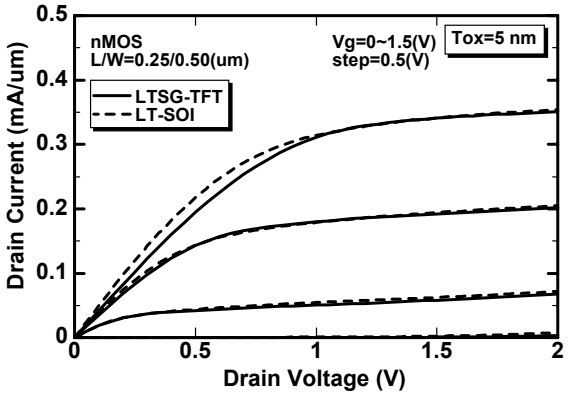


Fig. 9 Output characteristics between LTSG-nTFT and LT-SOI nMOSFET. Both drain currents are almost the same.

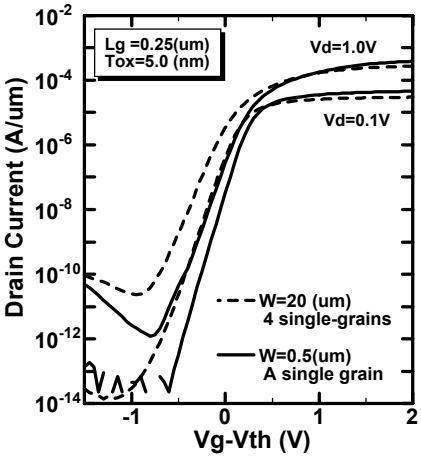


Fig.10 Subthreshold characteristics of a long channel (20μm) LTSG-nTFT device including four single-grains, together with a single-grain device (0.5μm) for comparison

intervals of 5μm (W=20μm) including four single-grains, as shown in Fig. 11, together with a single grain LTSG-nTFT for comparison. Slight off-current increase was observed mainly due to a random grain boundaries effect [4]. The performance with around 30% drive current degradation was also observed, which could be due to surface orientation mixing. A 101-stage ring oscillator using 0.25μm LTSG-CMOS with a tiled array of grain filter at intervals of 5μm (width (n/p)=10/20μm, shown in Fig. 12), however, can be demonstrated successfully as shown in Fig. 13. The LTSG-CMOS and conventional LTPS-CMOS device propagation gate delay time (Tpd) dependence on Vdd are shown in Fig. 14. Excellent Tpd of less than 100psec (65psec at Vdd=2.0V with 4nm-Tox, which, to our knowledge, is the highest speed ever achieved for a TFT CMOS device) was observed despite the use of fully low temperature processing.

Conclusion

We succeeded in fabricating LTSG-TFT devices with excellent characteristics by using the CMP-flattened μ-Czochralski process. The LTSG-TFT devices demonstrated high drivability comparable to that of SOI-MOSFETs. Furthermore, the gate delay time of 65psec at Vdd=2.0V with LTSG-TFT CMOS (Lg=0.25μm, Tox=4nm) makes these the fastest TFT CMOS devices to our knowledge, even though they were obtained via a fully low temperature process. We believe that this technology can be used to realize ultra-scaled high performance 3-D integrated circuits and TFTs on glass substrates for super high resolution LCD projectors. In addition, this technology could be applied for SUFTLA technology [16], which provides a flexible sheet computer on a plastic substrate.

Acknowledgements

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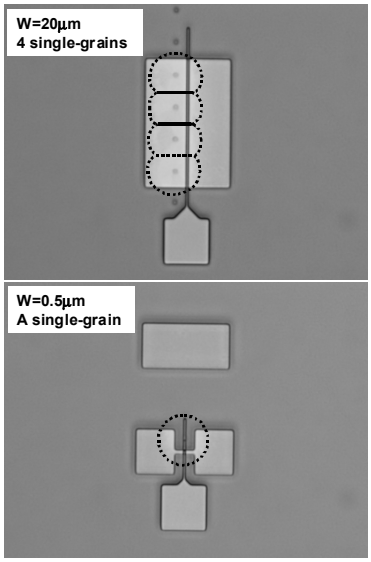

Fig. 11 Photographs of 0.25μm LTSG-TFT with four single-grains (W=20μm) and a single grain (W=0.5μm)

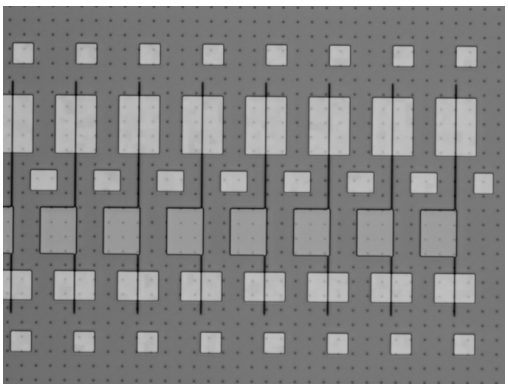

Fig.12 SEM image of 101-stage ring oscillator (partly magnified view) using LTSG-CMOS with a tiled array of grain filter at intervals of 5μm. (W(n/p)=10/20μm)

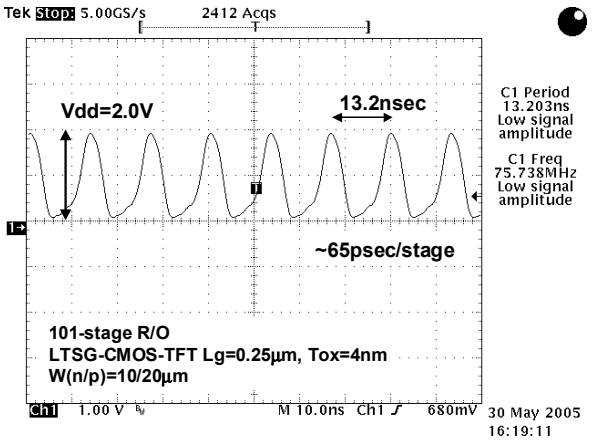

Fig. 13 Waveform of 101-stage ring oscillator at Vdd of 2.0V using 0.25μm LTSG-CMOS with a tiled array of grain filter.

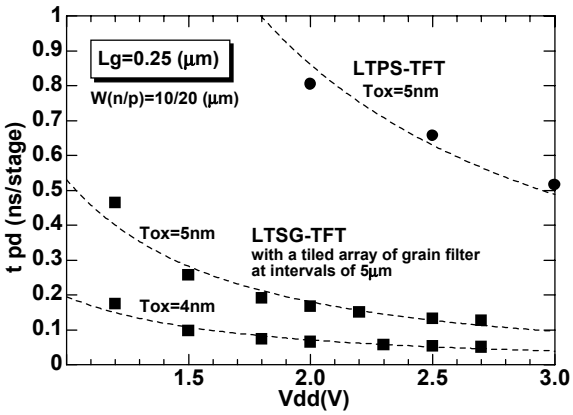

Fig. 14 LTSG-CMOS-TFT and conventional LTPS-CMOS-TFT device propagation delay time on Vdd

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