

6.4 Single-Chip RF CMOS UMTS/EGSM Transceiver with Integrated Receive Diversity and GPS

A. Hadjichristos¹, M. Cassia¹, H. Kim², C.H. Park², K. Wang¹, W. Zhuo¹, B. Ahrari², R. Brockenbrough², J. Chen², C. Donovan², R. Jonnalagedda², J. Kim², J. Ko², H. Lee², S. Lee², E. Lei², T. Nguyen², T. Pan², S. Sridhara¹, W. Su¹, H. Yan¹, J. Yang², C. Conroy², C. Persico¹, K. Sahota¹, B. Kim²

¹Qualcomm, San Diego, CA, ²Qualcomm, Santa Clara, CA

The large commercial success of multiband multimode 3rd-generation cellular products has driven single-chip integration, SAW-filter reduction and low power consumption. State-of-the-art solutions require quad-band EGSM combined with multiband WCDMA/HSPA receiver diversity and integrated GPS. Compact form factors make single-chip SAW-less solutions highly desirable. A Quad-Band GSM/EDGE-only transceiver was published in [1], and Triple-Band WCDMA-only transceiver solutions were published in [2-4]. This work describes the first multiband WCDMA/HSPA/EGPRS single-chip transceiver with GPS and receiver diversity. This device supports UMTS Bands 1,2,3,4,5,6,8,9,10 and GSM/EDGE 800, 900, 1800, 1900MHz Bands. It is implemented in cost-effective 0.18 μ m RF CMOS technology and uses a reduced number of TX and RX SAW filters.

A detailed block diagram is shown in Fig. 6.4.1. This transceiver consists of a GSM TX/RX and UMTS TX $\Delta\Sigma$ PLL, an EGSM/UMTS linear-I/Q direct-conversion transmitter chain with single-ended outputs, a quad-band direct-conversion EGSM receiver, a WCDMA RX $\Delta\Sigma$ PLL, a WCDMA 4-LNA Primary Receiver having two Saw-less paths, a WCDMA 3-LNA Saw-less diversity receiver and a GPS receiver. Figures 6.4.3 and 6.4.4 show system-level performance data measured at the antenna port of a reference phone that utilizes the described transceiver and supports QB GSM/EDGE, QB WCDMA with receiver diversity and GPS.

The transmitter [5] is divided into two distinct signal paths, one for low frequency bands (824 to 915MHz) and one for high frequency bands (1710 to 1980MHz). The two paths share a common Baseband Filter and Baseband Amplifier while separate mixers are used for GSM and WCDMA/CDMA in order to optimize current consumption and noise performance. The transmitter uses on-chip baluns, integrates part of the output matching network and has 5 single-ended outputs. A simplified circuit diagram is shown in Fig. 6.4.2. An RF filter is placed between the upconverter and VGA to suppress high-order harmonics in GSM operation.

Three single-bit 3rd-order $\Delta\Sigma$ fractional PLLs are used in this transceiver [1]. The first PLL provides GSM RX, and GSM/WCDMA TX LO signals. Two different VCOs and dividers in the first synthesizer optimize performance and power consumption for GSM/EDGE and WCDMA TX. PFD, CP and loop filter in the first synthesizer are shared between GSM and WCDMA TX. The reference spurs in GSM mode are less than -105 dBc, which fulfills the GSM RX band-noise specification without any external filters as shown in Fig. 6.4.3. The RX band noise is clearly less than the -79dBm specification and uses none of the five spurious response exceptions allowed by the GSM standard. The second PLL generates the WCDMA primary and diversity RX LO signals. The third PLL creates the GPS LO signals. On-chip regulators are used in the three PLLs to meet spur and phase-noise performance. Each regulator is designed to meet both high- and low-frequency PSRR and achieves good noise filtering and spur rejection. Each PLL uses only one external component for its loop filter. It is very important that spurs from one system do not affect the other system in this multimode transceiver. Careful synthesizer programming avoids or minimizes any fractional spurs.

The GSM RX path consists of an RX front-end (RXFE) and a programmable-gain low-pass filter (PG LPF). The LNA has four inputs (850, 900, 1800, and 1900MHz). In each band, the two input stages share one output LC load and mixer. An RC filter placed between the mixers and PG LPF attenuates noise and jammers. The PG LPF is a 5th-order custom filter with a programmable bandwidth (125 to 155 KHz) and gain of max 80dB. An on-chip RC tuner uses the reference clock to tune the filter response with an accuracy of $\pm 3\%$. To prevent each stage of the PG LPF from saturation by DC offset (DCO), current

DACs and a digital state-machine calibrate the DCO stage-by-stage [1]. An AC coupling block between stages of the PG LPF blocks DCO generated by the RXFE and earlier gain stages. Typical NF is <3 dB, IIP3 >-15 dBm and IIP2 >+48 dBm at maximum gain. A GSM 850MHz Band RX sensitivity plot is shown in Fig. 6.4.3.

Quad-band UMTS RX operation is achieved with a 4-input zero-IF receiver. Two of the 4 front-ends are single-ended LNAs requiring SAW filters between the LNA and mixer to reduce TX leakage. This allows the use of duplexers with reduced TX/RX isolation. A wideband mixer is shared between those two paths. The two UMTS differential receiver inputs use no SAW filters between the LNA and mixer. Stringent FE linearity and challenging LO phase noise are required in the SAW-less paths to cope with the -25 dBm TX leakage from the duplexer. An on-chip IM2 calibration circuitry is implemented for those two paths to minimize the IM2 products generated by the TX leakage. A 5th- order lowpass filter (LPF) is shared among all UMTS RX paths. It has a 3dB bandwidth of 2.1MHz with an accuracy of $\pm 3\%$ over PVT achieved through automatic on-chip RC calibration. The measured receive gain is 58dB and the noise figure is 2.6dB. Typical (calibrated) IIP2 of the two receivers without SAW filter is +60dBm referred to the LNA input. Figure 6.4.4 shows the WCDMA RX sensitivity for BC 1 (IMT), BC4 (AWS) and BC5 (Cell). It can be seen that this receiver exceeds the sensitivity requirements by several dB even without the use of TX interstage SAW filters between this transceiver and the power amplifier.

The low-IF GPS receiver [6] operates simultaneously with the WCDMA/GSM/EDGE transceivers. The measured receive gain is 82dB, noise figure is 2.0dB, with 35dB image rejection and maximum out-of-band IIP3 is +6dBm. A secondary WCDMA diversity zero-IF receiver (DRX) achieves total receive gain of 57 to 58dB, IIP3 from -17 to -20dBm, and IIP2 better than +49dBm. Since the GPS and DRX receivers do not need to operate at the same time by design, they share a reconfigurable 3rd-order Chebychev baseband filter. The filter has a 3dB bandwidth of 1MHz in GPS mode, and 2.1MHz in WCDMA mode, with an accuracy of $\pm 3\%$ over PVT achieved through automatic on-chip RC calibration.

Figure 6.4.5 shows a summary of typical parametric performance and Fig. 6.4.6 shows the battery current (at 3.7V) vs output power in Full-Duplex WCDMA Cell (850MHz) and PCS (1900MHz) band operation. This device uses 2.1V and 2.7V supplies and consumes 63.4mA (at the battery) in Cell Band and 69mA (at the battery) in PCS Band for a chip $P_o = -8$ dBm. In a typical 3G phone this corresponds to 0dBm at the phone antenna (a phone spends approximately >90% time at power levels lower than 0dBm). Note that these current consumption figures are very competitive when compared with the data in [2-4] considering the significant amount of integration and the SAW-less receivers in these bands. The transceivers in [2-4] are WCDMA only and use interstage SAW filters in all bands and modes. Figure 6.4.7 shows the micrograph of the presented chip which has a die size of 5.6x5.6mm².

Acknowledgments:

The authors would like to acknowledge Tim Nacita for leading the layout effort, Wes Sampson for leading the RF systems effort, Pat Cantey and Rick Staszewski for designing and implementing the reference design phones used to produce the final measurements, and Sean Weng for leading the RF SW driver effort.

References:

- [1] O.E. Erdogan et al., "A Single-Chip Quad-Band GSM/GPRS Transceiver in 0.18 μ m Standard CMOS," *ISSCC Digest Tech. Papers*, pp. 318-601, Feb. 2005.
- [2] W. Thomann et al., "A Single-Chip 75GHz/0.35 μ m SiGe BiCMOS W-CDMA Homodyne Transceiver for UMTS Mobiles," *IEEE Radio Frequency Integrated Circuits Symp.*, pp. 69-72, June 2004.
- [3] D. L. Kaczman et al., "A Single-Chip Tri-Band (2100, 1900, 850/800MHz) WCDMA/HSDPA Cellular Transceiver," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1122-1132, May 2006.
- [4] R. Koller, T. Ruhlicke, D. Pimingsdorfer, B. Adler, "A Single-Chip 0.13 μ m CMOS UMTS W-CDMA Multiband Transceiver," *IEEE Radio Frequency Integrated Circuits Symp.*, pp. 11-13, June 2006.
- [5] M. Cassia et al., "A Low-Power CMOS SAW-Less Quad-Band WCDMA/HSPA/1X/EGPRS Transmitter," *European Solid-State Circuits Conf.*, Sept. 2008.
- [6] X. Yang et al., "A Low-IF CMOS Simultaneous GPS Receiver Integrated in a Multimode Transceiver," *IEEE Custom Integrated Circuits Conf.*, pp. 107-110, Sept. 2007.

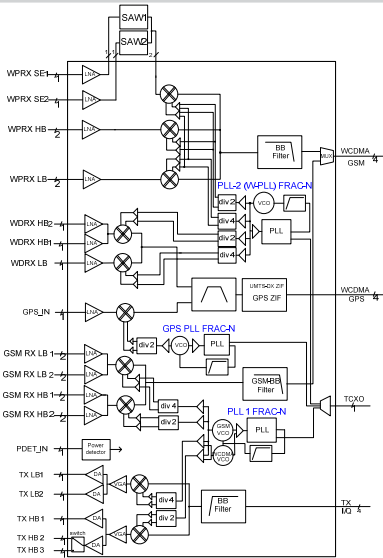


Figure 6.4.1: Transceiver detailed block diagram.

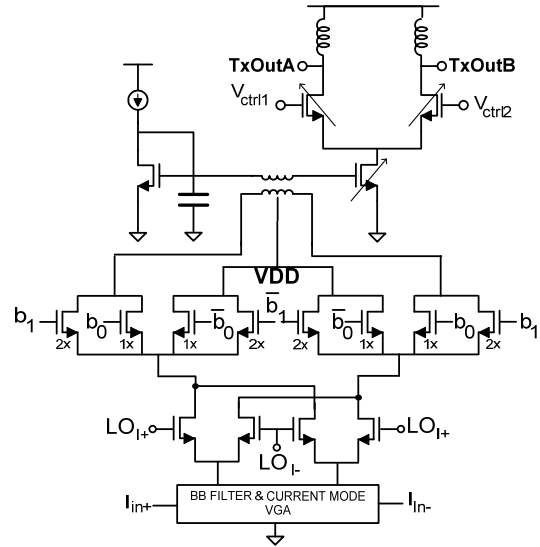


Figure 6.4.2: Transmitter simplified schematic.

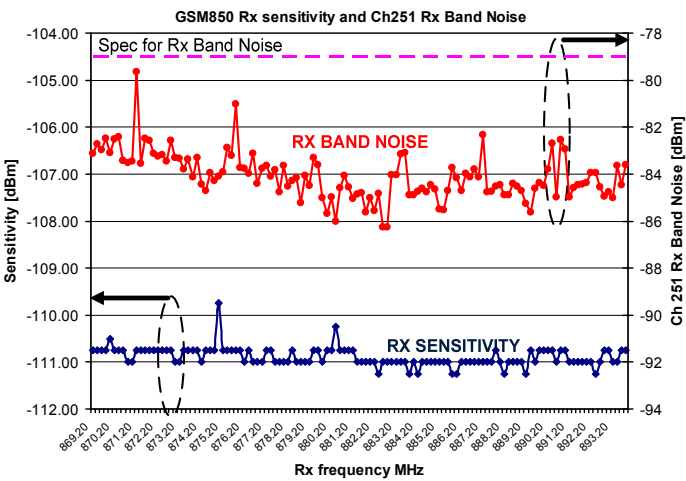


Figure 6.4.3: Typical GSM 850MHz receiver sensitivity and GSM 850MHz transmitter receive-band noise.

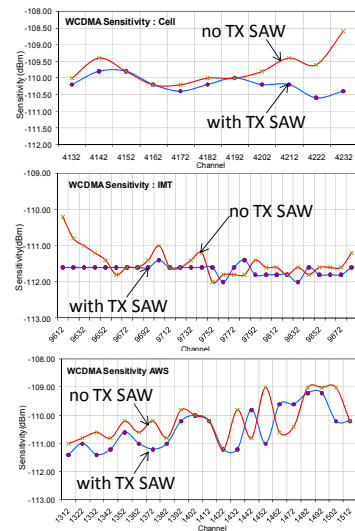


Figure 6.4.4: Typical Cell, IMT & AWS WCDMA receiver sensitivity with and without TX interstage SAW filters.

BAND	PARAMETER	Typical Chip Measured Performance	Standard Requirement
GSM 850MHz	RX NF	2.6dB	na
	TX 400KHz mod	69dBc	60dBc
	Phase Error rms	1.1°	5°
GSM 900MHz	RX band noise	167dBc/Hz	162dBc/Hz
	RX NF	2.6dB	na
	TX 400KHz mod	68.7dBc	60dBc
GSM 1800MHz	RX band noise	166dBc/Hz	162dBc/Hz
	Phase Error rms	1.1°	5°
	RX NF	2.6dB	na
GSM 1900MHz	TX 400KHz mod	67.2dBc	60dBc
	RX band noise	158dBc/Hz	153dBc/Hz
	Phase Error rms	1.2°	5°
UMTS 850 MHz	RX NF	2.6dB	na
	Primary RX IP2 (diff input)	55dBm (un-calibrated)	na
	TX ACLR 5MHz @ 5dBm	50dBm	33dBc
UMTS 900 MHz	EVM rms	< 4%	17.50%
	Primary RX IP2 (diff input)	55dBm (un-calibrated)	na
	TX ACLR 5MHz @ 5dBm	49dBc	33dBc
UMTS 1900 MHz	EVM rms	< 4%	17.50%
	Primary RX NF	2.6dB	na
	Primary RX IP2 (diff input)	55dBm (un-calibrated)	na
UMTS 2100 MHz	Primary RX NF (SE input)	2.5dB	na
	Primary RX IP2 (SE input)	50dBm (un-calibrated)	na
	TX ACLR 5MHz @ 5dBm	46.7dBc	33dBc
GPS	EVM rms	< 4%	17.50%
	RX NF	2dB	na

Figure 6.4.5: Typical transceiver performance summary.

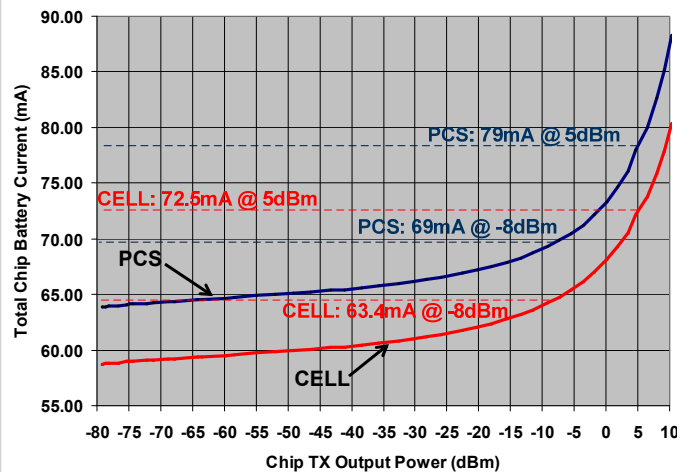


Figure 6.4.6: Typical DC battery current vs transmitter output power for WCDMA full-duplex CELL and PCS operation.

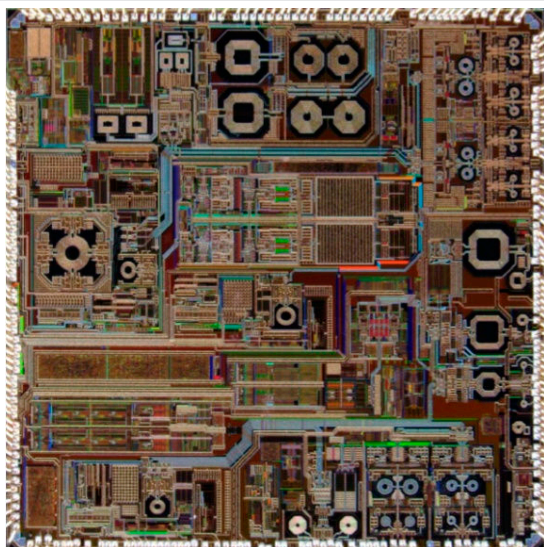


Figure 6.4.7 Chip micrograph.