A Digitized LVDS Driver with Simultaneous Switching Noise Rejection

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ABSTRACT

In this paper, a Digitized LVDS Driver with SSN (Simultaneous switching noise) rejection is proposed, which is fabricated by TSMC 0.18um CMOS technology. First, the power consumption and chip area are greatly decreased due to the design of digitized driver but we suffered the SSN noise. Second, the method which modifies the driver's control signal greatly reduces the ground bounce, and simultaneously solved the ground bound problem mentioned above. Third, the driver can calibrate the output differential mode by the control signal outside the chip by way of the controllable driver. According to the simulation results, ground bounce reduced from 175mV to 95mV, 55% diminished, and the measurement output jitter (pk-pk) is less than 48ps @1.25Gbps. The driver area is only 210um x 210um and power consumption is less than 19mW, which are extremely lower then the conventional LVDS Driver. The proposed programmable driver can also be applied to the 1.5Gbps Serial ATA standard or 2.5Gbps PCI-Express.

Keywords

Low Voltage Differential Signal (LVDS), Simultaneous switching noise (SSN), Transmitter.

1. INTRODUCTION

CMOS technologies have grown exponentially in recent years. As we scale down CMOS devices into submicron region (<0.35um), the operating frequency of an output driver increases and benefit the rise/fall times and pulse width. With increasing data bit-rate and decreasing supply voltages, the transient current injected into the power and ground planes of Print-Circuit Board (PCB) is growing rapidly. There are two sources that the transient current entering the planes, one is current spikes arising from the switching activity of the silicon core and I/O cells. The other is signal return current associated with the signals through the system interconnects [1]. Owing to faster switching speed and chip package, the SSN is created when output drivers switch simultaneously. Some of the encountered problems with false operations due to SSN are: (1) false trigging, (2) double clocking, and/or (3) missing clocked pulse.

The SSN caused by package parasitism and current switching are described below. Output pad driver is the main source of the SSN because of the large transient currents during switching. SSN may even appear at low operation frequency signal that has sharp transition. The peak of SSN usually occurs in the beginning of the transition. Different pad and package structure has different value of parasitic inductance and capacitance. Hence, the design must be careful here. To reduce SSN mechanism, we can use better package architecture such as Flip-chip. One may also use some circuit technologies to reduce SSN effect. In power system analysis, it uses appropriate decoupled capacitance to reject SSN effect.

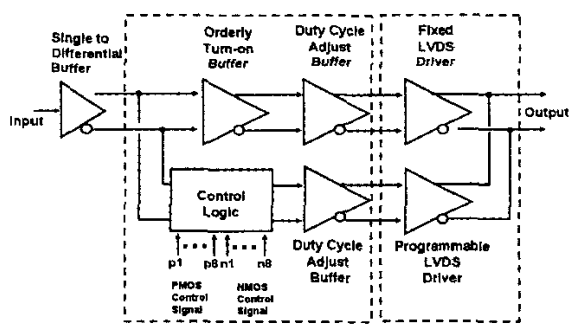

Fig. 1. The proposed circuit architecture

In this paper, we propose the new methodology to reduce the SSN effect based on turn on spreading and duty cycle controlling. In the future, when designers confront the high-speed interface (over gigabit per second) like gigabit Serializer and Deserializer (SerDes) application in SONET/SDH transmission interface, Gigabit Ethernet, 3GIO,etc, this mechanism can also be used to reduce SSN effect.

2. PROPOSED CIRCUIT ARCHITECTURE

2.1 Overall Architecture and New LVDS

The architecture contains two main blocks, one is the fixed LVDS driver and the other is the programmable driver we will describe later. In Figure 1, the first signal path is the upper path and the programmable driver path is the lower one. All signals have to be passed to the orderly turn-on buffer block, and the duty cycle adjust buffer to make the first two or three input of the driver gate "orderly turn-on". Besides, because of the process error or layout mismatch, the output level is not guaranteed to have an expected voltage. So the additional, controllable LVDS drivers can enhance the output driver current to compensate the output.

Traditionally, the methods of reducing SSN are to improve package architecture, to decrease the bonding wire inductance or increase the number of the chip power pads. However, the main source of the SSN is the large current change. So we recommended a circuit technique to decrease the transient current. The driver we proposed is shown in Figure 2. The left driver [2] includes two current sources. However, our driver has no current source. This methodology has some advantages. First, the driver needs no current source so the output signal swing is enlarged. It also reduces the sizes of switch transistors. Therefore, the sizes of the pre-driver are reduced as well. It reduces the overall chip area substantially. Further, the whole driver architecture looks is like the two inverter connected back to back, it makes the control and layout easier. Notice that, the common-mode voltage is decreased from 1.25V to 0.9V to be used in a 1.8V supply environment.

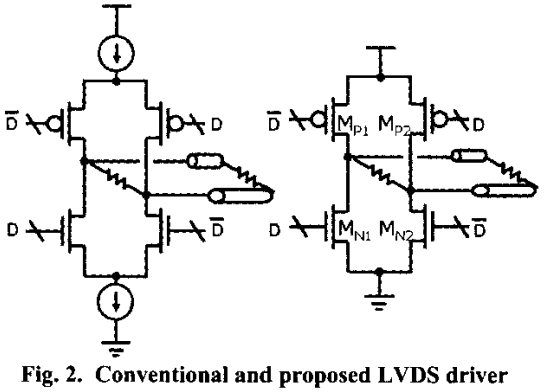

Fig. 2. Conventional and proposed LVDS driver

2.2 Orderly Turn-on Buffer

The First block, orderly turn-on block, takes the input signal which the driver input separated by several pico-seconds.

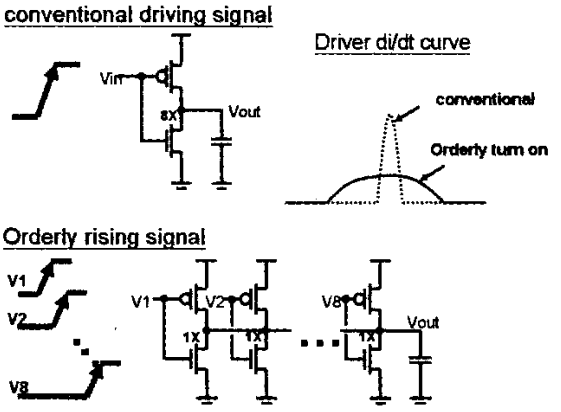

Fig. 3. The orderly turn-on concept

Figure 3 shows the difference between conventional and the proposed driver concept. In conventional driver, all drivers operate at the same time. It results in a large current change in a very short time. For this reason, we make the drivers operate at different time which is separated by a tiny interval (<15ps). In the microcosmic point, the total current will divide into several small current and orderly flows into the ground plane. Therefore, we can see that the transient current is very smooth. The current variation is reduced and so the SSN is modified.

How to produce such small time interval signal? The digital method which uses many kinds of inverter-loading combination can produce such signals. The circuit and simulation result are in Figure 4.

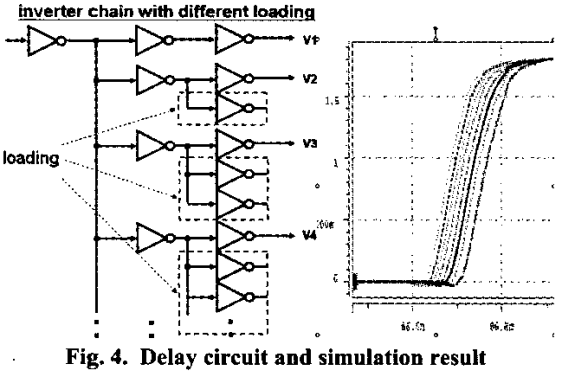

Fig. 4. Delay circuit and simulation result

2.3 Duty Cycle Adjust Buffer

The second block of the signal path is duty-cycle modulation. We follow the experiences from conventional I/O pad design to reduce SSN. As shown in Figure 2, the normal operating mode of LVDS is: (MP2, MN1) and (MP1, MN2) are turned on and off alternately. It means that there appears a large circuit current change when the signal is in transient. Therefore, we propose a new method to reduce longer current change. When the signal changes,

the turn off time of MP2 and MN1 is delayed. In other words, the four transistor of driver will be partially turned on at the same time in the transient time. MP1 and MN2 are turned on gradually while MP2 and MN1 are being turned off. In microcosmic, the current through MP2 and MN1 will be conducted to MP1 and MN2 when signal changes. After the input signal exceeds the threshold voltage, the current will be totally switched. Hence, it minimizes the current charge to power and ground and reduces the SSN.

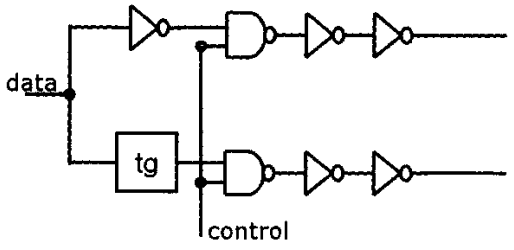

Fig. 5. Duty-cycle and tri-state control circuit

Unlike the AGTL, the decoder only turns on or turns off of NMOS transistors. Hence, if only eight transistors of the driver need to be turned on to reach the output voltage level; the remainder of the driver must always be turned off by the control signal. The control signal is simply set to zero to turn off the transistor in the past but it is unworkable in LVDS system. The LVDS is differential signaling. The control signal cannot turn off both the transistors of the differential circuit by simply being set to zero. We need tri-state circuit. We utilize some NAND gates and NOR gates to implement the tri-state circuit, like Figure 5. When the control pin is at low level, it guarantees all transistors to be turned off and the output signal follows the input signal when control pin is at high level. This is so-called the "programmable driver" in Figure 1.

3. SIMULATION AND MEASUREMENT RESULT

3.1 Simulation Result

The simulation of the ground bounce is shown in Figure 6, According to the method reducing the SSN we describe above. The value of the SSN is reduced from 175mV to 95mV, which is 55% diminished, and the measurement output jitter (pk-pk) is less than 48ps. The power pad SSN is also reduced from 160mV to 110mV. The difference in output eye diagram between this new approach and conventional one is the output slew rate. The slew rate of new approach is slower. But the signal integrity is better obviously.

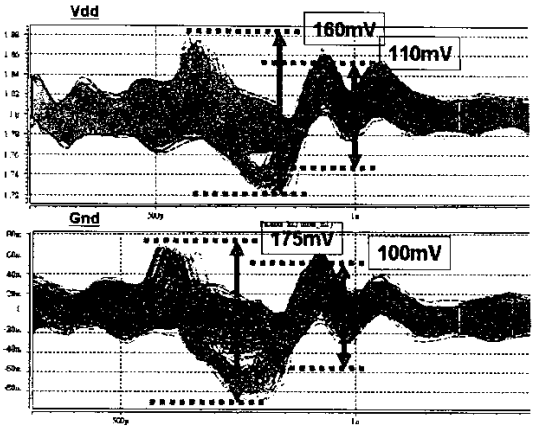

Fig. 6. The compare of simulation SSN

Owing to the programmable driver, the output level can be adjusted by control signal outside the chip. Figure 7 is the driver output swing and the common mode voltage in the TT, SS and FF situations by SPICE simulation. The swing can be around 400mV and common mode can be equal to 0.9V in any corner of process by output control signals. It will turn on more drivers if the process is in SS and turn off some in FF case. In this design, we turn on half number of the programmable drivers in TT case.

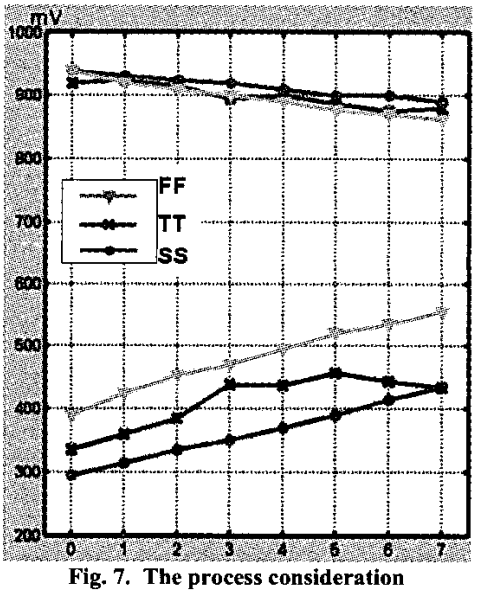

Fig. 7. The process consideration

3.2 Measurement Result

Figure 8 shows the measurement output eye diagram. The swing is about 400mV which fit in with the LVDS standard. The peak to peak jitter is less than 48ps when driver is operating in 1.25Mbps or about 98ps at 2.5Gbps.

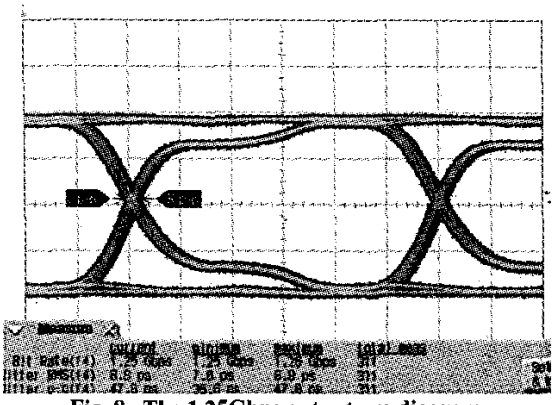

Fig. 8. The 1.25Gbps output eye diagram

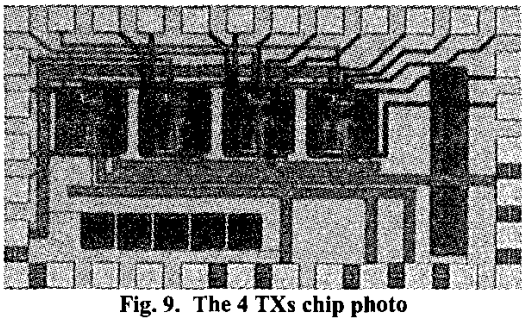

Fig. 9. The 4 TXs chip photo

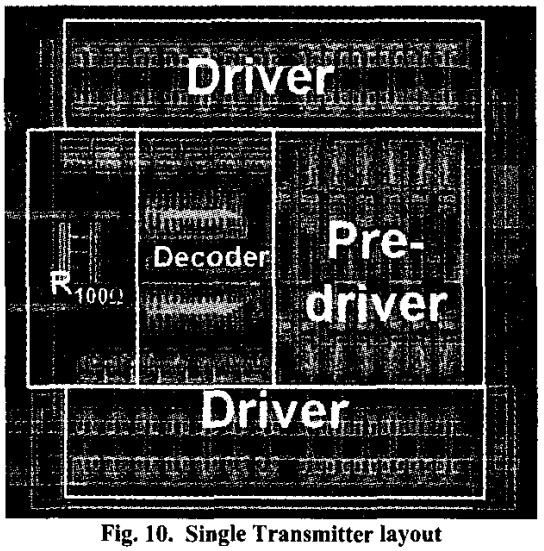

Fig. 10. Single Transmitter layout

4. CONCLUSION

This paper describes circuit techniques for a low power, low area, 625Mbps, SSN reduced, and programmable LVDS driver. The circuit is capable of operating at 78.125Mbyte/s to 312.5Mbyte/sec data rate, which results in 625 Mbps to 2.5 Gbps transmitting. The highest operating speed is limited by inductive bouncing caused by bonding wire in conventional circuit design. In this novel circuit technique to reduce SSN, the transmitter speed can be higher than former one. In addition, we can also operate four transmitters at the same time in a single chip. It will help to make SOC design more easily in the future, too. Figure 9 is the chip photo and the Figure 10 is the single transmitter layout. The chip performance summary is shown in TABLE I. There are four transmitters with together in this chip and only one power supply for driver. The output jitter will be several times than original one if all four transmitters operate at the same time because of the serious SSN impact. The special feature about the single transmitter is the low power and lower area. The area is only 210um x 210um and power consumption is about 19mW, which are extremely lower to the conventional LVDS Driver.

TABLE I
Chip performance summary

Function	Tx
Technology	0.18um 1P6M
Operation voltage	1.8V
Chip size	1380*1500 (um^2)
Core size (Tx)	210*210 (um^2)
Transistor/Gate Count	43014 / 3574
Power consumption	~19.7mW (Tx)
Jitter (Tx)	<48p @1.25Gbps

5. REFERENCES

[1] I. Novak, "Reducing simultaneous switching noise and EMI on ground/power planes by dissipative edge termination," *Electrical Performance of Electronic Packaging, 1998. IEEE 7th topical Meeting on,* 26-28 Oct 1998

[2] *IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)*, IEEE Std 1596.3-1996, 31 Jul 1996