Automatic and Continuous Offset Compensation of MOS Operational Amplifiers Using Floating-Gate Transistors

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Abstract— **This paper presents a new approach that exploits floating-gate MOS transistors and a feedback control loop to automatically compensate the offset of MOS operational amplifiers in a continuous manner that substantially improves the state of the art in the field. The proposed method can be repeatedly used to compensate the effects of environmental and device modifications, while the possibility to accurately program an arbitrary value of the offset can be exploited to realize high performance and/or programmable comparators and A/D converters.**

Index Terms—**Calibration, EEPROM, offset compensation, operational amplifiers.**

I. INTRODUCTION

CRITICAL analog circuits can be trimmed and calibrated by suitably adjusting the characteristics of a few selected devices, realized by means of floating-gate transistors (FGT's) [1], whose threshold voltages (V_{TH}) can be electrically adjusted within a wide range of values (ultimately limited by reliability considerations).

Although, in practice, FGT's are overwhelmingly used in digital mode (storing only two distinct values of charge on the floating gate to obtain a binary threshold adjustment), analog applications have also been proposed [2]–[5], where the transistor threshold voltage (V_{TH}) is continuously varied over a wide range of values.

In these cases, however, so far the V_{TH} of FGT's has only been adjusted in a discrete manner, normally by means of a number of small programming operations (followed by the evaluation of the obtained circuit characteristics), to be repeated until a predefined target is achieved [6].

Such a procedure, however, is normally very long and exhibits an inherent discretization error that decreases with the duration (hence the effect) of each programming operation. Thus, a tradeoff is in order between the duration and the accuracy of circuit calibration. As the programming pulse duration and/or amplitude is reduced, in fact, the number of pulses and of verifications needed to obtain the desired offset compensation increases. Thus, the duration of the whole procedure may become excessive when high accuracy is required. Furthermore, complex logic and accurate analog circuits are required to control the injection and test its effects.

In this context, this work introduces a new concept, exploiting a feedback loop to freeze (continuous) programming of crucial FGT's to obtain desired circuit behavior; this over-

comes the limitations mentioned above and achieves fast and accurate circuit trimming.

As an example of application, this basic idea is used here to cancel the offset of MOS operational amplifiers (op amps), automatically and without the need of external references and *ad hoc* verification, achieving high accuracy in minimum calibration time.

II. THE BASIC IDEA

The basic idea of this work is schematically illustrated in Fig. 1, where the block within the dotted line represents the analog circuit to be calibrated. This operation concerns circuit characteristics (output voltage, time constants, . . .) substantially depending on the threshold voltage of an FGT that in Fig. 1 is explicitly separated from the rest of the circuit.

Such an FGT is first roughly programmed so as to unambiguously unbalance the characteristic of interest on one side of the target value. Then, a (continuous) programming operation is started to change the V_{TH} of the FGT in the direction required to approach the target condition. This programming is controlled by a feedback loop, able to automatically interrupt the operation upon reaching the target value of the characteristic of interest. This way of using FGT's can offer an ideal application to the programming technique described in [7], although other possibilities can also be conceived. The operation is fully analog (no sampling is performed) thus allowing the injection into the FG of the exact amount of charge needed to calibrate the circuit.

Naturally, in principle, the accuracy of the obtained calibration depends on the gain and bandwidth of the feedback loop, as well as, to a smaller extent, the characteristics of the FGT programming circuitry. In practice, however, good calibration accuracy can be obtained without special characteristics of the feedback loop and the programming circuitry.

It is important to notice that the programming effectiveness is intrinsically independent of the charge injection dynamics, and in particular from the programming pulse shape and injection efficiency.

III. APPLICATION TO OP AMPS

The basic concept briefly described above is here applied to the specific case of offset calibration of CMOS operational amplifiers.

To this purpose, we use the simple CMOS circuit shown in Fig. 2 that represents an ideal vehicle to test the actual performance of the calibration procedure.

In this circuit, the differential input stage has been modified by replacing conventional transistors with FGT's as input
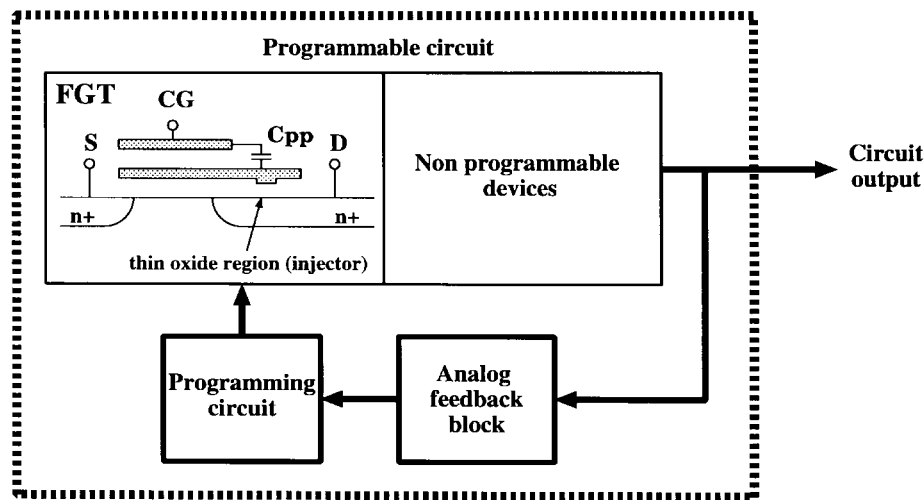
Fig. 1. Schematic illustration of the basic idea of this work. An analog block is used to stop programming of the FGT's included into the programmable circuit when a target output condition is reached.
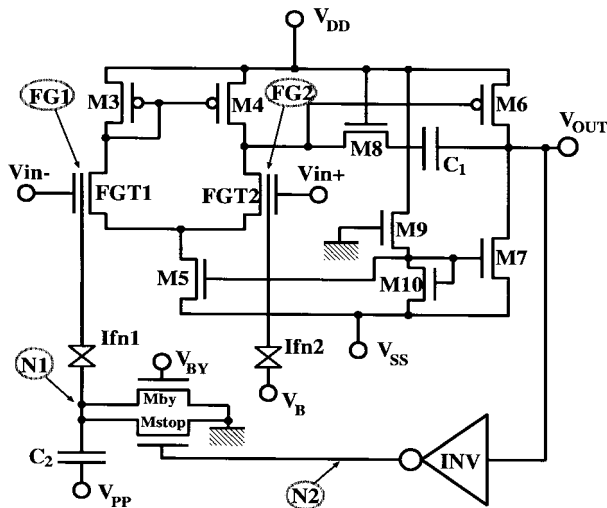

Fig. 2. Schematic diagram of the operational amplifier with the circuit for automatic offset compensation. Input transistors FGT1 and FGT2 are floating gate devices specifically designed to increase the coupling capacitance between floating- and control-gate.

devices. These FGT's have been specifically designed so as to present a high control-gate to floating-gate coupling capacitance (C_{PP}), in order to reduce the FG sensitivity to the voltages applied to the drain during device trimming. The tunnel injector I_{fn1} is connected to a separate node that is normally grounded through transistor M_{by} to avoid charge injection from/to the FG1. Such an injector is designed with minimum geometry, for improved reliability. An identical injector I_{fn2}, connected to FG2 and driven by a constant bias V_B, is never used to inject electrons to/from FG2 but is needed to obtain perfect symmetry of the input stage.

The as-fabricated offset, typically of a few tens of millivolts, can be drastically reduced by means of a trimming operation where: 1) the transistor FGT1 is first programmed to a high voltage (to unambiguously determine the offset sign) and 2) part of the charge injected into the FG of such a device is selectively removed until reaching the zero offset condition.

In particular, after UV erasing both FGT's, a high voltage pulse is applied to the node V_{IN-}, while V_{IN+} is grounded and transistor M_{BY} is turned on. Under this condition, because of the high value of the capacitance C_{PP1} between CG and FG1 this latter is at high potential and a current flows through the Fowler–Nordheim (FN) injector I_{fn1}, increasing the threshold voltage of FGT1 and making the op-amp offset positive. The successive controlled offset cancellation is conveniently described by means of the simulated waveforms shown in Fig. 3.

A high voltage pulse is applied to node V_{PP}, with both op amp inputs grounded. Since the offset has been made positive, the voltage at node N_2 is V_{SS} and M_{stop} is off. Node N_1 is then driven to a high voltage by capacitor C_2, and the induced current through I_{fn1} discharges the FG1, thus reducing V_T of FGT1 and the operational amplifier offset. This process stops automatically when the op amp output (V_{OUT}) goes to zero. At this moment M_{stop} (driven by the inverter *INV*) turns on and the potential drop across the FN injector is abruptly lowered, and thus the injection of electrons from FG1 stops.

As is clear from the analysis of the circuit, the behavior of the trimming circuit is essentially independent of programming characteristics (duration and height of the programming pulse, tunnel oxide thickness and wear-out, programming capacitance, etc.) and of the starting values of the threshold voltage (UV erase is used here essentially as a good conventional starting point).

In addition, the trimming process stops when the exact amount of charge needed to compensate the offset has been injected, overcoming the discretization problems typical of circuits that perform calibration by injecting small quantities of charge until a pass/fail condition is satisfied.

IV. EXPERIMENTAL RESULTS

The circuit of Fig. 2 has been realized in standard 0.5-μm CMOS technology, featuring single-poly EEPROM cells [8] (the particular technology used to fabricate FGT's is not essential for the purposed of this paper). With the same
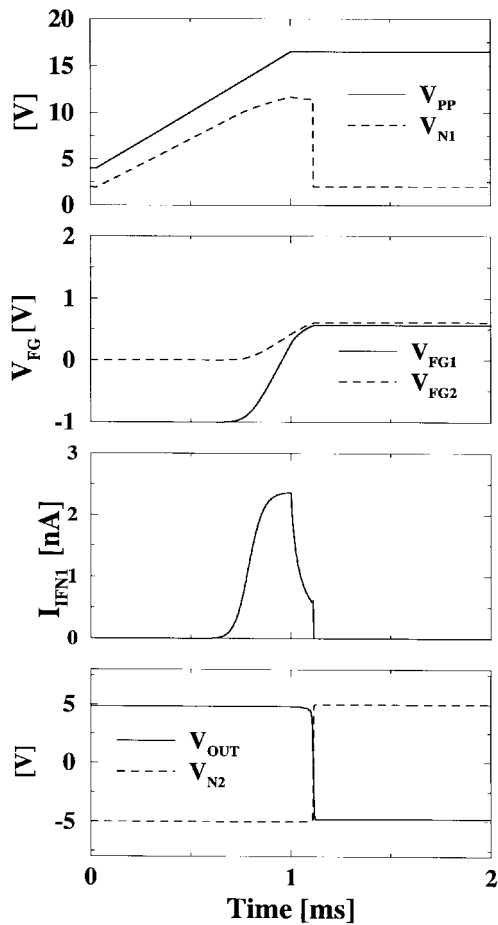
Fig. 3. Simulations of the main waveforms during trimming operation. As can be seen, the tunnel current is abruptly reduced when the output node of the operational amplifier switches, corresponding to the zero offset situation.
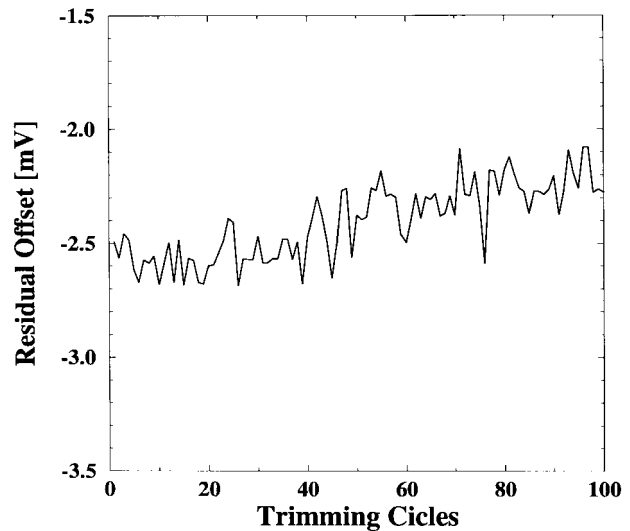

Fig. 4. Measured residual offset after compensation as a function of the number of trimming operations. The offset before trimming was ≈ 0.9 V.
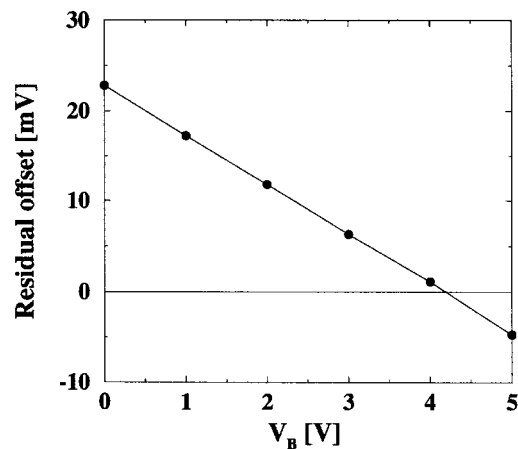

Fig. 5. Residual offset as a function of the voltage at node V_B during programming. In normal operation this node is driven to 0 V.

technology, op amps similar to those of interest here, but for the use of standard transistors instead of the FGT's, have also been realized to be used as reference devices.

The relevant experimental results are illustrated in Fig. 4, showing the residual offset voltage after trimming as a function of the number of (re)calibration operations. As can be seen, the residual offset is on the order of a few millivolts and changes only slightly with reprogramming cycles (each performed after UV cancelling the FGT's, so as to reproduce the original offset).

From the point of view of accuracy of the calibration process, the coupling capacitance between the tunnel injectors and the floating gates is an important parameter to take into account. Fig. 5 shows the effect on the final offset value of the voltage V_B applied to accessible terminal of the FN injector I_{fn2} during the trimming operation. As can be seen, the final offset (measured with $V_B = 0$ V), is a linear function of V_B during trimming operation. This dependence can be explained considering that, while the offset is measured with both nodes V_{PP} and V_B grounded, the programming operation is performed with V_{PP} and V_B at different potentials. This asymmetry is partially compensated if V_B is raised during programming, resulting in a reduced residual offset. From a technological point of view, this effect can be made negligible

by increasing the capacitive coupling between CG and FG (i.e., C_{PP1} and C_{PP2}), as well as choosing the appropriate value (5 V in the presented case) of V_B during trimming. In the case considered here, the capacitive ratios were $C_{PP1}/C_{TUN} = 50$ and $C_{PP1}/C_2 = 1$.

The measured ac characteristics of the realized op amps are shown in Fig. 6, illustrating the frequency response in the follower configuration compared to that of the control (i.e., conventional) circuits.

As can be seen, the ac characteristics are not significantly degraded by the introduction of FGT's in the differential stage. In particular, this result indicates that the extra capacitors coupling the FG to the other nodes of the FGT's do not play a major role as far as ac performance is concerned.

Further measurements have been performed applying a nonzero voltage to input V_{IN-} during programming in order to determine well defined, target offset.

The resulting measured offset, shown in Fig. 7, is found to be a linear function of the voltage applied to node V_{IN-}, thus clearly suggesting the use of FGT op amps as programmable
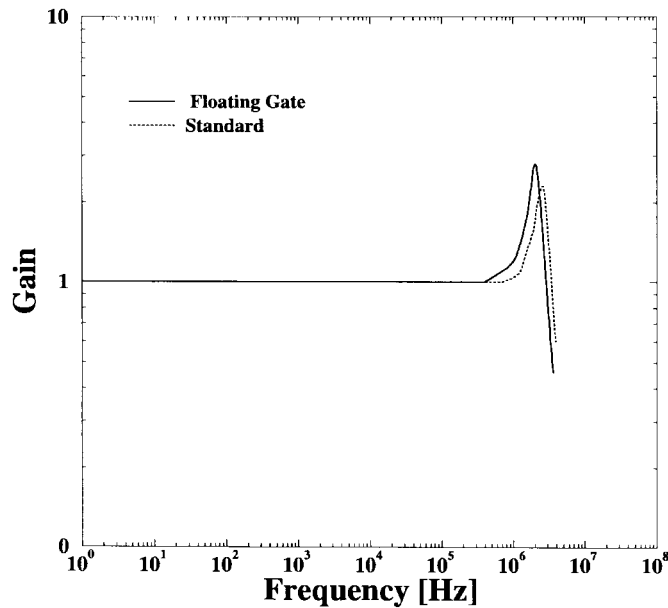
Fig. 6.   Frequency response of the programmable op amps compared with that of the control ones using standard MOS transistors as input devices.

Fig. 7.   Measured offset as a function of the voltage applied to node $V_{\text{IN}-}$ during trimming.

comparators. The obtained absolute error is found to be confined in a band of $\pm 0.8\%$ (that can be further reduced optimizing V_2 during programming), while the linearity error is negligible.

V. CONCLUSION

This paper has presented a new concept to accurately calibrate analog circuits by programming the threshold voltage of selected FGT's that, as opposed to previous works, operates automatically and continuously, performing a real-time auto-evaluation by means of a feedback loop.

As a result, the proposed method achieves excellent accuracy in calibration with a very fast, unique operation, that can be arbitrarily repeated to compensate environmental and device modification during the circuit lifetime.

As a significant application, the proposed method has been used to program the voltage offset of MOS operational amplifiers realized with a standard CMOS technology featuring single-poly EEPROM floating-gate transistors, and the obtained results suggest that the method can be satisfactorily applied to real circuits (for instance, to obtain low offset amplifiers, programmable voltage comparators, . . .).
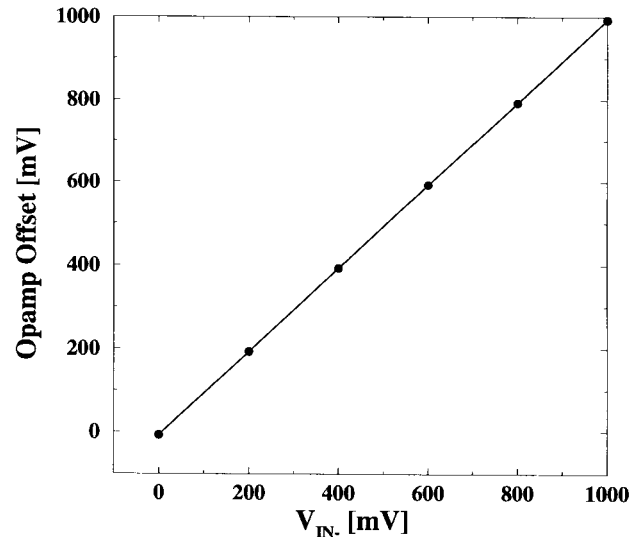
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