(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
20 October 2016 (20.10.2016)

WIPO | PCT

(10) International Publication Number
WO 2016/167763 A1

(51) International Patent Classification:
B41J 2/045 (2006.01) *B41J 2/17* (2006.01)
B41J 2/07 (2006.01)

(21) International Application Number:
PCT/US2015/025944

(22) International Filing Date:
15 April 2015 (15.04.2015)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.** [US/US]; 11445 Compaq Center Drive W., Houston, Texas 77070 (US).

(72) Inventors: **GE, Ning**; 1501 Page Mill Rd., Palo Alto, California 94304-1100 (US). **LI, Zhiyong**; 1501 Page Mill Rd., Palo Alto, California 94304-1100 (US). **KOH, Ser Chia**; Depot 2 138 Depot Road #01-01, #02-01, #04-01, #05-01, #06-01, & #07-01, Singapore 109683 (SG). **HO, Chaw Sing**; Depot 2 138 Depot Road #01-01, #02-01, #04-01, #05-01, #06-01, & #07-01, Singapore 109683 (SG).

(74) Agents: **COLLINS, David W.** et al.; Hewlett-Packard Company, Intellectual Property Administration, 3404 E. Harmony Road, Mail Stop 35, Fort Collins, Colorado 80528 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:
— *as to the identity of the inventor (Rule 4.17(i))*
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

Published:
— *with international search report (Art. 21(3))*

(54) Title: PRINTHEADS WITH HIGH DIELECTRIC EPROM CELLS

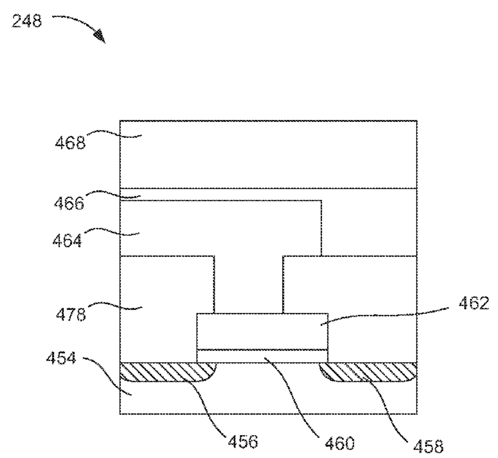


Fig. 4B

(57) Abstract: In one example in accordance with the present disclosure a printhead with a number of high dielectric EPROM cells is described. The printhead is to deposit fluid onto a print medium. The printhead also includes a number of EPROM cells. Each EPROM cell includes a substrate having a source and a drain, a floating gate separated from the substrate by a first dielectric layer, and a control gate separate from the floating gate by a second dielectric layer. The second dielectric layer includes a high-dielectric constant material.

WO 2016/167763 A1

PRINTHEADS WITH HIGH DIELECTRIC EPROM CELLS

BACKGROUND

[0001] A memory system may be used to store data. In some examples, imaging devices, such as printheads may include memory to store information relating to printer cartridge identification, security information, and authentication information, among other types of information.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The accompanying drawings illustrate various examples of the principles described herein and are a part of the specification. The illustrated examples do not limit the scope of the claims.

[0003] Fig. 1 is a diagram of a printing system according to one example of the principles described herein.

[0004] Fig. 2 is a block diagram of a printer cartridge that uses a printhead with a number of high dielectric erasable programmable read only memory (EPROM) cells according to one example of the principles described herein.

[0005] Fig. 3A is a diagram of a printer cartridge with a number of high dielectric EPROM cells according to one example of the principles described herein.

[0006] Fig. 3B is a cross-sectional diagram of a printer cartridge with a number of high dielectric EPROM cells according to one example of the principles described herein.

[0007] Fig. 3C is a cross-sectional diagram of a printhead with a number of high dielectric EPROM cells according to one example of the principles described herein.

[0008] Fig. 4A is a circuit diagram of a high dielectric EPROM cell according to one example of the principles described herein.

[0009] Fig. 4B is a cross-sectional view of a high dielectric EPROM cell according to one example of the principles described herein.

[0010] Fig. 5 is a circuit diagram of a printhead with a high dielectric EPROM cell according to examples of the principles described herein.

[0011] Fig. 6 is a cross-sectional view of a printhead including a high dielectric EPROM cell, a memristor, and a firing resistor according to one example of the principles described herein.

[0012] Throughout the drawings, identical reference numbers designate similar, but not necessarily identical, elements.

DETAILED DESCRIPTION

[0013] Memory devices are used to store information for a printer cartridge. Printer cartridges include memory to store information related to the operation of the printhead. For example, a printhead may include memory to store information related 1) to the printhead; 2) to fluid, such as ink, used by the printhead; or 3) to the use and maintenance of the printhead. Other examples of information that may be stored on a printhead include information relating to 1) a fluid supply, 2) fluid identification information, 3) fluid characterization information, and 4) fluid usage data, among other types of fluid or imaging device related data. More examples of information that may be stored include identification information, serial numbers, security information, feature information, Anti-Counterfeiting (ACF) information, among other types of information. While memory usage on printheads is desirable, changing circumstances may reduce their efficacy in storing information.

[0014] For example, an increasing trend in counterfeiting may lead to current memory devices being too small to contain sufficient anti-counterfeiting information and security and authentication information. Additionally, with loyalty customer reward programs, new business models and other customer relation management programs through cloud-printing and other printing architectures, additional market data, customer appreciation value information, encryption information, and other types of information on the rise, a manufacturer may desire to store more information on a memory device of a printer cartridge.

[0015] Moreover, as new technologies develop, circuit space is at a premium. Accordingly, it may be desirable for the greater amounts of data storage to occupy less space within a device. Erasable programmable read only memory (EPROM) cells may be used for their simple construction, non-volatility, and efficient storage of data. EPROM arrays include a conductive grid of columns and rows. EPROM cells located at intersections of rows and columns have two gates that are separated from each other by a dielectric layer. One of the gates is called a floating gate and the other is called a control gate. A logical value may be represented by either allowing current to flow through, or preventing current from flowing through the EPROM cell. In other words, the logical value of an EPROM cell may be determined by the resistance of the EPROM cell. Such a resistance is dependent upon the voltage at the floating gate of the EPROM cell. While EPROM cells may serve as beneficial memory storage devices, their use presents a number of complications.

[0016] For example, printheads are formed by depositing layers of material on a substrate surface. As an EPROM cell includes two gates, multiple additional layers of material are used to form these EPROM cells. The additional layers increase the thickness of the printhead and overall size of the printhead. Moreover, as will be described below, in order to generate an EPROM that is easily read from and written to, the dielectric layer, i.e., the layer between a control gate and a floating gate of the EPROM cell, can be rather thick, which thickness further increases the size and inefficiency of EPROM as a memory storage device.

[0017] Accordingly, the present disclosure describes a printhead with EPROM cells that alleviate these and other complications. For example, an

EPROM cell may be formed that uses a memristive capacitor to form a portion of the EPROM cell. More specifically, a first conductive layer, that forms part of the floating gate, may be separated from a second conductive layer, that forms the control gate, by a dielectric layer. The dielectric layer may be formed of an oxide material having a high dielectric constant. Using such a sandwiched layering with a high dielectric constant oxide material as the dielectric material between two conductive, or metal plates, may allow for a thinner EPROM cell to be formed while maintaining a sufficient capacitance for effective memory storage.

[0018] More specifically, the present disclosure describes a printhead with a number of high dielectric erasable programmable read only memory (EPROM) cells. The printhead includes a number of nozzles to deposit an amount of fluid onto a print medium. Each nozzle includes a firing chamber to hold the amount of fluid, an opening to dispense the amount of fluid onto the print medium, and an ejector to eject the amount of fluid through the opening. The printhead also includes a number of EPROM cells. Each EPROM cell includes a substrate having a source and a drain disposed therein, a floating gate separated from the substrate by a first dielectric layer, and a control gate separate from the floating gate by a second dielectric layer. The second dielectric layer includes a high-dielectric constant material.

[0019] The present disclosure also describes a printer cartridge having a number of high dielectric EPROM cells. The cartridge includes a fluid supply and printhead to deposit fluid from the fluid supply onto a print medium. The printhead includes a number of EPROM cells. Each EPROM cell includes a substrate having a source and a drain disposed therein, a polysilicon layer separated from the substrate by a first dielectric layer, and a first conductive layer separated from the polysilicon layer by a third dielectric layer. The first conductive layer contacts the polysilicon layer through a gap in the third dielectric layer and the first conductive layer and the polysilicon layer form a floating gate of the EPROM cell. The printhead also includes a second conductive layer separated from the first conductive layer by a second dielectric layer. The second conductive layer forms a control gate of the EPROM cell and the second dielectric layer has a high dielectric constant.

[0020] A printer cartridge and a printhead that utilize high dielectric EPROM cells may provide memory storage to a printhead in the form of EPROM memory, while reducing the number and thickness of layers used to form the printhead. Moreover, the layers used to form the EPROM may correspond to layers used to form other components, such as firing resistors and memristors of the printhead. Accordingly, a set number of layers may be co-utilized to form the EPROM memory cells.

[0021] As used in the present specification and in the appended claims, the term "printer cartridge" may refer to a device used in the ejection of ink, or other fluid, onto a print medium. In general, a printer cartridge may be a fluidic ejection device that dispenses fluid such as ink, wax, polymers, or other fluids. A printer cartridge may include a printhead. In some examples, a printhead may be used in printers, graphic plotters, copiers, and facsimile machines. In these examples, a printhead may eject ink, or another fluid, onto a medium such as paper to form a desired image or a desired three-dimensional geometry.

[0022] Accordingly, as used in the present specification and in the appended claims, the term "printer" is meant to be understood broadly as any device capable of selectively placing a fluid onto a print medium. In one example the printer is an inkjet printer. In another example, the printer is a three-dimensional printer. In yet another example, the printer is a digital titration device.

[0023] Still further, as used in the present specification and in the appended claims, the term "fluid" is meant to be understood broadly as any substance that continually deforms under an applied shear stress. In one example, a fluid may be a pharmaceutical. In another example, the fluid may be an ink. In another example, the fluid may be a liquid.

[0024] Still further, as used in the present specification and in the appended claims, the term "print medium" is meant to be understood broadly as any surface onto which a fluid ejected from a nozzle of a printer cartridge may be deposited. In one example, the print medium may be paper. In another example, the print medium may be an edible substrate. In yet another example, the print medium may be a medicinal pill.

[0025] Still further, as used in the present specification and in the appended claims, the term “memristor” may refer to a passive two-terminal circuit element that maintains a functional relationship between the time integral of current, and the time integral of voltage.

[0026] Still further, as used in the present specification and in the appended claims, the term “high dielectric” may refer to any structure that includes a dielectric layer having a dielectric constant of greater than 6. For example, a high dielectric EPROM may be an EPROM that has at least one dielectric layer, i.e., the second dielectric layer, having a dielectric constant greater than 6. Similarly a high dielectric oxide material, may be an oxide material with a dielectric constant greater than 6.

[0027] Still further, as used in the present specification and in the appended claims, the term “short-channel” may refer to a transistor that has a short channel length. For example, the channel, the space between source and drain, may be of the same order of magnitude as the depletion-layer widths. As a numeric example, the distance between a source and a drain of a short-channel transistor may be less than 2.4 microns.

[0028] Yet further, as used in the present specification and in the appended claims, "a", "an", and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise.

[0029] Yet further, as used in the present specification and in the appended claims, the term “a number of” or similar language may include any positive number including 1 to infinity; zero not being a number, but the absence of a number.

[0030] In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present systems and methods. It will be apparent, however, to one skilled in the art that the present apparatus, systems, and methods may be practiced without these specific details. Reference in the specification to "an example" or similar language means that a particular feature, structure, or characteristic described is included in at least that one example, but not necessarily in other examples.

[0031] Turning now to the figures, Fig. 1 is a diagram of a printing system (100) with a printer cartridge (114) and printhead (116) according to one example of the principles described herein. In some examples, the printing system (100) may be included on a printer. The system (100) includes an interface with a computing device (102). The interface enables the system (100) and specifically the processor (108) to interface with various hardware elements, such as the computing device (102), external and internal to the system (100). Other examples of external devices include external storage devices, network devices such as servers, switches, routers, and client devices among other types of external devices.

[0032] In general, the computing device (102) may be any source from which the system (100) may receive data describing a job to be executed by the controller (106) in order to eject fluid onto the print medium (126). For example, via the interface, the controller (106) receives data from the computing device (102) and temporarily stores the data in the data storage device (110). Data may be sent to the controller (106) along an electronic, infrared, optical, or other information transfer path. The data may represent a document and/or file to be printed. As such, data forms a job for and includes job commands and/or command parameters.

[0033] A controller (106) includes a processor (108), a data storage device (110), and other electronics for communicating with and controlling the printhead (116). The controller (106) receives data from the computing device (102) and temporarily stores data in the data storage device (110).

[0034] The controller (106) controls the printhead (116) in ejecting fluid from the nozzles (124). For example, the controller (106) defines a pattern of ejected fluid drops that form characters, symbols, and/or other graphics or images on the print medium (126). The pattern of ejected fluid drops is determined by the print job commands and/or command parameters received from the computing device (102). The controller (106) may be an application specific integrated circuit (ASIC), on a printer for example, to determine the level of fluid in the printhead (116) based on resistance values of EPROM cells integrated on the printhead (116). The ASIC may include a current source and an analog to digital converter (ADC). The ASIC converts a voltage present at the current source to determine a resistance of an EPROM cell, and then determine a corresponding digital resistance value through the ADC. Computer readable program code, executed through executable instructions enables the resistance determination and the subsequent digital conversion through the ADC.

[0035] The processor (108) may include the hardware architecture to retrieve executable code from the data storage device (110) and execute the executable code. The executable code may, when executed by the processor (108), cause the processor (108) to implement at least the functionality of ejecting fluid onto the print medium (126). The executable code may also, when executed by the processor (108), cause the processor (108) to implement the functionality of providing instructions to the power supply (130) such that the power supply (130) provides power to the components of the system (100).

[0036] The data storage device (110) may store data such as executable program code that is executed by the processor (108) or other processing device. The data storage device (110) may specifically store computer code representing a number of applications that the processor (108) executes to implement at least the functionality described herein.

[0037] The data storage device (110) may include various types of memory modules, including volatile and nonvolatile memory. For example, the data storage device (110) of the present example includes Random Access Memory (RAM), Read Only Memory (ROM), and Hard Disk Drive (HDD) memory. Many other types of memory may also be utilized, and the present specification contemplates the use of many varying type(s) of memory in the data storage device (110) as may suit a particular application of the principles described herein. In certain examples, different types of memory in the data storage device (110) may be used for different data storage needs. For example, in certain examples the processor (108) may boot from Read Only

Memory (ROM), maintain nonvolatile storage in the Hard Disk Drive (HDD) memory, and execute program code stored in Random Access Memory (RAM).

[0038] Generally, the data storage device (110) may include a computer readable medium, a computer readable storage medium, or a non-transitory computer readable medium, among others. For example, the data storage device (110) may be an electronic, magnetic, optical, electromagnetic, infrared, or semiconductor system, apparatus, or device, or any suitable combination of the foregoing. More specific examples of the computer readable storage medium may include, for example, the following: an electrical connection having a number of wires, a portable computer diskette, a hard disk, a random access memory (RAM), a read-only memory (ROM), an erasable programmable read-only memory (EPROM or Flash memory), a portable compact disc read-only memory (CD-ROM), an optical storage device, a magnetic storage device, or any suitable combination of the foregoing. In the context of this document, a computer readable storage medium may be any tangible medium that can contain, or store computer usable program code for use by or in connection with an instruction execution system, apparatus, or device. In another example, a computer readable storage medium may be any non-transitory medium that can contain, or store a program for use by or in connection with an instruction execution system, apparatus, or device.

[0039] The printing system (100) includes a printer cartridge (114) that includes a printhead (116) and a fluid supply (112). The printer cartridge (114) may be removable from the system (100) for example, as a replaceable printer cartridge (114).

[0040] The printer cartridge (114) includes a printhead (116) that ejects drops of fluid through a plurality of nozzles (124) towards a print medium (126). The print medium (126) may be any type of suitable sheet or roll material, such as paper, card stock, transparencies, polyester, plywood, foam board, fabric, canvas, and the like. In another example, the print medium (126) may be an edible substrate. In yet one more example, the print medium (126) may be a medicinal pill.

[0041] Nozzles (124) may be arranged in columns or arrays such that properly sequenced ejection of fluid from the nozzles (124) causes characters, symbols, and/or other graphics or images to be printed on the print medium (126) as the printhead (116) and print medium (126) are moved relative to each other. In one example, the number of nozzles (124) fired may be a number less than the total number of nozzles (124) available and defined on the printhead (116).

[0042] The printer cartridge (114) also includes a fluid supply (112) to supply an amount of fluid to the printhead (116). In general, fluid flows between the fluid supply (112) and the printhead (116). In some examples, a portion of the fluid supplied to the printhead (116) is consumed during operation and fluid not consumed during printing is returned to the fluid supply (112).

[0043] In some examples, a mounting assembly positions the printhead (116) relative to a media transport assembly, and media transport assembly positioning the print medium (126) relative to printhead (116). Thus, a print zone (128), indicated by the dashed box, is defined adjacent to the nozzles (124) in an area between the printhead (116) and the print medium (126). In one example, the printhead (116) is a scanning type printhead (116). As such, the mounting assembly includes a carriage for moving the printhead (116) relative to the media transport assembly to scan the print medium (126). In another example, the printhead (116) is a non-scanning type printhead (116). As such, the mounting assembly fixes the printhead (116) at a prescribed position relative to the media transport assembly. Thus, the media transport assembly positions the print medium (126) relative to the printhead (116).

[0044] The printhead (116) also includes a high dielectric EPROM array (134). As described above, a high dielectric EPROM array (134) may be used to store data. For example, each EPROM cell initially may have all gates, i.e., the control gate and floating gate open, putting each EPROM cell in the array (134) in a low resistance state. To program an EPROM cell of the EPROM array (134), or to change the state of the EPROM cell for example to a high resistance state, a programming voltage is applied to a control gate and drain of the EPROM cell while a source and substrate of the EPROM are held at ground. This programming voltage draws electrons from the drain to the floating gate through hot carrier injection. The excited electrons are pushed through and trapped on the other side of the dielectric layer, giving the floating gate a more negative charge, thereby increasing the effective threshold voltage of the floating gate of the EPROM cell. The threshold voltage referring to a minimum voltage to turn on the transistor or the EPROM cell. During use of the EPROM cell, a cell impedance measurement unit monitors the resistance of the EPROM cell. If the EPROM cell resistance is low, the EPROM cell is determined to be in a first state (or pre-programmed state) associated with a first logic value. If the cell resistance is high, the cell is determined to be in a second state (or programmed state) associated with a second logic value. Accordingly, a string of programmed and un-programmed EPROM cells in an EPROM array (134) form a string of ones and zeros which are used to represent data stored in the printhead (116).

[0045] During reading, a single EPROM cell in an EPROM array (134) may be identified. In this example, each EPROM cell is connected to a column select transistor and a row select transistor for multiplexing. When both transistors are turned on, then the EPROM cell is selected. The select transistors are controlled by multiplexing signals.

[0046] The EPROM array (134) is a high dielectric EPROM array (134) meaning that the EPROM array (134) is formed of EPROM cells having at least one dielectric layer that has a high dielectric constant. For example, a layer of dielectric material having a high dielectric constant may be positioned between the floating gate and the control gate of the EPROM cells. A material with a high dielectric constant may allow for a thinner EPROM cell, and corresponding thinner EPROM array (134) to be used on the printhead (116) all while maintaining an EPROM cell with sufficient distinction between states. Put another way, the high dielectric constant may result in a larger gap between voltages corresponding to an un-programmed and programmed state of an EPROM cell such that easy detection of different voltages and corresponding logic values is enabled. As will be described below, the EPROM cell may include a short-channel transistor including a source, a drain, and a gate oxide.

[0047] As will be described below, the high dielectric EPROM array (134) may be used to store any type of data. Examples of data that may be stored in the high dielectric EPROM array (134) include fluid supply specific data and/or fluid identification data, fluid characterization data, fluid usage data, printhead (116) specific data, printhead (116) identification data, warranty data, printhead (116) characterization data, printhead (116) usage data, authentication data, security data, Anti-Counterfeiting data (ACF), ink drop weight, firing frequency, initial printing position, acceleration information, and gyro information, among other forms of data. In a number of examples, the high dielectric EPROM array (134) is written at the time of manufacturing and/or during the operation of the printer cartridge (114). The data stored by it may provide information to the controller to adjust the operation of the printer and ensure correct operation.

[0048] Fig. 2 is a block diagram of a printer cartridge (114) that uses a printhead (116) with a number of high dielectric EPROM cells (248) according to one example of the principles described herein. In some examples, the printer cartridge (114) includes a printhead (116) that carries out at least a part of the functionality of the printer cartridge (114). For example, the printhead (116) may include a number of nozzles (Fig. 1, 124). The printhead (116) ejects drops of fluid from the nozzles (Fig. 1, 124) onto a print medium (Fig. 1, 126) in accordance with a received print job. The printhead (116) may also include other circuitry to carry out various functions related to printing. In some examples, the printhead (116) is part of a larger system such as an integrated printhead (IPH). The printhead (116) may be of varying types. For example, the printhead (116) may be a thermal inkjet (TIJ) printhead or a piezoelectric inkjet (PIJ) printhead, among other types of printhead (116).

[0049] The printhead (116) includes a high dielectric EPROM array (134) to store information relating to at least one of the printer cartridge (114) and the printhead (116). In some examples, the high dielectric EPROM array (134) includes a number of high dielectric EPROM cells (248-1, 248-2) formed in the printhead (116). To store information, an EPROM cell (248) may be set to a particular logic value.

[0050] As will be described below, an EPROM cell (248) includes a control gate, a floating gate, and a semiconductor substrate. The control gate and the floating gate are capacitively coupled to one another with a dielectric material between them such that the control gate voltage is coupled to the floating gate voltage. Another layer of dielectric material is also disposed between the floating gate and the semiconductor substrate.

[0051] An EPROM array (134) may store information by setting a number of EPROM cells (248) to different logic values. Setting an EPROM cell (248) to a value other than its initial value may be referred to as programming the EPROM cell (248). During programming, a high voltage bias on the drain of the EPROM cell (248) generates energetic "hot" electrons. A positive voltage bias between the control gate and the drain pulls some of these hot electrons onto the floating gate. As electrons are pulled onto the floating gate, for example through Fowler-Nordheim (FN) tunneling, the threshold voltage of the EPROM cell (248), that is, the voltage used to regulate the gate/drain to conduct current, increases. If sufficient electrons are pulled onto the floating gate, the effective cell threshold voltage will increase. As a result, for a given gate and drain bias voltage, the source-to-drain current will be reduced or suspended. This will cause the EMPROM cell (248) to block current at that voltage level, which changes the operating state of the EPROM cell (248) from a low resistance state to a high resistance state. After programming of the EPROM cell (248), a cell sensor (not shown) is used during operation to detect the state of the EPROM cell (248).

[0052] A specific numeric example is provided below. In this example, before programming a resistance of an EPROM cell (248) may be low, for example approximately 3,000 Ohms. During programming a positive bias is applied to the gate and drain of the EPROM cell (248) such that a potential is created between the drain and the control gate. The positive bias applied to the drain may be near breakdown levels, such as between 12-16 volts. At the same time, the source and a substrate in which the source and drain are disposed may be set to ground. The positive voltage difference between the source and the drain draws electrons towards the drain. The large positive potential excites electrons and when the electrons have sufficient energy, pulls electrons from the drain to the floating gate, through hot carrier injection, giving the floating gate a more negative charge, thereby increasing the effective threshold voltage of the floating gate. The threshold voltage of the floating gate is a voltage to turn on the transistor or the EPROM cell (248). Accordingly, in some examples enough electrons may be passed to the floating gate to increase its resistance, for example to 6,000 Ohms. In other words, the trapped electrons may cause a threshold voltage of approximately -5 V. Accordingly, when a signal of 5 V is applied to the control gate, no channel would be formed in the floating gate, thus increasing the resistance; which increase in resistance can be read by a controller (Fig. 1, 106) to determine a logical value of the EPROM cell (248). Accordingly, the resistance, and corresponding logical value of the EPROM cell (248) relies on the voltage of the floating gate.

[0053] The number of EPROM cells (248) are grouped together into an EPROM array (134). In some examples, the EPROM array (134) may be a cross bar array. In this example, EPROM cells (248) may be formed at an intersection of a first set of elements and a second number of elements, the elements forming a grid of intersecting nodes, a node defining an EPROM cell (248).

[0054] The EPROM array (134) may be used to store any type of data. Examples of data that may be stored in the EPROM array (134) include fluid supply specific data and/or fluid identification data, fluid characterization data, fluid usage data, printhead (116) specific data, printhead (116) identification data, warranty data, printhead (116) characterization data, printhead (116) usage data, authentication data, security data, Anti-Counterfeiting data (ACF), ink drop weight, firing frequency, initial printing position, acceleration information, and gyro information, among other forms of data. In a number of examples, the EPROM array (134) is written at the time of manufacturing and/or during the operation of the printer cartridge (114).

[0055] In some examples, the printer cartridge (114) may be coupled to a controller (Fig. 1, 106) that is disposed within the system (100). The controller (Fig.1, 106) receives a control signal from an external computing device (Fig. 1, 102). The controller (Fig. 1, 106) may be an application-specific integrated circuit (ASIC) found on a printer. A computing device (Fig. 1, 102) may send a print job to the printer cartridge (114), the print job being made up of text, images, or combinations thereof to be printed. The controller (Fig. 1, 106) may facilitate storing information to the EPROM array (134). Specifically, the controller (Fig. 1, 106) may pass at least one control signal to the number of EPROM cells (248). For example, the controller (Fig. 1, 106) may be coupled to the printhead (116), via a control line such as an identification line. Via the identification line, the controller (Fig. 1, 106) may change the logic state of EPROM cells (248) in the EPROM array (134) to effectively store information to an EPROM array (134). For example, the controller (106) may send data such as authentication data, security data, and print job data, in addition to other types of data to the printhead (116) to be stored on the EPROM array (134).

[0056] Figs. 3A and 3B are diagrams of a printer cartridge (114) with a number of high dielectric EPROM cells (248) according to one example of the principles described herein. As discussed above, the printhead (116) may include a number of nozzles (124). In some examples, the printhead (116) may be broken up into a number of print dies with each die having a number of nozzles (124). The printhead (116) may be any type of printhead (116) including, for example, a printhead (116) as described in Figs. 3A-3C. The examples shown in Figs. 3A-3C are not meant to limit the present description. Instead, various types of printheads (116) may be used in conjunction with the principles described herein.

[0057] The printer cartridge (114) also includes a fluid reservoir (112), a flexible cable (336), and conductive pads (338). In some examples, the fluid may be ink. For example, the printer cartridge (114) may be an inkjet printer cartridge, the printhead (116) may be an inkjet printhead, and the ink may be inkjet ink.

[0058] The EPROM array (134) depicted in Fig. 3C may be similar to the EPROM array (134) depicted in Figs. 1 and 2. Specifically, the EPROM array (134) may include EPROM cells (Fig. 2, 248) formed at least in part with a dielectric layer formed of a high dielectric oxide material. The flexible cable

(336) is adhered to two sides of the printer cartridge (114) and contains traces that electrically connect the EPROM array (134) and printhead (116) with the conductive pads (338).

[0059] The printer cartridge (114) may be installed into a cradle that is integral to the carriage of a printer. When the printer cartridge (114) is correctly installed, the conductive pads (338) are pressed against corresponding electrical contacts in the cradle, allowing the printer to communicate with, and control the electrical functions of, the printer cartridge (114). For example, the conductive pads (338) allow the printer to access and write to the EPROM array (134).

[0060] The EPROM array (134) may contain a variety of information including the type of printer cartridge (114), the kind of fluid contained in the printer cartridge (114), an estimate of the amount of fluid remaining in the fluid reservoir (112), calibration data, error information, and other data. In one example, the EPROM array (134) may include information regarding when the printer cartridge (114) should be maintained.

[0061] To create an image, the system (Fig. 1, 100) moves the carriage containing the printer cartridge (114) over a print medium (Fig. 1, 126). At appropriate times, the system (Fig. 1, 100) sends electrical signals to the printer cartridge (114) via the electrical contacts in the cradle. The electrical signals pass through the conductive pads (338) and are routed through the flexible cable (336) to the printhead (116). The printhead (116) then ejects a small droplet of fluid from the reservoir (112) onto the surface of the print medium (Fig. 1, 126). These droplets combine to form an image on the surface of the print medium (Fig. 1, 126).

[0062] Fig. 3C is a diagram of a printhead (116) with a number of high dielectric EPROM cells (Fig. 2, 248) according to one example of the principles described herein. More specifically, as depicted in Fig. 3A, the printhead (116) may include a high dielectric EPROM array (134) that includes a number of high dielectric EPROM cells (Fig. 2, 248) as described herein. The printhead (116) may also include a number of components for depositing a fluid onto a print medium (Fig. 1, 126). For example, the printhead (116) may include a number of nozzles (124). For simplicity, Fig. 3C details a single nozzle (124); however a number of nozzles (124) are present on the printhead (116). The printhead (116) may include any number of nozzles (124). In an example where the fluid is an ink, a first subset of nozzles (124) may eject a first color of ink while a second subset of nozzles (124) may eject a second color of ink. Additional groups of nozzles (124) may be reserved for additional colors of ink.

[0063] A nozzle (124) may include an ejector (342), a firing chamber (344), and an opening (346). The opening (346) may allow fluid, such as ink, to be deposited onto a surface, such as a print medium (Fig. 1, 126). The firing chamber (344) may include a small amount of fluid. The ejector (342) may be a mechanism for ejecting fluid through an opening (346) from a firing chamber (344), where the ejector (342) may include a firing resistor or other thermal device, a piezoelectric element, or other mechanism for ejecting fluid from the firing chamber (344).

[0064] For example, the ejector (342) may be a firing resistor. The firing resistor heats up in response to an applied voltage. As the firing resistor heats up, a portion of the fluid in the firing chamber (344) vaporizes to form a bubble. This bubble pushes liquid fluid out the opening (346) and onto the print medium (Fig. 1, 126). As the vaporized fluid bubble pops, a vacuum pressure within the firing chamber (344) draws fluid into the firing chamber (344) from the fluid supply (112), and the process repeats. In this example, the printhead (116) may be a thermal inkjet printhead.

[0065] In another example, the ejector (342) may be a piezoelectric device. As a voltage is applied, the piezoelectric device changes shape which generates a pressure pulse in the firing chamber (344) that pushes a fluid out the opening (346) and onto the print medium (Fig. 1, 126). In this example, the printhead (116) may be a piezoelectric inkjet printhead.

[0066] The printhead (116) and printer cartridge (114) may also include other components to carry out various functions related to printing. For simplicity, in Figs. 3A-3C, a number of these components and circuitry included in the printhead (116) and printer cartridge (114) are not indicated; however such components may be present in the printhead (116) and printer cartridge

(114). In some examples, the printer cartridge (114) is removable from a printing system for example, as a disposable printer cartridge.

[0067] Figs. 4A and 4B are diagrams of a high dielectric EPROM cell (248) according to one example of the principles described herein. Specifically, Fig. 4A is a circuit diagram of the high dielectric EPROM cell (248) and Fig. 4B is a cross-sectional diagram of the layers of the high dielectric EPROM cell (248).

[0068] The EPROM cell (248) includes a control gate (450), a floating gate (452), a source (456) and a drain (458). In some examples, the source (456) and the drain (458) may be formed in a substrate (454). In some examples, the substrate (454) maybe an n-type substrate (454) with p-doped portions forming the source (456) and drain (458). In other examples, the substrate (454) may be a p-type substrate (454) with n-doped portions forming the source (456) and the drain (458). In some examples, the EPROM cell (248) may include a short-channel transistor. For example, the EPROM cell (248) may include a short-channel transistor that includes the source (456) the drain (458) and a first dielectric layer (460) such as a gate oxide. The width of the gate oxide in a short-channel EPROM transistor may be between 2.2 microns and 2.4 microns.

[0069] The floating gate (452) of the EPROM cell (248) may be separated from the substrate (454) by a first dielectric layer (460). The first dielectric layer (460) may be a gate oxide that electrically isolates the floating gate (452) from the source (456) and the drain (458). In some examples, the gate oxide may be made of a high dielectric constant material, such as that used between the control gate (450) and the floating gate (452). In some examples, the first dielectric layer (460) may be silicon dioxide, silicon carbide, and silicon nitride among other dielectric materials. In some examples, the gate oxide may be 700 Angstroms thick.

[0070] In some examples, the floating gate (452) of the EPROM cell (248) may be formed by a polysilicon layer (462) and a first conductive layer (464) that is electrically coupled to the polysilicon layer (462). In some examples, the polysilicon layer (462) may be polycrystalline silicon that may be doped. For example, the polysilicon layer (462) may be polycrystalline silicon that is n-doped. The first conductive layer (464) may be formed of a conductive material. Examples of conductive materials may include an aluminum copper alloy, an aluminum copper silicon alloy, and a tantalum aluminum alloy with an aluminum copper alloy, and a tantalum silicon nitride with an aluminum copper alloy, among other conductive materials.

[0071] The layering of the substrate (454), the first dielectric layer (460) and polysilicon layer (462) can be depicted in a circuit as a capacitor as detailed below in Fig. 5. In some examples, during formation, the polysilicon layer (462) may initially be separated from the first conductive layer (464) by a third dielectric layer (478). The third dielectric layer (478) may be formed from phosphosilicate glass (PSG), borophosphosilicate glass (BPSG) and/or undoped silicate glass (USG), among other dielectric materials. The first conductive layer (464) may contact the polysilicon layer (462) via a gap in the third dielectric layer (478). In summary, the floating gate (452) of the EPROM cell (248) may be formed from a first conductive layer (464) and a polysilicon layer (462) that may be electrically coupled to one another through a gap in a third dielectric layer (478). The first dielectric layer (460) between the polysilicon layer (462) and the substrate (454) creates a capacitive coupling between the polysilicon layer (462) and the substrate (454).

[0072] The control gate (450) of the EPROM cell (248) may be separated from the floating gate (452) by a second dielectric layer (466). In some examples, the second dielectric layer (466) may be formed from tetraethyl orthosilicate (TEOS) or other dielectric material. The control gate (450) may be provided by a second conductive layer (468). The second conductive layer (468) may be formed of a conductive material. Examples of conductive materials may include an aluminum copper alloy, an aluminum copper silicon alloy, and a tantalum aluminum alloy with an aluminum copper alloy, and tantalum silicon nitride with an aluminum copper alloy, among other conductive materials.

[0073] The second dielectric layer (466) between the first conductive layer (464) of the floating gate (452) and the second conductive layer (468) of the control gate (450) creates a capacitive coupling between the first conductive layer (464) and the second conductive layer (468). In other words, the second conductive layer (468) forms the control gate (450) and the first conductive layer (464) and the polysilicon layer (462) form the floating gate (452) of the EPROM cell (248), with the second dielectric layer (466) and first dielectric layer (460) respectively forming a capacitive coupling between the corresponding layers.

[0074] In some examples, the second dielectric layer (466) may be an oxide material with a high dielectric constant. For example, the second dielectric layer (466) may be formed of a material having a dielectric constant of at least 6. The second dielectric layer (466) may be a nitride material with a high dielectric constant. Specifically, the second dielectric layer (466) may be formed of tantalum oxide, aluminum oxide, silicon nitride ($Si3N4$), halfnium oxide, zirconium oxide, titanium oxide (having a dielectric constant of 80) or combinations thereof. While specific reference is made to various materials that may be used to form the second dielectric layer (466) any suitable material may be used.

[0075] Including a second dielectric layer (466) with a high dielectric constant may allow for a thinner EPROM cell (248) by reducing the size of the second dielectric layer (466) while preserving a desired capacitance of the EPROM cell (248). For example, as described above, the resistance of the EPROM cell (248), and corresponding logic value, is dependent upon the voltage at the floating gate (452). The voltage at the floating gate (452) is dependent at least in part, upon the capacitance of the control gate (450), a larger capacitance at the control gate (450) being desired so as to yield a more clear distinction between states of the EPROM cell (248). Accordingly, using a material with a smaller dielectric constant may necessitate a larger dielectric to achieve the desired capacitance at the control gate (450). In other words, the high dielectric constant second dielectric layer (466) may allow for a thinner second dielectric layer (466) than would otherwise be possible while maintaining a desired capacitance. For example, the second dielectric layer (466) may be between 2 and 100 nanometers thick. For example, the second dielectric layer (466) may be between 5 and 15 nanometers thick. In some examples, the thickness of the second dielectric layer (466) may be manipulated to achieve a desired capacitance.

[0076] In some examples, the second dielectric layer (466) may have a capacitance of at least 0.15 picofarads. As described above, using a second dielectric layer (466) of a highly dielectric material, such as an oxide or nitride of aluminum, tantalum, silicon, or combinations thereof, a smaller EPROM cell (248) for a given capacitance may be formed. In some examples, at least one of the first conductive layer (464) and the second conductive layer (468) may be less than 400 squared micrometers. For example, at least one of the first conductive layer (464) and the second conductive layer (468) may be less than 100 squared micrometers. Put another way, in some examples, the dielectric constant of the second dielectric layer (466) may be sufficiently high such that the area of the second dielectric layer (466) may be smaller than 400 squared micrometers and the thickness may be between 2 nanometers and 100 nanometers thick while exhibiting a capacitance of at least 0.15 picofarads.

[0077] In some examples, the second dielectric layer (466) may be defined by a ratio of a control gate (450) capacitance and a floating gate (452) capacitance. The control gate (450) capacitance refers to the capacitance created by the first conductive layer (464)/second dielectric layer (466)/second conductive layer (468) and the floating gate (452) capacitance refers to the capacitance created by the substrate (454)/first dielectric layer (460)/ polysilicon layer (462). In other words, the capacitance of the control gate (450) and the floating gate (452) may be defined by the properties of the dielectric layers (462, 466). For example, the separation of the first conductive layer (464) from the second conductive layer (468) by the second dielectric layer (466) creates a capacitive coupling of the control gate (450). In other words, parallel opposing capacitor plates are formed in the first conductive layer (464) and the second conductive layer (468). Similarly, the separation of the polysilicon layer (462) from the substrate (454) by the first dielectric layer (460) creates a capacitive coupling of the floating gate (452) and the source (456) and drain (458).

[0078] Returning to the ratio, the EPROM cell (248) according to the present specification may have a ratio of control gate (450) capacitance and the floating gate (452) capacitance of at least 2. In this example, the floating gate (452) may have a capacitance of 70 femtofarads. Having a conductance ratio of at least 2 as described above may further increase the voltage of the floating gate (452) and may improve the control of the EPROM cell (248). In other words, the ratio described above may further increase the gap between the programmed and un-programmed states by increasing the floating gate (452) voltage. For example, as depicted in Fig. 5, the EPROM cell (248) may be diagramed as a circuit similar to a voltage divider. Accordingly, the voltage (570), V_{float}, seen at the floating gate (Fig. 4, 452) relative to an applied voltage (572), V_{dd}, applied at the control gate (Fig. 4, 450) may be represented by Equation 1 below.

$$V_{float} = \frac{C_{cg}}{C_{fg}+C_{cg}} \cdot V_{dd} \qquad \text{Equation 1.}$$

[0079] In Equation 1, C_{cg} refers to the control gate capacitance (574), and C_{fg} refers to the floating gate capacitance (576). Accordingly, a larger control gate capacitance (574) results in a larger voltage (570), V_{float}, seen at the floating gate (Fig. 4, 452), which increases the programmed resistance of the EPROM cell (248).

[0080] Fig. 6 is a cross-sectional view of a printhead (116) including a high dielectric EPROM cell (248), a memristor (680), and a firing resistor (342) according to one example of the principles described herein. As described above, the printhead (116) may include an EPROM cell (248) that includes a source (456) and a drain (458). The source (456) and drain (458) may be separated from the polysilicon layer (462-1) by a first dielectric layer (460-1).

[0081] As described above, the EPROM cell (248) also includes a first conductive layer (464), a second dielectric layer (466) and a second conductive layer (468). In some examples, the second conductive layer (468) may include multiple sub-layers with different oxidative properties. For example, the first sub-layer (468-1) may include tantalum aluminum alloy and the second sub-layer (468-2) may include an aluminum copper alloy. As depicted in Fig. 6 in some examples, the layers of the EPROM cell (248) may be planar.

[0082] In some examples, at least one of these layers may have the same material properties, or be the same material as other components in the printhead (116). For example, the printhead (116) may include a memristor (680) that includes a first electrode (684), a switching oxide (686) disposed on top of the first electrode (684), and a second electrode (688) disposed on top of the switching oxide (686). In some examples, as depicted in Fig. 6, the second electrode (688) may be a dual layer electrode, i.e., it may include multiple layers of material. For example, the second electrode may include a first sub-layer (688-1) and a second sub-layer (688-2).

[0083] In this example, the first conductive layer (464) of the EPROM cell (248) may be the same material, and in some cases formed of the same layer of the same material, as at least one of the first electrode (684) of the memristor (680) and a first layer (690) of the firing resistor (342). Similarly, the second dielectric layer (466) of the EPROM cell (248) may be the same material, and in some cases formed of the same layer of the same material, as the switching oxide (686) of the memristor. Still further, the second conductive layer (468) of the EPROM cell (248) may be the same material, and in some cases formed of the same layer of the same material, as at least one of the second electrode (688) of the memristor (680) and a second layer (692) and/or third layer (694) of the firing resistor (342).

[0084] More specifically, each of the first EPROM sub-layer (468-1), the first sub-layer (688-1) of the second electrode (688), and a second layer (692) of the firing resistor (342) may each be a similar material such as a tantalum aluminum alloy. In some examples, each of the first EPROM sub-layer (468-1), the first sub-layer (688-1) of the second electrode (688), and a second layer (692) of the firing resistor (342) may be the same layer of material. In other words these components may be formed simultaneously by depositing a single layer of material.

[0085] Similarly, each of the second EPROM sub-layer (468-2), the second sub-layer (688-2) of the second electrode (688), and a third layer (694) of the firing resistor (342) may be formed of the same material such as an aluminum copper alloy. In some examples, each of the second EPROM sub-layer (468-2), the second sub-layer (688-2) of the second electrode (688), and a third layer (694) of the firing resistor (342) may be the same layer of material. In other words these components may be formed simultaneously by depositing a single layer of material.

[0086] The printhead (116) may also include a number of passivation layers (696, 699) that may be from 3,000 to 6,000 Angstroms thick. While the different components may share a printhead (116), the components may be associated with different transistors. For example, a first transistor (698-1) corresponding to the gate (460-1) and the first dielectric layer (462-1) may be utilized by the EPROM cell (248) while a second transistor (698-2) corresponding to the gate (460-2) and the first dielectric layer (462-2) may not be utilized by the EPROM cell (248). Each transistor may be different, for example, the second transistor (698-2) may be a transistor with a width of approximately 2.8 microns and the first transistor (698-1) may be a short-channel transistor with a width between 2.2 and 2.4 microns thick.

[0087] By co-utilizing these layers, multiple layers of different components may be formed simultaneously thus reducing the operations to form the components of a printhead (116). Moreover, as the layers used to form the high dielectric EPROM cell (248) may be presently used for other components such as the memristor (680) and firing resistor (342), the high dielectric EPROM cells (248) may be formed without additional manufacturing equipment or processes.

[0088] Certain examples of the present disclosure are directed to a printer cartridge (Fig. 1, 114) and printhead (Fig. 1, 116) with a number of high dielectric EPROM cells (Fig. 2, 248) that provide a number of advantages not previously offered including, to creating an EPROM memory device that is compact and has a high coupling ratio which leads to an improved programming ratio of the memory device; reducing the footprint of an EPROM cell (Fig. 2, 248) so as to free up valuable silicon space for other components and providing backwards compatibility with existing printers. However, it is contemplated that the devices disclosed herein may provide useful in addressing other issues and deficiencies in a number of technical areas. Therefore the systems and methods disclosed herein should not be construed as addressing any of the particular issues discussed

[0089] The preceding description has been presented to illustrate and describe examples of the principles described. This description is not intended to be exhaustive or to limit these principles to any precise form disclosed. Many modifications and variations are possible in light of the above teaching.

CLAIMS

WHAT IS CLAIMED IS:

1. A printhead with a number of high dielectric erasable programmable read only memory (EPROM) cells, the printhead comprising:

a number of nozzles to deposit an amount of fluid onto a print medium, each nozzle comprising:

a firing chamber to hold the amount of fluid;

an opening to dispense the amount of fluid onto the print medium; and

an ejector to eject the amount of fluid through the opening; and

a number of EPROM cells, each EPROM cell comprising:

a substrate having a source and a drain disposed therein;

a floating gate separated from the substrate by a first dielectric layer; and

a control gate separate from the floating gate by a second dielectric layer;

in which the second dielectric layer comprises a high-dielectric constant material.

2. The printhead of claim 1, in which the fluid is inkjet ink.

3. The printhead of claim 1, in which the second dielectric layer comprises a high-dielectric constant oxide material, a high-dielectric constant nitride material, or combinations thereof.

4. The printhead of claim 1, in which:

the floating gate comprises:

a polysilicon layer; and

a first conductive layer in contact with the polysilicon layer; and

the control gate comprises a second conductive layer.

5. The printhead of claim 1, in which the second dielectric layer has a dielectric constant of greater than 6.

6. The printhead of claim 1, in which a ratio of a capacitance of the second dielectric layer to a capacitance of the first dielectric layer is greater than 2.

7. The printhead of claim 1, in which the second dielectric layer comprises aluminum oxide, tantalum oxide, or combinations thereof.

8. A printer cartridge having a number of high dielectric erasable programmable read only memory (EPROM) cells, the cartridge comprising:

a fluid supply; and

a printhead to deposit fluid from the fluid supply onto a print medium, the printhead comprising;

a number of EPROM cells, each EPROM cell comprising:

a short-channel EPROM transistor comprising a source, a drain, and a gate oxide disposed on a substrate;

a polysilicon layer separated from the substrate by the gate oxide;

a first conductive layer separated from the polysilicon layer by a third dielectric layer; in which:

the first conductive layer contacts the polysilicon layer through a gap in the third dielectric layer; and

the first conductive layer and the polysilicon layer form a floating gate of the EPROM cell; and

a second conductive layer separated from the first conductive layer by a second dielectric layer, in which:

the second conductive layer forms a control gate of the EPROM cell; and

the second dielectric layer has a high dielectric constant.

9. The cartridge of claim 8, in which:

the fluid is inkjet ink;

the printer cartridge is an inkjet printer cartridge; and

the printhead is an inkjet printhead.

10. The cartridge of claim 8, in which the second dielectric layer is between 2 nanometers and 100 nanometers thick.

11. The cartridge of claim 8, in which one of the first conductive layer and the second conductive layer has an area less than 400 squared micrometers.

12. The cartridge of claim 8, in which a capacitance of the second dielectric layer is greater than 0.15 picofarads.

13. The cartridge of claim 8, in which the second dielectric layer comprises aluminum oxide, tantalum oxide, or combinations thereof.

14. The cartridge of claim 8, further comprising a memristor, the memristor comprising:

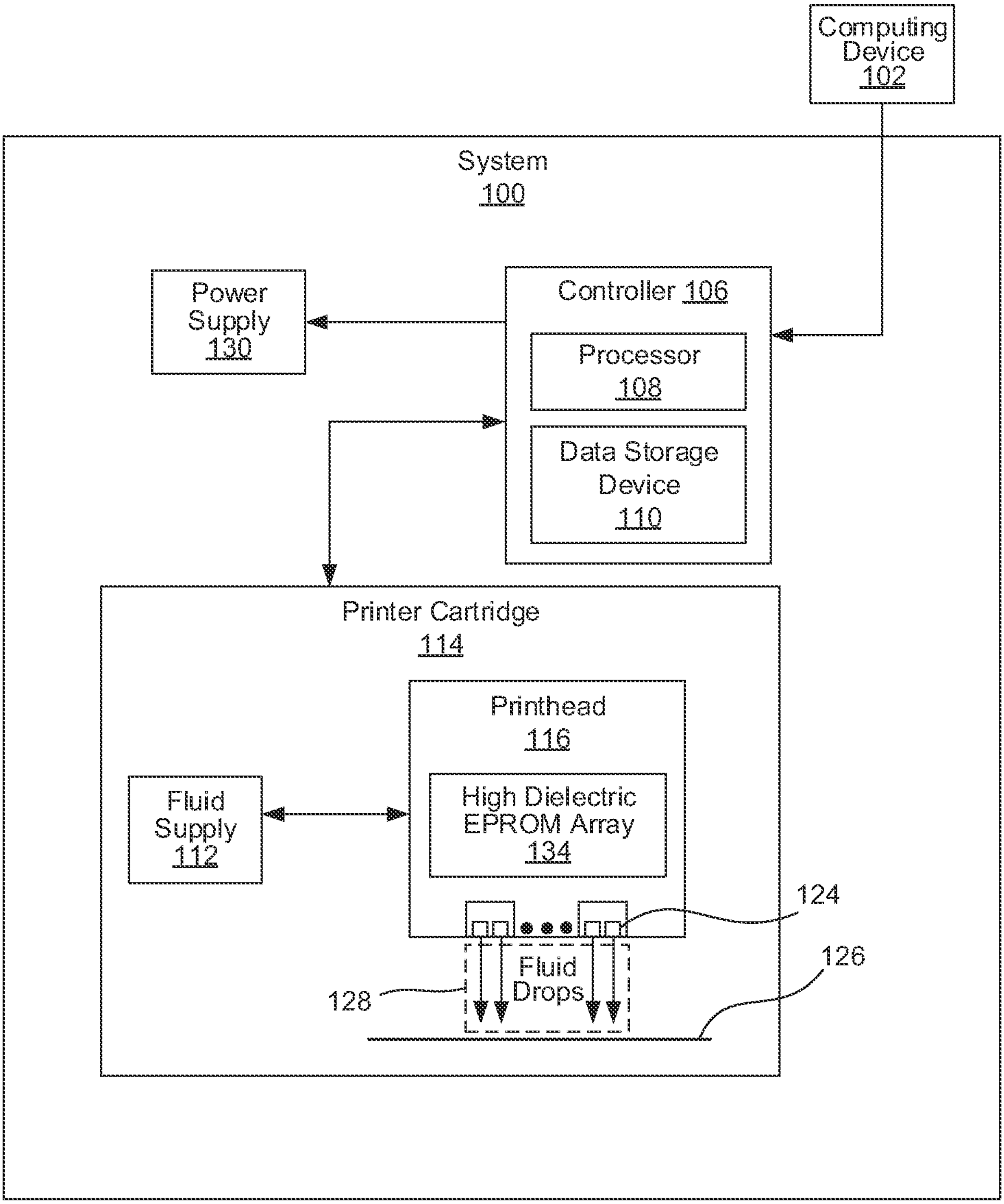
a first electrode;

a switching oxide disposed on top of the first electrode; and

a second electrode disposed on top of the switching oxide;

in which the switching oxide of the memristor comprises the same material as the second dielectric layer of the number of EPROM cells.

15. The cartridge of claim 14, in which the switching oxide of the memristor is formed in a same layer as the second dielectric layer of the number of EPROM cells.



Computing Device 102
System 100
Power Supply 130
Controller 106
Processor 108
Data Storage Device 110
Printer Cartridge 114
Printhead 116
Fluid Supply 112
High Dielectric EPROM Array 134
124
126
128
Fluid Drops

Fig. 1

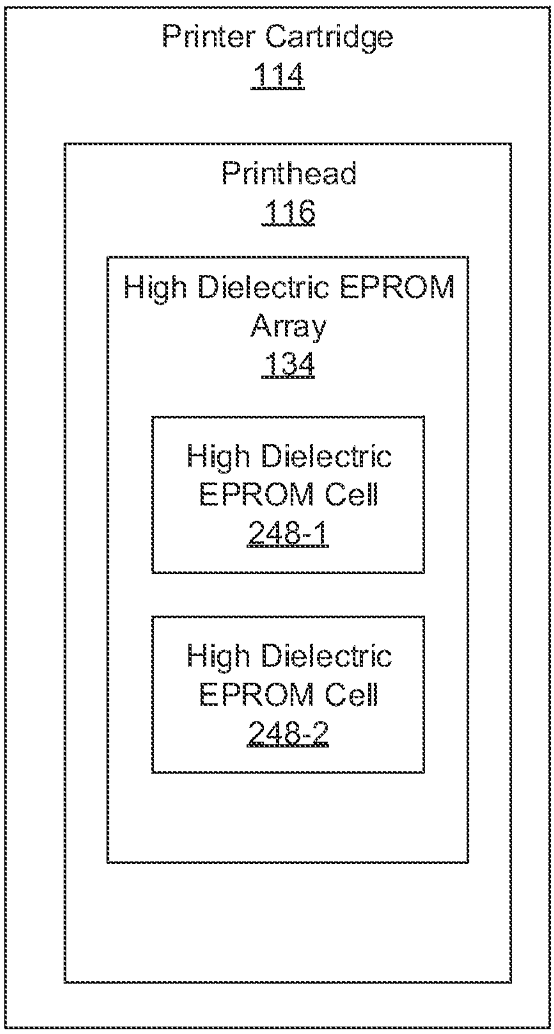

Printer Cartridge
114
Printhead
116
High Dielectric EPROM Array
134
High Dielectric EPROM Cell
248-1
High Dielectric EPROM Cell
248-2

Fig. 2

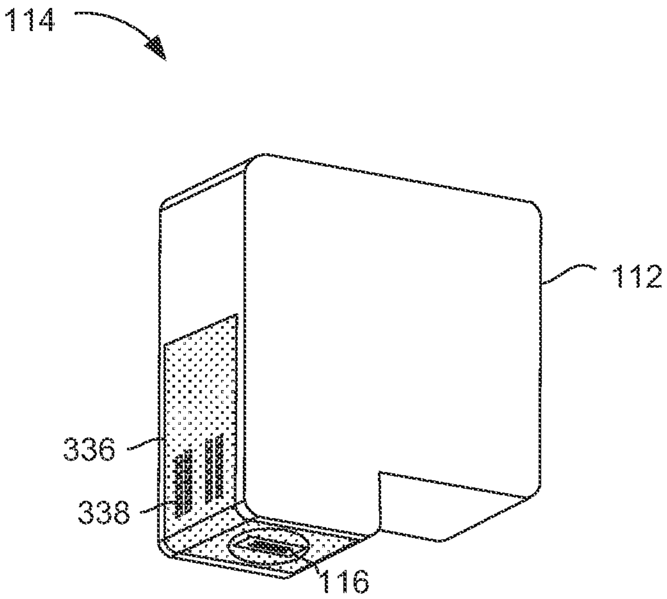


Fig. 3A

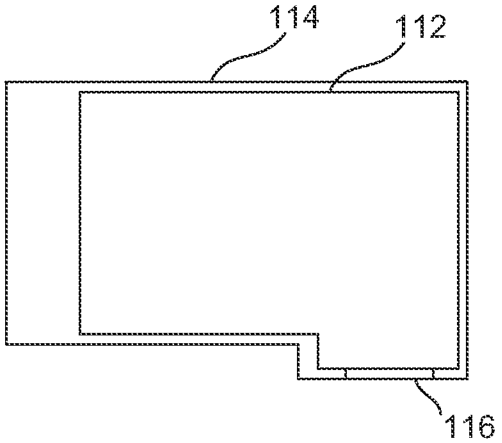


Fig. 3B

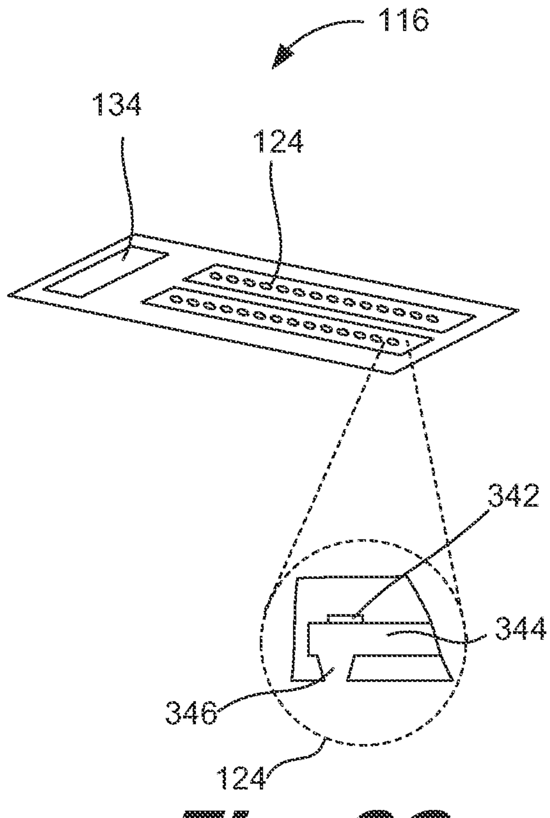


Fig. 3C

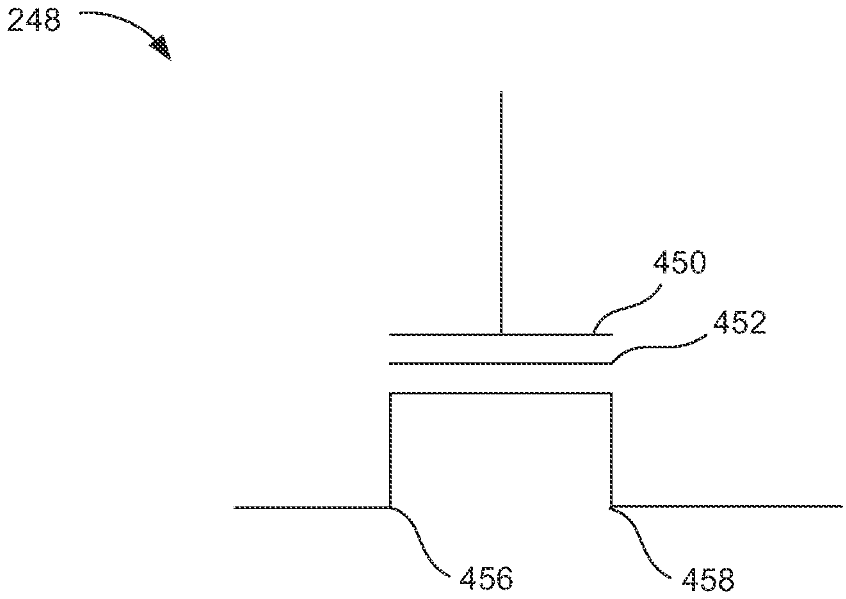


Fig. 4A

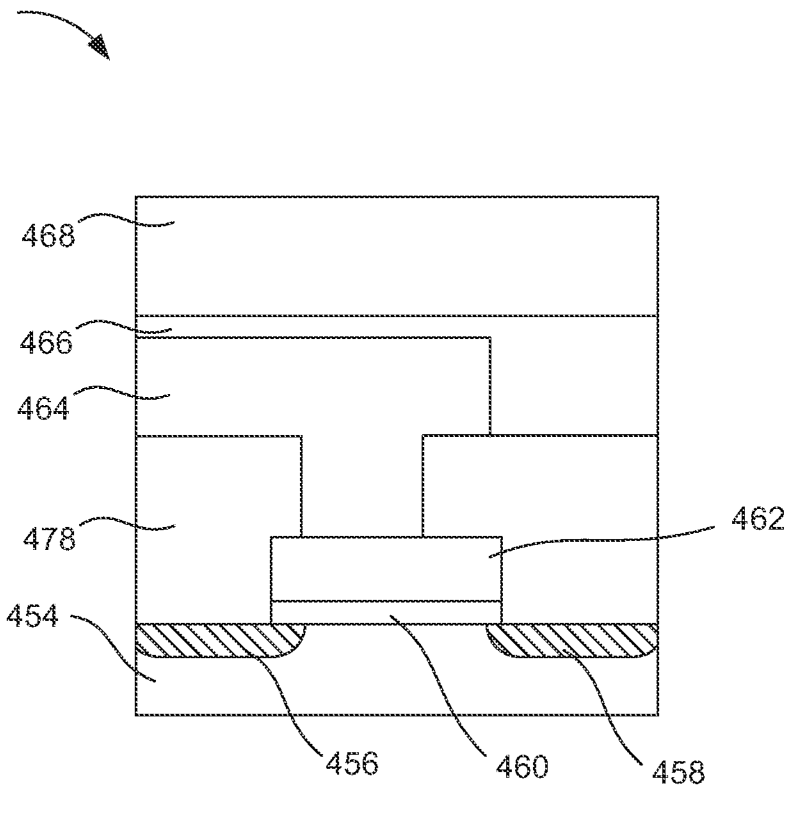


Fig. 4B

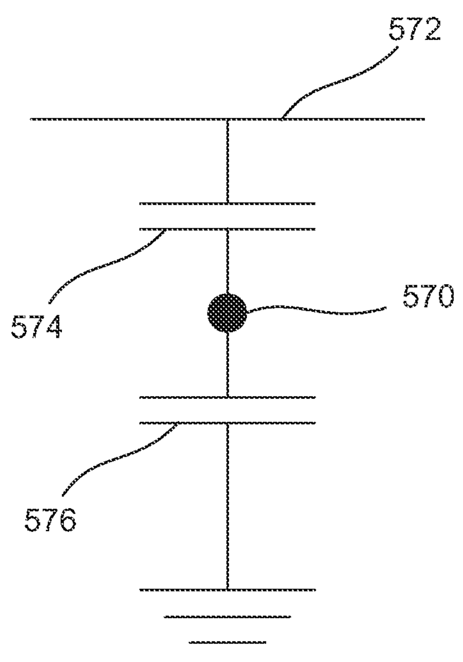


Fig. 5

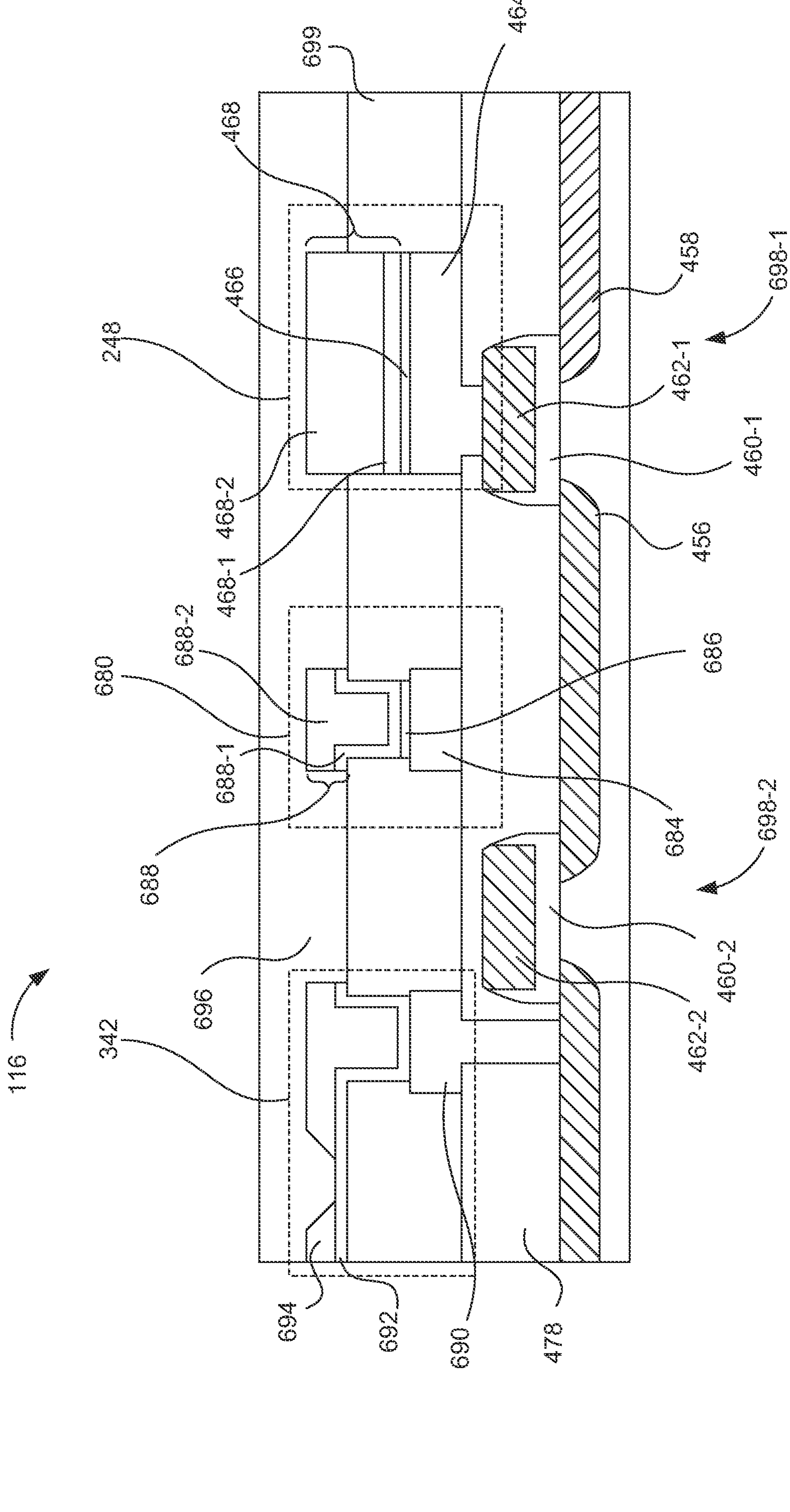

116
342
696
688
688-1
680
688-2
248
468-2
468-1
466
468
699
464
458
462-1
460-1
456
686
684
698-1
698-2
460-2
462-2
694
692
690
478

Fig. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/025944

A. CLASSIFICATION OF SUBJECT MATTER

B41J 2/045(2006.01)i, B41J 2/07(2006.01)i, B41J 2/17(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
B41J 2/045; G11C 11/34; H01L 21/28; G11C 16/04; H01L 21/02; H01L 29/788; H01L 21/00; B41J 2/07; B41J 2/17

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: EPROM, printhead, substrate, source, drain, floating gate, control gate, dielectric layer, electric constant, conductive

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2007-0194371 A1 (BENJAMIN, TRUDY) 23 August 2007 See abstract, paragraphs [0023], [0029], [0030], [0055], [0059], and figures 1, 2, 5, 7.	1-3,5-7
A		4,8-15
Y	WO 2007-019046 A1 (SPANSION LLC et al.) 15 February 2007 See abstract, page 3, lines 5-14, claims 1, 3, and figure 1.	1-3,5-7
A	US 2014-0218436 A1 (GE et al.) 07 August 2014 See abstract, paragraphs [0015], [0016], [0018], [0019], and figures 1, 2.	1-15
A	US 2009-0067256 A1 (BHATTACHARYYA et al.) 12 March 2009 See abstract, paragraph [0024], and figure 3.	1-15
A	US 2004-0191988 A1 (SANDHU et al.) 30 September 2004 See abstract, paragraphs [0031]-[0040], and figures 3-11.	1-15

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 November 2015 (21.11.2015)	**23 November 2015 (23.11.2015)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 35208, Republic of Korea
Facsimile No. +82-42-472-7140

Authorized officer
KIM, Jin Ho
Telephone No. +82-42-481-8699

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/025944

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007-0194371 A1	23/08/2007	AU 2007-238482 A1	25/10/2007
		AU 2007-238482 B2	18/08/2011
		BR PI0707017 A2	12/04/2011
		CA 2641471 A1	25/10/2007
		CN 101390196 A	18/03/2009
		CN 101390196 B	08/09/2010
		EP 1994553 A2	26/11/2008
		JP 2009-528183 A	06/08/2009
		JP 4824780 B2	30/11/2011
		KR 10-1313389 B1	01/10/2013
		KR 10-2008-0106909 A	09/12/2008
		US 7365387 B2	29/04/2008
		WO 2007-120988 A2	25/10/2007
		WO 2007-120988 A3	10/04/2008
WO 2007-019046 A1	15/02/2007	TW I440189 B	01/06/2014
		US 2007-0029601 A1	08/02/2007
		US 7446369 B2	04/11/2008
US 2014-0218436 A1	07/08/2014	CN 103828048 A	28/05/2014
		EP 2761656 A1	06/08/2014
		WO 2013-048376 A1	04/04/2013
US 2009-0067256 A1	12/03/2009	KR 10-2010-0051121 A	14/05/2010
		WO 2009-032606 A2	12/03/2009
		WO 2009-032606 A3	07/05/2009
US 2004-0191988 A1	30/09/2004	US 6750502 B1	15/06/2004
		US 6924186 B2	02/08/2005