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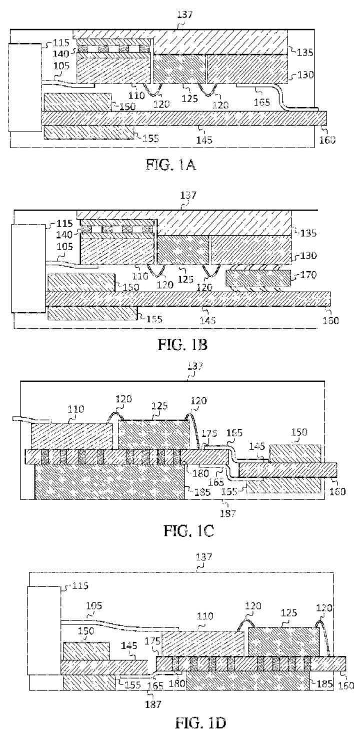

FIG. 1A

FIG. 1B

FIG. 1C

FIG. 1D

(57) Abstract: Optoelectronic module includes: a housing, a substantially planar subcarrier, a photonic integrated circuit, and an analog electronic integrated circuit. The subcarrier has a thermal conductivity greater than 10 W/m/K. The photonic integrated circuit and the analog electronic integrated circuit are secured to a first side of the subcarrier, and the subcarrier is secured to a first wall of the housing. A second side of the subcarrier, opposite the first side of the subcarrier, is parallel to, secured to, and in thermal contact with, an interior side of the first wall of the housing. Transceiver assembly includes an optical subassembly having inter alia a plurality of contact pads for establishing electrical connections to test equipment probes. The optical subassembly is separately testable by supplying power through the contact pads and sending data to and/or receiving data from the optical subassembly through the contact pads.

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MODULE WITH TRANSMIT OPTICAL SUBASSEMBLY AND RECEIVE OPTICAL SUBASSEMBLY

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] The present application claims priority to and the benefit of U.S. Provisional Application No. 62/539,929, filed August 1, 2017, entitled "OPTOELECTRONIC PLUGGABLE TRANSCEIVER MODULE WITH TRANSMIT OPTICAL SUBASSEMBLY AND RECEIVE OPTICAL SUBASSEMBLY", the entire content of which is incorporated herein by reference.

FIELD

[0002] One or more aspects of embodiments according to the present invention relate to optoelectronic modules.

BACKGROUND

[0003] Pluggable transceivers which include (i) one or more transmitters to convert electrical signals carrying data to optical signals carrying the same data and (ii) one or more receivers to convert optical signals to electrical signals may be used, for example, in switching systems. The design of a pluggable module may pose various challenges, including respecting space constraints, and keeping components in the module within acceptable temperature ranges.

SUMMARY

[0004] According to an embodiment of the present disclosure there is provided a transceiver assembly, including: a housing; and an optical subassembly, the optical subassembly including: a fiber, a photonic integrated circuit, an analog electronic integrated circuit, and a substantially planar subcarrier; the subcarrier having a thermal conductivity greater than 10 W/m/K; the photonic integrated circuit and the analog electronic integrated circuit being on the subcarrier; the fiber being coupled to the photonic integrated circuit; the subcarrier being parallel to, secured to, and in thermal contact with, a first wall of the housing; the photonic integrated circuit being connected to the analog electronic integrated circuit; and the optical subassembly having a plurality of contact pads for establishing electrical connections between the analog electronic integrated circuit and test equipment probes, the optical subassembly being configured to be separately testable by supplying power to the optical subassembly through one or more of the contact pads and sending data to and and/or receiving data from the optical subassembly through one or more of the contact pads.

1 **[0005]** In one embodiment, the analog electronic integrated circuit is adjacent to the photonic integrated circuit and connected to the photonic integrated circuit by a first plurality of wire bonds. In one embodiment, the wire bonds extend from wire bond pads along an edge of the analog electronic integrated circuit to wire bond
5 pads along an edge, of the photonic integrated circuit, nearest the analog electronic integrated circuit.

[0006] In one embodiment, the optical subassembly further includes a flexible printed circuit, connected to the analog electronic integrated circuit.

[0007] In one embodiment, the optical subassembly further includes a routing
10 board, and the analog electronic integrated circuit is connected to the flexible printed circuit through the routing board.

[0008] In one embodiment, the routing board is a printed circuit including an organic insulating material and conductive traces, the routing board is connected to the analog electronic integrated circuit, along an edge of the analog electronic
15 integrated circuit, by wire bonds.

[0009] In one embodiment, the flexible printed circuit is further connected to the host board.

[0010] According to an embodiment of the present disclosure there is provided a module, including: a housing; a substantially planar subcarrier; a photonic integrated
20 circuit; and an analog electronic integrated circuit, the subcarrier having a thermal conductivity greater than 10 W/m/K, the photonic integrated circuit and the analog electronic integrated circuit being secured to a first side of the subcarrier, the subcarrier being secured to a first wall of the housing, wherein a second side of the subcarrier, opposite the first side of the subcarrier, is parallel to, secured to, and in
25 thermal contact with, an interior side of the first wall of the housing.

[0011] In one embodiment, the photonic integrated circuit is adjacent to the analog electronic integrated circuit.

[0012] In one embodiment, the photonic integrated circuit is connected to the analog electronic integrated circuit by wire bonds.

30 **[0013]** In one embodiment, the wire bonds extend from wire bond pads along an edge of the analog electronic integrated circuit to wire bond pads along an edge, of the photonic integrated circuit, nearest the analog electronic integrated circuit.

[0014] In one embodiment, the module further includes an optical subassembly including: the subcarrier; the photonic integrated circuit; and the analog electronic
35 integrated circuit, the optical subassembly having a plurality of contact pads for establishing electrical connections between the analog electronic integrated circuit and test equipment probes, the optical subassembly being configured to be separately testable by supplying power to the optical subassembly through one or

1 more of the contact pads and sending data to and and/or receiving data from the optical subassembly through one or more of the contact pads.

[0015] In one embodiment, the optical subassembly further includes a flexible printed circuit, connected to the analog electronic integrated circuit

5 **[0016]** In one embodiment, the optical subassembly further includes a routing board connected to the analog electronic integrated circuit, along an edge of the analog electronic integrated circuit, by wire bonds; the analog electronic integrated circuit is connected to the flexible printed circuit through the routing board; and the routing board is a printed circuit including an organic insulating material and
10 conductive traces.

[0017] In one embodiment, the flexible printed circuit is connected to the routing board by solder.

[0018] In one embodiment, the module further includes a host board including a microcontroller and/or a DC-DC converter, the host board being connected to the
15 routing board through the flexible printed circuit.

[0019] According to an embodiment of the present disclosure there is provided method for manufacturing a module, the method including: assembling an optical subassembly including: a fiber, a photonic integrated circuit, an analog electronic integrated circuit, and a substantially planar subcarrier, the photonic integrated circuit
20 and the analog electronic integrated circuit being on the subcarrier; testing the optical subassembly; determining that the testing of the optical subassembly was successful; and in response to determining that the testing of the testing the optical subassembly was successful, installing the optical subassembly in a housing, with the subcarrier being parallel to, secured to, and in thermal contact with, a first wall of
25 the housing.

[0020] In one embodiment, the optical subassembly has a plurality of contact pads for establishing electrical connections between the analog electronic integrated circuit and test equipment probes; and the testing of the optical subassembly includes: transmitting modulated light into the photonic integrated circuit through the
30 fiber, and verifying the presence, at the contact pads, of electrical signals corresponding to the modulation; or the testing of the optical subassembly includes: applying electrical signals to the contact pads, and verifying the presence, in light transmitted through the fiber from the photonic integrated circuit, of modulation corresponding to the electrical signals.

35 **[0021]** In one embodiment, the method further includes: in response to determining that the testing of the testing the optical subassembly was successful, connecting a host board including a microcontroller and/or a DC-DC converter to the optical subassembly.

1 **[0022]** In one embodiment, the connecting of the host board to the optical subassembly includes soldering the host board to the optical subassembly.

BRIEF DESCRIPTION OF THE DRAWINGS

5 **[0023]** These and other features and advantages of the present disclosure will be appreciated and understood with reference to the specification, claims, and appended drawings wherein:

[0024] FIG. 1A is a schematic cross-sectional view of an optoelectronic module, according to an embodiment of the present disclosure;

10 **[0025]** FIG. 1B is a schematic cross-sectional view of an optoelectronic module, according to an embodiment of the present disclosure;

[0026] FIG. 1C is a schematic cross-sectional view of an optoelectronic module, according to an embodiment of the present disclosure;

[0027] FIG. 1D is a schematic cross-sectional view of an optoelectronic module, 15 according to an embodiment of the present disclosure;

[0028] FIG. 2 is a bottom view of a portion of an optoelectronic module, according to an embodiment of the present disclosure;

[0029] FIG. 3 is a bottom view of a portion of an optoelectronic module, according to an embodiment of the present disclosure;

20 **[0030]** FIG. 4 is an assembly sequence diagram, according to an embodiment of the present disclosure;

[0031] FIG. 5 is an assembly sequence diagram, according to an embodiment of the present disclosure;

[0032] FIG. 6 is an assembly sequence diagram, according to an embodiment of 25 the present disclosure;

[0033] FIG. 7A is a view of a host board, according to an embodiment of the present disclosure;

[0034] FIG. 7B is a view of testable optical subassembly, according to an embodiment of the present disclosure;

30 **[0035]** FIG. 7C is a view of a portion of an optoelectronic module, according to an embodiment of the present disclosure;

[0036] FIG. 8A is a top view of a housing, according to an embodiment of the present disclosure;

[0037] FIG. 8B is a top view of a portion of an optoelectronic module, according to 35 an embodiment of the present disclosure;

[0038] FIG. 9A is a top view of a portion of an optoelectronic module, according to an embodiment of the present disclosure;

1 **[0039]** FIG. 9B is a top view of an optoelectronic module, according to an embodiment of the present disclosure;

[0040] FIG. 10A is a top view of a portion of an optoelectronic module, according to an embodiment of the present disclosure;

5 **[0041]** FIG. 10B is a cross-sectional view, along section line 10B-10B of FIG. 10A, of a portion of an optoelectronic module, according to an embodiment of the present disclosure;

[0042] FIG. 11A is a schematic cross-sectional view of an optoelectronic module, according to an embodiment of the present disclosure;

10 **[0043]** FIG. 11B is a schematic cross-sectional view of an optoelectronic module, according to an embodiment of the present disclosure;

[0044] FIG. 11C is a schematic cross-sectional view of an optoelectronic module, according to an embodiment of the present disclosure;

[0045] FIG. 12A is a schematic cross-sectional view of an optoelectronic module, 15 according to an embodiment of the present disclosure;

[0046] FIG. 12B is a schematic top view of a portion of an optoelectronic module, according to an embodiment of the present disclosure; and

[0047] FIG. 12C is a cross-sectional view, along section line 12C-12C of FIG. 12B, of an optoelectronic module, according to an embodiment of the present 20 disclosure.

DETAILED DESCRIPTION

[0048] The detailed description set forth below in connection with the appended drawings is intended as a description of exemplary embodiments of a module with 25 transmit optical subassembly and receive optical subassembly provided in accordance with the present disclosure and is not intended to represent the only forms in which the present disclosure may be constructed or utilized. The description sets forth the features of the present disclosure in connection with the illustrated embodiments. It is to be understood, however, that the same or equivalent functions 30 and structures may be accomplished by different embodiments that are also intended to be encompassed within the scope of the disclosure. As denoted elsewhere herein, like element numbers are intended to indicate like elements or features.

[0049] FIGs. 1A-1D show schematic cross-sectional views of several 35 embodiments each including a transceiver in a quad small form factor pluggable (QSFP) package. Referring to FIGs. 1A and 1B, in some embodiments an optical fiber 105 connects a photonic integrated circuit (PIC) 110 to a Multi-fiber Push On (MPO) connector 115. The PIC 110 is connected by one or more wire bonds 120 to

1 an analog electronic integrated circuit, e.g., an analog application specific integrated circuit (aASIC) 125, which is connected by one or more wire bonds 120 to a routing board 130, which may be a printed circuit board on an organic substrate (e.g., a polymer or fiberglass-reinforced polymer substrate). The PIC 110 may be one of a 5 plurality of PICs 110 (e.g., the module may include both a transmitter PIC and a receiver PIC), and the aASIC 125 may be one of a plurality of aASICs 125 (there being, for example, one aASIC 125 for each PIC 110). The aASIC 125 and the PIC may be bare die. For example, the aASIC 125 may be a bare silicon die, and the PIC 110 may be a bare silicon die (which, in the case of a transmitter PIC, may 10 include a bare laser die (e.g., a bare die of another semiconductor, different from silicon) mounted on a bare silicon die (as discussed in further detail below)). The routing board 130 may be fabricated using a process capable of forming fine pitch features, e.g., traces and wire bond pads on a pitch of 100 microns. The PIC 110, aASIC 125, and routing board 130 may be secured to (e.g., bonded to), and 15 supported by, a subcarrier 135, which may be a block, or a block with a stepped thickness as shown, formed of a thermally conductive material (e.g., a material having a thermal conductivity exceeding 10 W/m/K), e.g., copper. The subcarrier may be substantially planar, i.e., it may have the shape of a sheet having different thicknesses in different regions of the sheet, e.g., having a greater thickness in the 20 region to which the aASIC 125 is secured than in the region to which the PIC 110 and a TEC 140 (discussed in further detail below) are secured. In a system using a QSFP package, thermal control of the top package wall 137 may be provided (e.g., the system may be designed – e.g., with a heat sink – to ensure that the temperature of the top package wall not exceed a specified value). As such, in the embodiments 25 of FIGs. 1A and 1B, heat may be conducted out of the package through the subcarrier 135 and through the top package wall 137.

[0050] The PIC 110 may be secured to a thermoelectric cooler (TEC) 140 which may be secured to the subcarrier 135, as shown. In some embodiments, a host board 145, which may be an organic printed circuit board, has installed on it a 30 microcontroller 150 and a DC-DC converter 155, and it has a card-edge connector 160 at the electrical end of the QSFP package. The routing board may be connected to the host board by a flexible circuit or “flex circuit” 165 (FIG. 1A) or by a low profile connector array 170 (or “socket”) (e.g., a Z-RAY^{TM} ultra-low profile array available from Samtec (samtec.com)) (FIG. 1B). Because the conductors may spread out on 35 the routing board 130 and/or on the flex circuit 165, the host board is, in some embodiments, fabricated using a lower-cost process not capable of forming fine pitch features. A similar configuration may be used regardless of whether the PIC 110 and the aASIC 125 form a transmitter (transmitting light through the fiber) or a receiver

1 (receiving light through the fiber). In the case of a transmitter, the PIC may include a modulator, and a laser (e.g., a separate laser chip) may be mounted on the PIC, and optically coupled to it, and the aASIC may include a drive circuit for the modulator. In the case of a receiver, the PIC may include a photodetector, and the aASIC may
5 include a transimpedance amplifier to amplify the signal from the photodetector. Each PIC 110 may include an array of modulators or photodetectors, and each aASIC 125 may include a corresponding array of drive circuits or transimpedance amplifiers.

[0051] Each PIC 110 may include a waveguide having transverse dimensions of
10 approximately 10 microns at a point at which light couples into the waveguide from the fiber 105, or from the fiber 105 into the waveguide. A mode adapter, e.g., a taper, may guide the light and transform the optical mode to one that propagates in a waveguide having transverse dimensions of approximately 3 microns. The 3 micron waveguide may be used to guide the light to a photodetector, or from a modulator.
15 Further mode adapters (e.g., at a modulator) may be used to effect further changes in the size or shape of the optical mode, e.g., to enable light to propagate through a modulator fabricated on a waveguide with smaller transverse dimension (for improved modulator performance). In some embodiments similar to that of FIG. 1A, the routing board 130 is omitted and the aASIC 125 is connected directly to the flex
20 circuit 165, which is bonded directly to the subcarrier 135. In such an embodiment, longer wire bonds may be used to accommodate the difference in height between the surface of the aASIC 125 and the surface of the flex circuit (which may be significantly thinner than the aASIC 125), or the difference in height may be reduced by thinning the aASIC die, or by using a subcarrier 135 with a stepped thickness
25 (i.e., a subcarrier 135 having a greater thickness under the flex circuit 165 than under the aASIC 125). The flex circuit 165 may be a printed circuit composed of one or more layers of conductive traces and one or more flexible insulating layers. The flexible insulating layers may be composed of a film of plastic (e.g., a film of polyimide) capable of withstanding soldering temperatures, and the flex circuit 165
30 may be connected to the routing board 130 and to the host board 145 by soldering.

[0052] In some embodiments the TEC 140 is absent and the PIC 110 is bonded directly to the subcarrier, or is bonded to an insulating layer bonded to the subcarrier. In some embodiments, a heater is secured to or integrated into the PIC 110 and the temperature of the PIC 110 is actively controlled, based on a signal from a
35 temperature sensor on or integrated into the PIC 110. In such an embodiment, the insulating layer may enable the heater to raise the temperature of the PIC 110 without consuming an excessive amount of power.

1 **[0053]** FIG. 1C shows an embodiment in which the MPO connector 115 is absent and the fiber 105 extends directly from the PIC 110 to the exterior of the package. Such a configuration may be referred to as an active optical cable (AOC) configuration. FIG. 1D shows a related embodiment in which the PIC 110 is more
5 distant from the front end (or "optical end") of the package, facilitating the inclusion of an MPO connector 115. In FIGs. 1C and 1D, the PIC 110 and the aASIC 125 may be bonded to a substrate 175, which may be a printed circuit board including one or more layers containing conductive traces and one or more organic insulating layers (e.g., polymer or fiberglass-reinforced polymer insulating layers), with thermal vias
10 180 for forming a thermal path between (i) the PIC 110 and the aASIC 125 and (ii) a thermal block 185 which supports the substrate 175 and provides a thermal path between the substrate and the bottom wall (or "lower wall") 187 of the package enclosure. In some systems using QSFP packages the lower wall 187 of the package is not directly connected to the heat sink; accordingly, in the embodiments
15 of FIGs. 1C and 1D the side walls of the package may be used to conduct heat to the top package wall. Wire bonds 120 may be used to connect the PIC 110 to the aASIC 125 and to connect the aASIC 125 to the substrate 175. The substrate 175 may be fabricated using a process capable of forming fine pitch features, e.g., traces and wire bond pads on a pitch of 100 microns.
20 **[0054]** A dual flex circuit (i.e., two parallel flex circuits 165), is used in the embodiment of FIG. 1C to connect the substrate 175 to a host board 145 which has a card-edge connector 160 at the electrical end of the QSFP package, and which has installed on it a microcontroller 150 and a DC-DC converter 155. In the embodiment of FIG. 1D the card-edge connector 160 at the electrical end of the
25 QSFP package is on the substrate 175, and a separate host board 145 has installed on it a microcontroller 150 and a DC-DC converter 155 and is connected to the substrate 175 by a flex circuit 165.
[0055] FIG. 2 shows a bottom view of the embodiment of FIGs. 1A and 1B, in one embodiment, and FIG. 3 shows a bottom view of the embodiment of FIGs. 1A and
30 1B, in another embodiment. The routing board extends around the aASICs 125 and the PICs 110 so that wire bonds (not shown), for delivering power or control signals to these components (or for providing laser drive current to the laser on the transmitter PIC) may be formed along the side edges of these components. The host board 145 and flex circuit 165 are not shown in FIGs. 2 and 3. Wire bonds for data
35 connections (shown in FIGs. 1A and 1B, and, for the data connections between the aASICs and the PICs, in FIGs. 2 and 3) may be present along the end edges of the aASICs and the PICs.

1 **[0056]** FIGs. 4-9 show an assembly sequence for the embodiment of FIGs. 1A and 1B. Referring to FIG. 4, each fiber 105 (of the fibers of a fiber ribbon 405, the other end of which is terminated in an MPO connector 115 (FIG. 7B; not shown in FIGs. 4-6) is aligned in a respective V-groove (e.g., of an array of V-grooves) on the
5 PIC 110 and secured in place to form a “PICtail” 410. The PICtails 410 are secured to the subcarrier (or “carrier”) 135 along with the aASICs 125, either directly, to form a first subassembly 415, or (in the alternate sequence shown by dashed arrows) the PICs 110 may be bonded to a TEC 140 which may be bonded to the subcarrier 135. Referring to FIG. 5, a rigid-flex circuit 505 (the combination of the routing board 130
10 and the flex-circuit 165, which may be separately assembled) is then bonded to the first subassembly 415 of FIG. 4 to form a testable transmit-receive optical subassembly (TROSA) 510 (including the fiber-coupled PICs 110 and the aASICs 125), with pads 515 suitable for making contact with test equipment probes, that may provide power to the TROSA and send or receive data through it. The testable
15 TROSA 510 thus makes it possible to identify and discard a defective optical subassembly without discarding with it, e.g., a host board having installed on it a microcontroller and a DC-DC converter.

[0057] Referring to FIG. 6, a cover 610 may then be secured to the TROSA (e.g., to protect it during further handling before the package is assembled). The TROSA
20 510 may be tested (by supplying modulated light to the receivers and verifying that suitable corresponding electrical signals are produced at the pads 515, and by supplying electrical signals to the pads 515, and verifying that suitably modulated light is produced by the transmitters) either before or after installation of the cover 610. If the test is successful, assembly of the module may proceed; if it is
25 unsuccessful, the TROSA 510 may be discarded or reworked.

[0058] Referring to FIGs. 7A-7C, the flex circuit of the TROSA 510 is then soldered to the host board 145. FIG. 7C shows the TROSA 510 soldered to the host board 145, with the subcarrier 135 facing up and the cover 610 facing the host board 145. Semicircular cutouts 710 (not shown in the preceding drawings) may be used to
30 register the TROSA 510 and the host board 145 to the module housing.

[0059] The resulting subassembly may then be installed in a QSFP package housing. FIG. 8A shows the cast housing 805 with registration features 810 for engaging the semicircular cutouts 710 of the TROSA 510 and of the host board 145. FIG. 8B shows the TROSA 510 and the host board 145 installed in the housing 805.
35 A thermal pad 905 may be placed on the subcarrier (FIG. 9A) and a lid may be installed on the QSFP package housing, to complete the assembly (FIG. 9B). FIG. 10A shows a top view of the assembly with the lid removed and FIG. 10B shows a cross-sectional view, along section line 10B-10B of FIG. 10A, of the assembly.

[0060] FIGs. 11A-11C show embodiments in which the PIC 110 and the aASIC 125 are secured, directly or indirectly, to a subcarrier to form a testable TROSA including the fiber 105, the MPO connector 115, the PIC 110, the aASIC 125, the TEC 140 (if present), and the subcarrier 135. After testing, the TROSA is installed into a cutout in the host board 145 and the aASIC 125 is wire bonded to the host board 145. In FIGs. 11A-11C, the module is shown in an orientation in which the wall of the module to which a heat sink is directly connected, in operation, is the lower wall. In the embodiment of FIG. 11C, a printed circuit board with thermal vias 1110 supports the PIC 110 and the aASIC 125 and is in turn supported by the subcarrier 135. Wire bonds from the PIC 110 to the printed circuit board with thermal vias 1110 and from the host board 145 to the printed circuit board with thermal vias 1110 provide (along with traces on the printed circuit board with thermal vias 1110) low speed connections such as power and control connections. In the embodiments of FIGs. 11A and 11B, testing may be accomplished by probing pads on the aASIC 125. In the embodiment of FIG. 11C, pads on the printed circuit board with thermal vias 1110 may instead be probed; this may facilitate testing, as the pads on the substrate may be larger and may have a coarser pitch than pads on the aASIC aASIC in the embodiments of FIGs. 11A and 11B. In the embodiment of FIG. 11C, a pedestal 1115 (e.g., a cast pedestal that is an integral part of the module housing) supports the thermal pad 905 which supports the subcarrier 135.

[0061] FIGs. 12A-12C show another embodiment of a transceiver module. In this embodiment a coined, “top-drop” subcarrier 135 (which may be a copper subcarrier) supports the PICs 110 and the aASICs 125 as shown. After the TROSA is tested, the subcarrier 135 is installed in (e.g., “dropped into”) a cutout (e.g., a rectangular cutout) in the host board 145 and the aASIC 125 is connected to the host board 145 by wire bonds. An electrical routing board 1210 is connected to the host board 145, to the PICs 110 and to the aASICs 125 by wire bonds, and provides low speed connections to the PICs 110 and to the aASICs 125.

[0062] Although exemplary embodiments of a module with transmit optical subassembly and receive optical subassembly have been specifically described and illustrated herein, many modifications and variations will be apparent to those skilled in the art. Accordingly, it is to be understood that a module with transmit optical subassembly and receive optical subassembly constructed according to principles of this disclosure may be embodied other than as specifically described herein. The invention is also defined in the following claims, and equivalents thereof.

1 **WHAT IS CLAIMED IS:**

1. A transceiver assembly, comprising:
a housing; and
an optical subassembly,
5 the optical subassembly comprising:
a fiber,
a photonic integrated circuit,
an analog electronic integrated circuit, and
a substantially planar subcarrier;
10 the subcarrier having a thermal conductivity greater than 10 W/m/K;
the photonic integrated circuit and the analog electronic integrated circuit being on the subcarrier;
the fiber being coupled to the photonic integrated circuit;
the subcarrier being parallel to, secured to, and in thermal contact with, a first
15 wall of the housing;
the photonic integrated circuit being connected to the analog electronic integrated circuit; and
the optical subassembly having a plurality of contact pads for establishing electrical connections between the analog electronic integrated circuit and test
20 equipment probes, the optical subassembly being configured to be separately testable by supplying power to the optical subassembly through one or more of the contact pads and sending data to and and/or receiving data from the optical subassembly through one or more of the contact pads.

25 2. The transceiver assembly of claim 1, wherein the analog electronic integrated circuit is adjacent to the photonic integrated circuit and connected to the photonic integrated circuit by a first plurality of wire bonds.

3. The transceiver assembly of claim 2, wherein the wire bonds extend
30 from wire bond pads along an edge of the analog electronic integrated circuit to wire bond pads along an edge, of the photonic integrated circuit, nearest the analog electronic integrated circuit.

4. The transceiver assembly of claim 3, wherein the optical subassembly
35 further comprises a flexible printed circuit, connected to the analog electronic integrated circuit.

5. The transceiver assembly of claim 4, wherein:

1 the optical subassembly further comprises a routing board, and
the analog electronic integrated circuit is connected to the flexible printed circuit through the routing board.

5 6. The transceiver assembly of claim 5, wherein:
the routing board is a printed circuit comprising an organic insulating material and conductive traces,
the routing board is connected to the analog electronic integrated circuit, along an edge of the analog electronic integrated circuit, by wire bonds.

10

7. The transceiver assembly of claim 6, wherein the flexible printed circuit is further connected to the host board.

8. A module, comprising:
15 a housing;
a substantially planar subcarrier;
a photonic integrated circuit; and
an analog electronic integrated circuit,
the subcarrier having a thermal conductivity greater than 10 W/m/K,
20 the photonic integrated circuit and the analog electronic integrated circuit being secured to a first side of the subcarrier,
the subcarrier being secured to a first wall of the housing,
wherein a second side of the subcarrier, opposite the first side of the subcarrier, is parallel to, secured to, and in thermal contact with, an interior side of
25 the first wall of the housing.

9. The module of claim 8, wherein the photonic integrated circuit is adjacent to the analog electronic integrated circuit.

30 10. The module of claim 9, wherein the photonic integrated circuit is connected to the analog electronic integrated circuit by wire bonds.

11. The module of claim 10, wherein the wire bonds extend from wire bond pads along an edge of the analog electronic integrated circuit to wire bond
35 pads along an edge, of the photonic integrated circuit, nearest the analog electronic integrated circuit.

1 12. The module of claim 11, further comprising an optical subassembly comprising:

the subcarrier;

the photonic integrated circuit; and

5 the analog electronic integrated circuit,

the optical subassembly having a plurality of contact pads for establishing electrical connections between the analog electronic integrated circuit and test equipment probes, the optical subassembly being configured to be separately testable by supplying power to the optical subassembly through one or more of the 10 contact pads and sending data to and and/or receiving data from the optical subassembly through one or more of the contact pads.

13. The module of claim 12, wherein the optical subassembly further comprises a flexible printed circuit, connected to the analog electronic integrated 15 circuit.

14. The transceiver assembly of claim 4, wherein:

the optical subassembly further comprises a routing board connected to the analog electronic integrated circuit, along an edge of the analog electronic integrated 20 circuit, by wire bonds;

the analog electronic integrated circuit is connected to the flexible printed circuit through the routing board; and

the routing board is a printed circuit comprising an organic insulating material and conductive traces.

25

15. The module of claim 14, wherein the flexible printed circuit is connected to the routing board by solder.

16. The module of claim 15, further comprising a host board comprising a 30 microcontroller and/or a DC-DC converter, the host board being connected to the routing board through the flexible printed circuit.

17. A method for manufacturing a module, the method comprising:

assembling an optical subassembly comprising:

35 a fiber,

a photonic integrated circuit,

an analog electronic integrated circuit, and

a substantially planar subcarrier,

1 the photonic integrated circuit and the analog electronic integrated circuit being on the subcarrier;

testing the optical subassembly;

determining that the testing of the optical subassembly was successful; and

5 in response to determining that the testing of the testing the optical subassembly was successful, installing the optical subassembly in a housing, with the subcarrier being parallel to, secured to, and in thermal contact with, a first wall of the housing.

10 18. The method of claim 17, wherein:

the optical subassembly has a plurality of contact pads for establishing electrical connections between the analog electronic integrated circuit and test equipment probes; and

the testing of the optical subassembly comprises:

15 transmitting modulated light into the photonic integrated circuit through the fiber, and

verifying the presence, at the contact pads, of electrical signals corresponding to the modulation; or

the testing of the optical subassembly comprises:

20 applying electrical signals to the contact pads, and

verifying the presence, in light transmitted through the fiber from the photonic integrated circuit, of modulation corresponding to the electrical signals.

19. The method of claim 18, further comprising:

25 in response to determining that the testing of the testing the optical subassembly was successful, connecting a host board comprising a microcontroller and/or a DC-DC converter to the optical subassembly.

20. The method of claim 19, wherein the connecting of the host board to

30 the optical subassembly comprises soldering the host board to the optical subassembly.

35

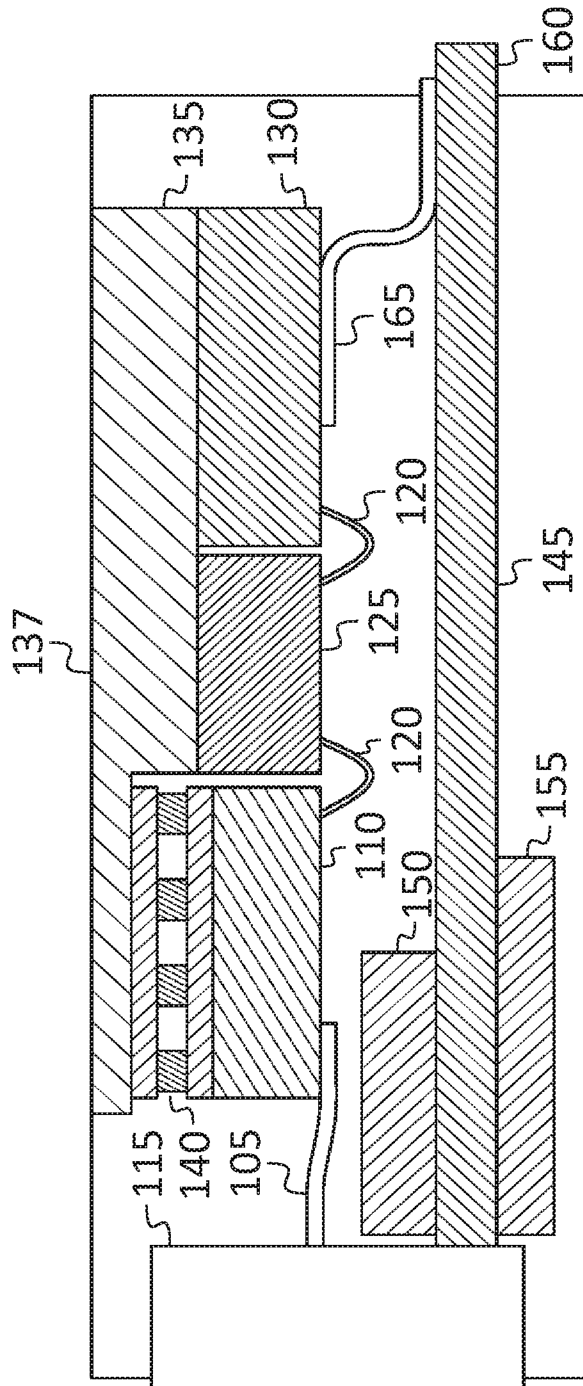

FIG. 1A

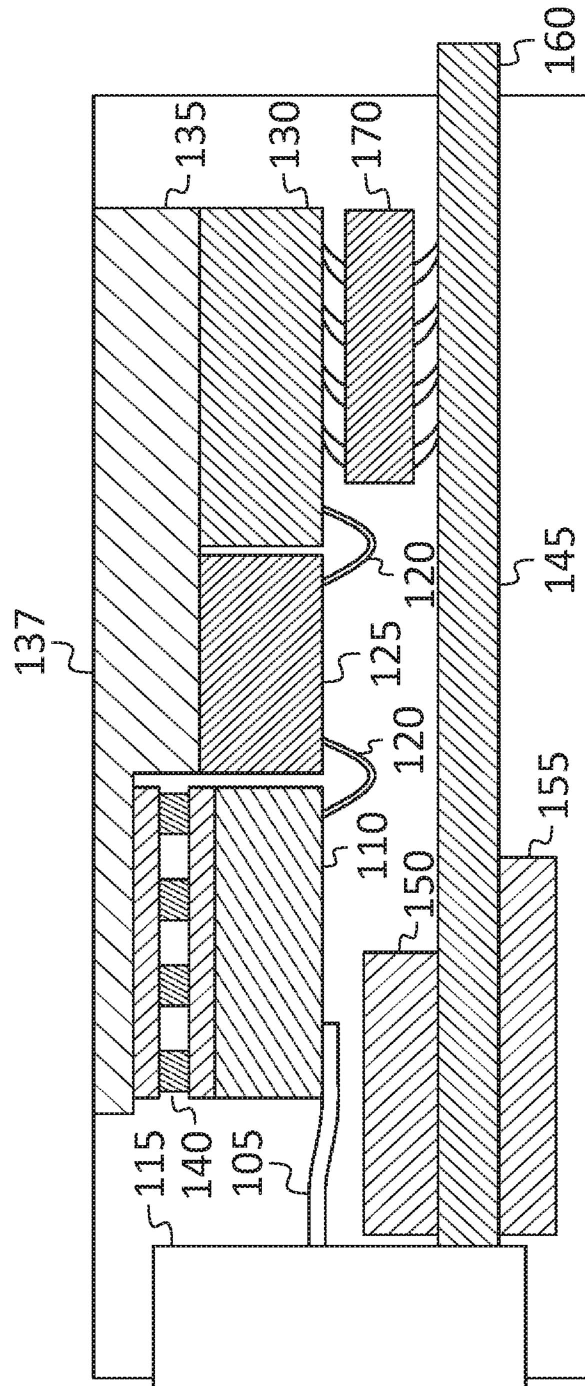

FIG. 1B

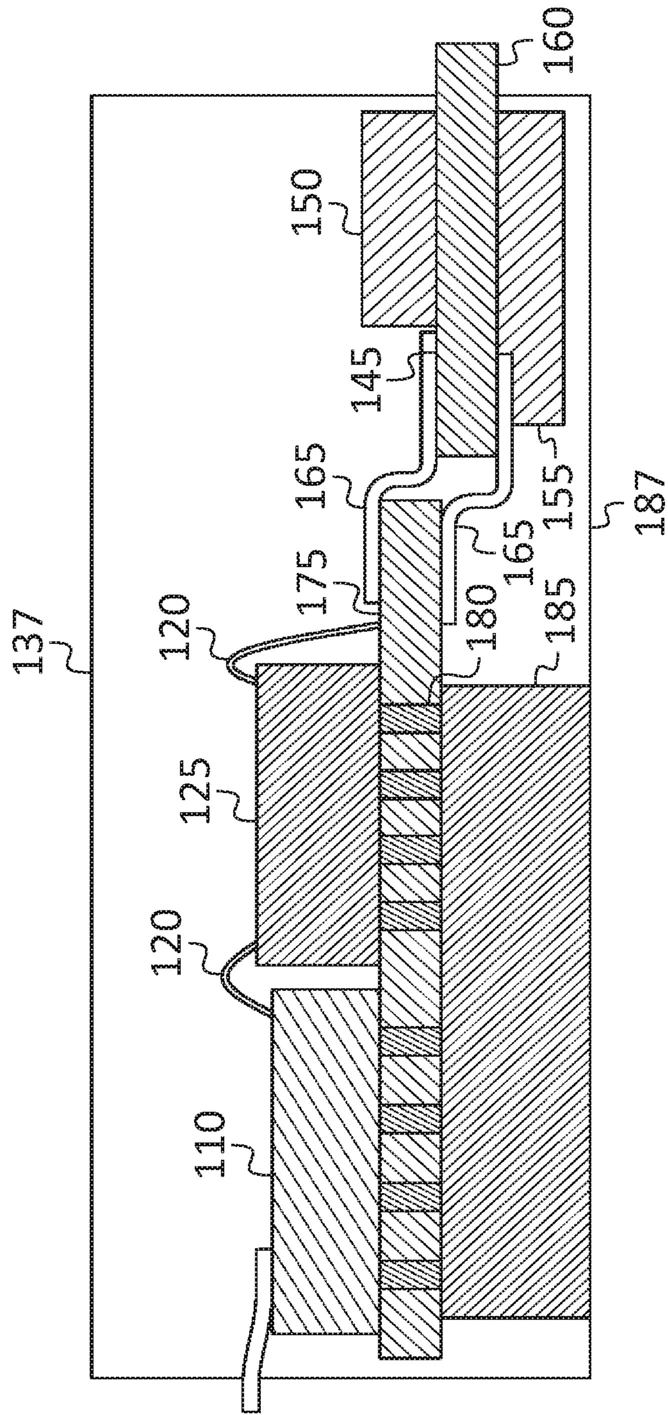

FIG. 1C

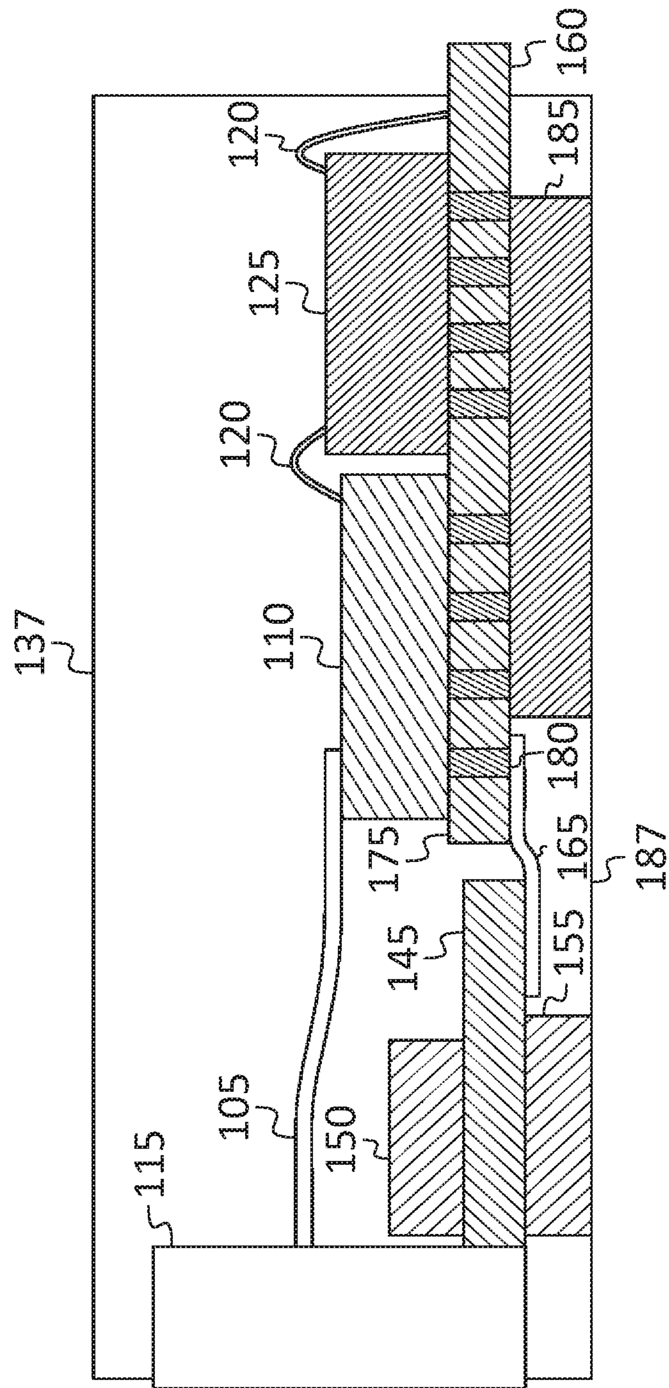

FIG. 1D

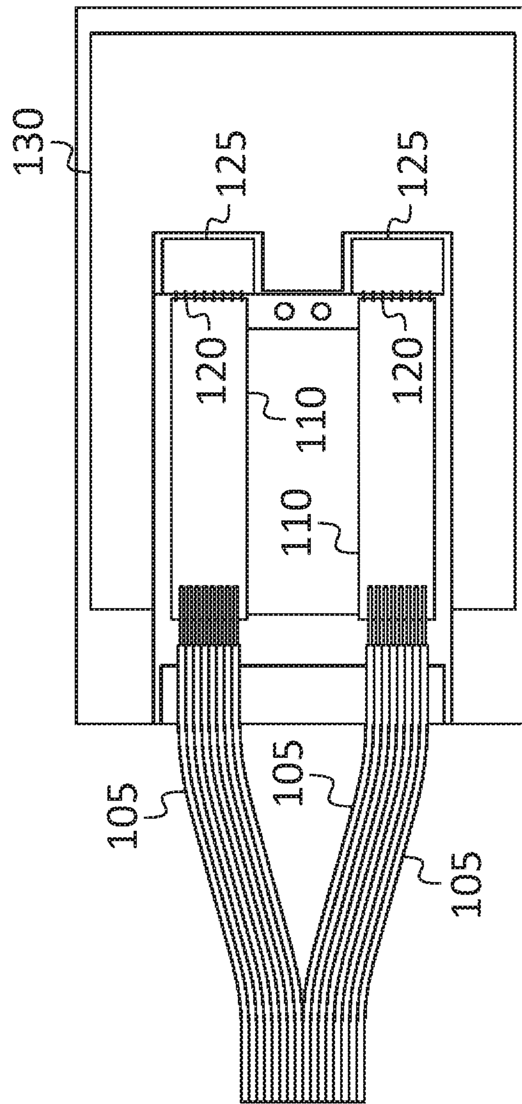

FIG. 2

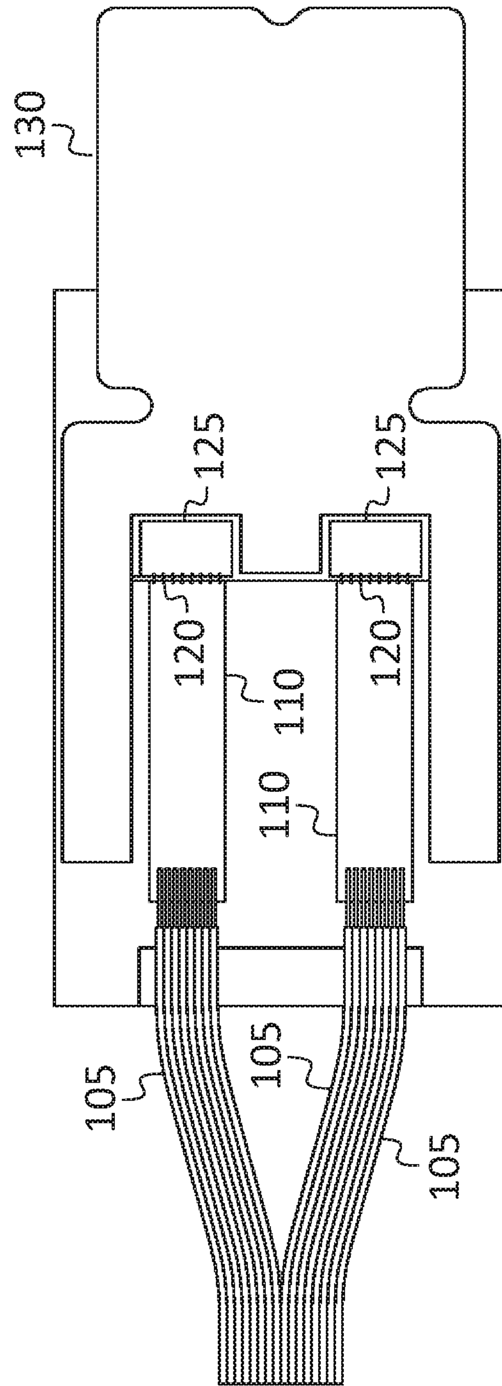

FIG. 3

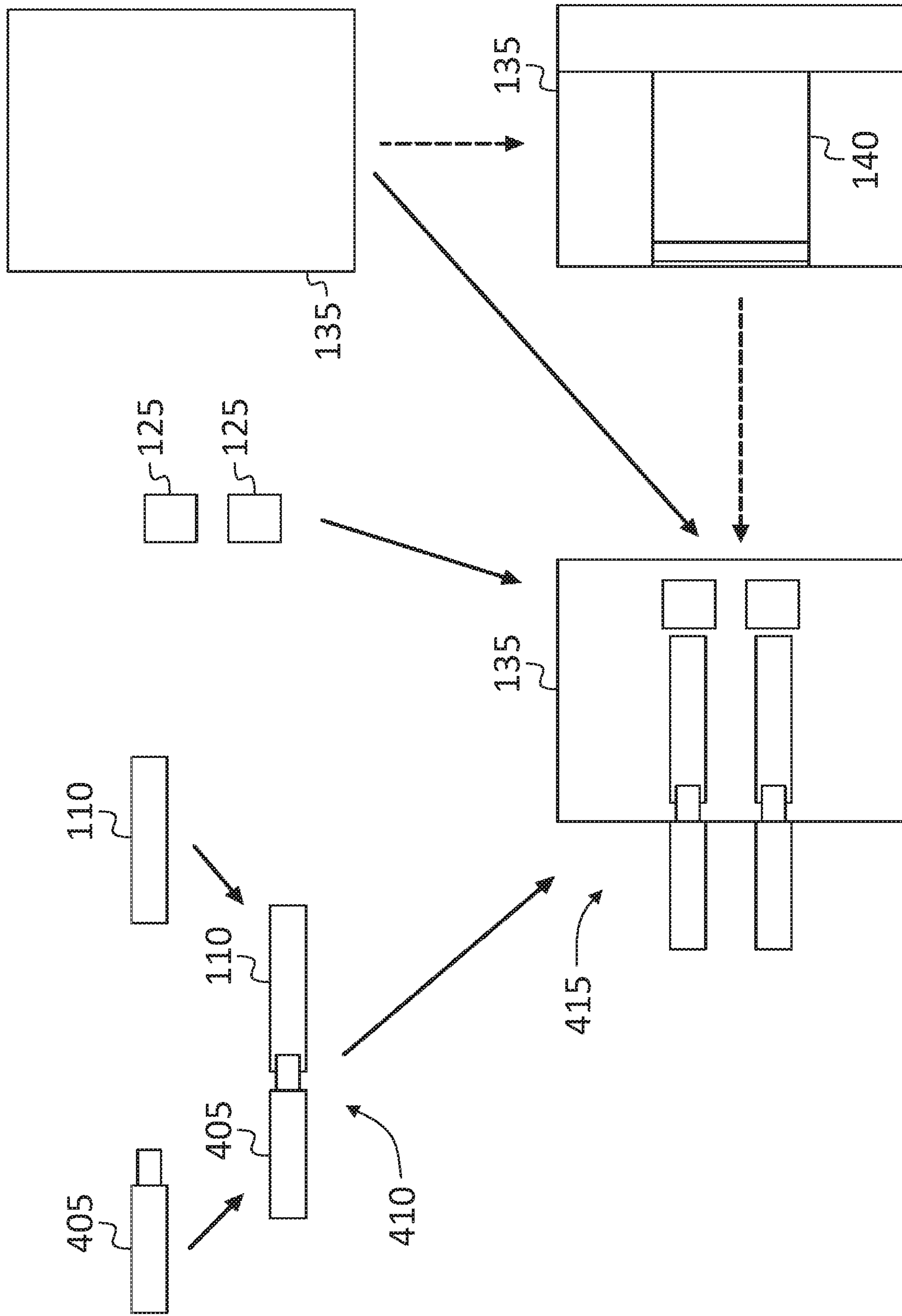

FIG. 4

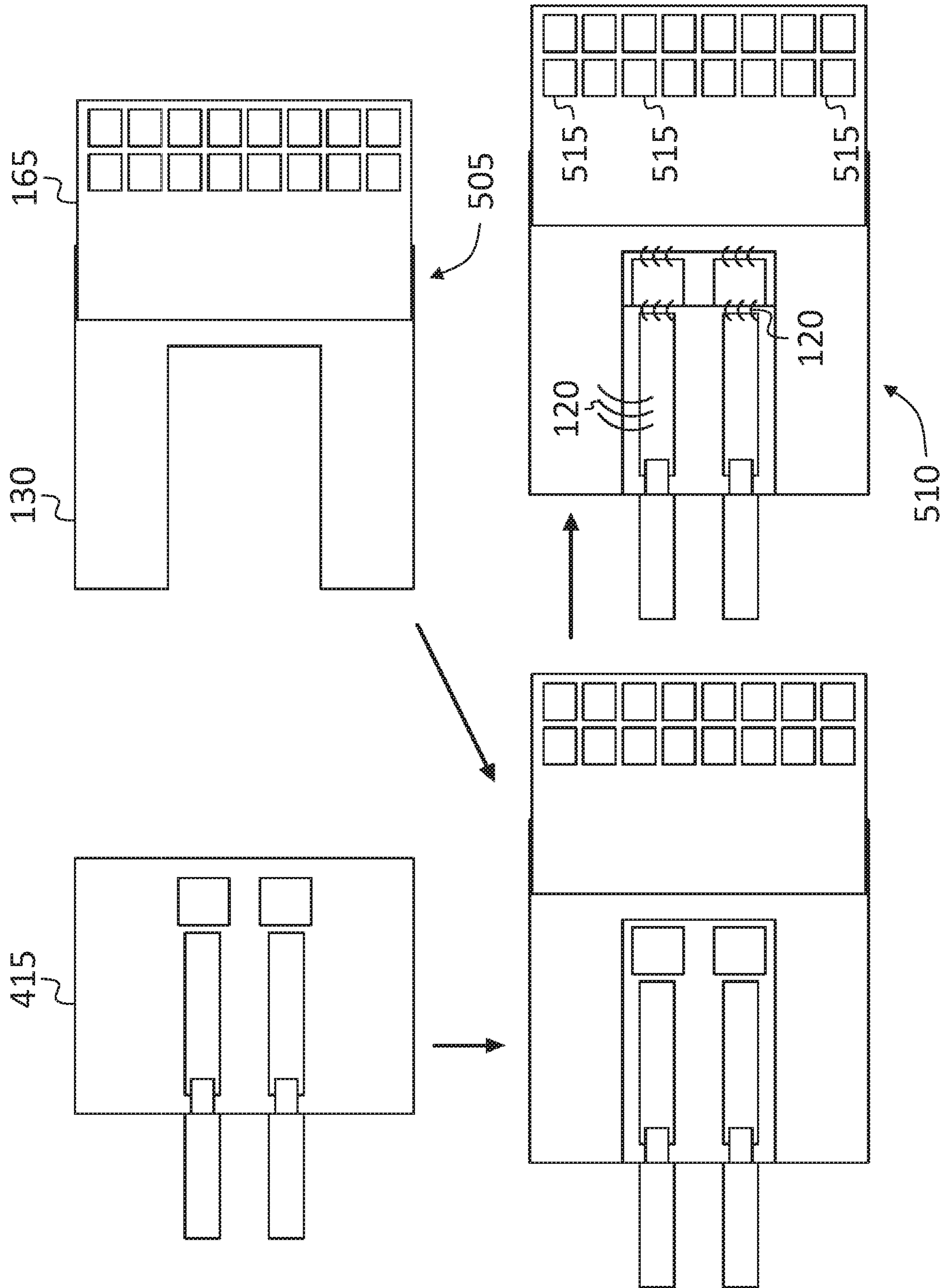

FIG. 5

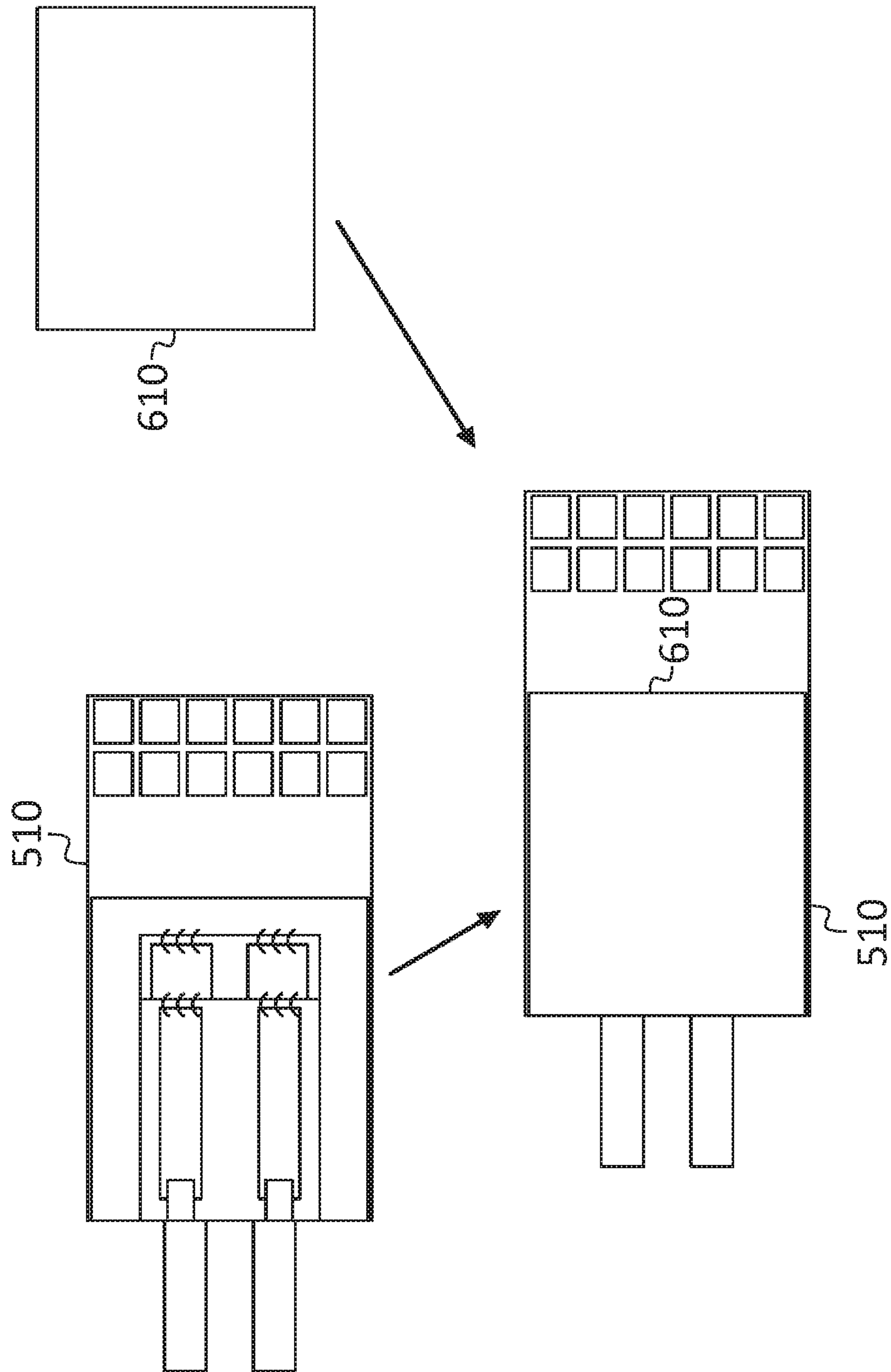

FIG. 6

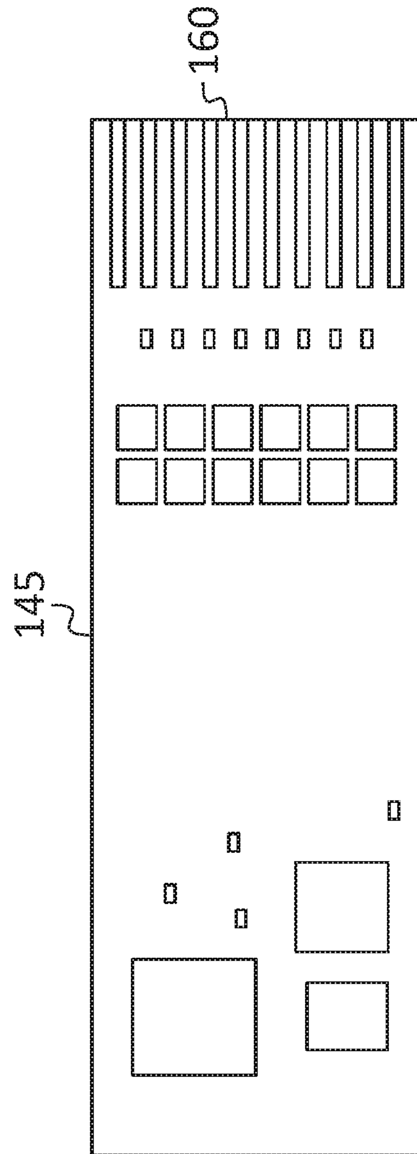

FIG. 7A

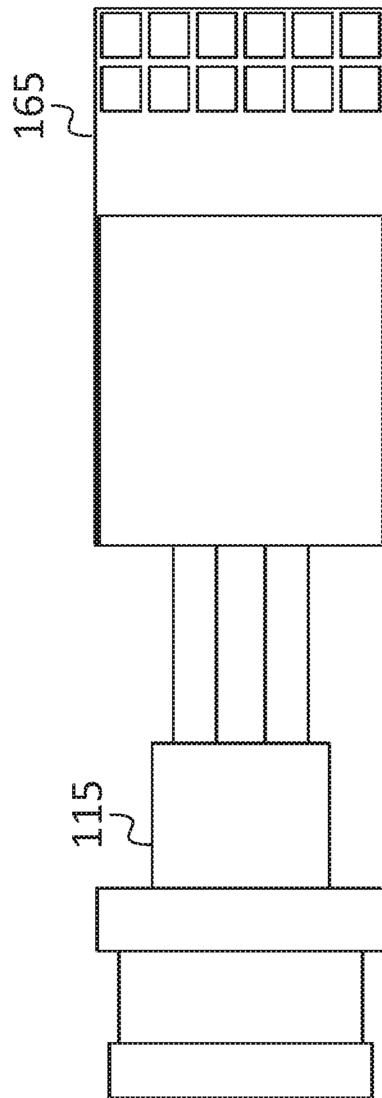

FIG. 7B

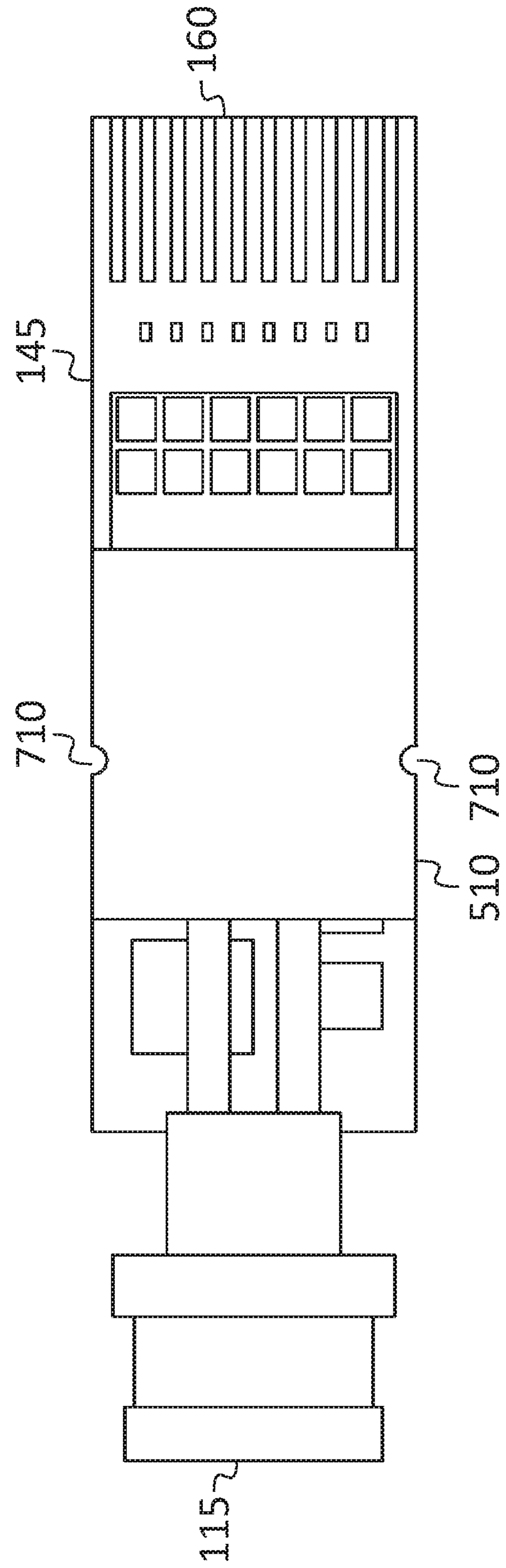

FIG. 7C

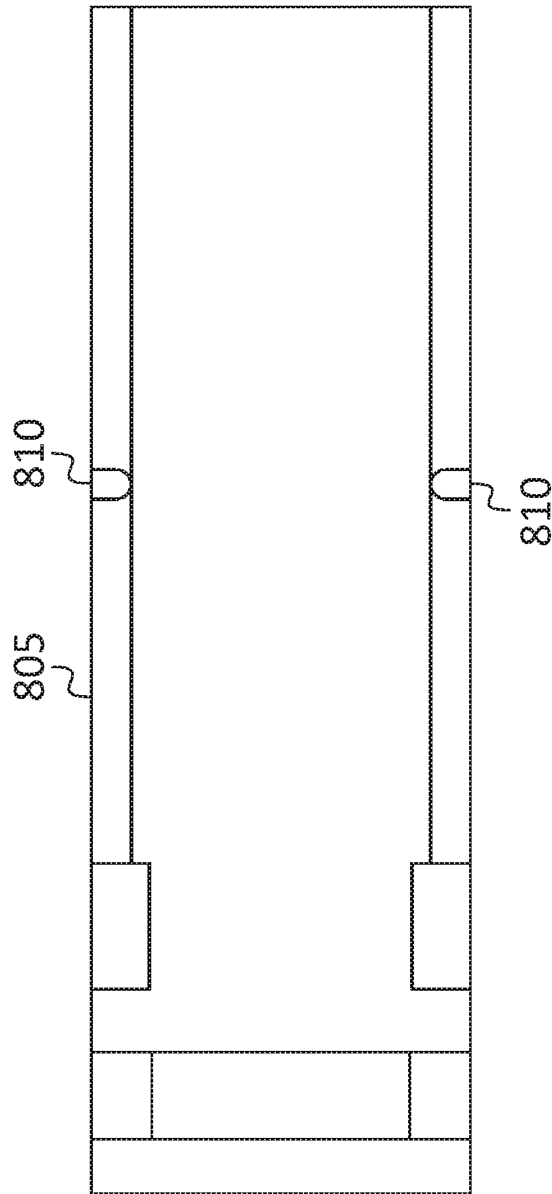

FIG. 8A

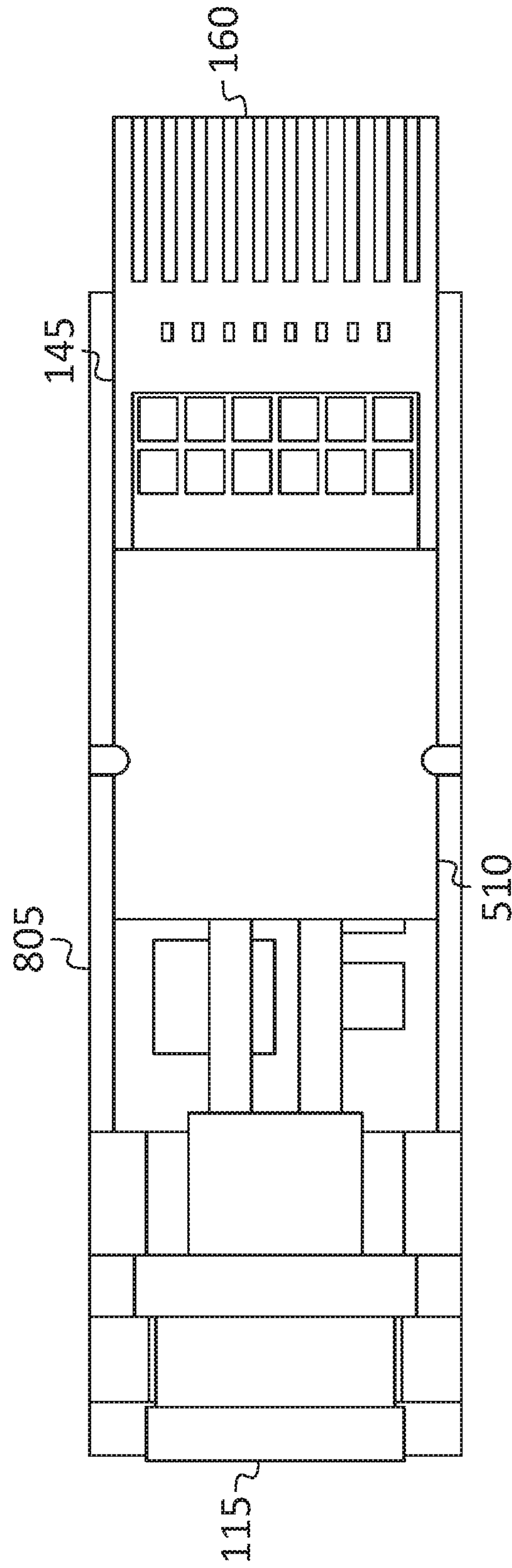

FIG. 8B

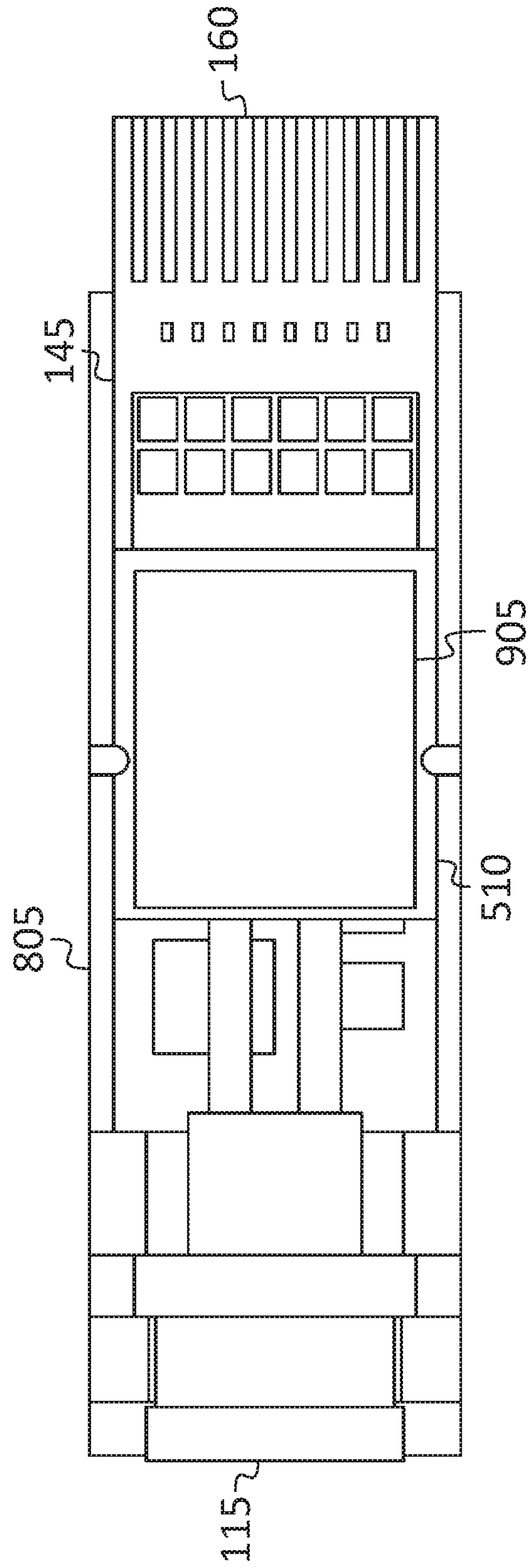

FIG. 9A

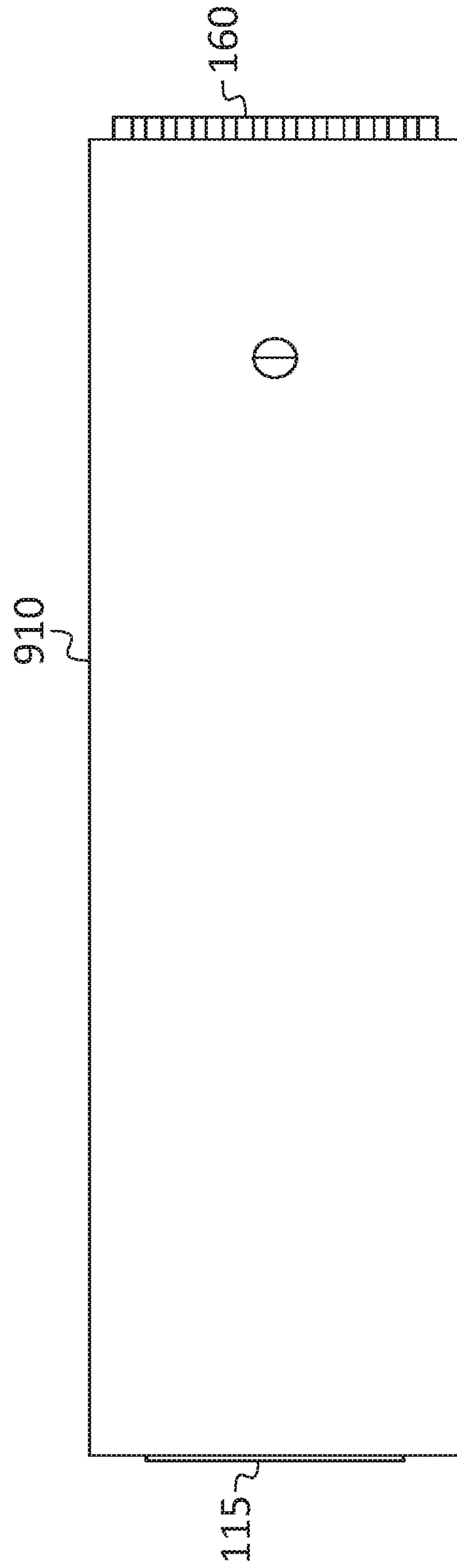

FIG. 9B

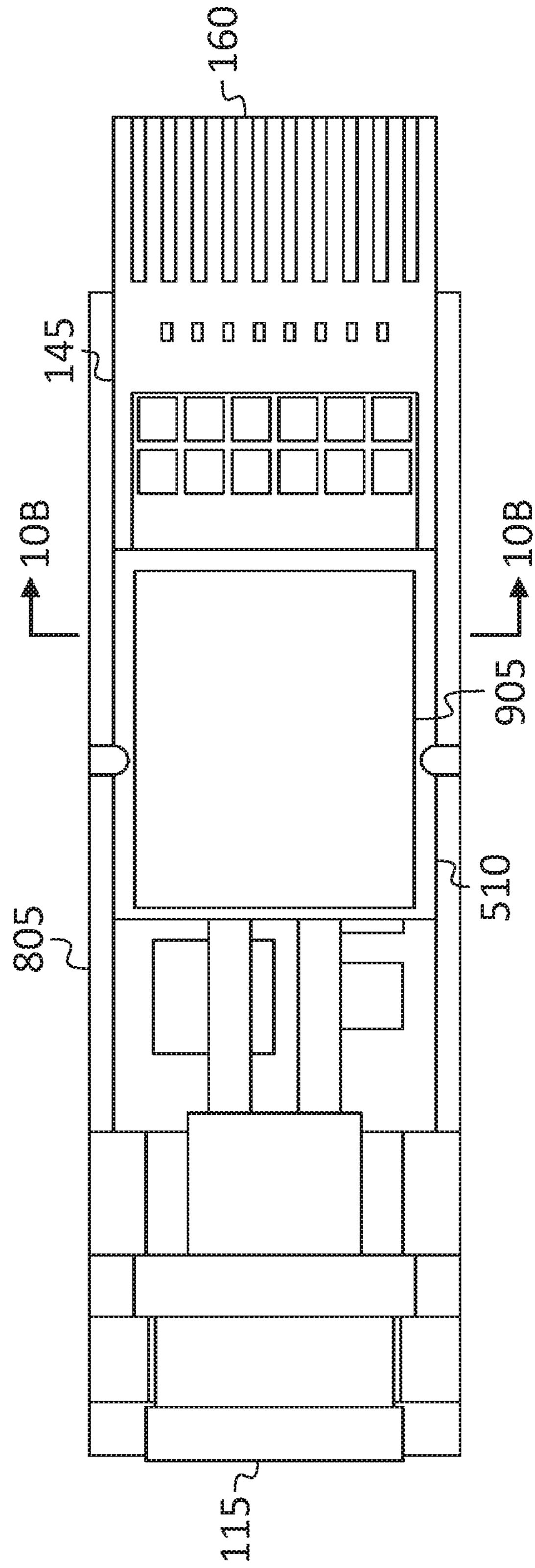

FIG. 10A

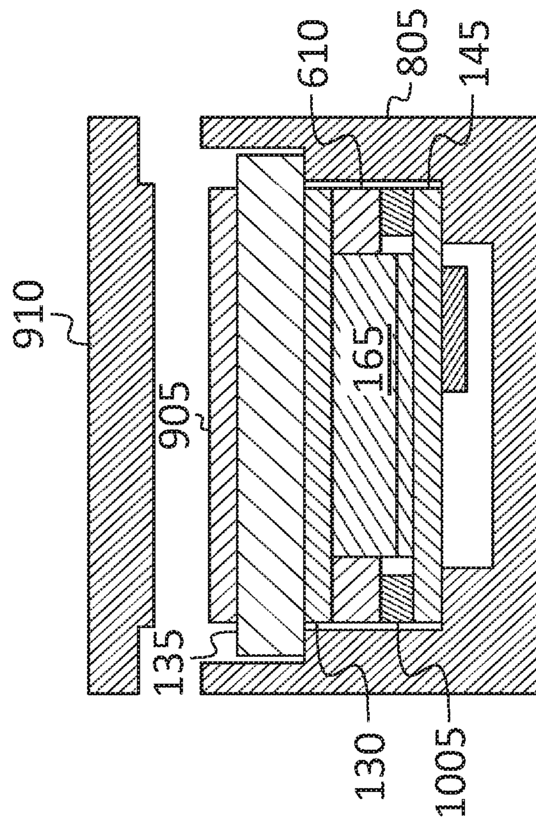

FIG. 10B

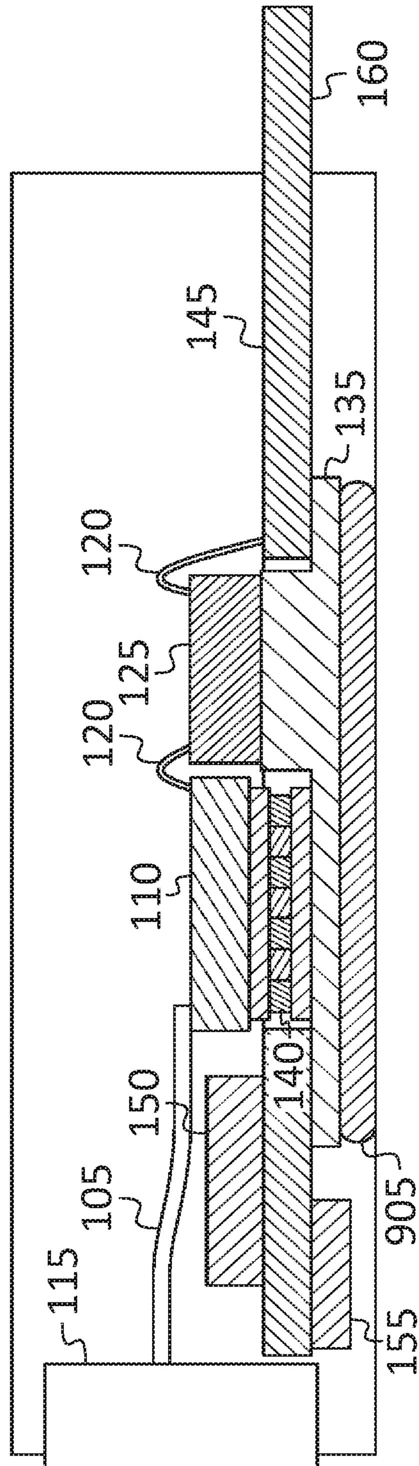

FIG. 11A

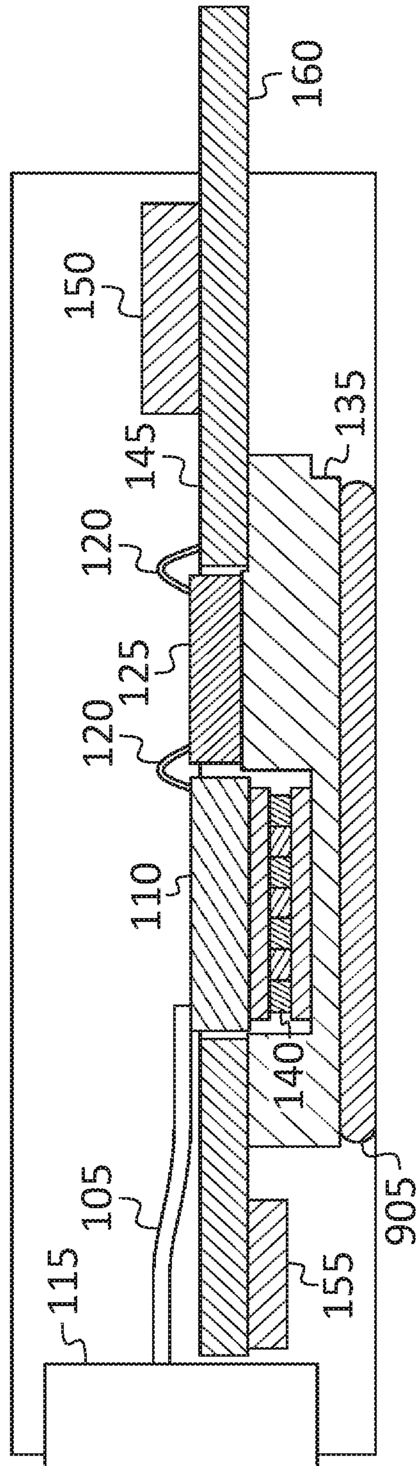

FIG. 11B

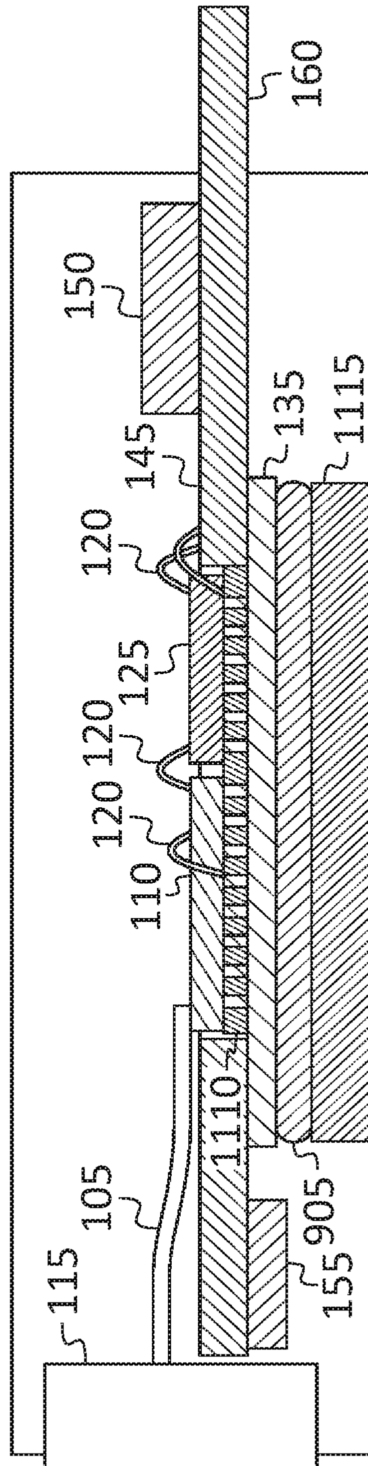

FIG. 11C

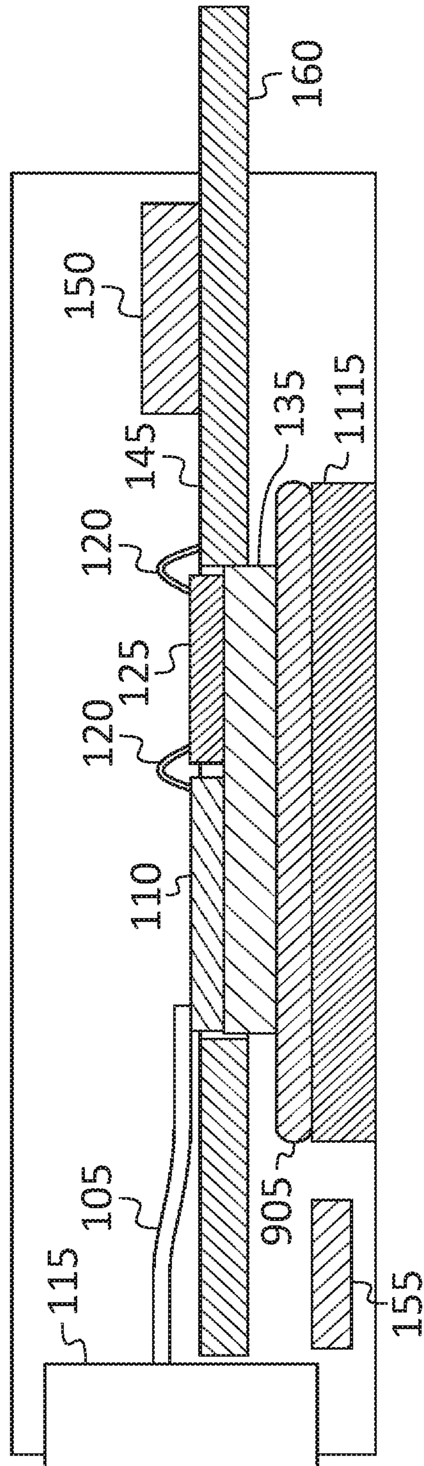

FIG. 12A

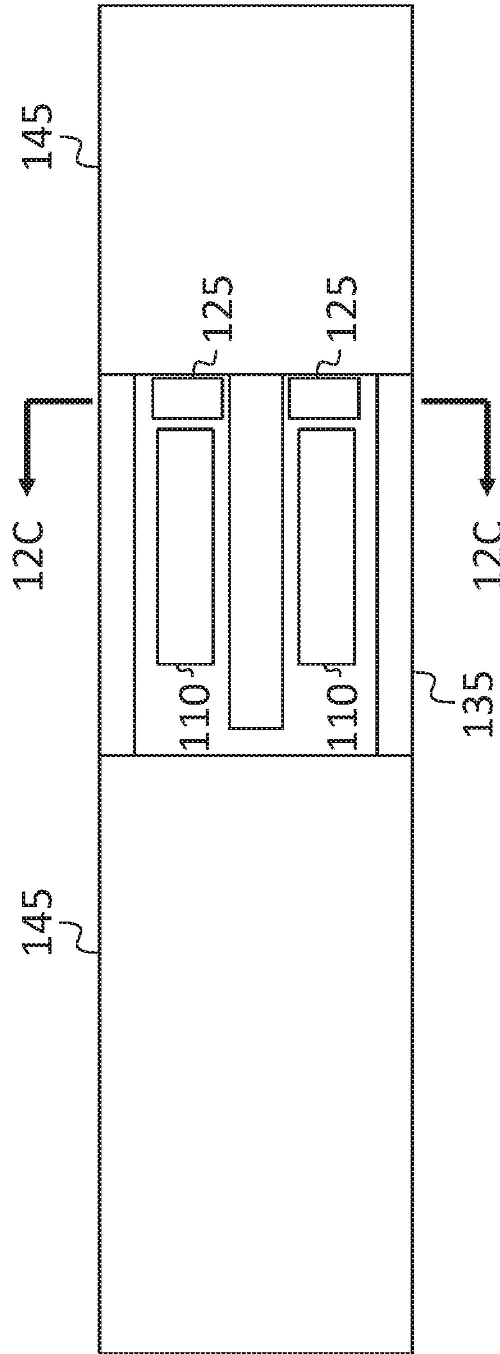

FIG. 12B

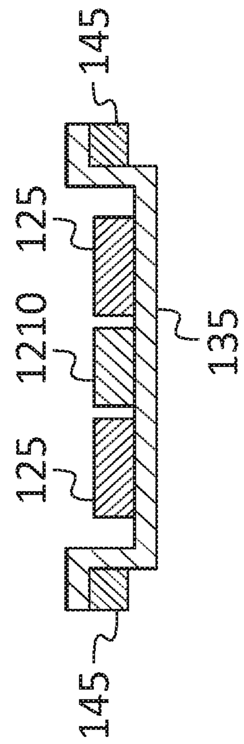

FIG. 12C

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2018/000980

A. CLASSIFICATION OF SUBJECT MATTER
INV. G02B6/42
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G02B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2013/193304 A1 (YU JUHYUN [JP] ET AL) 1 August 2013 (2013-08-01) paragraph [0045] - paragraph [0098]; figures 1-11	1-7, 17-20 8,9,12
X	US 2015/277069 A1 (OKAMOTO DAISUKE [JP] ET AL) 1 October 2015 (2015-10-01) paragraph [0069] - paragraph [0072]; figure 4 paragraph [0040] - paragraph [0062]; figures 2-3	8-16
X	US 2005/058408 A1 (COLGAN EVAN G [US] ET AL) 17 March 2005 (2005-03-17) paragraph [0015] - paragraph [0023]; figures 1-4	8-11

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 November 2018	30/11/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	A. Jacobs

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INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2018/000980

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2012/033208 A1 (HARA HIDEO [JP] ET AL) 9 February 2012 (2012-02-09) paragraphs [0034] - [0040], [0048], [0062] - [0064], [0072] - [0073], [0095] - [0102]; figures 1, 2, 5, 6A-C, 8, 14 -----	1-7, 17-20
A	US 6 910 812 B2 (PEREGRINE SEMICONDUCTOR CORP [US]) 28 June 2005 (2005-06-28) column 49, line 11 - line 67; figures 22, 23 figures 1, 2C, 4B, 5A, 15-17 -----	1,17

2

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2018/000980

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