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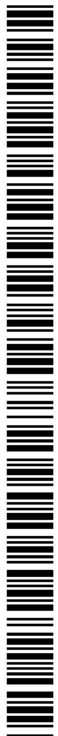

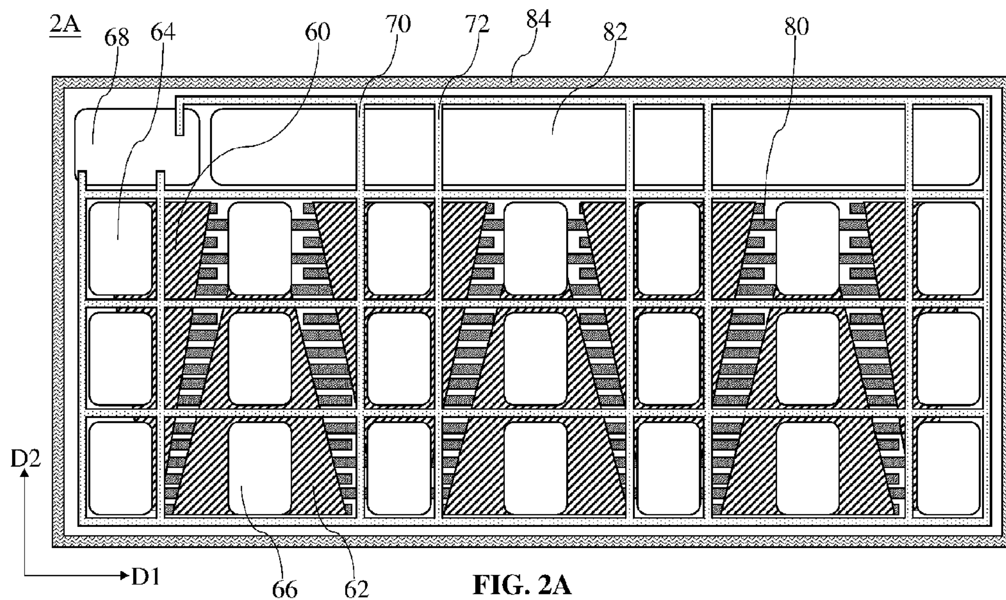

FIG. 2A

(57) **Abstract:** A nitride-based semiconductor device includes a nitride-based transistor, a first conductive layer, first pads, a second conductive layer, second pads, and a patterned conductive layer. The nitride-based transistor includes a source electrode and a drain electrode. The first conductive layer is connected to the source electrode. The first pads are connected to the first conductive layer, in which the first pads are arranged along a first direction. The second conductive layer is connected to the drain electrode. The second pads are connected to the second conductive layer, in which the second pads are arranged along the first direction. The patterned conductive layer includes gate lines which extend along a second direction, in which the first direction is different than the second direction so as to pass through a first spacing between the two adjacent first pads and a second spacing between the two adjacent second pads.

[Continued on next page]

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NITRIDE-BASED SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

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Field of the Disclosure:

[0001] The present disclosure generally relates to a nitride-based semiconductor device. More specifically, the present disclosure relates to a nitride-based semiconductor device having gate lines in grid distribution.

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Background of the Disclosure:

[0002] In recent years, intense research on high-electron-mobility transistors (HEMTs) has been prevalent, particularly for high power switching and high frequency applications. III-nitride-based HEMTs utilize a heterojunction interface between two materials with different bandgaps to
15 form a quantum well-like structure, which accommodates a two-dimensional electron gas (2DEG) region, satisfying demands of high power/frequency devices. In addition to HEMTs, examples of devices having heterostructures further include heterojunction bipolar transistors (HBT), heterojunction field effect transistor (HFET), and modulation-doped FETs (MODFET).

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Summary of the Disclosure:

[0003] In accordance with one aspect of the present disclosure, a nitride-based semiconductor device is provided. The nitride-based semiconductor device includes at least one nitride-based transistor, a first conductive layer, a plurality of first pads, a second conductive layer, a plurality of second pads, and a patterned conductive layer. The nitride-based transistor includes a source
25 electrode and a drain electrode. The first conductive layer is connected to the source electrode. The first pads are connected to the first conductive layer, in which the first pads are arranged along a first direction. The second conductive layer is connected to the drain electrode. The second pads are connected to the second conductive layer, in which the second pads are arranged along the first direction. The patterned conductive layer includes a plurality of gate lines which extend along a
30 second direction, in which the first direction is different than the second direction so as to pass through a first spacing between the two adjacent first pads and a second spacing between the two adjacent second pads.

[0004] In accordance with one aspect of the present disclosure, a method for manufacturing a nitride-based semiconductor device is provided. The method has steps as follows: forming at least
35 one nitride-based transistor comprising a source electrode and a drain electrode; forming a first conductive layer connected to the source electrode and a second conductive layer connected to the

drain electrode; forming a conductive layer cover the first and second conductive layers; patterning the conductive layer such that a plurality of first pads connected to the first conductive layer and a plurality of second pads connected to the second conductive layer are formed; and forming a patterned conductive layer comprising a plurality of gate lines which extend along a second direction, wherein the first direction is different than the second direction so as to pass through a first spacing between the two adjacent first pads and a second spacing between the two adjacent second pads.

[0005] In accordance with one aspect of the present disclosure, a nitride-based semiconductor device is provided. The nitride-based semiconductor device includes at least one nitride-based transistor, a first conductive layer, a plurality of first pads, a second conductive layer, a plurality of second pads, and a patterned conductive layer. The nitride-based transistor includes a source electrode and a drain electrode. The first conductive layer is connected to the source electrode; The first pads are connected to the first conductive layer, in which the first pads are arranged along a first direction. The second conductive layer is connected to the drain electrode. The second pads are connected to the second conductive layer, in which the second pads are arranged along the first direction. The patterned conductive layer includes a plurality of gate lines which collectively form a plurality of first grids enclosing the first pads.

[0006] By the above configuration, the distribution of the gate lines can be expanded as much as possible, so as to reduce gate resistance issue. This configuration is advantageous to high voltage requirement, such as 1200V.

Brief Description of the Drawings:

[0007] Aspects of the present disclosure are readily understood from the following detailed description when read with the accompanying figures. It should be noted that various features may not be drawn to scale. That is, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion. Embodiments of the present disclosure are described in more detail hereinafter with reference to the drawings, in which:

[0008] FIG. 1 is a vertical cross-sectional view of a nitride-based semiconductor device according to some embodiments of the present disclosure;

[0009] FIG. 2A is a top view of a nitride-based semiconductor device according to some embodiments of the present disclosure;

[0010] FIG. 2B depicts an enlarged drawing of a region in FIG. 2A; and

[0011] FIG. 3 is a block diagram showing a flowchart of a method for manufacturing the semiconductor device according to some embodiments of the present disclosure.

Detailed Description:

[0012] Common reference numerals are used throughout the drawings and the detailed description to indicate the same or similar components. Embodiments of the present disclosure will be readily understood from the following detailed description taken in conjunction with the accompanying drawings.

[0013] Spatial descriptions, such as "on," "above," "below," "up," "left," "right," "down," "top," "bottom," "vertical," "horizontal," "side," "higher," "lower," "upper," "over," "under," and so forth, are specified with respect to a certain component or group of components, or a certain plane of a component or group of components, for the orientation of the component(s) as shown in the associated figure. It should be understood that the spatial descriptions used herein are for purposes of illustration only, and that practical implementations of the structures described herein can be spatially arranged in any orientation or manner, provided that the merits of embodiments of this disclosure are not deviated from by such arrangement.

[0014] Further, it is noted that the actual shapes of the various structures depicted as approximately rectangular may, in actual device, be curved, have rounded edges, have somewhat uneven thicknesses, etc. due to device fabrication conditions. The straight lines and right angles are used solely for convenience of representation of layers and features.

[0015] In the following description, semiconductor devices/dies/packages, methods for manufacturing the same, and the likes are set forth as preferred examples. It will be apparent to those skilled in the art that modifications, including additions and/or substitutions may be made without departing from the scope and spirit of the present disclosure. Specific details may be omitted so as not to obscure the present disclosure; however, the disclosure is written to enable one skilled in the art to practice the teachings herein without undue experimentation.

[0016] FIG. 1 is a vertical cross-sectional view of a nitride-based semiconductor device 1A according to some embodiments of the present disclosure. The nitride-based semiconductor device 1A includes a substrate 10, nitride-based semiconductor layers 12, 14, electrodes 20 and 22, a doped nitride-based semiconductor layer 30, a gate electrode 32, passivation layers 40 and 42, and contact vias 50.

[0017] The substrate 10 may be a semiconductor substrate. The exemplary materials of the substrate 10 can include, for example but are not limited to, Si, SiGe, SiC, gallium arsenide, p-doped Si, n-doped Si, sapphire, semiconductor on insulator, such as silicon on insulator (SOI), or other suitable substrate materials. In some embodiments, the substrate 10 can include, for example, but is not limited to, group III elements, group IV elements, group V elements, or combinations thereof (e.g., III-V compounds). In other embodiments, the substrate 10 can include, for example

but is not limited to, one or more other features, such as a doped region, a buried layer, an epitaxial (epi) layer, or combinations thereof.

[0018] In some embodiments, the semiconductor device 1A may further include a buffer layer (not shown). The buffer layer is disposed between the substrate 10 and the nitride-based semiconductor layer 12. The buffer layer can be configured to reduce lattice and thermal mismatches between the substrate 10 and the nitride-based semiconductor layer 12, thereby curing defects due to the mismatches/difference. The buffer layer may include a III-V compound. The III-V compound can include, for example but are not limited to, aluminum, gallium, indium, nitrogen, or combinations thereof. Accordingly, the exemplary materials of the buffer layer can further include, for example but are not limited to, GaN, AlN, AlGaN, InAlGaN, or combinations thereof.

[0019] In some embodiments, the semiconductor device 1A may further include a nucleation layer (not shown). The nucleation layer may be formed between the substrate 10 and a buffer layer. The nucleation layer can be configured to provide a transition to accommodate a mismatch/difference between the substrate 10 and a III-nitride layer of the buffer layer. The exemplary material of the nucleation layer can include, for example but is not limited to AlN or any of its alloys.

[0020] The nitride-based semiconductor layer 12 can be disposed on/over/above the buffer layer 12. The nitride-based semiconductor layer 14 can be disposed on/over/above the nitride-based semiconductor layer 12. The exemplary materials of the nitride-based semiconductor layer 12 can include, for example but are not limited to, nitrides or group III-V compounds, such as GaN, AlN, InN, $In_xAl_yGa_{(1-x-y)}N$ where $x+y \leq 1$, $Al_xGa_{(1-x)}N$ where $x \leq 1$. The exemplary materials of the nitride-based semiconductor layer 14 can include, for example but are not limited to, nitrides or group III-V compounds, such as GaN, AlN, InN, $In_xAl_yGa_{(1-x-y)}N$ where $x+y \leq 1$, $Al_yGa_{(1-y)}N$ where $y \leq 1$.

[0021] The exemplary materials of the nitride-based semiconductor layers 12 and 14 are selected such that the nitride-based semiconductor layer 14 has a bandgap (i.e., forbidden band width) greater/higher than a bandgap of the nitride-based semiconductor layer 12, which causes electron affinities thereof different from each other and forms a heterojunction therebetween. For example, when the nitride-based semiconductor layer 12 is an undoped GaN layer having a bandgap of approximately 3.4 eV, the nitride-based semiconductor layer 14 can be selected as an AlGaN layer having bandgap of approximately 4.0 eV. As such, the nitride-based semiconductor layers 12 and 14 can serve as a channel layer and a barrier layer, respectively. A triangular well potential is generated at a bonded interface between the channel and barrier layers, so that electrons accumulate in the triangular well, thereby generating a two-dimensional electron gas (2DEG)

region adjacent to the heterojunction. Accordingly, the semiconductor device 1A is available to include at least one GaN-based high-electron-mobility transistor (HEMT).

[0022] The electrodes 20 and 22 are disposed on the nitride-based semiconductor layer 14. The electrode 20 can make contact with the nitride-based semiconductor layer 14. The electrode 22
5 can make contact with the nitride-based semiconductor layer 14. Each of the electrodes 20 and 22 can serve as a source electrode or a drain electrode.

[0023] In some embodiments, the electrodes 20 and 22 can include, for example but are not limited to, metals, alloys, doped semiconductor materials (such as doped crystalline silicon), compounds such as silicides and nitrides, other conductor materials, or combinations thereof. The
10 exemplary materials of the electrodes 20 and 22 can include, for example but are not limited to, Ti, AlSi, TiN, or combinations thereof. The electrodes 20 and 22 may be a single layer, or plural layers of the same or different composition. In some embodiments, the electrodes 20 and 22 form ohmic contact with the nitride-based semiconductor layer 14. The ohmic contact can be achieved by applying Ti, Al, or other suitable materials to the electrodes 20 and 22.

15 [0024] In some embodiments, each of the electrodes 20 and 22 is formed by at least one conformal layer and a conductive filling. The conformal layer can wrap the conductive filling. The exemplary materials of the conformal layer, for example but are not limited to, Ti, Ta, TiN, Al, Au, AlSi, Ni, Pt, or combinations thereof. The exemplary materials of the conductive filling can include, for example but are not limited to, AlSi, AlCu, or combinations thereof.

20 [0025] The doped nitride-based semiconductor layer 30 is disposed over the nitride-based semiconductor layer 30. The doped nitride-based semiconductor layer 30 is located between the electrodes 20 and 22. The doped nitride-based semiconductor layer 30 may be p-type. The doped nitride-based semiconductor layer 30 is configured to bring the device into enhancement mode. The doped nitride-based semiconductor layer 30 can be a p-type doped III-V semiconductor layer.
25 In some embodiments, the doped nitride-based semiconductor layer 30 can be omitted so the device is operated in depletion mode.

[0026] The exemplary materials of the doped nitride-based semiconductor layer 30 can include, for example but are not limited to, p-doped group III-V nitride semiconductor materials, such as p-type GaN, p-type AlGaN, p-type InN, p-type AlInN, p-type InGaN, p-type AlInGaN, or
30 combinations thereof. In some embodiments, the p-doped materials are achieved by using a p-type impurity, such as Be, Mg, Zn, Cd, and Mg.

[0027] The gate electrode 32 is disposed on the doped nitride-based semiconductor layer 30. The gate electrode 32 is located between the electrodes 20 and 22. The exemplary materials of the electrode 32 may include metals or metal compounds. The electrode 32 may be formed as a single
35 layer, or plural layers of the same or different compositions. The exemplary materials of the metals

or metal compounds can include, for example but are not limited to, W, Au, Pd, Ti, Ta, Co, Ni, Pt, Mo, TiN, TaN, metal alloys or compounds thereof, or other metallic compounds.

[0028] The electrodes 20 and 22 and the gate electrode 32 can collectively constitute a nitride-based transistor using the 2DEG region.

5 [0029] The passivation layer 40 is disposed on the nitride-based semiconductor layer 14. The passivation layer 40 covers the doped nitride-based semiconductor layer 30 and the gate electrode 36. The electrodes 20 and 22 can penetrate the passivation layer 40 to make contact with the nitride-based semiconductor layer 14. The material of the passivation layer 40 can include, for example but are not limited to, dielectric materials. For example, the passivation layer 40 can

10 include SiN_x, SiO_x, SiON, SiC, SiBN, SiCBN, oxides, nitrides, plasma enhanced oxide (PEOX), or combinations thereof.

[0030] The passivation layer 42 is disposed on the passivation layer 42. The passivation layer 42 covers the electrodes 20 and 22. In some embodiments, the passivation layer 42 can serve as a planarization layer which has a level top surface to support other layers/elements. In some

15 embodiments, the passivation layer 42 can be formed as a thicker layer, and a planarization process, such as chemical mechanical polish (CMP) process, is performed on the passivation layer 42 to remove the excess portions, thereby forming a level top surface. The material of the passivation layer 42 can include, for example but are not limited to, dielectric materials. For example, the passivation layer 42 can include SiN_x, SiO_x, SiON, SiC, SiBN, SiCBN, oxides, nitrides, PEOX, or

20 combinations thereof.

[0031] The contact vias 50 are disposed within the passivation layer 42. The contact vias 50 can penetrate the passivation layer 42. The contact vias 50 can extend longitudinally to connect to the electrodes 20 and 22 and the gate electrode 32. The exemplary materials of the contact vias 50 can include, for example but are not limited to, conductive materials, such as metals or alloys.

25 The nitride-based transistor can be electrically coupled with at least one conductive source through the contact vias 50. For example, the electrodes 20 and 22 can be electrically coupled with a source pad or a drain pad through the contact vias 50; the gate electrode 32 can be electrically coupled with a gate pad through the contact vias 50.

[0032] FIG. 2A is a top view of a nitride-based semiconductor device 2A according to some

30 embodiments of the present disclosure. FIG. 2B depicts an enlarged drawing of a region in FIG. 2A. In order to make the description clear, directions D1 and D2 are labeled in FIG. 2A and FIG. 2B, which are different than each other. For example, the direction D1 is a horizontal direction of FIG. 2A; and the direction D2 is a vertical direction of FIG. 2A which is perpendicular to the direction D1.

[0033] The nitride-based semiconductor device 2A includes at least one nitride-based transistor, conductive layers 60 and 62, pads 64, 66, 68, a patterned conductive layer 70, conductive straps 80, an electrostatic discharge (ESD) protection pad 82, a seal ring 84.

[0034] The nitride-based transistor can include a structure as afore-mentioned. For example, 5 the nitride-based transistor can include a source electrode and a drain electrode. The one or more nitride-based transistors are not illustrated in FIG. 2A but embedded in elements illustrated in FIG. 2A. The exemplary illustration of FIG. 2A is to show a layout of the nitride-based semiconductor device 2A above the one or more nitride-based transistors.

[0035] The conductive layers 60 and 62 are alternately arranged along the direction D1. The 10 conductive layers 60 and 62 are arranged along the direction D1. The conductive layers 60 and 62 may have opposite shapes. For example, the conductive layers 60 are in inverted trapezoid and the conductive layers 60 are in trapezoid.

[0036] The conductive straps 80 are partially covered by the conductive layers 60 and 62. The conductive straps 80 can extend along the direction D1. The conductive straps 80 can be arranged 15 along the direction D2. The conductive layers 60 can be indirectly connected to the one or more source electrodes of the nitride-based transistors via the conductive straps 80. The conductive layers 62 can be indirectly connected to the one or more drain electrodes of the nitride-based transistors via the conductive straps 80.

[0037] The pads 64 are disposed over the conductive layers 60. The pads 64 can be connected 20 to conductive layers 60. For the pads 64 correspondingly to the same conductive layer 60, the pads 64 are arranged along the direction D2. In some embodiments, the pads 64 arranged along the direction D2 are arranged by the same spacing. In some embodiments, each of the pads 64 has a width and a length greater than the width. In some embodiments, all of the pads 64 have the same area. Such the design for the pads 64 is made to successfully build the layout.

25 [0038] The pads 66 are disposed over the conductive layers 62. The pads 66 can be connected to conductive layers 62. For the pads 66 correspondingly to the same conductive layer 62, the pads 66 are arranged along the direction D2. In some embodiments, the pads 66 arranged along the direction D2 are arranged by the same spacing. In some embodiments, each of the pads 66 has a width and a length greater than the width. In some embodiments, all of the pads 66 have the 30 same area. Such the design for the pads 66 is made to successfully build the layout.

[0039] In some embodiments, in order to successfully build the layout, the pads 64 and 66 may have the same area. A distance between the pads 64 to the pads 66 is greater than a distance between the pads 66. An external voltage source can be electrically coupled with the one or more source electrodes/drain electrodes of the nitride-based transistors via the pads 64 and the pads 66,

so as to operate the nitride-based transistors. In this regard, the pads 64 can serve as source pads, and the pads 66 can serve as drain pads.

[0040] The pad 68 can serve as a gate pad. The pads 64 and the pads 66 can form an array, in which the pad 68 is out of the range of the array. The patterned conductive layer 70 includes gate lines 72. The gate lines 72 are connected to the pad 68. The gate lines 72 can extend from the pad 68 to make electrical couple with one or more gate electrodes of the nitride-based transistors.

[0041] The gate lines 72 can extend along the directions D1 and D2. The gate lines 72 extending along the direction D1 can pass through the spacing between the two adjacent pads 64 and the spacing between the two adjacent pads 66. The gate lines 72 can extend between the pads 64, between the pads 66, and between the pads 64 and 66. Accordingly, the gate lines 72 collectively form grids enclosing the pads 64 and 66. The grids enclosing the pads 64 are smaller than the grids enclosing the pads 66.

[0042] The gate lines 72 can form an electrical route extending along the directions D1 and D2. The electrical route is in grid distribution so the transmission of electrical signals can get more uniform. In addition, such the configuration is to expand the distribution of the gate lines 72 as much as possible, so as to reduce gate resistance issue. That is, resistance between the pad 68 and one or more gate electrodes of the nitride-based transistors can decrease. This configuration is advantageous to high voltage requirement, such as 1200V. Furthermore, as the configuration is applied to the high voltage requirement, distance from the gate lines 72 to the pad 66 serves as an important factor for device reliability. The average distance from the gate lines 72 to the pad 66 is less than the average distance from the gate lines 72 to the pad 64. The reason is that high voltage will be applied to the pad 66 so there is a parasitic capacitance issue once distance between gate lines and drain pads is too close.

[0043] The ESD protection pad 82 is adjacent to the pad 68. the ESD protection pad 82 is out of the range of the array of pads 64 and 66. The seal ring 84 surrounds/encloses elements of the semiconductor device 1A.

[0044] FIG. 3 is a block diagram showing a flowchart of a method for manufacturing the semiconductor device 1A according to some embodiments of the present disclosure. To manufacture the semiconductor device 1A, the process includes steps S10-S50, in which S10 is forming at least one nitride-based transistor; S20 is forming conductive layers; S30 is forming a blanket conductive layer; S40 is patterning the blanket conductive layer; and S50 is forming gate lines.

[0045] In the stage S10, at least one nitride-based transistor including a source electrode, a drain electrode, and a gate electrode is formed. During the stage S10, two nitride-based semiconductor layers are formed as well. One nitride-based semiconductor layer is stacked on another nitride-

based semiconductor layer, in which the upper one has a bandgap greater than a bandgap of the bottom one.

[0046] In the stage S20, conductive layers are formed, in which these conductive layers are correspondingly indirectly connected to the source electrodes and the drain electrodes of one or
5 more nitride-based transistors, so as to electrically couple with them.

[0047] In the stage S30, a blanket conductive layer is formed to cover the conductive layers.

[0048] In the stage S40, the blanket conductive layer is patterned such that pads are formed. These pads are correspondingly connected to the conductive layers, so as to electrically couple with them. The pads may include a gate pad, source pads, and drain pads.

10 [0049] In the stage S50, gate lines are formed for connection between the gate electrode and the gate pad. The gate lines can be formed by patterning a blanket conductive layer.

[0050] The embodiments were chosen and described in order to best explain the principles of the disclosure and its practical application, thereby enabling others skilled in the art to understand the disclosure for various embodiments and with various modifications that are suited to the
15 particular use contemplated. Furthermore, the term “connection” in the present disclosure may include “indirect connection”, “direct connection”, or combinations thereof.

[0051] As used herein and not otherwise defined, the terms "substantially," "substantial," "approximately" and "about" are used to describe and account for small variations. When used in conjunction with an event or circumstance, the terms can encompass instances in which the event
20 or circumstance occurs precisely as well as instances in which the event or circumstance occurs to a close approximation. For example, when used in conjunction with a numerical value, the terms can encompass a range of variation of less than or equal to ±10% of that numerical value, such as less than or equal to ±5%, less than or equal to ±4%, less than or equal to ±3%, less than or equal to ±2%, less than or equal to ±1%, less than or equal to ±0.5%, less than or equal to ±0.1%, or less
25 than or equal to ±0.05%. The term “substantially coplanar” can refer to two surfaces within micrometers of lying along a same plane, such as within 40 μm, within 30 μm, within 20 μm, within 10 μm, or within 1 μm of lying along the same plane.

[0052] As used herein, the singular terms “a,” “an,” and “the” may include plural referents unless the context clearly dictates otherwise. In the description of some embodiments, a
30 component provided “on” or “over” another component can encompass cases where the former component is directly on (e.g., in physical contact with) the latter component, as well as cases where one or more intervening components are located between the former component and the latter component.

[0053] While the present disclosure has been described and illustrated with reference to specific
35 embodiments thereof, these descriptions and illustrations are not limiting. It should be understood

by those skilled in the art that various changes may be made and equivalents may be substituted without departing from the true spirit and scope of the present disclosure as defined by the appended claims. The illustrations may not necessarily be drawn to scale. There may be distinctions between the artistic renditions in the present disclosure and the actual apparatus due to manufacturing processes and tolerances. Further, it is understood that actual devices and layers may deviate from the rectangular layer depictions of the FIGS. and may include angles surfaces or edges, rounded corners, etc. due to manufacturing processes such as conformal deposition, etching, etc. There may be other embodiments of the present disclosure which are not specifically illustrated. The specification and the drawings are to be regarded as illustrative rather than restrictive. Modifications may be made to adapt a particular situation, material, composition of matter, method, or process to the objective, spirit and scope of the present disclosure. All such modifications are intended to be within the scope of the claims appended hereto. While the methods disclosed herein have been described with reference to particular operations performed in a particular order, it will be understood that these operations may be combined, sub-divided, or re-ordered to form an equivalent method without departing from the teachings of the present disclosure. Accordingly, unless specifically indicated herein, the order and grouping of the operations are not limitations.

Claims:

1. A nitride-based semiconductor device comprising:

at least one nitride-based transistor comprising a source electrode and a drain electrode;

a first conductive layer connected to the source electrode;

5 a plurality of first pads connected to the first conductive layer, wherein the first pads are arranged along a first direction;

a second conductive layer connected to the drain electrode;

a plurality of second pads connected to the second conductive layer, wherein the second pads are arranged along the first direction; and

10 a patterned conductive layer comprising a plurality of gate lines which extend along a second direction, wherein the first direction is different than the second direction so as to pass through a first spacing between the two adjacent first pads and a second spacing between the two adjacent second pads.

15 2. The nitride-based semiconductor device of any one of the preceding claims, wherein all of the first pads arranged along the first direction are arranged by the first spacing.

3. The nitride-based semiconductor device of any one of the preceding claims, wherein all of the second pads arranged along the first direction are arranged by the second spacing.

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4. The nitride-based semiconductor device of any one of the preceding claims, wherein each of the first pads has a width and a length greater than the width.

5. The nitride-based semiconductor device of any one of the preceding claims, wherein 25 each of the second pads has a width and a length greater than the width.

6. The nitride-based semiconductor device of any one of the preceding claims, wherein the gate lines collectively form a plurality of first grids enclosing the first pads.

7. The nitride-based semiconductor device of any one of the preceding claims, wherein the gate lines collectively form a plurality of second grids enclosing the second pads.

8. The nitride-based semiconductor device of any one of the preceding claims, wherein the each of the first grids is smaller than each of the second grids.

9. The nitride-based semiconductor device of any one of the preceding claims, wherein the first pads have the same area.

10. The nitride-based semiconductor device of any one of the preceding claims, wherein the second pads have the same area.

11. The nitride-based semiconductor device of any one of the preceding claims, wherein the first pads and the second pads have the same area.

12. The nitride-based semiconductor device of any one of the preceding claims, a distance between the first pad to the second pads is greater than a distance between the second pads.

13. The nitride-based semiconductor device of any one of the preceding claims, wherein the gate lines form an electrical route extending along the first direction and the second direction.

14. The nitride-based semiconductor device of any one of the preceding claims, further comprising a gate pad, wherein the gate lines are connected to the gate pad.

15. The nitride-based semiconductor device of any one of the preceding claims, wherein the nitride-based transistor comprises a first nitride-based semiconductor layer and a second nitride-based semiconductor layer disposed on the first nitride-based semiconductor layer and having a bandgap greater than a bandgap of the first nitride-based semiconductor layer.

16. A method for manufacturing a nitride-based semiconductor device, comprising:

forming at least one nitride-based transistor comprising a source electrode and a drain electrode;

forming a first conductive layer connected to the source electrode and a second conductive layer connected to the drain electrode;

forming a conductive layer cover the first and second conductive layers;

patterning the conductive layer such that a plurality of first pads connected to the first conductive layer and a plurality of second pads connected to the second conductive layer are formed; and

forming a patterned conductive layer comprising a plurality of gate lines which extend along a second direction, wherein the first direction is different than the second direction so as to pass through a first spacing between the two adjacent first pads and a second spacing between the two adjacent second pads.

17. The method of the any one of the preceding claims, wherein the gate lines collectively form a plurality of first grids enclosing the first pads.

18. The method of the any one of the preceding claims, wherein the gate lines collectively form a plurality of second grids enclosing the second pads.

19. The method of the any one of the preceding claims, wherein the each of the first grids is smaller than each of the second grids.

20. The method of any one of the preceding claims, wherein forming at least one nitride-based transistor comprises:

forming a first nitride-based semiconductor layer; and

forming a second nitride-based semiconductor layer disposed on the first nitride-based semiconductor layer and having a bandgap greater than a bandgap of the first nitride-based semiconductor layer.

21. A nitride-based semiconductor device comprising:

at least one nitride-based transistor comprising a source electrode and a drain electrode;

a first conductive layer connected to the source electrode;

a plurality of first pads connected to the first conductive layer, wherein the first pads are arranged along a first direction;

a second conductive layer connected to the drain electrode;

a plurality of second pads connected to the second conductive layer, wherein the second pads are arranged along the first direction; and

a patterned conductive layer comprising a plurality of gate lines which collectively form a plurality of first grids enclosing the first pads.

22. The nitride-based semiconductor device of any one of the preceding claims, wherein the gate lines collectively form a plurality of second grids enclosing the second pads.

23. The nitride-based semiconductor device of any one of the preceding claims, wherein the each of the first grids is smaller than each of the second grids.

24. The nitride-based semiconductor device of any one of the preceding claims, wherein the gate lines form an electrical route extending along the first direction and the second direction.

5 25. The nitride-based semiconductor device of any one of the preceding claims, further comprising a gate pad, wherein the gate lines are connected to the gate pad.

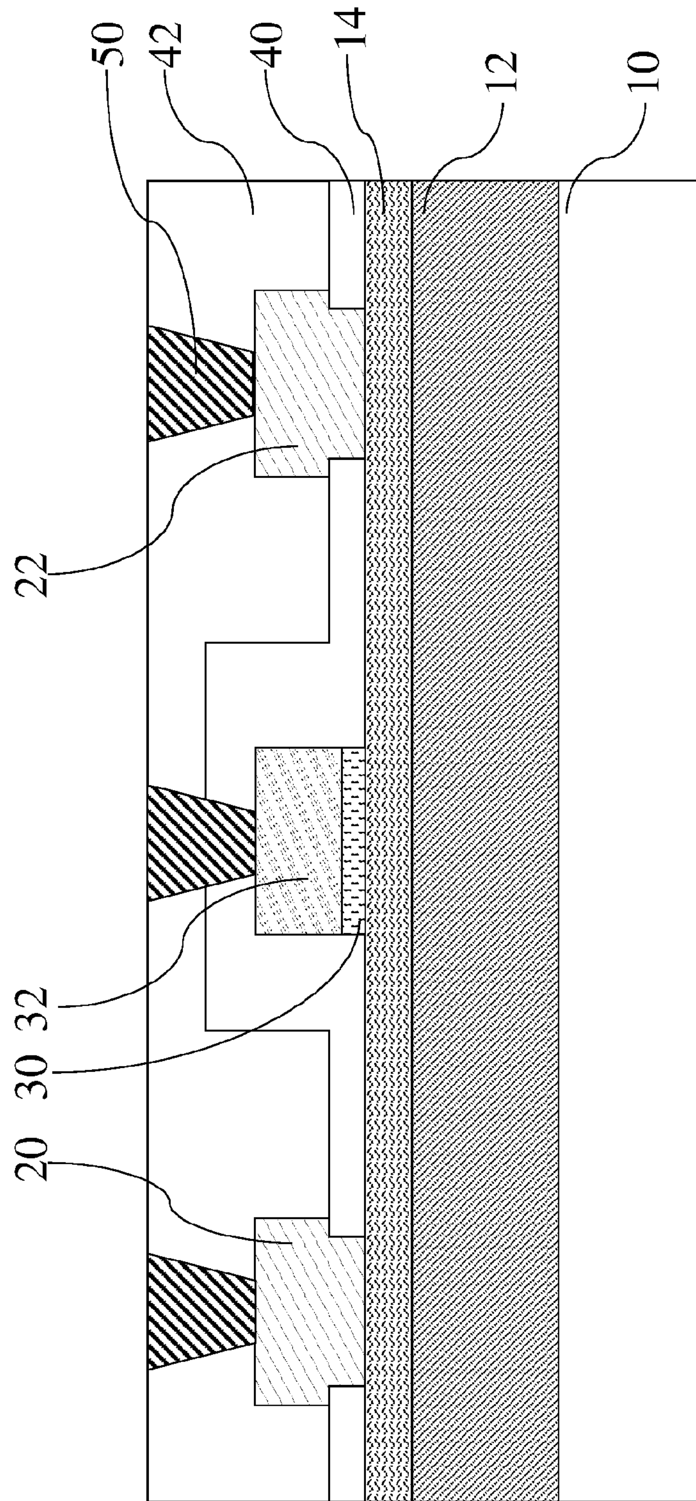

FIG. 1

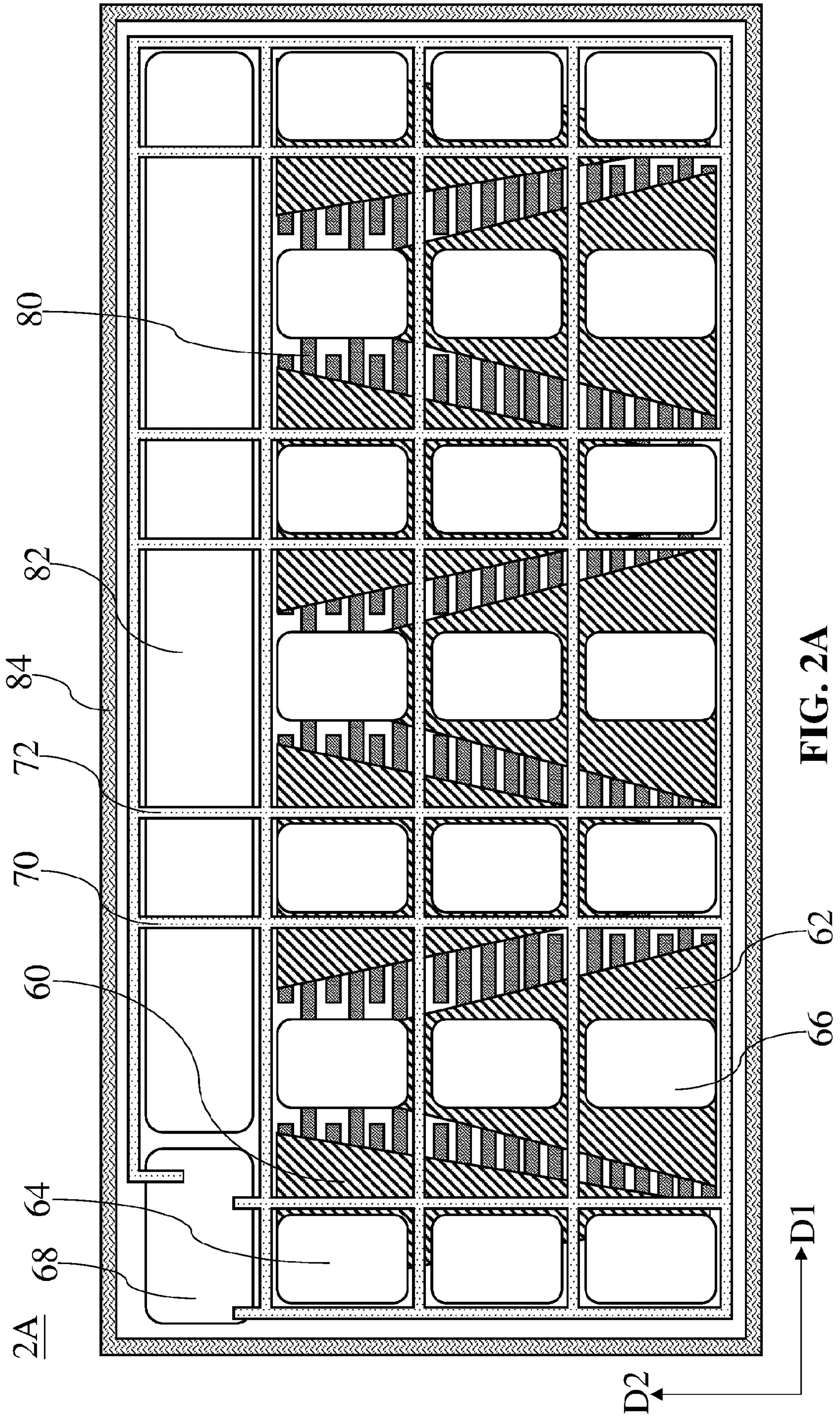

FIG. 2A

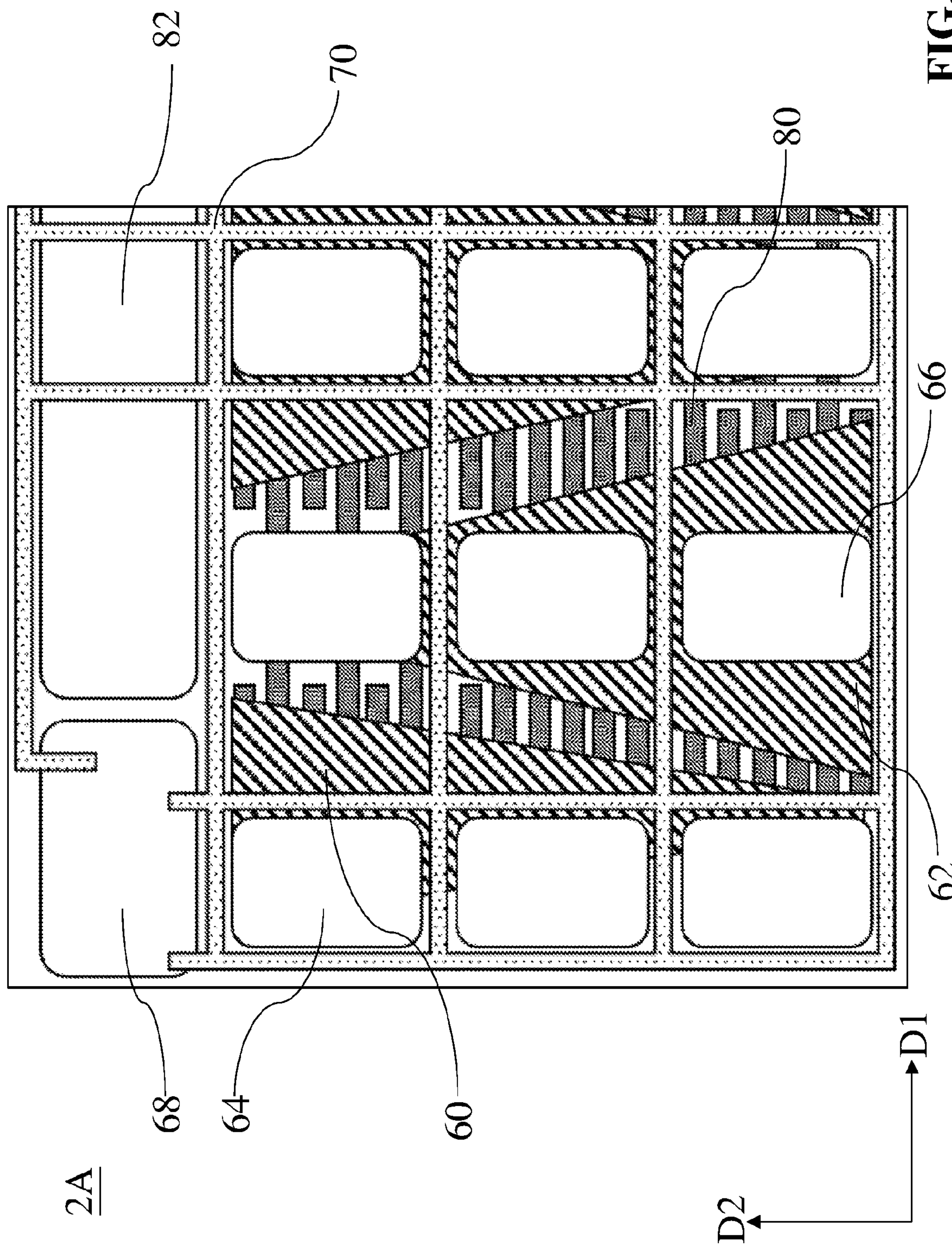

FIG. 2B

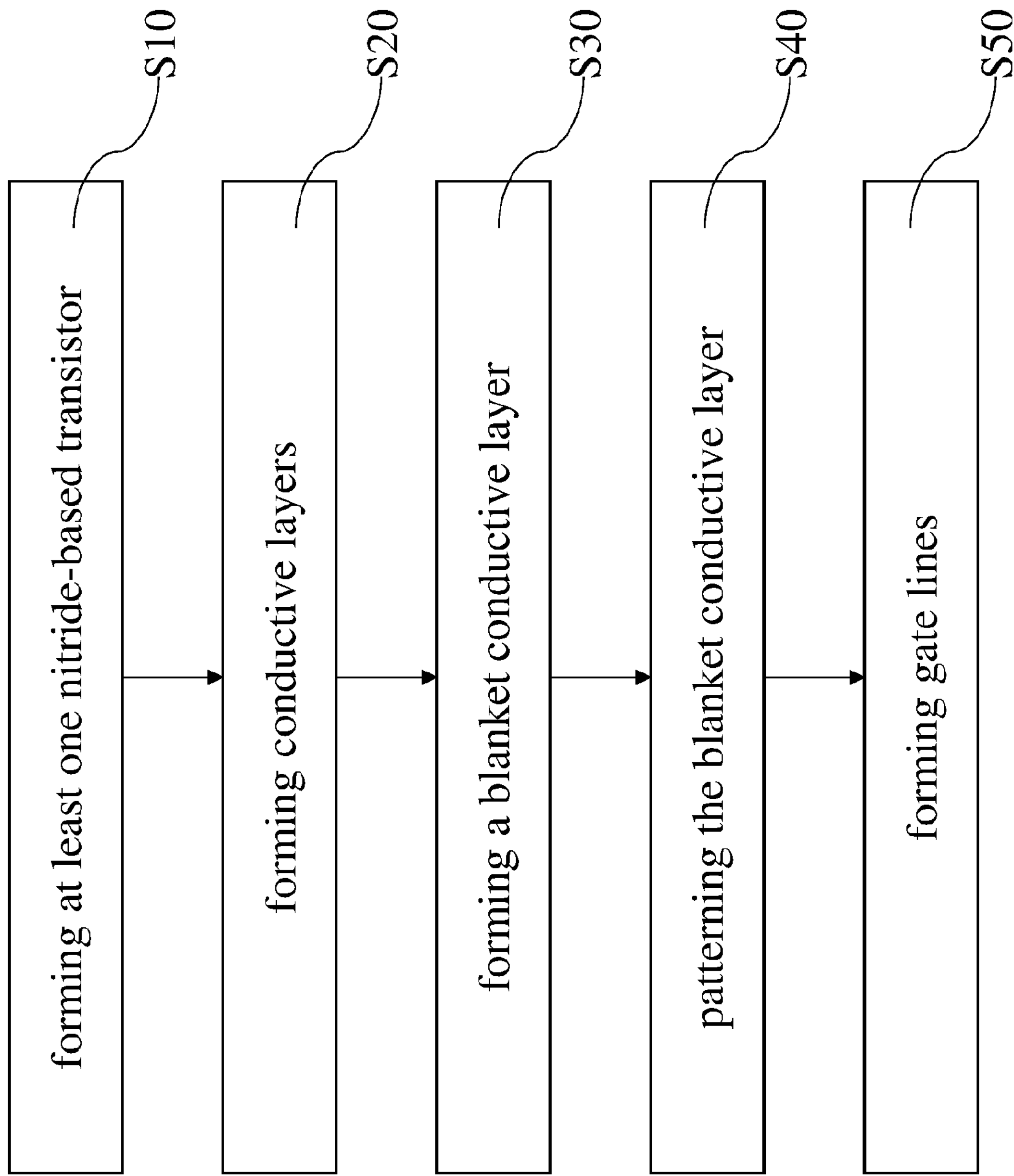

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2022/127221

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/538(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNTXT, ENTXT, ENTXTC, DWPI, CNKI: semiconductor, transistor, source, drain, gate, pad, layer, metal, conductive, electrode

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2018138134 A1 (ROHM CO LTD) 17 May 2018 (2018-05-17) the whole document	1-25
A	US 2016020207 A1 (RENESAS ELECTRONICS CORP) 21 January 2016 (2016-01-21) the whole document	1-25
A	US 2020152572 A1 (ST MICROELECTRONICS SRL) 14 May 2020 (2020-05-14) the whole document	1-25

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier application or patent but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed
- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 November 2022	**12 January 2023**
Name and mailing address of the ISA/CN **National Intellectual Property Administration, PRC** **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China**	Authorized officer **LI,Ying**
Facsimile No. **(86-10)62019451**	Telephone No. **62089296**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2022/127221

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		EP 2975647 A1	20 January 2016
		US 9293457 B2	22 March 2016
US 2020152572 A1	14 May 2020	IT 201800010195 A1	09 May 2020