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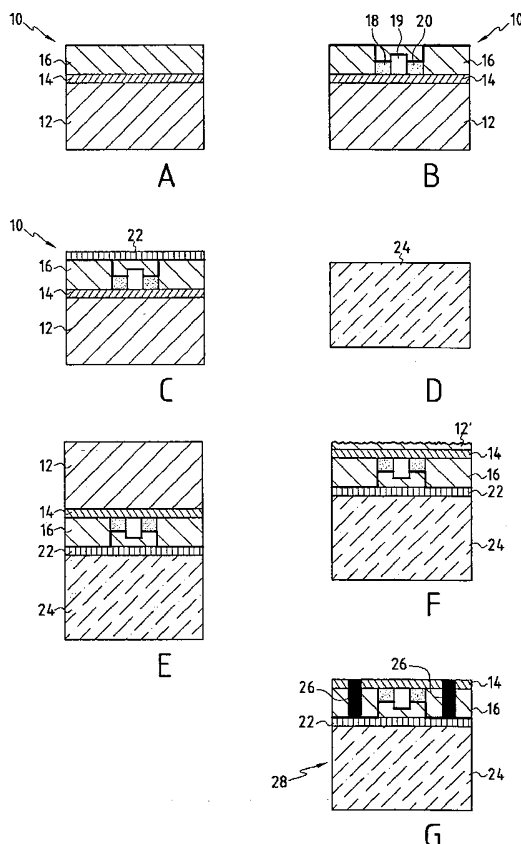
(54) Title: METHOD OF PRODUCING A HYBRID DEVICE AND HYBRID DEVICE



(57) Abstract: A silicone on insulator device (10) comprising electronical structures (18, 20, 22;46) is assembled with a second device, in particular an electro-optical device or a thermo-optical device (24, 50). The assembling is made in such a manner such as to place the electronical structures as close as possible to functional portions in the elecro-optical or thermo-optical device. After the assembling step, the substrate (12) of the semiconductor device is at least partially removed. Thereby, one obtains a very compact, highly integrated device (28, 44, 60) in which the electronical structures present in the semiconductor device can control functional structures in the electro-optical or thermo-optical device.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Method of producing a hybrid device and hybrid device

Field of the invention and technological background :

5 The invention relates to a method of producing hybrid devices or devices of the type comprising two substrates each one having components, for example either electronic or electrical and/or optical (for example thermo-optical) components.

10 In many such hybrid devices, a functional part has to be controlled by a driver part. The functional part for example comprises an electro-optical or thermo-optical device, and the driver part comprises a semiconductor device with electronic components therein.

15 Thus one example of a device concerned by the invention comprises an electro-optical or thermo-optical device representing a functional part and a semiconductor device representing a driver part. The invention also concerns a hybrid device comprising two semiconductor devices, each having electronic components formed 20 therein, in particular two SOI devices.

In the past, many attempts have been made to integrate these different parts on a single device, for instance a single chip. The monolithic approach, however, is not as ideal as thought : such an 25 approach often requires compromising between two completely different technologies, for example technologies for semiconductor devices and technologies for electro-optical or thermo-optical devices.

Therefore, new attempts have been started from the completely 30 opposite side. The two parts have been fabricated independently of each other and have been combined. For example, both devices have been plugged on a motherboard. To the advanced technologies of combining two different devices also pertain flip-chip bonding and wire-bonding.

35

However, these technologies do not provide for a hybrid device in which both parts are assembled in an optimum manner.

The same problem arises when making a hybrid device
5 comprising two substrates or two semiconductor devices each one having electronic components.

Summary of the invention :

10 It is therefore an object of the present invention to provide a method of producing a hybrid device, for example with a first part being a semiconductor part and a second part comprising an electro-optical and/or a thermo-optical part and/or an electronic part. Both parts are very reliably assembled in a compact manner, thereby
15 yielding a highly integrated device.

To this end, the present invention provides a method of producing a hybrid device, comprising the steps of:

20 a) providing a first device or wafer comprising a semiconductor substrate covered with an insulating layer, which is itself covered with at least one semiconductor layer, wherein in the semiconductor layer, electronic structures are provided,

25 b) providing a second device or wafer, in particular an electrical or electronic or electro-optical or thermo-optical device,

c) aligning both devices or wafer with respect to each other, wherein the top surfaces of both devices are facing each other,

30

d) assembling both devices or wafer,

e) at least partially thinning the substrate of the first device or wafer.

35

The first device or wafer can be of the SOI type, for example comprising a silicon substrate, a dielectric layer and a mono-crystalline silicon layer on top of it. It can also be a semiconductor on insulator structure, comprising a layer of semiconductor material (for example: SiGe, InP, AsGa), a dielectric or an insulator layer and a semiconductor substrate. It can also be a bulk semiconductor substrate of InP, or AsGa or Si.

Various methods of thinning the substrate can be used. Furthermore, the layered structure of the semiconductor on insulator device allows for a very compact, highly integrated hybrid device or wafer.

Since both the first device and the second device or wafer are fabricated independently prior to the assembling step, different technologies that might be incompatible can be used for their production, and therefore the quality of both devices or wafers can be very high. Compromises which have to be developed when the monolithic approach is used, are no longer necessary whilst at the same time, a device or wafer is obtained which is practically as highly integrated as a monolithic device.

According to preferred embodiments of the present method, a dielectric layer is deposited onto at least one of the devices or wafers prior to the aligning step. The dielectric layer aids in assembling the two devices or wafers because it provides for a better adhesion of the two layers. Typical dielectric materials are SiO_2, Si_3N_4, Al_2O_3, diamond, HfO_2, ZrO_2, La_2O_3 , Y_2O_3 and $LiNbO_3$

According to one embodiment, the dielectric layer is covered with a multi-layer structure comprising more than one single semiconductor layer, possibly separated from each other by dielectric layers.

In other words, in order to provide for more complicated electronic structures, the first device or wafer can comprise a multi-layer structure on top of the insulating layer. For example, it can

include a sequence of alternating semiconductor and insulator layers with electronic structures in the semiconductor layers.

It is advisable to planarize at least one of the devices, and/or to activate the surface of at least one of the devices or wafers prior to the aligning (and to the assembling) step in order to provide for a better bonding. The planarization can be done either by chemical and mechanical methods or by purely chemical methods. The surface activation can include an RCA-like process, plasma activation etc. Thus the activated surfaces can be more easily bonded.

According to one embodiment, the step of thinning or at least partially removing the substrate is performed by chemical etchback grinding. Alternatively, mechanical grinding or polishing can be used.

A still further alternative is to split the substrate at a weak layer thereof. The weak layer can be a portion of the substrate into which atoms or ions have been implanted or into which a porous layer of semiconductor material is formed.

In a semiconductor or insulating device of the kind used in the method according to the present invention, the semiconductor layer is for example a layer of mono-crystalline silicon in which the electronic structures have been provided The insulating layer comprises silicon oxyde, and the substrate comprises silicon. The silicon oxyde is, for example, a result of an oxydation of the upper portion of the substrate.

The second device can comprise at least one of the elements in the group consisting of optical or microoptical elements, for example at least one optical waveguide, and/or at least one photodiode, and/or at least one laser (such as a vertical cavity surface emitting laser, VCSEL), and/or at least one liquid cristal display device and/or thermooptical elements.

Alternatively or in addition, it can also comprise electronic components or elements. The second device can be for example of the same type as the first device, for example a SOI device.

5 It is a further object of the present invention to provide for a device comprising a functional (electro-optical or thermo-optical) part and a driver part.

According to the present invention, a hybrid device comprises 10 an electro-optical or thermo-optical device and a layered semiconductor structure bonded thereto or on top thereof.

According to another aspect, a hybrid device according to the invention comprises a first and a second semiconductor device bonded 15 on said first device, each comprising a layered semiconductor structure.

The hybrid device according to the present invention has the advantage that electronic structures can be provided in the layered 20 semiconductor structure, and that a very compact device is obtained. The electronic structures (and/or devices) can be provided in a semiconductor layer on top of which an insulating layer can also be provided.

25 The semiconductor structure is advantageously attached to the second electro-optical device via a direct bonding. Thereby, the attachment is very reliable.

Brief description of the drawings :

30

These and other features, objects, and advantages of the present invention will become apparent upon consideration of the following detailled description of the invention when read in conjunction with the drawing in which:

35

- figures 1A-1G show steps of a method of producing a hybrid device according to a first embodiment of the present invention,

- figure 2A-2G show steps of a method of producing a hybrid device according to a second embodiment of the present invention,

- figures 3A-3D show steps of a method of producing a hybrid device according to a third embodiment of the present invention in which a multi-layer structure is placed on an electro-optical device, and

- figures 4A-4G show steps of a method of producing a hybrid device of a fourth embodiment of the present invention.

Detailled description of preferred embodiments :

The method according to a first embodiment of the present invention starts with a first device 10 comprising a first semiconductor (for example silicon) substrate 12, a dielectric area or layer 14 (for example an oxide layer and in particular a silicon oxide SiO2), and a thin film or layer 16 of a second semiconductor material (for example mono-crystalline silicon). The thickness of substrate 12 may range from several hundreds to several thousands of nm. Layer 14 may be as thick as a few tens of nm to a few thousands of nm. For example, it may range from 10 nm to 50 nm or to 80 nm or to 100 nm or to 250 nm or to 500 nm or to 5000 nm.

Dielectric or insulating layer 14 can be chosen from SiO_2, Si_3N_4, Al_2O_3 diamond or any other dielectric material, for example of the high-K type (such as disclosed in the MRS Bulletin, March 2002, Vol.27, No3, "Alternative Gate Dielectris for Microelectronics"), or of the low-K type.

As an example the first device or wafer 10 is of the SOI type. One method for fabricating such a device is disclosed in EP-0 905 767 A1. Such a silicon on insulator device comprises a silicon substrate 12

with a buried insulating layer 14 (for example an oxide layer) on top thereof, which is covered with a layer 16 of mono-crystalline silicon. The second semiconductor material is not limited to silicon, but could also be another semiconductor material, for example SiGe.

5

Electronic structures or devices are provided in layer 16. Figure 1B shows a transistor comprising a source 18, drain 20 and gate 22. The transistor is shown by way of example only and layer 16 could comprise more complicated electronic devices. The electronic structure
10 may also comprise very simple devices such as resistors which can for example heat an electro-optical device in the final hybrid device.

A dielectric layer 22 can be deposited onto first device 10 with the electronic structures therein (figure 1C). The dielectric material can
15 be SiO_2, Si_3N_4, Al_2O_3, $LiNbO_3$, diamond or any other dielectric material such as of the high-K type. Any deposition process can be used, for example of the CVD type. Alternatively a plurality of dielectric layers is formed. Such layers may form part of the device itself (they form for example one or more waveguides) or they may combine different
20 properties; for example one layer is a thermal barrier, and another one is a diffusion barrier.

The surface of the SOI device 10 or the surface of the dielectric layer 22 can be planarised, for example by using MCP (mechanical -
25 chemical polishing) methods. The surface may be activated using an RCA (surface activation) - like process or plasma activation.

A second device 24 or wafer is also provided, as illustrated on figure 1D. It can be an electro-optical or a thermo-optical device or
30 even another electronic device, for example another device as the first one, in particular of the SOI type. Both first and second devices 10, 24 have to be attached to each other.

In order to perform said attachment the two parts 10 and 24
35 are precisely aligned with respect to each other. The firms Karl Suss or EVG provide equipments which allow a precision of +/- 1 µm.

Then, they are assembled by a wafer-bonding technique or by adherent contact, for example by molecular adhesion. According to the material, a normal or a high temperature, and a low or a high pressure are used. With regard to these techniques, see Q.Y. Tong and
5 U.Gösele "Semiconductor wafer bonding" (Science and Technology), Wiley Interscience Publications. A low temperature process will be preferred for hybrid devices having a large mismatch between both coefficients of thermal expansion. Another example of bonding method is anodic bonding, performed under an electrostatic field with a glass
10 interface from which alcaline elements migrate. Still another example is eutectic bonding. ***(Ces deux exemples sont ils décrits dans Tong et Gösele?)***. The resulting assembled device is shown in figure 1E.

15 Substrate 12 is then thinned or a portion of the substrate 12 is then detached so as to obtain the device shown in figure 1F in which a thin layer 12' of the substrate 12 is still present. Thinning can be made by chemical etch-back grinding or by mechanical methods such as polishing. Oxide layer 14 is used as a stopper.

20

In a further step, the rest 12' of the substrate 12 is removed in a finishing step, which is for example a further polishing step. Contacts 26 can be provided by using methods such as for example etching (with help of a photo-resist mask) and subsequent deposition of a
25 conducting material (figure 1G). A power source can be connected to the device through said contacts 26.

Thereby, the hybrid device 28 shown in figure 1G is obtained. As can be clearly seen, the electronic structures present in layer 16 are
30 placed very close to electro-optical or thermo-optical device 24. They are separated only by the small dielectric layer 22 when said layer is present. A hybrid device is thus formed, avoiding flip-chip or wire bonding.

35 Alternatively or in addition to contacts 26, side contacts can be provided.

In another variant, surface roughness of both substrate 12 and layer 14 is controlled so that a weak bonding results at the interface between both. A weak bonding at said interface may also result from a controlled bonding energy. A simple mechanical treatment at the step illustrated on figure 1e results in a simple debonding step. Such a weak bonding may also be made at the interface between layers 14 and 16 or within layer 14 itself.

In the above example, first device or wafer 10 is of the SOI type or of the semiconductor on insulator type. Alternatively, said first device or wafer 10 could also be a bulk semiconductor wafer, for example an InP, or AsGa or Si bulk substrate or wafer. Electronic structures or devices can be provided therein as already disclosed above in connection with figure 1B. An insulating layer 22 can be formed therein as in figure 1C, and both devices 10 and 24 can then be assembled as on figure 1E. The same thinning methods can then be used as disclosed above in connection with figure 1F or as explained above and contacts can be made as on figure 1G or as already explained above.

Figures 2A to 2G show steps of a method according to another embodiment of the present invention.

These steps are practically the same as those described with respect to figures 1A to 1G. The only difference is that the step of removing the substrate is performed in a different manner.

First device 10' initially comprises a weak layer 30 (figure 2A). Such a weak layer can be produced by implantation of hydrogen or helium as it is described in US patent 5,374,564 and in the article "Why can Smart Cut® change the future of microelectronics ?" by A.J. Auberton Hervé and Michel Bruel in International Journal of High Speed Electronics and Systems, volume 10, number 1 (2000), p.131 to 146.

Alternatively, layer 30 can be a porous layer as described in EP-0 849 788A2 or in the paper by K.Sataguchi et al. "ELTRAN by splitting porous Si Layers", Proceedings of the 9th Int. Symp. On Silicon-on-Insulator Tech. And Devices, 99 –3, The Electrochemical Society, Seattle, p.117 – 121, 1999.

Due to the presence of weak layer 30, substrate 12 can be easily removed (at least most of it) by using the Smart-Cut splitting technique such as described in the above-mentioned article by A.J.Auberton-Hervé et al.

One therefore obtains a rest portion or layer 12'. Finally a hybrid device 28' is obtained which is very similar to that shown in figure 1G.

The electronic devices in the semiconductor structure need not necessarily be provided in a single semiconductor layer 16. Rather, a plurality of such layers can be provided in the initial first, semiconductor device. In other words, in a variant, other layers of semiconductor material, possibly including further semiconductor devices, may be added on top of layer 16, for example by adding further semiconductor layers as illustrated on figure 3A. On this figure a semiconductor device 10" comprises a silicon substrate 12, a first insulating layer 14, a layer 16 of mono-crystalline silicon with electronic devices therein, a second insulating layer 32, a second layer 34 of mono-crystalline silicon with electronic devices therein, a third insulating layer 36 and a third layer 38 of mono-crystalline silicone with electronic devices therein. Several layers of semiconductor material can also be stacked without any insulating layer 14, 32, 36 between each other.

As an example, the initial device 10" shown in figure 3A comprises three layers which include electronic structures and/or devices connected via wirings 40.

The device 42 shown in figure 3A is assembled with a second device 24 as shown on figure 3B. Said second device is for example an electronic device, for example of the SOI type, or an electro-optical or

a thermo-optical device. Assembling is performed in the same manner as described with respect to figures 1C to 1E, and one obtains a combined device which is shown in figure 3C. Thereafter, the substrate 12 is removed in a manner analogous to that described with respect to
5 figures 1E and 1F. Alternatively, a weak layer can be initially provided in substrate 42 and the removal can be performed in a manner analogous to that described with respect to figures 2E and 2F.

Once again, in the finishing step, the rests of the substrate 12
10 are removed, and wirings 42 are provided in a manner similar to that described with respect to figure 1G. The resulting hybrid device 44 comprises a second device 24 onto which an alternating structure of mono-crystalline semiconductor layers with electronic structures and/or devices and dielectric layers is placed or onto which a plurality of
15 crystalline semiconductor layers with electronic structures and/or devices is placed. The resulting hybrid device 44 is very compact and highly integrated.

Figure 4A to figure 4G show the method according to another
20 embodiment of the present invention. Most of the steps are very similar to those described with respect to figures 1A to 1G. One starts with a semiconductor device 10 similar to device 10 of figure 1A, for example a silicon on insulator device (figure 4A). An electronic device 46 such as a transistor or electrodes or heaters is/are made by using
25 techniques such as successive steps of etching and/or use of photo-resists, and/or deposition of wirings. Finally a dielectric layer 48 is formed thereon. The device shown in figure 4C is assembled with an optical wave-guide device 50 comprising a substrate 52 made of silicon or of any other type of semiconductor material or of an oxyde such as
30 silicon dioxyde, and further comprising an optical wave-guide 54 and possibly a semiconductor top layer 56. The two devices shown on figure 4C and figure 4D are assembled in a manner analogous to that described with respect to figures 1C and 1D, and one obtains the device shown in figure 4E. Thereafter, a portion of the semiconductor
35 substrate 12 or the whole substrate 12 is removed such as to obtain

the device shown on figure 4F. After the finishing step and etching of contacts 58, the device 60 shown on figure 4G is obtained.

As it is clearly visible, the optical wave-guide 54 is placed very
5 close to the electronic device 46, and the behaviour of the optical wave-guide can be controlled by sending control signals via the wirings 58.

The above description relates to the use of silicon as semi-
10 conductor material. Other semiconductor materials (for example SiGe, SiC, AsGa, InP, GaN) can be used instead of silicon, and other semiconductor materials than silicon can be used as substrate 12.

As already mentionned above in connection with figures 1A –
15 1G, other structures can be used instead of the SOI structure disclosed on figures 1A, 2A, 3A, 4A. For example, a bulk semiconductor substrate could be used, the semiconductor material being for example chosen among InP, AsGa or Si. All other steps, like the formation of electronic structures or devices therein, and of an insulating layer on
20 top of said substrate, the assembly with a second device, the thinning step and the formation of contacts can be performed in the same way as disclosed above in connection with any embodiment or variant.

Claims

1) A method of producing a hybrid device (28, 44, 60),
5 comprising the steps of:

a) providing a first semiconductor device (10) including a semiconductor substrate (12) wherein electronic components (18, 20, 22, 46) are provided in said device,
10

b) providing a second device (24, 50),

c) aligning both devices with respect to each other, wherein the top surfaces of both devices are facing each other,
15

d) assembling both devices,

e) at least partially thinning the substrate (12) of the first semiconductor device (10).
20

2) The method according to claim 1, further comprising the step of depositing a dielectric layer (22, 48) onto at least one of the devices (10;24, 50) prior to the aligning step.

25 3) The method according to claim 2, wherein a dielectric layer is deposited onto both devices (10; 24, 50) prior to the aligning step.

4) The method according to claim 2 or 3, wherein at least
30 one dielectric layer comprises a multi-layer structure.

5) The method according to one of claims 1 to 4, further comprising the steps of planarizing at least one of the devices and/or activating the surface of at least one of the devices prior to the aligning
35 step.

6) The method according to one of the preceding claims, wherein the step of thinning the substrate (12) is performed by chemical etch back grinding or by mechanical polishing.

5 7) The method according to one of claims 1 to 5, wherein the step of thinning the substrate (12) is performed by splitting the substrate (12) along a weak layer (30) thereof.

8) The method according to claim 7, wherein the weak layer 10 (30) is a portion of the substrate (12) into which ions or atoms have been implanted.

9) The method of claim 8, wherein hydrogen ions or helium ions or a mixture of hydrogen and helium ions are implanted.

15

10) The method of claim 7, wherein the weak layer (30) is a layer of porous semiconductor material.

11) The method of any of claims 1 – 10, said first semiconductor 20 device comprising a bulk substrate (12).

12) The method of any of claims 1 – 10, said first semiconductor device further comprising an insulating layer (14) on top of said substrate (12), said insulating layer being covered with at least one 25 semiconductor layer (16; 16, 34, 38) in which said eletronic components are provided.

13) The method of any of claims 1 - 5, said first semiconductor device further comprising an insulating layer (14) on top of said 30 substrate, said insulating layer being covered with at least one semiconductor layer (16; 16, 34, 38), a weak bonding being formed at the interface between said substrate and said insulating layer, or between said insulating layer and said semiconductor layer, or within said insulating layer, the step of at least partially thinning the substrate 35 comprising a debonding step along said interface.

14) The method according to one of the claims 1 - 10, wherein said first device (42) comprises an insulating layer (14), a multi-layer structure on top of said insulating layer, said multi-layer structure including a sequence of insulator (32, 36) layers and/or alternating
5 semiconductor (16, 34, 38) layers with electronic structures therein.

15) The method according to one of claims 12 to 14, wherein said insulating layer (14) is made of a material chosen from silicon nitride, diamond, sapphire, silicone dioxide, hafnium oxide, zirconium
10 oxide, alumina, lanthanum oxide and yttrium oxide.

16) The method according to one of the preceding claims, wherein said substrate (12) comprises silicon or SiGe or SiC or AsGa or InP or GaN as a semiconductor material.
15

17) The method according to one of the preceding claims, wherein said second device (24, 50) is an electro-optical or a thermo-optical device.

20 18) The method according to one of claims 1 - 16, wherein said second device (24, 50) is an electronic device.

19) The method according to claim 18, wherein said second device comprises a semiconductor substrate, with an insulating layer
25 on top thereof which is covered with at least one semiconductor layer (16; 16, 34, 38), wherein in the semiconductor layer, electronic components (18, 20, 22, 46) are provided.

20) The method according to any of claims 1 – 16 wherein said
30 second device (24, 50) comprises at least one optical wave-guide (54), and/or at least one photodiode, and/or at least one laser, for example a vertical cavity surface emitting laser, and/or at least one liquid crystal display device.

35 21) The method according to any of claims 1 to 20, wherein both devices are assembled by direct-bonding.

22) The method according to any of claims 1 to 20, wherein both devices are assembled by anodic bonding.

5 23) A hybrid device (28, 44, 60) comprising:

- a first device comprising an optical and/or an electro-optical and/or a thermo-optical device and
- a second device comprising a layered semiconductor
10 structure bonded on said first device.

24) A hybrid device according to claim 23, wherein said first device (24, 50) comprises at least one optical wave-guide (54), and/or at least one photodiode, and/or at least one laser, for example a
15 vertical cavity surface emitting laser, and/or at least one liquid crystal display device.

25) A hybrid device comprising a first semiconductor device and a second semiconductor device bonded on said first device, each
20 comprising a layered semiconductor structure.

26) The hybrid device according to claim 25, wherein said first semiconductor device comprises at least one semiconductor layer having electronic structures and/or electronic devices therein.
25

27) The hybrid device according to any of claims 23 - 26, wherein said second semiconductor structure comprises at least one semiconductor layer (16) having electronic structures and/or devices (18, 22, 46) therein.
30

28) The hybrid device according to any of claims 23 to 27, wherein said first and second devices are bonded together via a dielectric layer (22, 48).

29) The hybrid device according to any of claims 23 to 28, wherein said semiconductor structure further comprises an insulating or a dielectric layer (14) over said semiconductor layer.

5 30) The hybrid device according to one of the claims 23 to 29, wherein said layered semiconductor structure comprises a control portion which is adapted to control a functional portion provided in the first device.

10 31) The hybrid device according to one of the claims 23 to 30, wherein said first and second devices are bonded together by molecular adhesion.

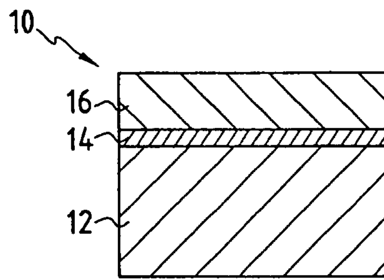

FIG.1A

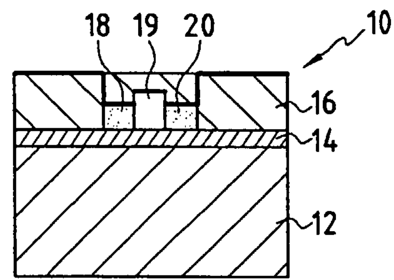

FIG.1B

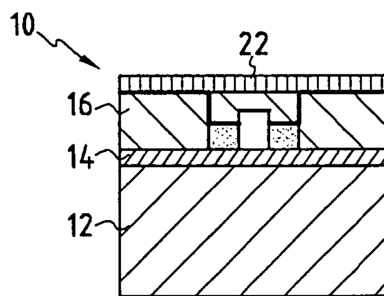

FIG.1C

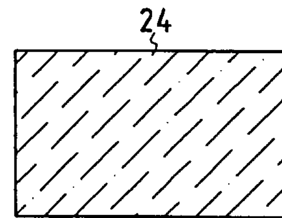

FIG.1D

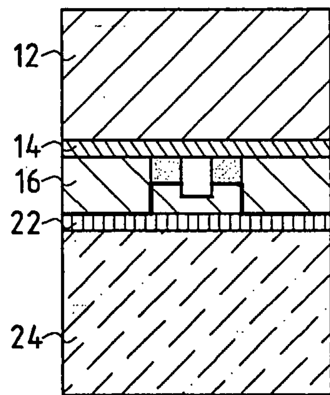

FIG.1E

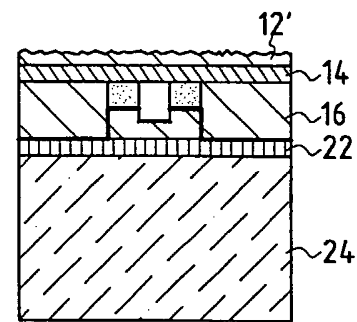

FIG.1F

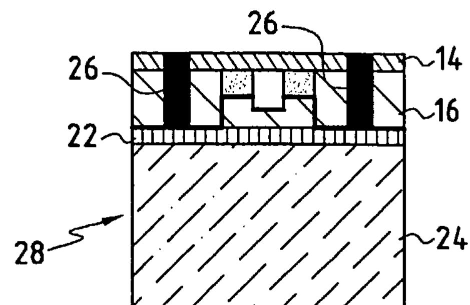

FIG.1G

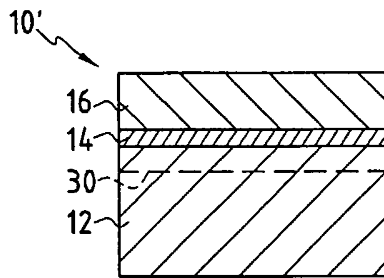

FIG.2A

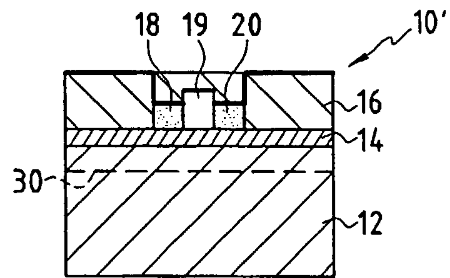

FIG.2B

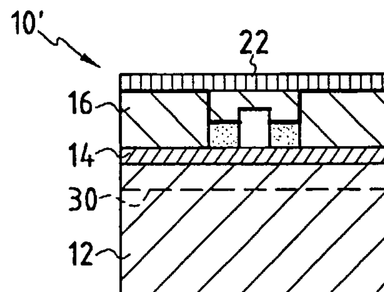

FIG.2C

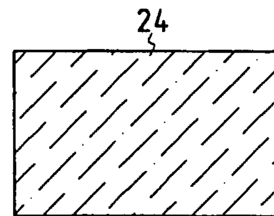

FIG.2D

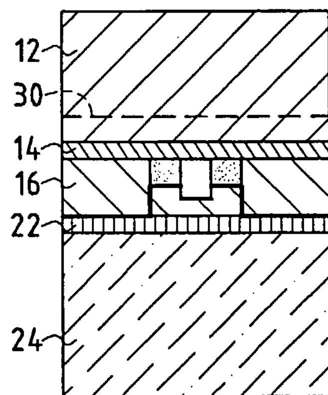

FIG.2E

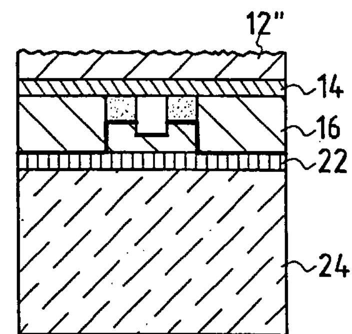

FIG.2F

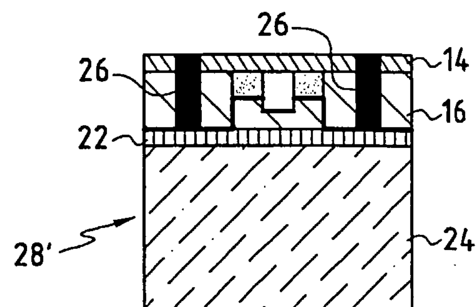

FIG.2G

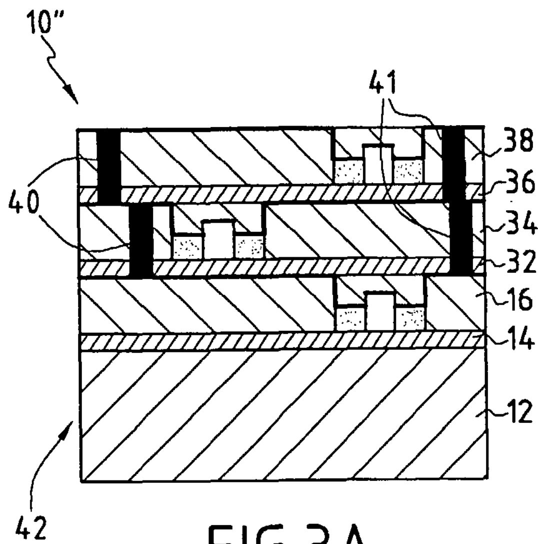

FIG.3A

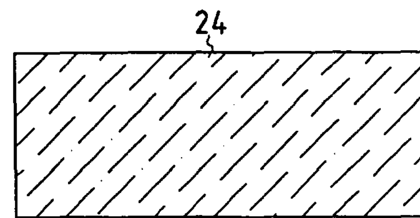

FIG.3B

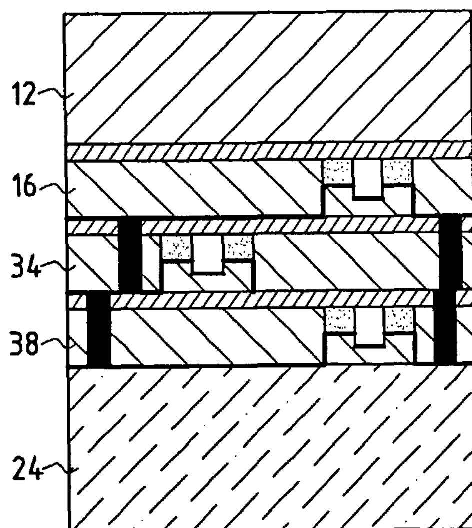

FIG.3C

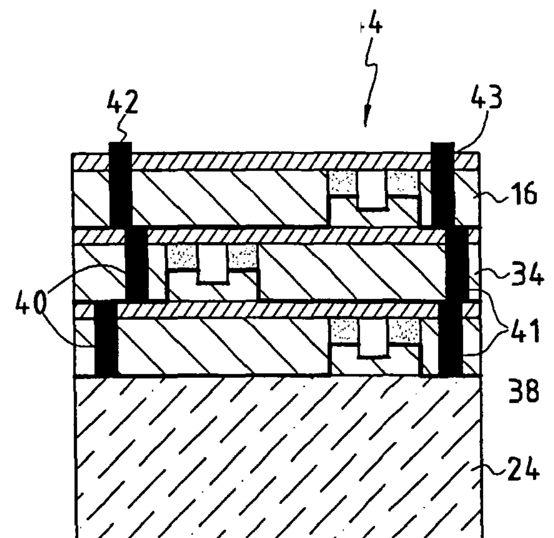

FIG.3D

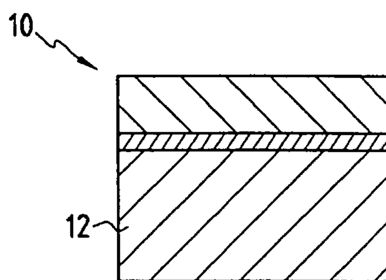

FIG.4A

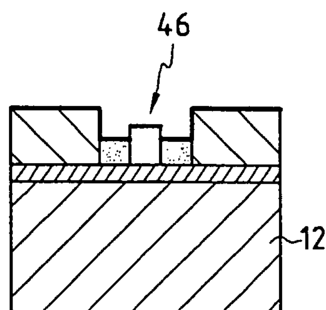

FIG.4B

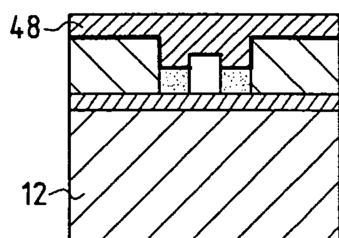

FIG.4C

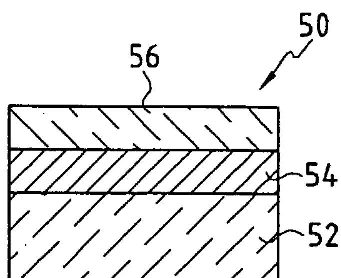

FIG.4D

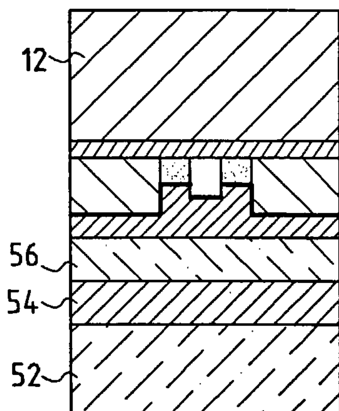

FIG.4E

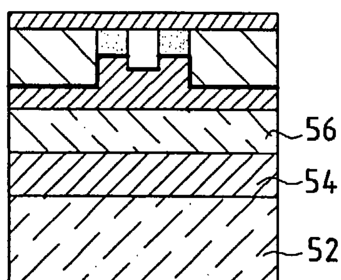

FIG.4F

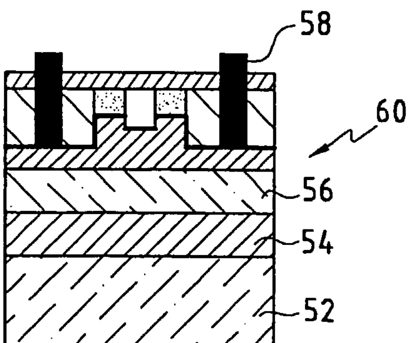

FIG.4G

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 03/04696

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 01 06546 A (MASSACHUSETTS INST TECHNOLOGY) 25 January 2001 (2001-01-25)	1-6,11, 12,14, 16-31
A	abstract; figures 1-4 page 2, line 30 -page 5, line 5 page 6, line 27 -page 21, line 28 page 24, line 13 - line 15 claims 1-27 ---	7-10,13, 15

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Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
6 October 2003	10/10/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Favre, P

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 03/04696

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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A	abstract; figures 5,6,10	3-5, 8-10,13, 19,22,31
	column 2, line 57 -column 4, line 57 column 6, line 39 -column 7, line 21 column 10, line 29 -column 12, line 57 claims 1-15 ---	
X	US 5 578 162 A (D ASARO LUCIAN A ET AL) 26 November 1996 (1996-11-26)	1,2,6, 11, 16-18, 20,21, 23-28,30
A	abstract; figures 2,3	3-5, 7-10,22, 31
	column 1, line 60 -column 2, line 12 column 3, line 6 -column 4, line 25 column 7, line 19 -column 8, line 41 claims 1-4,7-10,12-19 ---	
X	EP 0 785 580 A (MOTOROLA INC) 23 July 1997 (1997-07-23)	23-28,30
A	abstract; figure 4	1-22,29, 31
	column 3, line 19 -column 4, line 30 claims 1,4-6,8 ---	
X	US 5 760 479 A (YANG JAU-YUANN ET AL) 2 June 1998 (1998-06-02)	23-28,30
A	abstract; figure 5	1-22,29, 31
	column 2, line 7 - line 52 table 1 claims 1,2,9 ---	
A	US 5 374 564 A (BRUEL MICHEL) 20 December 1994 (1994-12-20) abstract; figures 1-4 column 2, line 6 -column 4, line 50 claim 1 ---	1,7-9
A	US 6 534 382 B1 (NISHIDA SHOJI ET AL) 18 March 2003 (2003-03-18) abstract; figure 4 column 8, line 1 - line 60 claims 1,5 -----	1,7,10

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