PATENT SPECIFICATION (11) 1 565 918

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(21) Application No. 395/78 (22) Filed 5 Jan. 1978
(31) Convention Application No. 2441385
(32) Filed 6 Jan. 1977
(31) Convention Application No. 2537101
(32) Filed 1 Nov. 1977
(31) Convention Application No. 2537006
(32) Filed 11 Nov. 1977 in
(33) Soviet Union (SU)
(44) Complete Specification published 23 April 1980
(51) INT CL³ H01L 27/04
(52) Index at acceptance
H1K 11A3A 11C4 11D 1AA2 1CB 4C1R 9E GAK

(19)

(54) IMPROVED INTEGRATED INJECTION CIRCUIT DEVICES

(71) We, ARTASHES RUBENOVICH NAZARIAN, of ploschad Junosti, 3, kv.16, Moscow, USSR., VYACHESLAV YAKOVLEWICH KREMLEV, of 103482 korpus 423, kv.81, Moscow, USSR., VILYAM NIKOLAEVICH KOKIN, of 103498, korpus 441, kv.115, Moscow, USSR., VIKTOR IVANOVICH SLADKOV, of Berezovaya alleya, 6, kv.77, Moscow, USSR., BORIS VALENTINOVICH VENKOV, of 103460, korpus 206, kv.46, Moscow, USSR, VADIM VALERIEVICH LAVROV, of Moskovskoi oblasti, ulitsa 8 Marta, 7, kv. 125, Khimki, USSR., all USSR citizens, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to micro-electronics technology and in particular to large-scale integrated injection circuits intended primarily for digital computers.

According to the invention there is provided an integrated injection device which comprises a constant current device and a normally cut-off n-channel field-effect transistor having a gate including at least one non-injecting rectifying contact connected to the constant current device and to an input electrode of the device, its source grounded and its drain connected to an output electrode of the device, wherein said field effect transistor is cut off when the, or one of, or all of said at least one contact is at a potential close to ground potential.

In order to increase the number of possible functional applications of the device a preferred embodiment comprises a field-effect transistor having two non-injecting contacts and an additional, complementary input electrode, the second said contact being connected to said complementary input electrode.

In order to increase the packing density it is preferred that the device comprises a constant current device formed by a bipolar transistor having a metal collector which is combined with a gate of the field-effect transistor.

Preferably the constant current device is a planar bipolar transistor provided with metal gate electrodes located on a masking dielectric layer, the gate zones of the field-effect transistor are located on the surface of the substrate and are arranged as interconnection sections located on unmasked substrate surface areas and protected with a dielectric layer from above, the drain electrode being partly located above said dielectric layer and extending therethrough to form an ohmic contact with the substrate at the area which is overlapped by space charge areas of the rectifying contacts of the gate zones.

In order to simplify the production procedure a preferred embodiment of the integrated circuit comprises a substrate wherein a complementary zone is provided at a distance from the surface which does not exceed the thickness of the space charge layer produced by the non-injecting rectifying contact of the gate zone, the conductivity of the complementary zone being opposite to that of the substrate, while this zone overlaps completely the ohmic contact between the drain zone and the substrate.

The invention will be better understood from the following description of its embodiments given by way of example with reference to the accompanying drawings in which:

Figure 1 presents a circuit diagram of an integrated injection circuit, according to the

invention, which performs the functions of a NOR gate;

Figurea 2 presents a diagrammatic plan of the semiconductor structure forming the integrated injection circuit shown in Figure 1;

Figure 3 presents a diagrammatic cross section of the semiconductor structure shown in Figure 2;

Figure 4 presents a diagrammatiac plan of a semiconductor structure, according to the invention, performing the functions of a double-input gate and including a constant current device made as a bipolar transistor having a metal collector which is combined with the gate of the field-effect transistor;

Figure 5 presents a diagrammatic cross section of the planar semiconductor structure of Figure 4 arranged as a field-effect transistor with gate zones made as interconnection sections; and

Figure 6 presents a diagrammatic cross section of a semiconductor structure according to the invention and performing the functions of a field-effect transistor which is provided with a complementary zone with the conductivity opposite to that of the substrate.

Figure 1 is a circuit diagram of one embodiment of the integrated circuit of the present invention which performs the functions of a logical gate.

The logical gate comprises a constant current device including a bipolar transistor 1 having its emitter 2 connected to an electrode 3 for connection to a current supply (not shown in Figure 1), its base 4 connected to a ground electrode 5 and its collectors 6 and 6′ connected to respective input electrodes 7 and 7′ of the logical gate. In addition, the gate comprises a normally cut-off n-channel field-effect transistor 8 having a source zone 9 connected to the ground electrode 5, a drain zone 10 connected to an output electrode 11 and gate zones 12 and 12′ made as non-injecting rectifying contacts which are connected to the respective input electrodes 7 and 7′ of the logical gate.

Figure 2 shows an unscaled diagram of the semiconductor structure of the logical gate shown in Figure 1.

The notations used in Figure 2 to denote major components of the circuit are the same as those used in Figure 1. The current generator, comprising bipolar transistor 1, and the field-effect transistor 8 are formed on the same n-type semiconductor substrate 13, the base zone 4 of the transistor 1 and the source zone 9 of the n-channel field-effect transitor 8 being combined.

Figure 3 shows the same semiconductor structure as shown in Figure 2, the notations to denote major components of the circuit are also the same. The drain zone 10 of the field-effect transistor 8 is located between the non-injecting rectifying contacts of the gate zones 12 and 12′, dashed lines indicate the boundaries of space charge layers of the rectifying contacts between the zones 12 and 12′ and the substrate 13.

Figure 4 shows a diagrammatic plan of a semiconductor structure performing the functions of a double-input logical gate which comprises a constant current device formed by a bipolar transistor with metal collectors unitary with the respective gates of the field-effect transistor. In the structure of Figure 4 the metal collectors 6 and 6′ of the bipolar transistor 1 are unitary with the gate zones 12 and 12′, formed as metal-semiconductor junctions of the Schottky-diode type.

The present structure makes is possible to increase the packing density due to the fact that the zones 6, 6′ and 12, 12′ are unitary, and hence there is no need to provide interconnections between the collectors 6, 6′ and the gate zones 12 and 12′. It should be pointed out that this zone combination becomes feasible because the constant current device comprises a bipolar transistor with a metal collector.

Figure 5 shows a schematic sectional view of a planar semiconductor structure which is suitable to form the normally cut-off n-channel field-effect transistor 8 which is an element of the logical gate integrated circuit as shown in the form of a circuit diagram in Figure 1. The remainder of the circuit is made just as shown in Figure 4.

The proposed design of the integrated circuit having a field-effect transistor of which the gate zones are made as non-injecting contacts allows the gate zones 12 and 12′ to be formed by portions of metal layers 14 located on such areas of the substrate 13 that are not protected by a masking dielectric layer 15. This arrangement makes it possible to fabricate the gate zones 12 and 12′ simultaneously with the first layer of integrated circuit interconnections. The fact that the drain electrode 10 is located partly above and extends through the dielectric layer 16 which protects the interconnections 14, to form an ohmic contact with the substrate at 18 allows the drain electrode 10 to be fabricated simultaneously with the second layer of integrated circuit interconnections (not shown in Figure 5).

Figure 6 shows a diagram of another embodiment of the semiconductor structure performing the functions of the field-effect transistor which forms an element of the integrated circuit structure of the invention. The structure differs from that described above and shown in Figure 5 in that it is provided with a complementary zone 17 located in the substrate 13 at a distance "a"

from the surface, the distance "a" being less than the thickness of the space-charge layer generated by the non-injecting rectifying contact of the gate zone 12. The conductivity type of the zone 17 is opposite to that of the substrate 13. In this case the zone 17 has p-type conductivity and is located so that it overlaps completely the ohmic contact 18 between the drain zone and the substrate 13. The introduction of the complementary zone 17 makes it possible to increase the distance between the gate zones 12 and 12' and to simplify the process of fabricating integrated circuits of this type since the requirements for the photomask used to form gate zones become less stringent.

The integrated injection circuit (a logical gate) described herein operates as follows. The emitter zone 2 of the bipolar transistor 1 injects holes into the base zone 4. These holes serve as minority carriers for the zone 4. The charge carriers are collected in the zones 6 and 6'. Depending on the voltage across the input electrodes 7 and 7' the logical gate will occupy one of the following states.

If there is a low, close to the "ground", voltage appled to both input electrodes 7 and 7', the charge carriers collected at the junctions of the zones 6 and 6' and constituting the current provided by the constant current device will "leak off" to "ground". In this case the output electrode 11 has no direct-current coupling with the "ground" electrode 5. Now, if the gate is loaded with a similar device (not shown in Figure 1) the electrode 11 will bear a high voltage equal in magnitude to that which opens the junction between the zones 12, 12' and 9.

This direct-current coupling will be broken in case the section of the substrate 13 located between the electrodes 11 and 5 is overlapped by the space charge layers of the closed junctions between the zones 12, 12' and 9 (the space charge layers are indicated with dashed lines in Figure 3).

In case the input electrodes 7 and 7' are fed with a high voltage exceeding that required to unlock the junctions between zones 12, 12' and 9 a direct-current coupling will appear between the electrodes 11 and 5 while the voltage at the output of the logical gate will drop to a level close to that of the "ground" electrode 5. This direct-current coupling is ensured by reducing the size of the space charge zone of the junctions between the zones 12, 12' and 9 in case the voltage across the input electrodes 7 and 7' becomes higher.

If one of the electrodes 7 or 7' is fed with a low voltage there are two alternatively possible results. The first result will occur when the resistivity of the zone 10 and the distance L between the zones 12 and 12' (Figure 2) are selected so that the width of the space charge layer of the junction between each of the zones 12, 12' and the zone 9 is greater than or equal to, the distance L. The second result will occur when the width of the space charge layer of this junction is less than the distance L. In the first case there will be no direct-current coupling between the electrode 11 and the "ground" electrode 5 so that a NOR action is obtained. In the second case the direct current coupling is interrupted only when both electrodes 7 and 11 are at a low voltages, so that a NAND action is obtained.

Hence, the logical gate described herein can perform NOR and NAND logical functions depending upon its constructional parameters and topology (the magnitude of L and the resistivity of the zone 10).

The speed of the logical gate is high due to the use of non-injecting rectifying contacts (metal-semiconductor junctions) which serve as the gate zones 12 and 12' and as the collector zones 6 and 6'. Since there is no injection of minority charge carriers from the gate zones 12 and 12' there will be no excess charge in the zone 13. Hence, when the logical gate switches over from the open state into the closed state the duration of the transients will be sharply reduced as compared with devices using injecting contacts.

The operation of the integrated circuit provided with field-effect transistor as shown in Figure 6 is as follows. The complementary zone 17 prevents current from flowing from the output electrode 11 to the source zone 9 in the direction orthogonal to the surface of the integrated circuit and makes it flow along a trajectory parallel to this surface. When a low voltage is applied to the gate zones 12 and 12' the space charge layer will block the current path since the complementary zone 17 completely overlaps the ohmic contact of the drain zone 10. The zone 17 can be either connected to "ground" or fed with a bias voltage form an additional power supply.

The integrated circuit described herein is easy to produce and can be manufactured with the use of planar technology with or without resorting to epitaxial films.

A broad field of functional applications and a high speed of operation make the integrated circuit proposed herein quite useful in the design of large-scale integrated devices having a high packing density of components on the chip.

WHAT WE CLAIM IS:

1. An integrated injection device which comprises a constant current device and n-channel field-effect transistor having a gate

including at least one non-injecting rectifying contact connected to the constant current device and to an input electrode of the device, its source grounded and its drain connected to an output electrode of the device, wherein said field effect transistor is cut off when the or one of or all of said non-injecting rectifying contacts is at a potential close to ground potential.

2. An integrated injection device as claimed in claim 1, wherein the field-effect transistor comprises two non-injecting contacts and has an additional complementary input electrode, the second contact being connected to said complementary input electrode.

3. An integrated injection device as claimed in claim 1 or 2, wherein the constant current device is a bipolar transistor having a metal collector which is combined with a gate of said field-effect transistor.

4. An integrated injection device as claimed in claim 1 or 2, wherein the constant current device is a planar bipolar transistor provided with metal gate electrodes located on a masking dielectric layer, the gate zones of the field-effect transistor are located on the surface of the substrate and are arranged as interconnection sections located on unmasked substrate surface areas and protected with a dielectric layer from above, the drain zone being located partly above said dielectric layer and extending therethrough to form an ohmic contact with the substrate at the area which is overlapped by space charge areas of the rectifying contacts of the gate zones.

5. An integrated injection device as claim in claim 4, wherein the substrate is provided with a complementary zone of the conductivity type opposite to that of the substrate, the complementary zone being located at a distance from the surface which does not exceed the thickness of the space charge layer of the non-injecting gate-source rectifying contact and being arranged so as to overlap completely the ohmic contact between the drain zone and the substrate.

6. An integrated injection device substantially as hereinbefore described with reference to the accompanying drawings.

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Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1980
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

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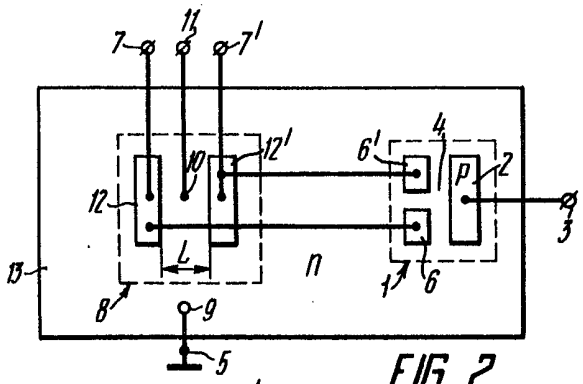

FIG. 2

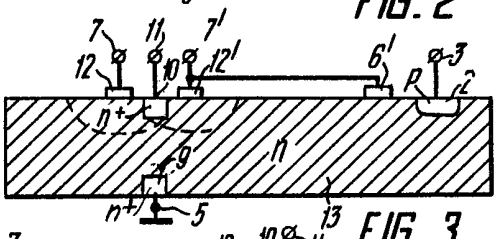

FIG. 3

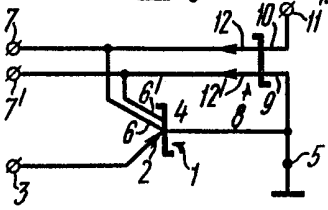

FIG. 1

1565918 COMPLETE SPECIFICATION
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Sheet 2

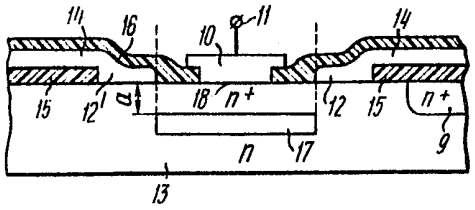

FIG. 6

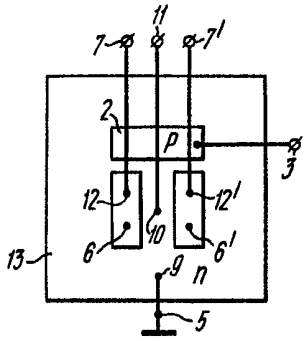

FIG. 4

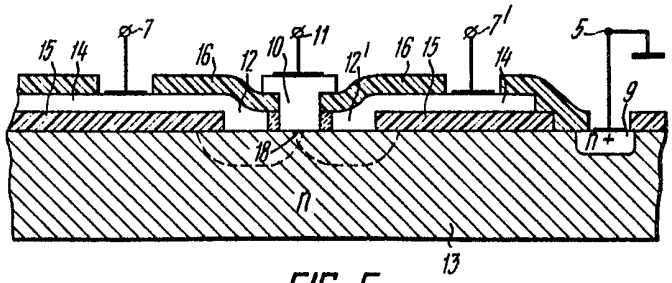

FIG. 5