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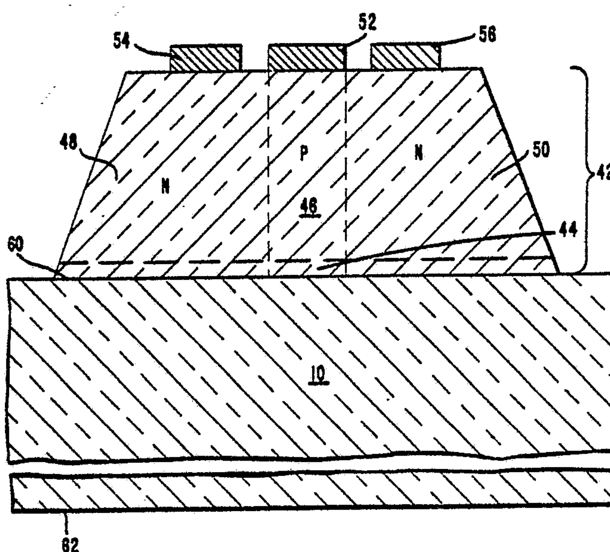
(54) Title: SOLID PHASE EPITAXY AND REGROWTH PROCESS WITH CONTROLLED DEFECT DENSITY PROFILING FOR HETEROEPITAXIAL SEMICONDUCTOR ON INSULATOR COMPOSITE SUBSTRATES

(57) Abstract

Method of fabricating a semiconductor on insulator composite substrate comprised of a semiconductor layer adjacent an insulator substrate, the defect density profile of the semiconductor layer being low and relatively uniform, a relatively thin region of the semiconductor layer at the semiconductor/insulator interface having a substantially greater defect density. The method comprises the steps of depositing the semiconductor layer (12a) adjacent the insulator substrate (10), amorphizing a buried portion (14) of the semiconductor layer without damaging the insulator substrate such as to release contaminants into the semiconductor layer, recrystallizing the amorphous portion of the semiconductor or layer, removing a portion of the semiconductor layer so as to expose the recrystallized layer (38) and depositing an additional semiconductor layer (40) of the recrystallized layer to provide an essentially defect free semiconductor layer of any desired thickness. The provision of semiconductor layers formed by either appropriately selecting the depth within the semiconductor layer at which the amorphization occurs and the width of the amorphized region or permitting self-annealing to occur during the amorphization, or both, having a desired high defect density and interposed between the recrystallized layer and the insulator substrate are also disclosed.



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SOLID PHASE EPITAXY AND REGROWTH PROCESS WITH CONTROLLED DEFECT DENSITY PROFILING FOR HETEROEPITAXIAL SEMICONDUCTOR ON INSULATOR COMPOSITE SUBSTRATES

1 ## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to the fabrication of semiconductor-on-insulator composite
5 substrates, such as silicon-on-sapphire (SOS), and, more particularly, to a process of forming a substantially monocrystalline silicon epitaxial layer having a highly controlled defect density profile and containing an extremely low concentration of substrate-
10 originated contaminants, such as aluminum when a sapphire substrate is utilized.

2. Description of the Prior Art

The advantages of utilizing a composite substrate comprised of a monocrystalline semiconductor layer,
15 such as silicon, epitaxially deposited on a supporting insulative substrate are well recognized. These advantages include the substantial reduction of parasitic capacitance between charged active regions and the substrate and the effective elimination of leakage
20 currents flowing between adjacent active devices. This is accomplished by employing as the substrate an insulative material with a high dielectric constant, such as sapphire (Al_2O_3), and providing that the conduction path of any interdevice leakage current must
25 pass through the substrate.

1 At present, all previous attempts to practically realize an "ideal" silicon-on-insulator composite substrate have been frustrated by a number of significant problems. The simplest "ideal" composite substrate
5 would include a completely monocrystalline, defect-free silicon layer of sufficient thickness to accommodate the fabrication of active devices therein. The silicon layer would be adjacent a highly insulative supporting substrate and would have a minimum of crystal
10 lattice discontinuities at the silicon/substrate interface. As will be explained in greater detail below, a substantially more complex composite substrate, with the silicon layer containing a particular defect density profile, may actually be preferred over
15 the simple "ideal" composite substrate.

Historically, the first significant problem encountered in attempts to fabricate the ideal composite substrate was the substantial incursion of contaminants into an epitaxially deposited silicon layer. In par-
20 ticular, substantial concentrations of aluminum contaminants were found throughout the silicon epitaxial layer when Al_2O_3 substrates were used. The inherent consequence of a high concentration of aluminum contaminants, effectively acting as acceptor-type impurities
25 in the silicon epitaxial layer, is that there are unacceptably high leakage currents between the source and drain regions of p-channel active devices, such as MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) and MESFETs (MEtal Semiconductor FET). These leakage currents
30 may be of sufficient magnitude that the p-channel active devices may be considered to be always in an "on", or conducting, state.

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1 The incursion of substrate-originated contaminants into the silicon layer was found to be an inherent consequence of high temperature processing steps. Such steps are typically utilized in both the initial 5 epitaxial deposition of the silicon layer and the subsequent annealing of the silicon layer to reduce crystalline defects contained therein. Thus, principally by trial and error, an approximate temperature of 910°C has become recognized as the maximum processing 10 temperature that can be utilized without resulting in the substantial incursion of substrate-originated contaminants into the silicon layer.

By effectively precluding the use of high temperature annealing, a second problem was immediately 15 realized. The crystalline quality of the silicon layer, as epitaxially deposited, was of insufficient quality to permit the fabrication of active devices therein. A process known as solid phase epitaxy (SPE) has been recently reported. See, S. S. Lau et al, "Improvement 20 of Crystalline Quality of Epitaxial Si Layers by Ion Implantation Techniques", Applied Physics Letters, Vol. 34, No. 1, pp. 76-78, January 1, 1979. The SPE process provides a low temperature subprocess for improving the crystallinity of the silicon epitaxial 25 layer of a silicon-on-sapphire composite substrate. The SPE process involves the high energy implantation (typically at 250 keV to 600 keV) of an ion species, such as silicon, into the silicon epitaxial layer at a sufficient dose to create a substantially amorphous 30 silicon layer lying adjacent the silicon/sapphire interface while leaving a substantially crystalline layer at the surface of the original epitaxial layer. The thickness of the silicon epitaxial layer is substantially that intended for the completed silicon-35 on-insulator composite substrate (typicaly 4000 Åor

1 greater). The ion species is implanted through the majority of the epitaxial layer so that the maximum disruption of the silicon crystal lattice is near, but not across, the silicon/sapphire interface to ensure
5 that the amorphous region is adjacent the sapphire substrate. Throughout the ion implantation, the sapphire substrate is maintained at a very low temperature, reported as approximately that of liquid nitrogen (77° K). A single step low temperature (between 500°-575°C) anneal-
10 ing of the composite substrate is then performed to convert the amorphous silicon layer into crystalline silicon. During this regrowth, the remaining crystalline surface portion of the silicon layer effectively acts as a nucleation seed so that the regrown portion of the
15 silicon epitaxial layer has a common crystallographic orientation and is substantially free of crystalline defects.

While the SPE process does significantly improve the crystallinity of the silicon epitaxial layer, as a
20 subprocess in the fabrication of silicon-on-insulator composite substrates, it also facilitates the incursion of insulator-originated contaminants into the silicon epitaxial layer. The contaminant concentration resulting from the use of the SPE process is, unfortunately, suf-
25 ficient to preclude the practical use of integrated circuits fabricated on composite substrates processed with the SPE subprocess. The reasons for the failure of active devices to operate correctly are essentially the same as given above with regard to composite substrates
30 fabricated utilizing high temperature processing steps.

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1 SUMMARY OF THE INVENTION

The general purpose of the present invention, therefore, is to provide a process for fabricating a semiconductor-on-insulator composite substrate wherein 5 the semiconductor layer, such as silicon, has a minimum of crystalline defects and an acceptably low concentration of contaminants while, though not recognized in the prior art, avoiding the problem of damaging the insulator substrate.

10 This purpose is achieved by the present invention through the formation of an initial semiconductor-on-insulator composite substrate typically comprising a thin silicon layer epitaxially deposited on a surface of an insulative substrate so as to have a given defect 15 density at the silicon/insulator interface, the defect density generally decreasing toward the exposed silicon layer surface and away from the silicon/insulator interface, subsequently performing a low energy ion implantation (less than approximately 900 keV) of a given ion 20 species into the silicon epitaxial layer so as to convert a portion of the epitaxial layer into a buried amorphous silicon layer, twice annealing the composite substrate first so that the amorphous layer regrows from an amorphous/crystal silicon interface (at between 500°-900°C) 25 and second, to reduce the crystalline defect density throughout the silicon (at up to approximately 910°C), whereby the regrown crystalline silicon layer is substantially free of defects and, further, is substantially free from insulator-originated contaminants.

30 An advantage of the present invention is that the contamination of the silicon epitaxial layer by contaminants originating from the insulator substrate can be highly controlled such that there is no significant contamination. In the alternative, a desired optimally

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1 small amount of contamination may be allowed to occur, thereby permitting various design parameters, such as radiation hardness, to be chosen without effectively rendering inoperative any active devices fabricated in 5 the silicon epitaxial layer.

Another advantage of the present invention is that the crystalline defect density profile, extending from the exposed silicon epitaxial layer surface to the silicon/insulator substrate interface, can be highly 10 controlled so as to provide for a substantially perfect monocrystalline silicon epitaxial layer. In the alternative, a complex defect profile can be obtained wherein the majority of the silicon epitaxial layer is substantially defect-free and a thin portion of the 15 silicon epitaxial layer immediately adjacent the insulator substrate contains a desired higher density of crystalline defects. This permits a very thin layer, relative to the entire silicon epitaxial layer, having a large number of crystal defects, and consequently 20 charge carrier recombination centers, to be formed at the silicon/insulator substrate interface. The controlled density and placement of these recombination centers permits the optimization of the speed, efficiency, and radiation hardness of active devices 25 fabricated in the silicon epitaxial layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Other attendant advantages of the present invention will become apparent and readily appreciated as the 30 same becomes better understood by reference to the following detailed description when considered in connection with the acompanying drawings, in which like reference numerals designate like parts throughout the figures and wherein:

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1 FIG. 1 is a cross-sectional view of an insulator substrate and a silicon layer epitaxially deposited on the surface thereof;

5 FIG. 2 is a cross-sectional view of the composite substrate shown in FIG. 1 further having a buried amorphous silicon layer formed within the silicon layer;

FIG. 3 is an idealized graph showing the implanted ion density versus the depth below the

10 exposed surface of the silicon layer at which the ions are implanted and further showing the delimiting boundaries of the amorphous layer centered about Rp, one boundary being adjacent the surface of the insulator, the amorphous layer thereby

15 corresponding to that shown in FIG. 2;

FIG. 4 is a cross-sectional view of the composite substrate of FIG. 1 further having an amorphous buried silicon layer formed within the silicon layer, the amorphous layer being

20 spaced apart from the insulator substrate by a relatively thin residual crystalline silicon interface layer;

FIG. 5 is an idealized graph showing the implanted ion density versus the depth beneath

25 the exposed silicon epitaxial layer surface at which the ions are implanted and further showing the delimiting boundaries of the amorphous layer, thereby corresponding to that shown in FIG. 4;

FIG. 6 is a cross-sectional view of the

30 composite substrate shown in FIG. 2 further showing a self-seeding, partially self-annealed layer propagating through a portion of the substantially amorphized buried silicon layer toward the silicon/insulator substrate interface;

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1 FIG. 7 is a cross-sectional view of the composite substrate shown in FIG. 2 further showing the initial anneal/regrowth of the buried amorphous silicon layer utilizing the crystalline
5 silicon surface layer as a nucleation seed for the regrowth;

FIG. 8 is a cross-sectional view of the composite substrate showing the completely regrown buried silicon layer;

10 FIG. 9 is a cross-sectional view of the composite substrate of FIG. 8 after the seed surface crystal silicon layer has been removed leaving the regrown crystalline silicon layer adjacent the insulator substrate;

15 FIG. 10 is a cross-sectional view of the completed composite substrate including a second silicon layer epitaxially deposited on the surface of the regrown crystalline silicon layer; and

FIG. 11 is a cross-sectional view of an
20 idealized active device, such as a MESFET, fabricated on an island portion of the silicon layer, a thin partially annealed or residual damaged silicon interface layer being adjacent the insulator substrate.

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DETAILED DESCRIPTION OF THE INVENTION

The present invention involves a process for providing a monocrystalline semiconductor layer on the surface of an insulator substrate to form a composite
30 substrate that is highly desirable for use in the fabrication of high-speed integrated circuits. The process is inherently adaptable to a wide variety of semiconductor and insulator materials. See, U.S. Patent

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1 No. 3,393,088 (silicon on alpha-aluminum oxide), U.S. Patent No. 3,414,434 (silicon on spinel insulators), U.S. Patent No. 3,475,209 (silicon on chrysoberyl), U.S. Patent No. 3,664,866 (IIb-VIa semiconductor com-
5 pounds on insulator substrates). For the purpose of clarity in the following discussion, essentially intrinsic silicon will be used as an exemplary semiconductor material and sapphire (Al_2O_3) will be used as an exemplary insulator material. Accordingly, the
10 specific embodiments described below are only representative of the many combinations of materials with which the present invention can be practiced.

Referring now to FIG. 1, a silicon layer 12 is shown as having been epitaxially deposited on the
15 surface of the sapphire substrate 10 to form a composite substrate 10, 12. Procedures for preparing the substrate 10 and for performing the epitaxial deposition are known in the art. See, U.S. Patent No. 3,508,962, U.S. Patent No. 3,546,036, and J. C. Bean et al., "Substrate
20 and Doping Effects upon Laser-Induced Epitaxy of Amorphous Silicon", Journal of Applied Physics, Vol. 50, No. 2, pp. 881-885, February 1979. The sapphire substrate 10 is preferably on the order of 10-13 mils in thickness and has a surface crystallographic orientation
25 of within 1° of ($\bar{1}102$) (hexagonal Miller indices notation). This particular crystal orientation is necessary for the subsequent epitaxial growth of a silicon layer having a crystallographic orientation of (100) (cubic Miller indices notation). The desirability of the
30 silicon epitaxial layer 12 having a (100) surface crystallographic orientation will be described in greater detail below.

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1 The first silicon epitaxial layer 12 is deposited on the surface of the sapphire surface 10 preferably by a chemical vapor deposition (CVD) step. The CVD growth of the epitaxial layer 12 is preferably performed by
5 the chemical decomposition of silane (SiH_4) in an appropriate reactor at approximately 910°C, as measured by an incandescent pyrometer (uncorrected). The epitaxial growth is performed so as to achieve a silicon epitaxial layer preferably between 1000-2500 Å in thickness
10 within a growth rate range of approximately 0.3-2.4 μm/min, preferably at a rate of 2.4 μm/min. The minimum film thickness must be sufficient to provide a continuous silicon film having a substantially uniform surface so as to facilitate the further processing of the composite
15 substrate 10, 12. The preferred minimum thickness of 1000 Å has been experimentally determined to correspond to a degree of surface pitting, resulting from defects at the silicon/sapphire interface that originate during the initial stages of the epitaxial deposition, that is
20 sufficiently insignificant to affect the further processing of the composite substrate 10, 12. The preferred maximum thickness of 2500 Å is established for reasons described in greater detail below. The preferred epitaxial growth rate of 2.4 μm/min. is selected over
25 slower growth rates to minimize the defect density in the silicon at the silicon/sapphire interface. Slower growth rates permit a higher concentration of defects, typically of the type referred to as microtwin defects, to form as the initial portion of the silicon
30 layer 12 is epitaxially deposited on the sapphire surface 60.

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1 A secondary reason for the choice of the preferred growth rate is that silicon/sapphire composite substrates fabricated in accordance with all of the above requirements, including a conventional growth
5 rate of 2.4 μm/min., are readily available as a commercial product of the Crystal Products Division of Union Carbide, Inc., 8888 Balboa Ave, San Diego, CA 92123.

Referring now to FIG. 2, a first principle
10 embodiment of the present invention, essentially equivalent to the "ideal" composite substrate, is shown. To provide this structure, an ion species 18 is implanted through the exposed surface of the silicon layer 12a so as to create a buried amorphous silicon layer 14
15 covered by a substantially crystalline silicon layer 16. For a silicon epitaxial layer 12a, the preferred ion species is also silicon so as to preclude the possibility of the undesirable contamination of the surface crystalline silicon layer 16. Other ion species, pre-
20 ferably inert and including argon and neon, may alternately be used.

In order to closely achieve the "ideal" composite substrate, the ion implant energy must be closely controlled so that the amorphous layer 14 lies imme-
25 diately adjacent the sapphire substrate 10. As shown in FIG. 3, there is a statistical distribution of the implanted ions 18 about a central maximum at a distance R_p beneath the exposed surface of the silicon epitaxial layer 12a. Both R_p and the standard deviation
30 of the distribution of implanted ions about R_p, ΔR_p, are dependent on the semiconductor material type and the ion species implanted. R_p and ΔR_p are also directly proportional to the ion implanted energy, both increasing with corresponding increases in the implant energy.

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1 For silicon ions implanted at various energies into a silicon material, as well as many other combinations of common ion species and semiconductor materials, the values of R_p and ΔR_p have been determined and tabulated.
5 See, J. F. Gibbons, W. F. Johnson, S. W. Mylroie, Projected Range Statistics, 2 ed. Halstead Press Stroudfburg 1975. The maximum disruption of the silicon crystal lattice structure naturally occurs at R_p since there is a maximum in the concentration of implanted ions at that
10 depth beneath the exposed surface of the epitaxial layer 12a. However, a sufficient number of ions must be implanted in order to disrupt, and thereby amorphize, a portion of the silicon layer 12a substantially symmetrically distributed around R_p. Naturally, the width of
15 the amorphized layer is substantially dependent on and increases with corresponding increases in the ion dose (ions/unit surface area) when implanted at a given implant energy. Increases in the implant energy widen the implanted distribution of the ions, thereby requiring
20 higher ion doses to maintain or increase the width of the amorphized layer.

In the present invention, the implantation energy and the ion dose of a given ion species are selected so that a substantially, if not completely, amorphous layer
25 14 is created about R_p, extending from approximately $R_p - 1.5\ \Delta R_p$ to $R_p + 1.5\ \Delta R_p$. Implantation energies and ion doses necessary to achieve an amorphous layer 14 width of up to and exceeding approximately 3 ΔR_p, consistant with the present invention, are readily
30 obtainable. For the amorphous layer 14 to lie adjacent the sapphire substrate 10, the thickness of the initial crystalline silicon layer 12 is specified as approximately equal to $R_p + 1.5\ \Delta R_p$.

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1 A key aspect of the present invention, distinct from the prior art, is that the implantation energy and the ion dose are constrained such that they are sufficiently low so as not to exceed the damage density
5 threshold of the sapphire substrate 10. The damage density of a crystalline material is herein defined as the dose of ions penetrating the surface of the crystal times the average energy of the penetrating ions. The damage density threshold for any crystalline
10 insulator material can be determined by a known experimental process. See, M. W. Thompson, "Defects and Radiation Damage in Metals," Cambridge University Press, Cambridge, Mass., 1969. The experimentally determined damage density threshold for sapphire is
15 approximately equal to or greater than 1×10^{15} keV-ions/cm^2, estimated for the sapphire surface 60. The inherent result of exceeding the sapphire damage density threshold during the formation of the amorphous layer 14 is that the near interface 60 region of the
20 sapphire crystal is damaged. This damage is believed to reduce a significant fraction of the sapphire 10 to the highly mobile AlO_2 species. As a consequence of the damaged nature of the interface region between epitaxial silicon layer 12 and the sapphire substrate 10, defect
25 enhanced diffusion, or "gettering", occurs during the present and subsequent processing steps even though performed at low temperatures. The mobile AlO_2 out-diffusion from the sapphire substrate 10 effectively contaminates the entire epitaxial silicon layer 12a.

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1 Consequently, a number of balancing trade-offs between the ion implantation energy, ion dose, and the thickness of the epitaxial layer 12 must be made so that a substantially amorphous layer 14 can be
5 formed adjacent the sapphire substrate 10 without exceeding the damage density threshold of the sapphire 10. For providing an amorphous silicon layer 14 immediately adjacent the sapphire substrate 10 and without significantly exceeding the sapphire damage density threshold,
10 the maximum silicon layer 12a thickness is approximately 2500 Å. The corresponding maximum implantation energy and ion dose are approximately 90 ± 10keV and 2×10^{15} ions/cm^2, respectively, which are substantially less than those prescribed by the prior art.

15 As an example, a composite substrate corresponding to that shown in FIG. 2 can be fabricated utilizing a 2000 Å ± 10% thick epitaxially deposited layer on the surface of an approximately 10 mil thick sapphire substrate. Silicon ions with an energy of approximately
20 55 keV are implanted substantially perpendicular to the exposed surface of the epitaxial silicon surface 12a at a dose rate of approximately 1×10^{12} ions/cm^2-sec until a dose of 1×10^{15} ions/cm^2 has been achieved. This ion implantation is performed while the rear
25 surface of the sapphire substrate 10 is maintained at a constant temperature below approximately -20°C. The reason for the temperature control and its particular magnitude will be discussed in greater detail below.

Referring now to FIG. 4, a second principal
30 embodiment of the present invention is shown. This embodiment differs from that shown in FIG. 2 in that a heavily ion implanted, yet substantial crystalline, residual damaged silicon crystal interface layer 20 is provided at the silicon/sapphire interface 60 and

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1 interposed between a substantially amorphous silicon layer 22 and the sapphire substrate 10. This structure is obtained by the implantation of an ion species 26, such as silicon, into an epitaxially deposited silicon
5 layer 12b. A surface layer 16 portion of the epitaxial layer 12b remains substantially crystalline while the majority of the epitaxial layer 12b is substantially, if not completely, amorphized due to the heavy implantation of ions. The implantation energy and dose are
10 controlled, however, such that the thin residual layer 20 is insufficiently implanted to be amorphized.

The implanted ion density profile, corresponding to the composite substrate shown in FIG. 4, is shown in FIG. 5. The profile is substantially symmetrically
15 centered around a maximum implanted ion density located at depth R_p below the exposed silicon layer 12b surface. With an appropriate implantation dose, the amorphous layer 22 extends from $R_p - 1.5\ \Delta R_p$ to $R_p + 1.5\ \Delta R_p$. The thickness, t, of the epitaxial silicon layer 12b
20 is greater than $R_p + 1.5\ \Delta R_p$. Consequently, there is a thin residual silicon layer 20 that is heavily implanted, and therefore containing a substantial number of crystal defects, effectively interposed between the sapphire substrate 10 and the amorphous silicon layer 22; the
25 layer 20 having a width of approximately $t - R_p + 1.5\ \Delta R_p$. The preferred width of the residual interface layer is approximately 200 ± 100 Å. Naturally, provision of this thin residual damaged interface layer 20 can be achieved by increasing the thickness, t, of the epitaxial
30 silicon layer 12b, decreasing the ion implantation energy to reduce R_p, decreasing the ion dose to reduce the width of the amorphous layer 22, or by any combination of the above.

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1 One particular consequence of providing a residual damaged interface layer 20 at the interface between the epitaxial silicon layer 12b and the sapphire substrate 10 is that the maximum epitaxial layer 12b 5 thickness, implantation energy, and ion dose, as noted above, may all be increased, though slightly, in proportion to the thickness of the residual layer 20. Other consequences will be discussed in greater detail below.

10 A major modification of the structure provided by processing in accordance with either of the two principal embodiments of the present invention described above can be obtained through the use of substrate temperature control. This modification ultimately provides a par- 15 tially annealed damaged silicon crystal interface layer at the silicon/sapphire interface 60. The modification, as applied to the processing of the composite substrate 10, 12 as necessary to provide the first principal embodiment of the present invention, is shown in FIG. 6. 20 An ion species 58, preferably silicon, is ion implanted into a silicon layer 12c epitaxially deposited on the surface of a sapphire substrate 10. Throughout the ion implantation, the rear surface of the sapphire substrate 10 is maintained at a specific, highly controlled 25 temperature. This can be accomplished by mounting the sapphire substrate 10 on a heat sink (not shown). Either a thin film of thermal paste or a thin film of silicon can be utilized to provide a high heat conductivity interface between the heat sink and the sapphire sub- 30 strate 10. The use of thermal paste in this manner is well-known in the art. The use of the silicon heat layer conduction may be preferred, since the thin uniform silicon layer, relative to a thicker, non-uniform film of thermal paste, permits the composite substrate

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1 10, 12c to be more readily and accurately oriented in subsequent processing steps, particularly the ion implantation. Since the silicon layer has a high thermal conductivity coefficient, the silicon heat sink interface 5 layer may be of any convenient thickness. Further, this interface layer can be epitaxially deposited on the rear surface of the sapphire substrate at any convenient time prior to the epitaxial deposition of the silicon layer 12 on the opposing surface of the sapphire 10 substrate 10, since the heat sink interface layer is relatively tolerant of low level contamination.

During the ion implantation, the temperature of the silicon layer 12c rises substantially, relative to the rear surface of the substrate 10, in response 15 to the absorption of the ion implant energy. Due to the thinness of the silicon layer 12c and the inherent high thermal conductivity of silicon, the temperature throughout the silicon layer 12c can be considered essentially uniform. The relatively lower thermal 20 conductivity of the sapphire substrate, along with its much greater relative thickness, results in a substantial thermal gradient (typically 150-200°C) occurring across the sapphire substrate 10, increasing from the rear substrate surface 62 to the silicon/sapphire interface 25 60. The temperature of the silicon layer 12c can be altered by modifying the implantation energy or the ion dose, or both, of the implanted ion species 58 so as to modify the magnitude of the energy provided to the silicon layer 12c. This can be further accom-30 plished by modifying the ion dose rate, thereby changing the rate at which energy is provided to the silicon layer 12c. Alternatively, by adjusting the controlled temperature of the heat sink (not shown) and, correspondingly, the rear surface of the sapphire substrate 10, 35 the temperature of the silicon layer 12c can be altered.

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1 The elevated temperature of the silicon layer 12c permits a partially annealed silicon interface layer to be formed at the silicon/sapphire interface 60. As shown in FIG. 6, a thin self-annealing layer 30, con-
5 taining a large number of crystalline defects, i.e., damaged, forms within the portion of the epitaxial silicon layer 12c that is to be amorphized. During the initial stages of the ion implantation, the maximum disruption of the crystal lattice and the initial,
10 localized heating occur at a depth of R_p beneath the exposed surface of the silicon layer 12c. Provided that the heating is sufficient to raise the temperature of the silicon atoms at a depth of approximately R_p to an average temperature of approximately 150°C or
15 greater, partial annealing of the silicon crystal lattice will occur above and below R_p. The thin self-annealing layer 30 below R_p will effectively propagate toward the silicon/sapphire interface 60. This occurs as the silicon layer 32 below the self-annealing layer
20 30 is increasingly damaged by the implantation of ions to the point of being pseudo-amorphous. The self-annealing layer 30 acts as a nucleation seed for the pseudo-amorphous layer 32 such that the lower boundary of the self-annealing layer 30 effectively grows toward
25 the silicon/sapphire interface 60. The upper boundary of the self-annealing layer 30 also propagates toward the silicon/sapphire interface 60. This regression of the upper boundary is due to the continued implantation of ions symmetrically distributed about R_p, thus
30 continuously disrupting the self-annealing layer 30 particularly at its upper boundary, thereby progressively reamphorizing the partially annealed silicon

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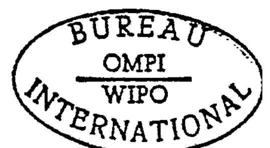

1 crystal. Consequently, the thin self-annealing interface layer 30 propagates through a portion of the eventually buried amorphous layer 14a until it reaches either the silicon/sapphire interface 60 or a substan-
5 tially crystalline layer, such as a residual interface layer 20, and stabilizes at a constant width.

The self-annealing layer formed immediately above R_p is not shown in FIG. 6, since the layer is typically completely re-amorphized prior to reaching the crystal/
10 amorphous silicon interface 64 between the remaining silicon crystal layer 16 and the amorphous silicon layer 28. The complete re-amorphization of this upper annealed layer results from the fact that it receives a greater flux of implanted ions, thereby substantially
15 failing to grow at the rate at which the self-annealing layer is re-amorphized.

The implantation energy, ion dose, ion dose rate, and heat sink temperature must be balanced in order to ensure the formation and proper propagation of the
20 self-annealing silicon interface layer 30. In order to ultimately provide for a partially annealed interface layer 30 adjacent the silicon/sapphire interface 60 having a preferred thickness of 200 ± 100 Å, an ion implantation step performed on a composite substrate
25 10, 12 and otherwise identical to that required for providing the first principal embodiment of the present invention described above, must achieve the preferred conditions (consistant with the example given above) of an implant energy of 55 keV providing an ion dose
30 of 1×10^{15} ions/cm^2 at a rate of 1×10^{12} ions/cm^2-sec while maintaining the heat sink at a constant temperature of approximately 23°C. Thinner, less distinct annealed interface layers may be obtained by decreasing the heat sink temperature until, at an

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1 approximate temperature of -20°C, essentially no annealed interface layer 30 will be realized. Conversely, heat sink temperatures above approximately 250°C will result in no amorphous layer 14b being ultimately formed 5 due to extremely accelerated self-annealing.

Alternately, a second ion implantation step can be performed to provide a partially self-annealed layer 30. Beginning with a composite substrate 10, 12 formed in accordance with either principal embodiment 10 of the present invention, the ion implantation substrate temperature maintained sufficiently low to preclude the formation of any self-annealing layer 30, a second ion implantation is performed utilizing a low mass ion species, such as hydrogen. The implantation energy 15 and ion dose are adjusted so as to provide sufficient localized heating within the amorphous layer 14 (FIG. 2), 22 (FIG. 4) for a substantially uniform layer to partially anneal. Since a low mass ion is used, there is substantially no disruption of the partially annealed 20 layer as it forms, the layer forms and substantially remains at a depth R_p beneath the surface of the silicon layer 12. Thus, the partially annealed layer anywhere within the amorphous layer 14 (FIG. 2), 22 (FIG. 4), though preferably at the silicon/sapphire interface 60 25 (first principal embodiment) or at the interface between the amorphous layer 22 and the residual damaged interface layer 20. However, in all cases, the implantation energy and ion dose must be limited so as not to exceed the damage density threshold of the sapphire substrate 10.

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1 Once the desired ion implantation step has been completed, pursuant to either of the principal embodiments of the present invention and the optional modification thereof as discussed above, the buried amorphous
5 layer is annealed utilizing a two-step heat treatment process. As shown in FIG. 7, the first step is performed at a temperature sufficient for the initial amorphous silicon layer 14b to begin nucleation only at the crystal/amorphous silicon interface 64 (tempera-
10 tures typically in the range of 500° to 900°C). For purposes of clarity, neither a residual damaged layer 20 or partially annealed 30 interface layer is shown in FIGS. 7-8. The use of a common nucleation source is required for the regrowth of the amorphous layer
15 14b to occur such that the resulting silicon crystal has a common crystallographic orientation. Annealing at temperatures sufficient for spontaneous nucleation within the bulk of the amorphous layer 14b are naturally to be avoided. Crystal regrowth progresses through
20 the remaining amorphous silicon layer 36, leaving behind a relatively defect-free crystal silicon layer 34, typically until the regrowth crystal/amorphous silicon interface reaches the silicon/sapphire interface 60. The regrowth crystal layer 34 is substantially
25 defect-free as the intended consequence of the choice of the crystallographic orientation of the initial epitaxial silicon layer 12. Inherent in the epitaxial deposition of a silicon layer onto a sapphire substrate having a $(1\bar{1}02)$ crystallographic orientation is that
30 the silicon growth is in the (100) direction. Thus, the subsequent regrowth of the crystal silicon layer 34 is also essentially in the (100) direction. The silicon/sapphire interface defects, and the residual

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1 defects propagating from the interface defects into the silicon layer 12, however, primarily have a (111) crystallographic orientation. Since defects not having the same crystallographic orientation as the crystal
5 growth inherently propagate at the nucleation regrowth interface, typically at an order of magnitude less than the speed of the crystal regrowth, these defects can be effectively "out-grown". Consequently, as the regrowth interface between the recrystallized silicon
10 layer 34 and the amorphous silicon layer 36 propagates away from the original crystal/amorphous silicon interface 64, the regrown crystal quickly becomes essentially defect-free. Naturally, if either a residual damaged interface layer 20, as provided for by the second
15 principal embodiment of the present invention, or an annealed damaged interface layer 30, as provided by the modification of either of the two principal embodiments of the present invention, or both, are present, then the propagation of the crystal/amorphous silicon
20 interface will halt once those layers are reached. Obviously, only amorphous silicon is recrystallized. The recrystallization anneal requires from 30 min. to 3 hours.

Once recrystallization is complete, a second
25 thermal annealing step is performed. Temperatures of up to approximately 910°C can be used since there is no danger of initiating any random nucleation of any amorphous silicon. Further, since the surface of the sapphire substrate 10 is undamaged, there is no danger
30 of contaminating the silicon layer 16, 38 with substrate originated contaminants. This high temperature anneal is performed for a short period of time, for up to 1 hour, principally to remove any defects that may have occurred at the original crystal/silicon amorphous silicon

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1 interface 64 in the earliest stages of the crystal regrowth. Also, defects in the residual damaged interface layer 20 and the partially annealed interface layer 30, if either is present, are uniformly reduced
5 to a desired density but not completely eliminated. This allows the desired defect density profile to be established.

For the above-given example, the initial annealing step for the recrystallization of the amorphous layer
10 14b is preferably performed at 600°C for three hours in a nitrogen ambient. The second annealing step is preferably performed at a temperature of 850°C for one hour, also in a nitrogen ambient. Naturally, however, neither of the annealing steps should be at a temperature
15 sufficient to result in the thermally induced incursion of aluminum contaminants into the silicon layers.

At this point, the composite substrate comprises of an essentially defect-free crystalline silicon layer 38 interposed between the sapphire substrate 10
20 and the original crystalline layer 16 of the initial epitaxial layer 12, as shown in FIG. 8. Due to the handling of the composite substrate between process steps, a relatively thin contaminant layer 66 may exist at the otherwise exposed surface of the silicon crystal
25 layer 16. This contaminant layer 66 is removed utilizing conventional processing techniques including, preferably, etching the contaminated surface of the composite substrate in a 50-50 mixture, by volume, of H_2SO_4 and HF.

The remaining original crystalline silicon layer
30 16 is then removed to leave a composite substrate consisting of the regrown crystal silicon layer 38 adjacent the sapphire substrate 10, as shown in FIG. 9. Naturally, any annealed interface layer or residual damaged interface layer as provided during the earlier

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1 ion implatation processing, would be interposed between the regrown crystal silicon layer 38 and the sapphire substrate 10. For purposes of clarity, these layers are not shown in FIGS. 9-10.

5 Preferably, the remaining crystalline silicon layer 16 is removed by reactively processing the composite substrate 10, 38, 16, in an H_2 ambient flowing at a rate of 100 liters per minute for approximately two hours while maintaining the system at a temperature

10 of approximately 910°C. By performing this step in a CVD reactor, the next step of epitaxially depositing a silicon layer onto the exposed surface of the regrown silicon crystal layer 38 can be performed without further handling the composite substrate 10, 38.

15 As shown in FIG. 10, an epitaxial layer 40 is deposited on the regrown crystal silicon layer 38 so as to form an essentially uniform silicon layer 42 adjacent the sapphire substrate 10. The second epitaxial silicon layer 40 can be deposited so that the full silicon

20 layer 42 has any desired thickness. Naturally, any conventional method of providing the silicon epitaxial layer 40 can be utilized. However, consistent with the desire not to incur any unnecessary handling of the composite substrate 10, 38, the epitaxial deposition of the

25 silicon layer 40 is preferably accomplished by the chemical decomposition of a silane mixture over the composite substrate 10, 38 in a CVD reactor. Silane introduced into the reactor at a flow rate of 100 sccm (standard cm^3/min), wherein the composite substrate

30 is maintained at 910°C, results in an epitaxial silicon growth rate of approximately 2.4 μm/min. The epitaxial deposition is continued until the desired silicon layer 42 thickness is achieved, preferably around 5000 Å.

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1 At this point, the formation of the composite substrate 10, 42 is essentially complete, the composite substrate 10, 42 being ready for the further fabrication of active devices in the silicon layer 42 thereof. As
5 shown in FIG. 11, this can be accomplished by standard processing steps providing for the ion implantation of source and drain regions 48, 50 (shown as n-type), separated by a gate region 46 (shown as p-type), into the silicon layer 42. Aluminum or refractory metal
10 contacts 52, 54, 56 are provided at the surface of the respective gate 46, source 48, and drain 50 regions, thereby forming, for example, a conventional MESFET. Portions of the silicon layer 42 are etched away so as to expose the sapphire substrate 10 surrounding the
15 active device so as to form an island and, thereby, effectively isolate the device from all other devices fabricated in the silicon layer 42.

Also shown in FIG. 11 is an interface layer 44. This layer 44 may be either a residual damaged interface
20 layer or an annealed interface layer, as provided for during the ion implantation steps described above. The interface layer 44 may also include both an annealed interface layer and a residual damaged interface layer adjacent one another, the residual damaged interface
25 layer being further adjacent the sapphire substrate 10. For reasons discussed in greater detail immediately below, it may be highly desirable to provide either one or both of the interface layers in the completed composite substrate 10, 42.

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1 A first basic reason for including at least one interface layer within the gate region of a FET device, the layer having a high defect density relative to the majority of the gate region material, is to prevent a 5 phenomena known as charge pumping. In the operation of a FET active device, inversion regions within the gate material are periodically induced to switch the device between conducting and non-conducting states. In order for the device to operate successfully at 10 high speeds, two conditions must be met. One is that the charge carriers must have a high mobility through the gate region of the active device so that the initiation of the conducting state is not current-limited. This, in turn, implies that the charge 15 carriers must have long lifetimes between generation and recombination. An inherent quality of an essentially defect-free semiconductor crystalline materials, such as silicon, is that charge carriers therein will exhibit high mobility and, therefore, long lifetimes.

20 The other requirement is that at the conclusion of the conducting state of the active device, the charge carriers within the gate region must quickly recombine. Should the lifetime of charge carriers within the gate region of the active device be comparable to 25 the operating frequency of the device, an accumulation of charge carriers within the gate region will result. This, in turn, will cause the operating parameters of the active device to change dramatically as a function of frequency and, potentially, prevent the device from 30 switching to a nonconducting state. This accumulation of charge carriers within the gate region is typically known as charge pumping.

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1 The provision of a high defect density region within, at least, the gate region of the active device will effectively prevent charge pumping. Defects in the crystal of a semiconductor material effectively
5 decrease both the mobility and lifetime of charge carriers by essentially acting as scattering and recombination centers. By providing that the high density defect region within the gate region occupies only a fraction of the total gate region, the conducting
10 state charge carrier mobility is effecitvely unchanged. However, the high defect density region within the gate, even though quite small, is sufficient to preclude charge pumping by causing charge carriers to recombine faster than they accumulate. Thus, providing an inter-
15 face layer 44 having a high density of defects, thereby acting as the desired high defect density region, permits the high speed operation of the active device to be optimized.

A second basic reason for including the high defect
20 density layer 44 is to increase the radiation hardness of the integrated circuits fabricated on the composite substrate 10, 42. A principal result of exposure of an integrated circuit to radiation is the spurious generation of charge carriers within the silicon layer
25 12. The radiation generated charge carriers, in turn, may substantially interfere with the intended operation of the active devices of the integrated circuit depending upon the intensity of the radiation and, therefore, the number of charge carriers generated. The radiation
30 generated charge carriers tend to accumulate at the silicon/sapphire interface 60. Consequently, the provision of a continuous interface layer 44 having a high defect density at the silicon/sapphire interface 60, thereby underlying each respective active device

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1 of the integrated circuit, will increase the tolerance, or hardness, of the integrated circuit to radiation. The crystal defects, acting again as recombination centers, substantially increase the rate at which the
5 radiation generated charge carriers recombine, thereby limiting their interference with the intended operation of the active devices.

A third basic reason for providing a high defect density silicon layer, at least within the gate region
10 of the active devices, is to prevent a phenomena known as back-channel leakage. Inherent in the juxtaposition of two dissimilar crystalline materials is the creation of a voltage potential across the interface. This voltage potential is essentially the consequence of
15 trapped charges at the interface. Additional trapped charges within the bulk of the sapphire substrate 10 may also be generated by exposure to radiation. These bulk trapped charges only increase the voltage potential across the interface. This voltage potential, though
20 small, effectively induces a thin inversion layer at the silicon/sapphire interface 60 between the source and drain regions 48, 50 of the active device. The current conducted by this inversion layer is commonly referred to as back-channel leakage. Since the inver-
25 sion inducing charge carriers are trapped at the silicon/sapphire interface 60, some minimum inversion layer is essentially permanent. However, the leakage current can be effectively reduced by substantially decreasing the mobility of the charge carriers through
30 the inversion layer. As before, this can be acomplished by providing a thin high defect density region, such as the interface layer 44, at the silicon/sapphire interface 60. The thickness of the interface layer 44 need be no more than the thickness of the back-channel

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1 inversion layer. The crystal defects essentially act as scattering centers and, thereby, effectively reduce the net back-channel leakage current flowing between the source and drain reigons 48, 50 of the active
5 device.

Concurrent considerations regarding the proper selection of the size, placement, and the particular defect density of the interface layer 44, as desirable for the reasons given above, involve the necessity of
10 ensuring the accurate, high yield fabrication of high-speed active devices a having minimum of junction leakage currents. Considering that the fabrication of an active device primarily involves the exposed surface of the silicon layer 42, the desired high defect density
15 reigon preferably should be located as far away from the exposed surface of the silicon layer 42 as possible. Placement of the high defect density interface layer 44 at the silicon/sapphire interface 60 optimally results in the layer 44 neither interferring with the further
20 fabrication of the active device or being significantly affected thereby.

In order to minimize junction leakage currents, the high defect density interface layer 44 is preferably made as thin as possible, with as high a defect density
25 as necessary to provide a desired number of recombination centers. Particularly, since the defects act as recombination centers, a leakage current will flow across a reverse biased p-n junction, as may exist between either the source 48 and gate 46 regions or the drain
30 50 and gate 46 regions of the active device. This leakage current is, therefore, directly proportional to the p-n junction area within the high defect density

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1 interface layer 44. Thus, the thickness and correspondingly, the junction area of the interface layer 44, should be kept as small as possible, the layer 44 preferably having a thickness on the order of approximately 200 Å.
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Thus, a process of fabricating semiconductor-on-insulator composite substrates having a highly controlled semiconductor defect density profile has been disclosed.

Obviously, many modifications and variations of
10 the present invention are possible in light of the above description of the preferred embodiments. These modifications may include changes in the specific semiconductor and insulator materials used, the specific conductivity type of the semiconductor layer, the
15 specific ion species, ion dose and dose rate, the implantation energy, and the processing times and temperatures employed within the limits disclosed herein. Further, the specific conventional and well-known processing steps, including the preparation
20 of the various materials and the epitaxial deposition of the semiconductor material onto the insulator material have not been described in detail in order not to obscure the present process. It is therefore to be understood, that within the scope of the appended claims, the
25 invention may be practiced otherwise than as specifically described above.

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CLAIMS

What is Claimed is:

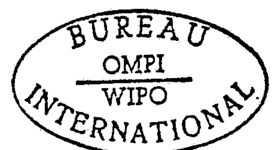
1 1. A method of fabricating a composite substrate characterized by the steps of:

a) providing a layer of a given semiconductor material having a given thickness
5 adjacent a surface of a given insulator material; and

b) amorphizing a buried portion of said semiconductor layer such that said insulator material is substantially
10 unaffected by the amorphization of said buried portion of said semiconductor layer.

1 2. The method of Claim 1 wherein the step of amorphizing said buried portion of said semiconductor layer is further characterized by:

implanting a given dose of a given ion
5 species at a given implantation energy into said semiconductor layer so that said buried portion of said semiconductor layer is amorphized, the dose and respective residual energies of the ions passing
10 through said semiconductor layer and into said insulator material being insufficient to damage said insulator material such that the number of impurities released as a consequence of any damage to said
15 insulator insignificantly contaminates said semiconductor layer.



1 3. The method of Claim 2 wherein the step of implanting said ion species is further characterized in that said given semiconductor layer thickness, said given ion dose and said given implantation energy are
5 such that said buried amorphous portion of said semiconductor layer exists immediately adjacent the surface of said insulator material.

1 4. The method of Claim 2 wherein the step of implanting said ion species is further characterized in that said given semiconductor layer thickness, said given ion dose, and said given implantation energy are
5 such that said buried amorphous portion of said semiconductor layer exists within said semiconductor material spaced apart from the surface of said insulator material by a residual interface layer having a given thickness and a given density of crystal lattice defects.

1 5. The method of Claims 1, 2, 3, or 4 wherein the step of amorphizing said buried portion of said semiconductor layer includes the step of:

maintaining the interface between said
5 semiconductor material and said insulator material at a given constant temperature so that a partially annealed layer having a given thickness and a given density of crystal lattice defects is ultimately
10 formed within said semiconductor material adjacent the boundary of said amorphous portion of said semiconductor layer disposed closest to the surface of said insulator material.

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1 6. The method of Claim 5 further comprising the steps of:

a) recrystallizing said buried amorphous portion of said semiconductor layer;

5 b) removing a portion of said semiconductor layer so as to substantially expose said recrystallized portion of said semiconductor layer; and

c) providing an additional layer of said 10 semiconductor material adjacent said recrystallized portion of said semiconductor layer such that said additional layer and said recrystallized portion of said semiconductor layer are substantially 15 free of crystal lattice defects.

1 7. The method of Claims 1, 2, or 3 further comprising the steps of:

a) recrystallizing said buried amorphous portion of said semiconductor layer;

5 b) removing a portion of said semiconductor layer so as to substantially expose said recrystallized portion of said semiconductor layer; and

c) providing an additional layer of said 10 semiconductor material adjacent said recrystallized portion of said semiconductor layer such that said additional layer and said recrystallized portion of said semiconductor layer are substantially 15 free of crystal lattice defects.

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1 8. The method of Claim 4 further comprising the steps of:

a) recrystallizing said buried amorphous portion of said semiconductor layer;

5 b) removing a portion of said semiconductor layer so as to substantially expose said recrystallized portion of said semiconductor layer; and

c) providing an additional layer of said
10 semiconductor material adjacent said recrystallized portion of said semiconductor layer such that said additional layer and said recrystallized portion of said semiconductor layer are substantially
15 free of crystal lattice defects.

1 9. The method of Claim 6 wherein the step of recrystallizing said buried amorphous portion of said semiconductor layer includes the step of:

a) regrowing said buried amorphous portion
5 of said semiconductor layer so as to form a recrystallized layer having a substantially uniform crystallographic orientation; and

b) annealing said semiconductor layer so as
10 to reduce the number of crystal lattice defects contained therein, the defect density within said recrystallized layer being low and relatively uniform, a substantially greater number of defects
15 persisting in the region of said semiconductor layer separating said recrystallized layer and said insulator material.

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1 10. The method of Claim 8 wherein the step of recrystallizing said buried amorphous portion of said semiconductor layer includes the step of:

a) regrowing said buried amorphous portion
5 of said semiconductor layer so as to form a recrystallized layer having a substantially uniform crystallographic orientation; and

b) annealing said semiconductor layer so as
10 to reduce the number of crystal lattice defects contained therein, the defect density within said recrystalized layer being low and relatively uniform, a substantially greater number of defects
15 persisting in the region of said semiconductor layer separating said recrystallized layer and said insulator material.

1 11. The method of Claim 2, 3, or 4 wherein the step of implanting said ion species is further characterized in that said insulator material has a damage density threshold and that the product of the
5 dose and the average residual energy of the ions passing through said semiconductor layer and into said insulator material is less than or equal to the damage density threshold of said insulator material.

1 12. The method of Claim 11 wherein said step of implanting said ion species is further characterized in that said insulator material is sapphire and that the damage density threshold of said insulator material is
5 approximately 1×10^{15} keV-ions/cm^2.

1 13. The method of Claim 2, 3, or 4 wherein the step of implanting said ion species is further characterized in that said given thickness of said semiconductor layer is equal to or less than approxi-
5 mately 2,500 Å.

1 14. The method of Claim 13 wherein the step of implanting said ion species is further characterized in that said given implantation energy is equal to or less than approximately 90 keV.

1 15. The method of Claim 14 wherein the step of implanting said ion species is further characterized in that said given ion dose is equal to or less than approximately 2×10^{15} ion/cm^2.

1 16. The method of Claim 15 wherein the step of implanting said ion species is further characterized in that said given ion species and said given semiconductor material are silicon.

1 17. The method of Claim 2, 3, or 4 wherein the step of implanting said ion species is further characterized in that said ion species is the same element or an element component of said given semi-
5 conductor material.

1 18. The method of Claim 17 wherein the step of implanting said ion species is further characterized in that said given ion species and said given semiconductor material are silicon.

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1 19. The method of Claim 17 wherein the step of implanting said ion species is further characterized in that said given ion species is arsenic and said given semiconductor material is GaAs.

Fig. 1.

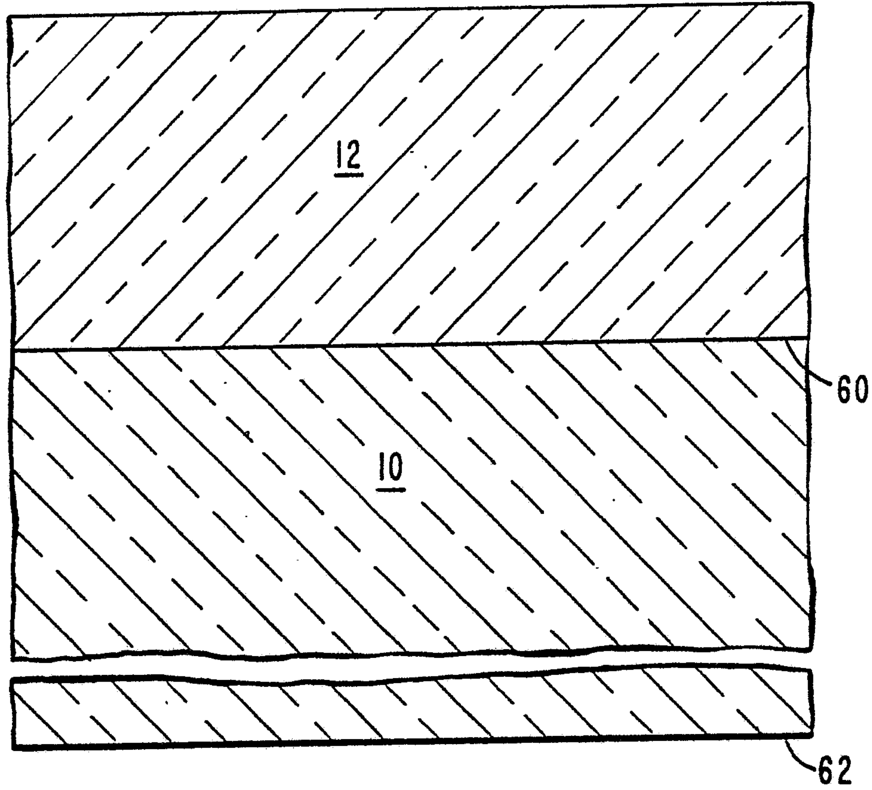
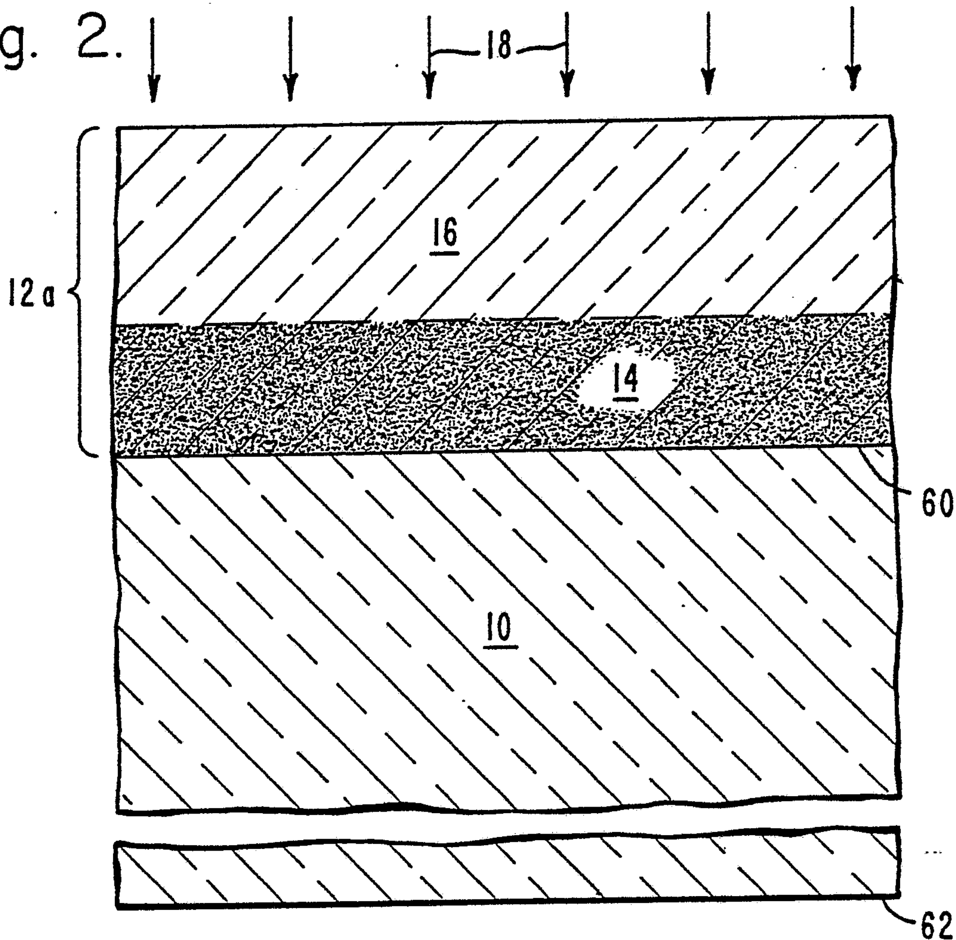


Fig. 2.



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ION IMPLANT DENSITY

SI SURFACE

0

Rp-1.5ΔRp

Rp-ΔRp

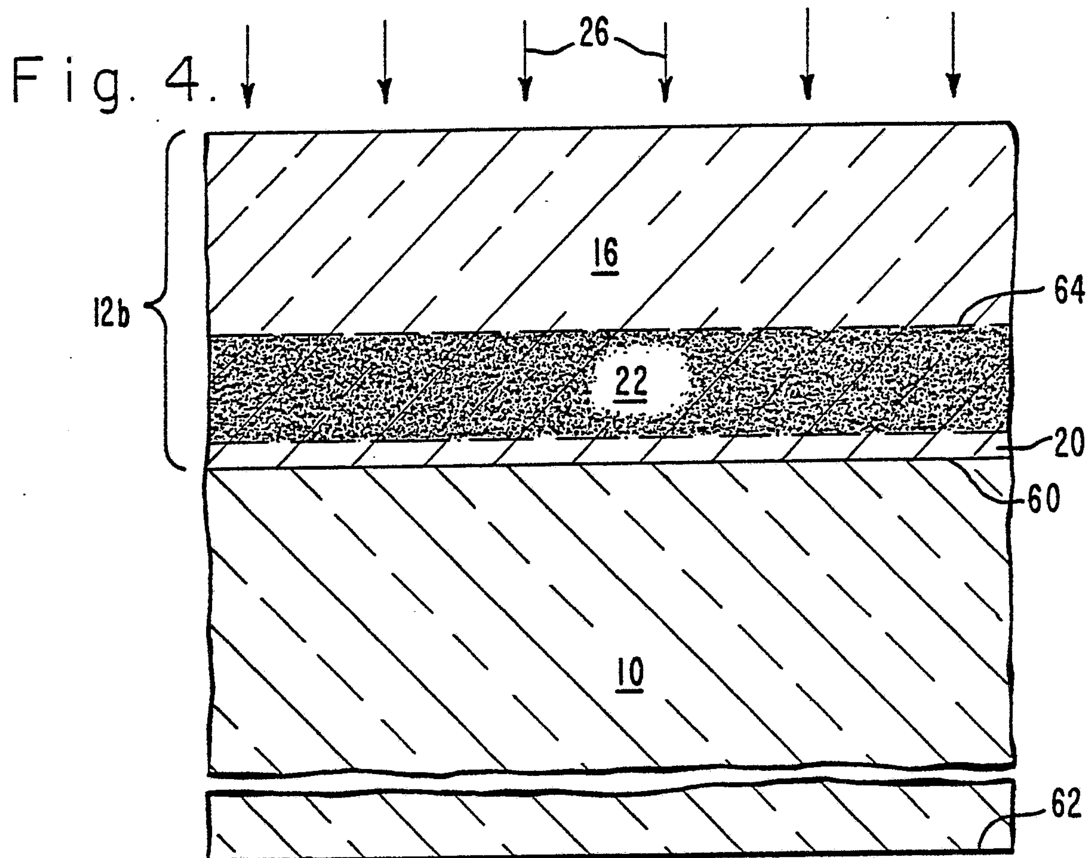
Rp

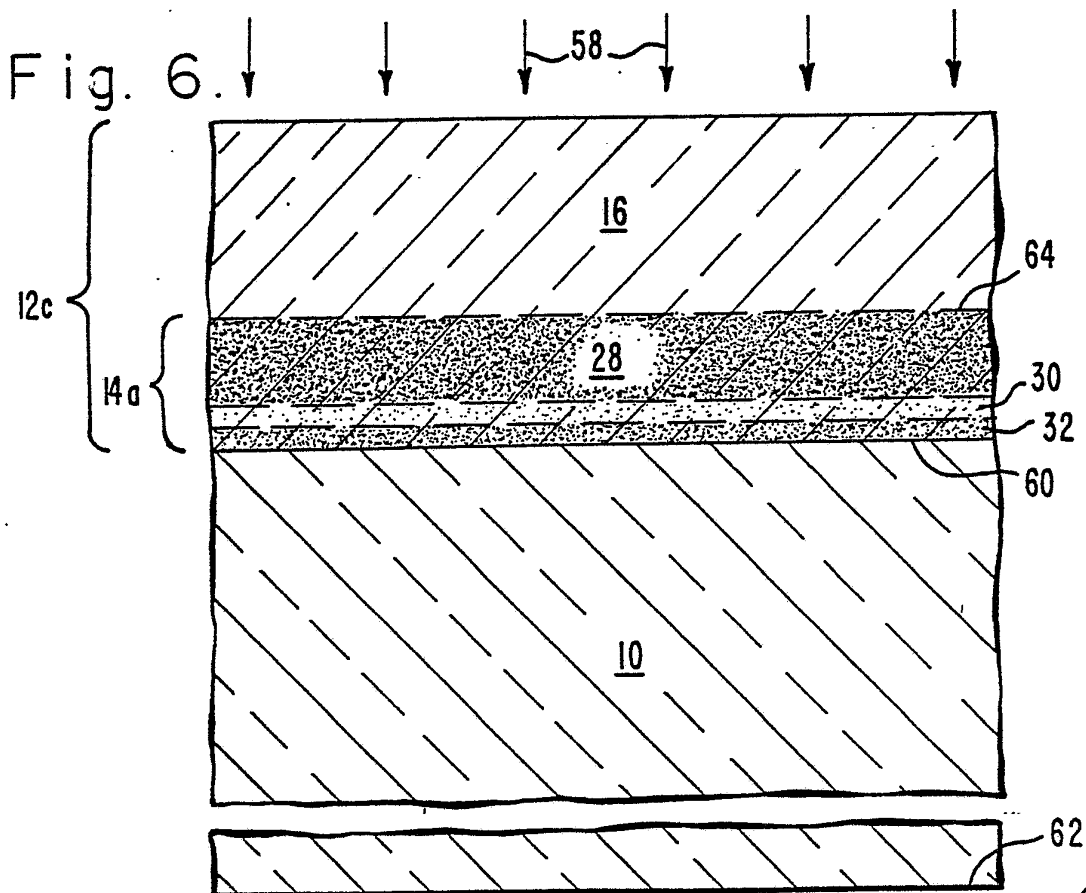
Rp+ΔRp

Rp+1.5ΔRp

SI/Al_2O_3 INTERFACE

Fig. 3.





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ION IMPLANT DENSITY

Si SURFACE

Si/Al_2O_3 INTERFACE

0 Rp−1.5ΔRp ΔRp Rp ΔRp Rp+1.5ΔRp t

Fig. 5.

Fig. 7.

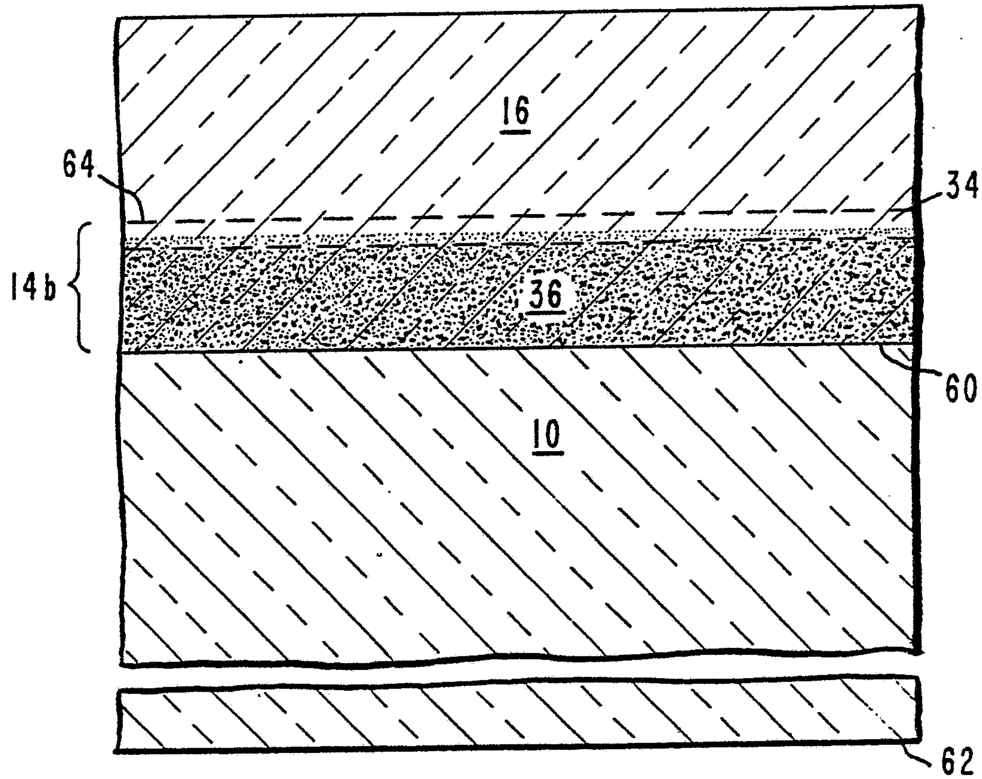


Fig. 8.

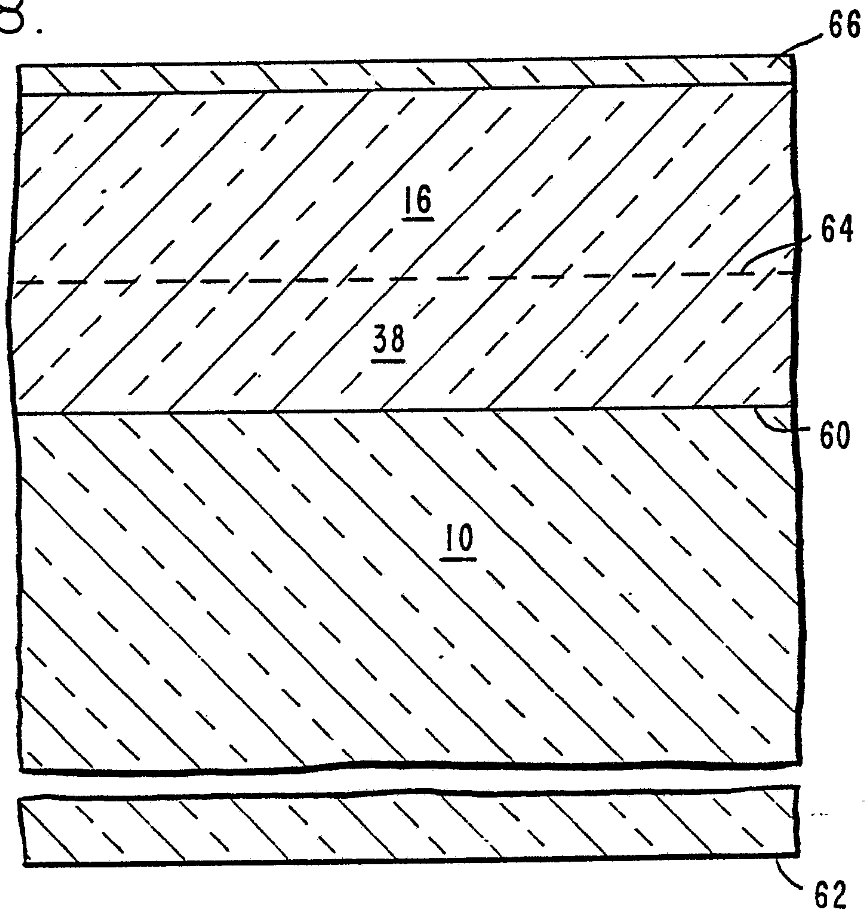


Fig. 9.

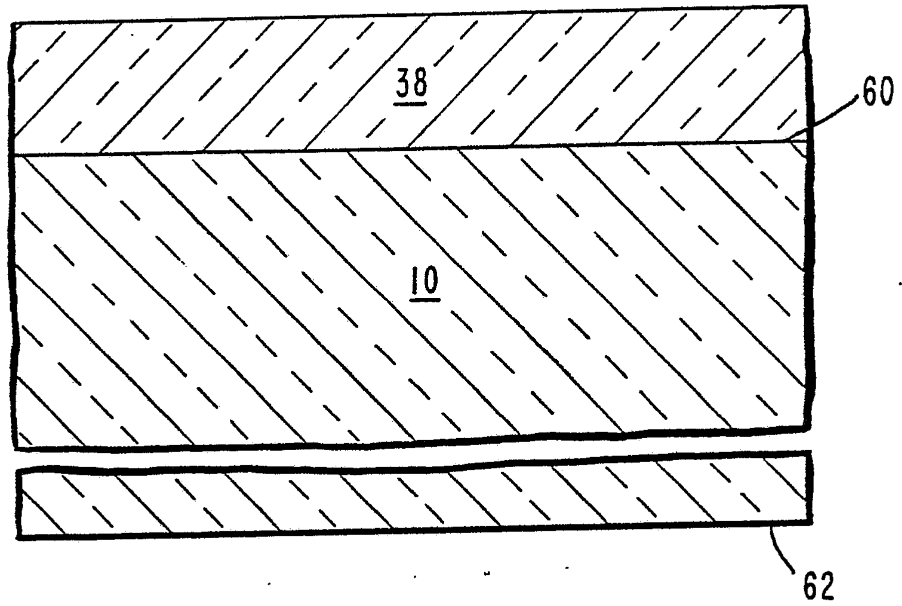
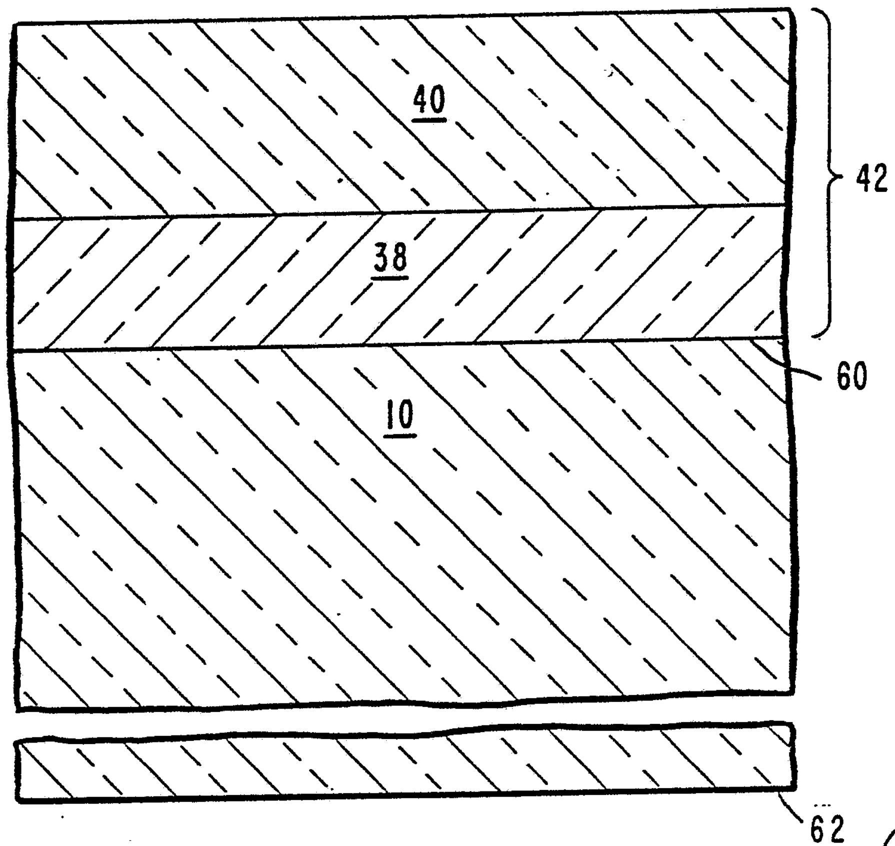


Fig. 10.



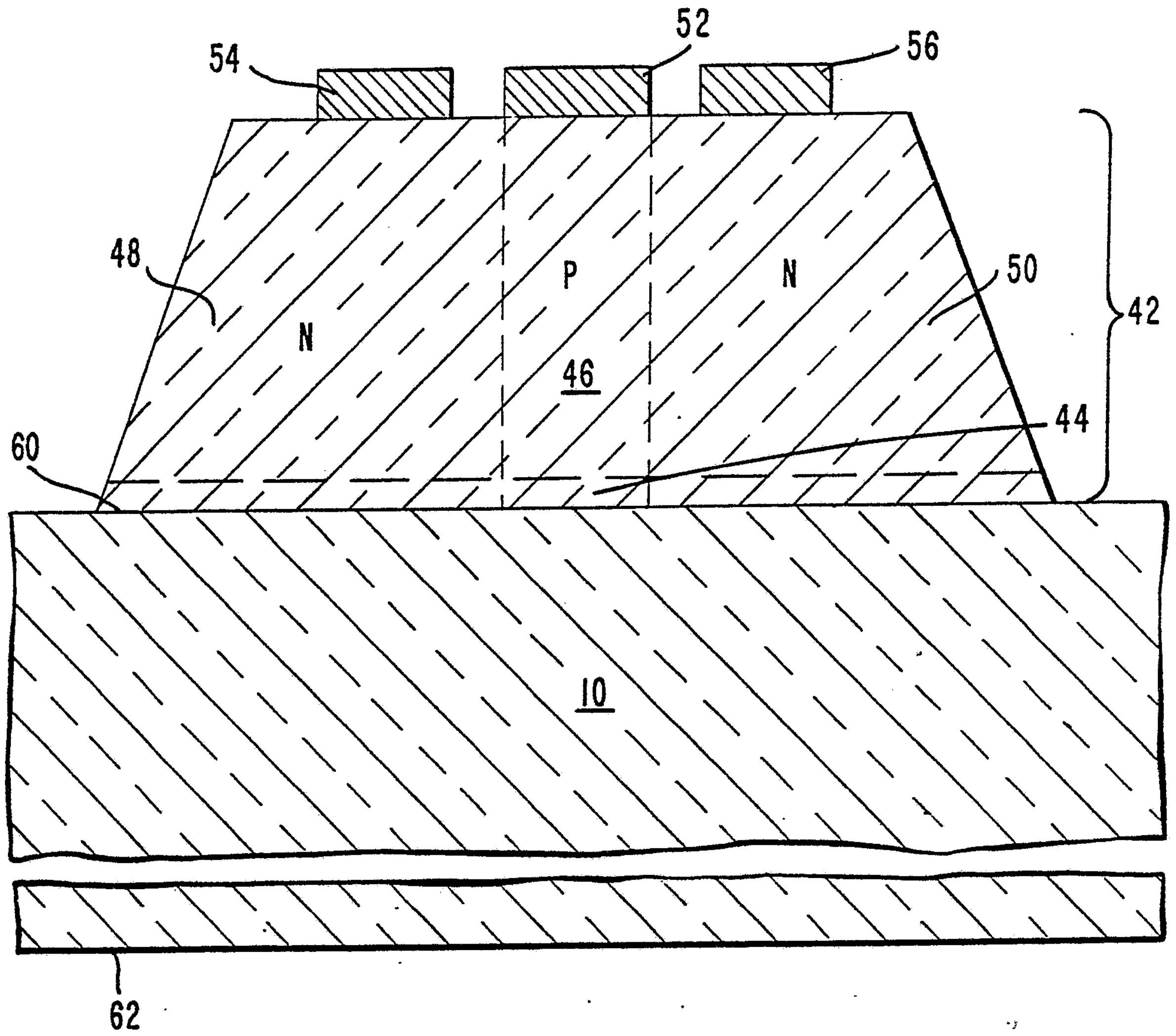


Fig. 11.

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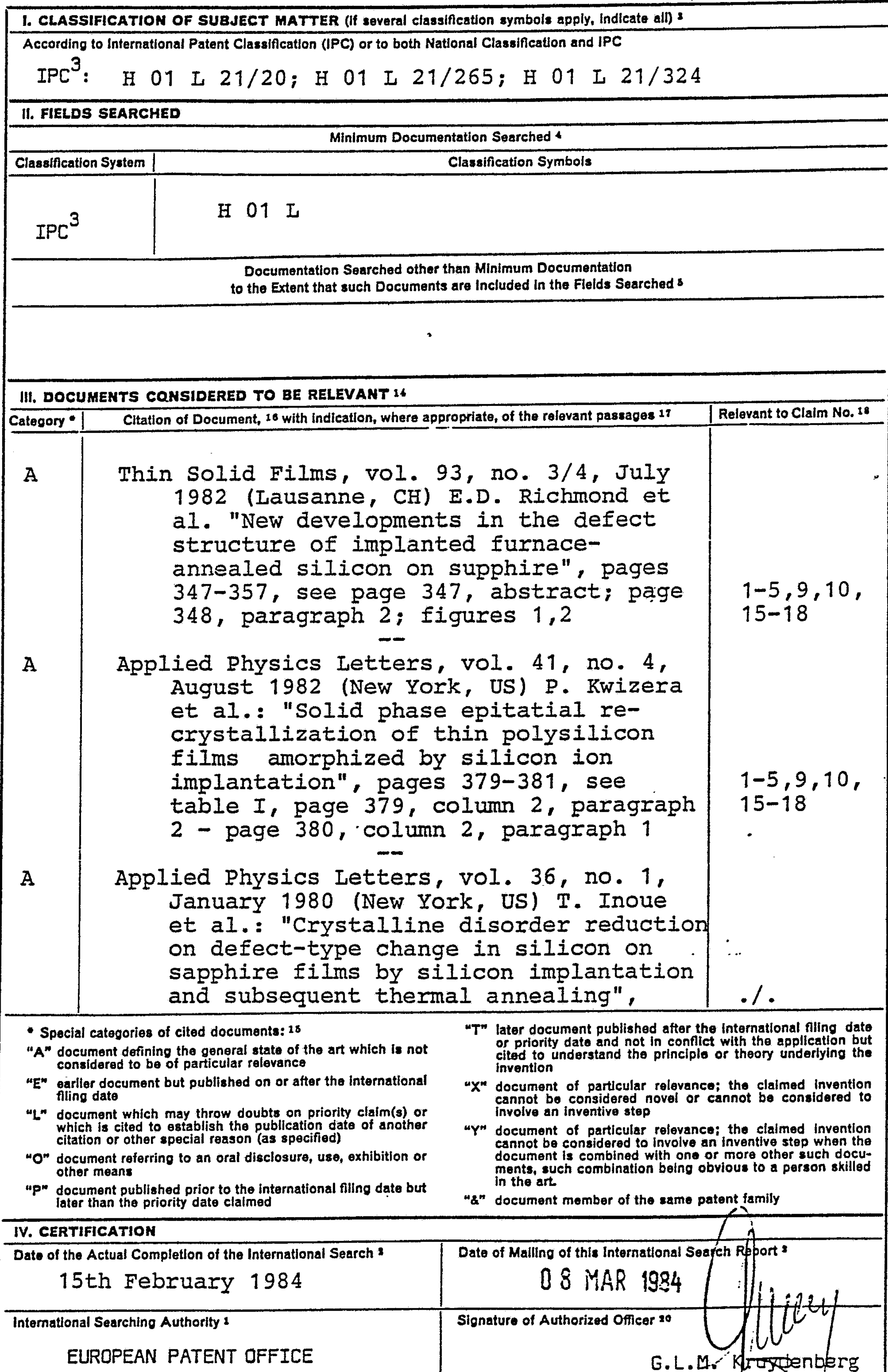

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 83/01622

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[3]: H 01 L 21/20; H 01 L 21/265; H 01 L 21/324

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC[3]	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	Thin Solid Films, vol. 93, no. 3/4, July 1982 (Lausanne, CH) E.D. Richmond et al. "New developments in the defect structure of implanted furnace-annealed silicon on supphire", pages 347-357, see page 347, abstract; page 348, paragraph 2; figures 1,2	1-5,9,10, 15-18
	--	
A	Applied Physics Letters, vol. 41, no. 4, August 1982 (New York, US) P. Kwizera et al.: "Solid phase epitatial re-crystallization of thin polysilicon films amorphized by silicon ion implantation", pages 379-381, see table I, page 379, column 2, paragraph 2 - page 380, column 2, paragraph 1	1-5,9,10, 15-18
	--	
A	Applied Physics Letters, vol. 36, no. 1, January 1980 (New York, US) T. Inoue et al.: "Crystalline disorder reduction on defect-type change in silicon on sapphire films by silicon implantation and subsequent thermal annealing",	./.

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
15th February 1984	08 MAR 1984
International Searching Authority [1]	**Signature of Authorized Officer** [20]
EUROPEAN PATENT OFFICE	G.L.M. Kruydenberg

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category*	Citation of Document,[16] with indication, where appropriate, of the relevant passages[17]	Relevant to Claim No[18]
	pages 64-66, see page 64, column 1, paragraph 2 - column 2, paragraph 1; table I	1-5,9,10, 15-18
A	Extended Abstracts of the Journal of the Electrochemical Society, vol. 79-1, May 1979 (Princeton, US) I. Golecki et al.: "Ion beam induced epitaxy of silicon", pages 305-307, see page 305, paragraphs 2,3	1-5
A	Proceedings of the 13th Conference on Solid State Devices, Tokyo, 1981, Japanese Journal of Applied Physics, vol. 21, Supplement 21-1, 1982 (Tokyo, JP) T. Yoshii et al.: "Improvement of SOS device performance by solid-phase epitaxy", pages 175-179, see the entire article	1-5,7-10, 13-18
A	US, A, 4177084 (S.S. Lam et al.) 4 December 1979 see claims	1-5,9,10, 15-18
A	Nuclear Instruments and Methods, vol. 182 /183, part 2, April/May 1981 (Amsterdam, NL) T. Inoue et al.: "Crystalline quality improvement of SOS films by Si implantation and subsequent annealing", pages 683-690 see the entire article	1-5,9,10, 13-18
A	Applied Physics Letters, vol. 40, no. 8, April 1982 (New York, US) I. Golecki et al.: "Reduction in crystallographic surface defects and strain in 0,2 μm thick silicon-on-sapphire films by repetitive implantation and solid-phase epitaxy", pages 670-672, see the entire article	1-5,9,10, 15-18
A	Extended Abstracts of the Journal of the Electrochemical Society, vol. 80-2, October 1980 (Princeton, US) M.G. Grimaldi et al.: "Low-temperature epitaxial regrowth of ion-implanted GaAs.", pages 1063-1064, see the entire article	1,19

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 83/01622 (SA 6060)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 28/02/84

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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For more details about this annex :
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