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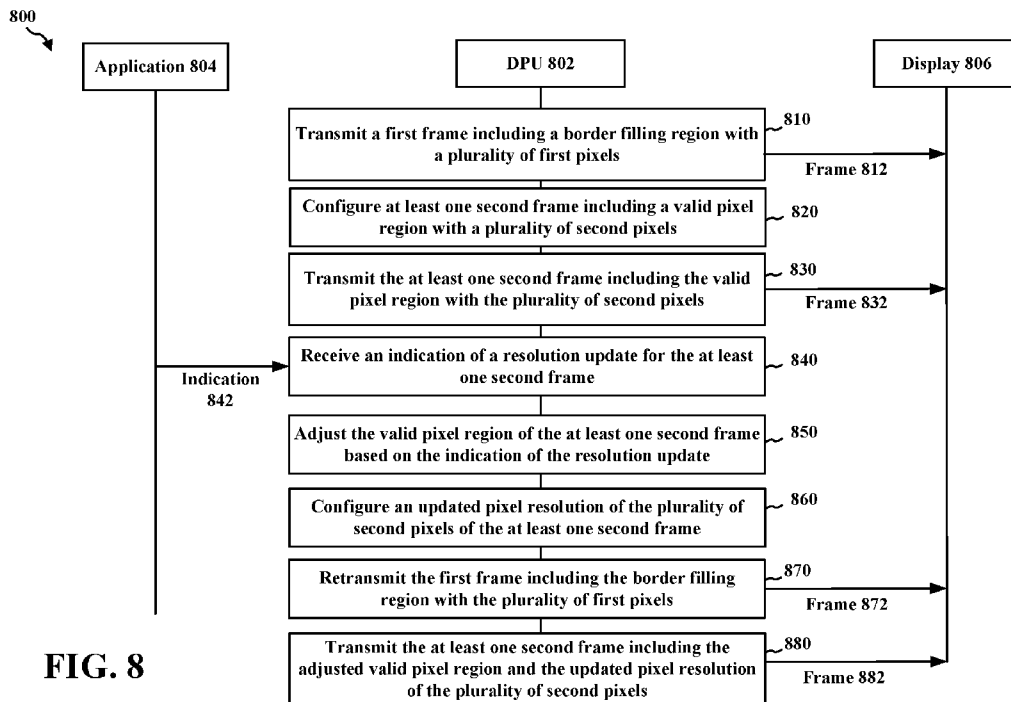


FIG. 8

(57) Abstract: Aspects presented herein relate to methods and devices for display processing including an apparatus, e.g., a DPU. The apparatus may transmit, to a panel, a first frame including a border filling region with a plurality of first pixels, each of the first pixels including a border filling color. The apparatus may also configure at least one second frame including a valid pixel region with a plurality of second pixels, each of the second pixels including content data and a second pixel resolution. The apparatus may also transmit, to the panel, the at least one second frame including the valid pixel region with the plurality of second pixels. Further, the apparatus may receive an indication of a resolution update for the at least one second frame. The apparatus may also adjust the valid pixel region of the at least one second frame based on the indication of the resolution update.



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SEQUENTIAL FLEXIBLE DISPLAY SHAPE RESOLUTION

TECHNICAL FIELD

[0001] The present disclosure relates generally to processing systems and, more particularly, to one or more techniques for display processing.

INTRODUCTION

[0002] Computing devices often perform graphics and/or display processing (e.g., utilizing a graphics processing unit (GPU), a central processing unit (CPU), a display processor, etc.) to render and display visual content. Such computing devices may include, for example, computer workstations, mobile phones such as smartphones, embedded systems, personal computers, tablet computers, and video game consoles. GPUs are configured to execute a graphics processing pipeline that includes one or more processing stages, which operate together to execute graphics processing commands and output a frame. A central processing unit (CPU) may control the operation of the GPU by issuing one or more graphics processing commands to the GPU. Modern day CPUs are typically capable of executing multiple applications concurrently, each of which may need to utilize the GPU during execution. A display processor is configured to convert digital information received from a CPU to analog values and may issue commands to a display panel for displaying the visual content. A device that provides content for visual presentation on a display may utilize a GPU and/or a display processor.

[0003] A GPU of a device may be configured to perform the processes in a graphics processing pipeline. Further, a display processor or display processing unit (DPU) may be configured to perform the processes of display processing. However, with the advent of wireless communication and smaller, handheld devices, there has developed an increased need for improved graphics or display processing.

BRIEF SUMMARY

[0004] The following presents a simplified summary of one or more aspects in order to provide a basic understanding of such aspects. This summary is not an extensive overview of all contemplated aspects, and is intended to neither identify key or critical elements of all aspects nor delineate the scope of any or all aspects. Its sole purpose

is to present some concepts of one or more aspects in a simplified form as a prelude to the more detailed description that is presented later.

[0005] In an aspect of the disclosure, a method, a computer-readable medium, and an apparatus are provided. The apparatus may be a display processing unit (DPU) or any apparatus that may perform display processing. The apparatus may transmit, to a display panel, a first frame including a border filling region with a plurality of first pixels, where each of the plurality of first pixels includes a border filling color. The apparatus may also configure at least one second frame including a valid pixel region with a plurality of second pixels, where each of the plurality of second pixels includes content data and a second pixel resolution. The apparatus may also transmit, to the display panel, the at least one second frame including the valid pixel region with the plurality of second pixels. Further, the apparatus may receive, from at least one application or an operating system, an indication of a resolution update for the at least one second frame. The apparatus may also adjust the valid pixel region of the at least one second frame based on the indication of the resolution update. The apparatus may also configure, upon adjusting the valid pixel region of the at least one second frame, an updated pixel resolution of the plurality of second pixels of the at least one second frame based on the indication of the resolution update. Moreover, the apparatus may retransmit, to the display panel, the first frame including the border filling region with the plurality of first pixels. The apparatus may also transmit, to the display panel, the at least one second frame including the adjusted valid pixel region and the updated pixel resolution of the plurality of second pixels.

[0006] The details of one or more examples of the disclosure are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the disclosure will be apparent from the description and drawings, and from the claims.

BRIEF DESCRIPTION OF DRAWINGS

[0007] FIG. 1 is a block diagram that illustrates an example content generation system.

[0008] FIG. 2 illustrates an example graphics processing unit (GPU).

[0009] FIG. 3 illustrates an example display framework including a display processor and a display.

[0010] FIG. 4 is a diagram illustrating an example frame for display processing.

- [0011] FIG. 5 is a diagram illustrating an example border filling process for display processing.
- [0012] FIG. 6 is a flowchart of an example method of display processing.
- [0013] FIG. 7A is a diagram illustrating an example frame for display processing.
- [0014] FIG. 7B is a diagram illustrating an example frame for display processing.
- [0015] FIG. 8 is a communication flow diagram illustrating example communications between an application, a DPU, and a display.
- [0016] FIG. 9 is a flowchart of an example method of display processing.

DETAILED DESCRIPTION

- [0017] Certain types of displays, such as flexible displays, dual displays, triple displays, round displays, and other novel display panel identifier (ID) designs, are becoming increasingly popular. Also, in certain types of displays and devices, display border filling is widely used to match the mechanical/ID design. In some aspects of display processing, border filling for a frame (e.g., display shape border filling) may be performed in a hardware (HW) mixer (e.g., a DPU hardware mixer). This may conflict with display post-processing functionalities. For instance, before all frame processing starts, the border filling lines may already be added. This kind of border filling solution is utilized in some aspects of industry practice and implementation. In a border filling pipeline, all blocks and processing that are after the hardware mixer (i.e., frame data generation) may process additional border filling lines. This may cause the border filling lines to be erroneously processed. Additionally, other types of display processing blocks and functions may suffer based on this erroneous processing. Some types of displays, such as dual flexible display projects/devices, may benefit from a solution to the border filling function problem. This problem may also be applicable to flexible IDs and flexible display devices. Aspects of the present disclosure may utilize a border filling function without any border filling errors. Aspects of the present disclosure may also utilize display processing features without any limitations. For instance, aspects presented herein may utilize DPU and display processing features and functionalities that are related to the border filling function without any limitations.
- [0018] Various aspects of systems, apparatuses, computer program products, and methods are described more fully hereinafter with reference to the accompanying drawings. This disclosure may, however, be embodied in many different forms and should not

be construed as limited to any specific structure or function presented throughout this disclosure. Rather, these aspects are provided so that this disclosure will be thorough and complete, and will fully convey the scope of this disclosure to those skilled in the art. Based on the teachings herein one skilled in the art should appreciate that the scope of this disclosure is intended to cover any aspect of the systems, apparatuses, computer program products, and methods disclosed herein, whether implemented independently of, or combined with, other aspects of the disclosure. For example, an apparatus may be implemented or a method may be practiced using any number of the aspects set forth herein. In addition, the scope of the disclosure is intended to cover such an apparatus or method which is practiced using other structure, functionality, or structure and functionality in addition to or other than the various aspects of the disclosure set forth herein. Any aspect disclosed herein may be embodied by one or more elements of a claim.

[0019] Although various aspects are described herein, many variations and permutations of these aspects fall within the scope of this disclosure. Although some potential benefits and advantages of aspects of this disclosure are mentioned, the scope of this disclosure is not intended to be limited to particular benefits, uses, or objectives. Rather, aspects of this disclosure are intended to be broadly applicable to different wireless technologies, system configurations, networks, and transmission protocols, some of which are illustrated by way of example in the figures and in the following description. The detailed description and drawings are merely illustrative of this disclosure rather than limiting, the scope of this disclosure being defined by the appended claims and equivalents thereof.

[0020] Several aspects are presented with reference to various apparatus and methods. These apparatus and methods are described in the following detailed description and illustrated in the accompanying drawings by various blocks, components, circuits, processes, algorithms, and the like (collectively referred to as “elements”). These elements may be implemented using electronic hardware, computer software, or any combination thereof. Whether such elements are implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system.

[0021] By way of example, an element, or any portion of an element, or any combination of elements may be implemented as a “processing system” that includes one or more processors (which may also be referred to as processing units). Examples of

processors include microprocessors, microcontrollers, graphics processing units (GPUs), general purpose GPUs (GPGPUs), central processing units (CPUs), application processors, digital signal processors (DSPs), reduced instruction set computing (RISC) processors, systems-on-chip (SOC), baseband processors, application specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), programmable logic devices (PLDs), state machines, gated logic, discrete hardware circuits, and other suitable hardware configured to perform the various functionality described throughout this disclosure. One or more processors in the processing system may execute software. Software may be construed broadly to mean instructions, instruction sets, code, code segments, program code, programs, subprograms, software components, applications, software applications, software packages, routines, subroutines, objects, executables, threads of execution, procedures, functions, etc., whether referred to as software, firmware, middleware, microcode, hardware description language, or otherwise. The term application may refer to software. As described herein, one or more techniques may refer to an application, i.e., software, being configured to perform one or more functions. In such examples, the application may be stored on a memory, e.g., on-chip memory of a processor, system memory, or any other memory. Hardware described herein, such as a processor may be configured to execute the application. For example, the application may be described as including code that, when executed by the hardware, causes the hardware to perform one or more techniques described herein. As an example, the hardware may access the code from a memory and execute the code accessed from the memory to perform one or more techniques described herein. In some examples, components are identified in this disclosure. In such examples, the components may be hardware, software, or a combination thereof. The components may be separate components or sub-components of a single component.

[0022] Accordingly, in one or more examples described herein, the functions described may be implemented in hardware, software, or any combination thereof. If implemented in software, the functions may be stored on or encoded as one or more instructions or code on a computer-readable medium. Computer-readable media includes computer storage media. Storage media may be any available media that may be accessed by a computer. By way of example, and not limitation, such computer-readable media may comprise a random access memory (RAM), a read-only memory (ROM), an electrically erasable programmable ROM (EEPROM), optical disk storage, magnetic

disk storage, other magnetic storage devices, combinations of the aforementioned types of computer-readable media, or any other medium that may be used to store computer executable code in the form of instructions or data structures that may be accessed by a computer.

[0023] In general, this disclosure describes techniques for having a graphics processing pipeline in a single device or multiple devices, improving the rendering of graphical content, and/or reducing the load of a processing unit, i.e., any processing unit configured to perform one or more techniques described herein, such as a GPU. For example, this disclosure describes techniques for graphics processing in any device that utilizes graphics processing. Other example benefits are described throughout this disclosure.

[0024] As used herein, instances of the term “content” may refer to “graphical content,” “image,” and vice versa. This is true regardless of whether the terms are being used as an adjective, noun, or other parts of speech. In some examples, as used herein, the term “graphical content” may refer to a content produced by one or more processes of a graphics processing pipeline. In some examples, as used herein, the term “graphical content” may refer to a content produced by a processing unit configured to perform graphics processing. In some examples, as used herein, the term “graphical content” may refer to a content produced by a graphics processing unit.

[0025] In some examples, as used herein, the term “display content” may refer to content generated by a processing unit configured to perform displaying processing. In some examples, as used herein, the term “display content” may refer to content generated by a display processing unit. Graphical content may be processed to become display content. For example, a graphics processing unit may output graphical content, such as a frame, to a buffer (which may be referred to as a framebuffer). A display processing unit may read the graphical content, such as one or more frames from the buffer, and perform one or more display processing techniques thereon to generate display content. For example, a display processing unit may be configured to perform composition on one or more rendered layers to generate a frame. As another example, a display processing unit may be configured to compose, blend, or otherwise combine two or more layers together into a single frame. A display processing unit may be configured to perform scaling, e.g., upscaling or downscaling, on a frame. In some examples, a frame may refer to a layer. In other examples, a frame may refer to two or more layers that have already been blended together to form the frame, i.e., the

frame includes two or more layers, and the frame that includes two or more layers may subsequently be blended.

[0026] FIG. 1 is a block diagram that illustrates an example content generation system 100 configured to implement one or more techniques of this disclosure. The content generation system 100 includes a device 104. The device 104 may include one or more components or circuits for performing various functions described herein. In some examples, one or more components of the device 104 may be components of an SOC. The device 104 may include one or more components configured to perform one or more techniques of this disclosure. In the example shown, the device 104 may include a processing unit 120, a content encoder/decoder 122, and a system memory 124. In some aspects, the device 104 may include a number of components, e.g., a communication interface 126, a transceiver 132, a receiver 128, a transmitter 130, a display processor 127, and one or more displays 131. Reference to the display 131 may refer to the one or more displays 131. For example, the display 131 may include a single display or multiple displays. The display 131 may include a first display and a second display. The first display may be a left-eye display and the second display may be a right-eye display. In some examples, the first and second display may receive different frames for presentment thereon. In other examples, the first and second display may receive the same frames for presentment thereon. In further examples, the results of the graphics processing may not be displayed on the device, e.g., the first and second display may not receive any frames for presentment thereon. Instead, the frames or graphics processing results may be transferred to another device. In some aspects, this may be referred to as split-rendering.

[0027] The processing unit 120 may include an internal memory 121. The processing unit 120 may be configured to perform graphics processing, such as in a graphics processing pipeline 107. The content encoder/decoder 122 may include an internal memory 123. In some examples, the device 104 may include a display processor, such as the display processor 127, to perform one or more display processing techniques on one or more frames generated by the processing unit 120 before presentment by the one or more displays 131. The display processor 127 may be configured to perform display processing. For example, the display processor 127 may be configured to perform one or more display processing techniques on one or more frames generated by the processing unit 120. The one or more displays 131 may be configured to display or otherwise present frames processed by the display

processor 127. In some examples, the one or more displays 131 may include one or more of: a liquid crystal display (LCD), a plasma display, an organic light emitting diode (OLED) display, a projection display device, an augmented reality display device, a virtual reality display device, a head-mounted display, or any other type of display device.

[0028] Memory external to the processing unit 120 and the content encoder/decoder 122, such as system memory 124, may be accessible to the processing unit 120 and the content encoder/decoder 122. For example, the processing unit 120 and the content encoder/decoder 122 may be configured to read from and/or write to external memory, such as the system memory 124. The processing unit 120 and the content encoder/decoder 122 may be communicatively coupled to the system memory 124 over a bus. In some examples, the processing unit 120 and the content encoder/decoder 122 may be communicatively coupled to each other over the bus or a different connection.

[0029] The content encoder/decoder 122 may be configured to receive graphical content from any source, such as the system memory 124 and/or the communication interface 126. The system memory 124 may be configured to store received encoded or decoded graphical content. The content encoder/decoder 122 may be configured to receive encoded or decoded graphical content, e.g., from the system memory 124 and/or the communication interface 126, in the form of encoded pixel data. The content encoder/decoder 122 may be configured to encode or decode any graphical content.

[0030] The internal memory 121 or the system memory 124 may include one or more volatile or non-volatile memories or storage devices. In some examples, internal memory 121 or the system memory 124 may include RAM, SRAM, DRAM, erasable programmable ROM (EPROM), electrically erasable programmable ROM (EEPROM), flash memory, a magnetic data media or an optical storage media, or any other type of memory.

[0031] The internal memory 121 or the system memory 124 may be a non-transitory storage medium according to some examples. The term “non-transitory” may indicate that the storage medium is not embodied in a carrier wave or a propagated signal. However, the term “non-transitory” should not be interpreted to mean that internal memory 121 or the system memory 124 is non-movable or that its contents are static. As one example, the system memory 124 may be removed from the device 104 and

moved to another device. As another example, the system memory 124 may not be removable from the device 104.

[0032] The processing unit 120 may be a central processing unit (CPU), a graphics processing unit (GPU), a general purpose GPU (GPGPU), or any other processing unit that may be configured to perform graphics processing. In some examples, the processing unit 120 may be integrated into a motherboard of the device 104. In some examples, the processing unit 120 may be present on a graphics card that is installed in a port in a motherboard of the device 104, or may be otherwise incorporated within a peripheral device configured to interoperate with the device 104. The processing unit 120 may include one or more processors, such as one or more microprocessors, GPUs, application specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), arithmetic logic units (ALUs), digital signal processors (DSPs), discrete logic, software, hardware, firmware, other equivalent integrated or discrete logic circuitry, or any combinations thereof. If the techniques are implemented partially in software, the processing unit 120 may store instructions for the software in a suitable, non-transitory computer-readable storage medium, e.g., internal memory 121, and may execute the instructions in hardware using one or more processors to perform the techniques of this disclosure. Any of the foregoing, including hardware, software, a combination of hardware and software, etc., may be considered to be one or more processors.

[0033] The content encoder/decoder 122 may be any processing unit configured to perform content decoding. In some examples, the content encoder/decoder 122 may be integrated into a motherboard of the device 104. The content encoder/decoder 122 may include one or more processors, such as one or more microprocessors, application specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), arithmetic logic units (ALUs), digital signal processors (DSPs), video processors, discrete logic, software, hardware, firmware, other equivalent integrated or discrete logic circuitry, or any combinations thereof. If the techniques are implemented partially in software, the content encoder/decoder 122 may store instructions for the software in a suitable, non-transitory computer-readable storage medium, e.g., internal memory 123, and may execute the instructions in hardware using one or more processors to perform the techniques of this disclosure. Any of the foregoing, including hardware, software, a combination of hardware and software, etc., may be considered to be one or more processors.

- [0034]** In some aspects, the content generation system 100 may include a communication interface 126. The communication interface 126 may include a receiver 128 and a transmitter 130. The receiver 128 may be configured to perform any receiving function described herein with respect to the device 104. Additionally, the receiver 128 may be configured to receive information, e.g., eye or head position information, rendering commands, or location information, from another device. The transmitter 130 may be configured to perform any transmitting function described herein with respect to the device 104. For example, the transmitter 130 may be configured to transmit information to another device, which may include a request for content. The receiver 128 and the transmitter 130 may be combined into a transceiver 132. In such examples, the transceiver 132 may be configured to perform any receiving function and/or transmitting function described herein with respect to the device 104.
- [0035]** Referring again to FIG. 1, in certain aspects, the display processor 127 may include a sequential display component 198 configured to transmit, to a display panel, a first frame including a border filling region with a plurality of first pixels, where each of the plurality of first pixels includes a border filling color. The sequential display component 198 may also be configured to configure at least one second frame including a valid pixel region with a plurality of second pixels, where each of the plurality of second pixels includes content data and a second pixel resolution. The sequential display component 198 may also be configured to transmit, to the display panel, the at least one second frame including the valid pixel region with the plurality of second pixels. The sequential display component 198 may also be configured to receive, from at least one application or an operating system, an indication of a resolution update for the at least one second frame. The sequential display component 198 may also be configured to adjust the valid pixel region of the at least one second frame based on the indication of the resolution update. The sequential display component 198 may also be configured to configure, upon adjusting the valid pixel region of the at least one second frame, an updated pixel resolution of the plurality of second pixels of the at least one second frame based on the indication of the resolution update. The sequential display component 198 may also be configured to retransmit, to the display panel, the first frame including the border filling region with the plurality of first pixels. The sequential display component 198 may also be configured to transmit, to the display panel, the at least one second frame including the adjusted valid pixel region and the updated pixel resolution of the plurality of second pixels.

Although the following description may be focused on display processing, the concepts described herein may be applicable to other similar processing techniques.

[0036] As described herein, a device, such as the device 104, may refer to any device, apparatus, or system configured to perform one or more techniques described herein. For example, a device may be a server, a base station, user equipment, a client device, a station, an access point, a computer, e.g., a personal computer, a desktop computer, a laptop computer, a tablet computer, a computer workstation, or a mainframe computer, an end product, an apparatus, a phone, a smart phone, a server, a video game platform or console, a handheld device, e.g., a portable video game device or a personal digital assistant (PDA), a wearable computing device, e.g., a smart watch, an augmented reality device, or a virtual reality device, a non-wearable device, a display or display device, a television, a television set-top box, an intermediate network device, a digital media player, a video streaming device, a content streaming device, an in-car computer, any mobile device, any device configured to generate graphical content, or any device configured to perform one or more techniques described herein. Processes herein may be described as performed by a particular component (e.g., a GPU), but, in further embodiments, may be performed using other components (e.g., a CPU), consistent with disclosed embodiments.

[0037] GPUs may process multiple types of data or data packets in a GPU pipeline. For instance, in some aspects, a GPU may process two types of data or data packets, e.g., context register packets and draw call data. A context register packet may be a set of global state information, e.g., information regarding a global register, shading program, or constant data, which may regulate how a graphics context will be processed. For example, context register packets may include information regarding a color format. In some aspects of context register packets, there may be a bit that indicates which workload belongs to a context register. Also, there may be multiple functions or programming running at the same time and/or in parallel. For example, functions or programming may describe a certain operation, e.g., the color mode or color format. Accordingly, a context register may define multiple states of a GPU.

[0038] Context states may be utilized to determine how an individual processing unit functions, e.g., a vertex fetcher (VFD), a vertex shader (VS), a shader processor, or a geometry processor, and/or in what mode the processing unit functions. In order to do so, GPUs may use context registers and programming data. In some aspects, a GPU may generate a workload, e.g., a vertex or pixel workload, in the pipeline based

on the context register definition of a mode or state. Certain processing units, e.g., a VFD, may use these states to determine certain functions, e.g., how a vertex is assembled. As these modes or states may change, GPUs may need to change the corresponding context. Additionally, the workload that corresponds to the mode or state may follow the changing mode or state.

[0039] FIG. 2 illustrates an example GPU 200 in accordance with one or more techniques of this disclosure. As shown in FIG. 2, GPU 200 includes command processor (CP) 210, draw call packets 212, VFD 220, VS 222, vertex cache (VPC) 224, triangle setup engine (TSE) 226, rasterizer (RAS) 228, Z process engine (ZPE) 230, pixel interpolator (PI) 232, fragment shader (FS) 234, render backend (RB) 236, level 2 (L2) cache (UCHE) 238, and system memory 240. Although FIG. 2 displays that GPU 200 includes processing units 220-238, GPU 200 may include a number of additional processing units. Additionally, processing units 220-238 are merely an example and any combination or order of processing units may be used by GPUs according to the present disclosure. GPU 200 also includes command buffer 250, context register packets 260, and context states 261.

[0040] As shown in FIG. 2, a GPU may utilize a CP, e.g., CP 210, or hardware accelerator to parse a command buffer into context register packets, e.g., context register packets 260, and/or draw call data packets, e.g., draw call packets 212. The CP 210 may then send the context register packets 260 or draw call packets 212 through separate paths to the processing units or blocks in the GPU. Further, the command buffer 250 may alternate different states of context registers and draw calls. For example, a command buffer may be structured in the following manner: context register of context N, draw call(s) of context N, context register of context N+1, and draw call(s) of context N+1.

[0041] GPUs may render images in a variety of different ways. In some instances, GPUs may render an image using rendering and/or tiled rendering. In tiled rendering GPUs, an image may be divided or separated into different sections or tiles. After the division of the image, each section or tile may be rendered separately. Tiled rendering GPUs may divide computer graphics images into a grid format, such that each portion of the grid, i.e., a tile, is separately rendered. In some aspects, during a binning pass, an image may be divided into different bins or tiles. In some aspects, during the binning pass, a visibility stream may be constructed where visible primitives or draw calls may be identified. In contrast to tiled rendering, direct rendering does not divide the frame into smaller bins or tiles. Rather, in direct rendering, the entire frame is

rendered at a single time. Additionally, some types of GPUs may allow for both tiled rendering and direct rendering.

[0042] FIG. 3 is a block diagram 300 that illustrates an example display framework including the processing unit 120, the system memory 124, the display processor 127, and the display(s) 131, as may be identified in connection with the exemplary device 104.

[0043] A GPU may be included in devices that provide content for visual presentation on a display. For example, the processing unit 120 may include a GPU 310 configured to render graphical data for display on a computing device (e.g., the device 104), which may be a computer workstation, a mobile phone, a smartphone or other smart device, an embedded system, a personal computer, a tablet computer, a video game console, and the like. Operations of the GPU 310 may be controlled based on one or more graphics processing commands provided by a CPU 315. The CPU 315 may be configured to execute multiple applications concurrently. In some cases, each of the concurrently executed multiple applications may utilize the GPU 310 simultaneously. Processing techniques may be performed via the processing unit 120 output a frame over physical or wireless communication channels.

[0044] The system memory 124, which may be executed by the processing unit 120, may include a user space 320 and a kernel space 325. The user space 320 (sometimes referred to as an “application space”) may include software application(s) and/or application framework(s). For example, software application(s) may include operating systems, media applications, graphical applications, workspace applications, etc. Application framework(s) may include frameworks used by one or more software applications, such as libraries, services (e.g., display services, input services, etc.), application program interfaces (APIs), etc. The kernel space 325 may further include a display driver 330. The display driver 330 may be configured to control the display processor 127. For example, the display driver 330 may cause the display processor 127 to compose a frame and transmit the data for the frame to a display.

[0045] The display processor 127 includes a display control block 335 and a display interface 340. The display processor 127 may be configured to manipulate functions of the display(s) 131 (e.g., based on an input received from the display driver 330). The display control block 335 may be further configured to output image frames to the display(s) 131 via the display interface 340. In some examples, the display control

block 335 may additionally or alternatively perform post-processing of image data provided based on execution of the system memory 124 by the processing unit 120.

- [0046]** The display interface 340 may be configured to cause the display(s) 131 to display image frames. The display interface 340 may output image data to the display(s) 131 according to an interface protocol, such as, for example, the MIPI DSI (Mobile Industry Processor Interface, Display Serial Interface). That is, the display(s) 131, may be configured in accordance with MIPI DSI standards. The MIPI DSI standard supports a video mode and a command mode. In examples where the display(s) 131 is/are operating in video mode, the display processor 127 may continuously refresh the graphical content of the display(s) 131. For example, the entire graphical content may be refreshed per refresh cycle (e.g., line-by-line). In examples where the display(s) 131 is/are operating in command mode, the display processor 127 may write the graphical content of a frame to a buffer 350.
- [0047]** In some such examples, the display processor 127 may not continuously refresh the graphical content of the display(s) 131. Instead, the display processor 127 may use a vertical synchronization (Vsync) pulse to coordinate rendering and consuming of graphical content at the buffer 350. For example, when a Vsync pulse is generated, the display processor 127 may output new graphical content to the buffer 350. Thus, generation of the Vsync pulse may indicate that current graphical content has been rendered at the buffer 350.
- [0048]** Frames are displayed at the display(s) 131 based on a display controller 345, a display client 355, and the buffer 350. The display controller 345 may receive image data from the display interface 340 and store the received image data in the buffer 350. In some examples, the display controller 345 may output the image data stored in the buffer 350 to the display client 355. Thus, the buffer 350 may represent a local memory to the display(s) 131. In some examples, the display controller 345 may output the image data received from the display interface 340 directly to the display client 355.
- [0049]** The display client 355 may be associated with a touch panel that senses interactions between a user and the display(s) 131. As the user interacts with the display(s) 131, one or more sensors in the touch panel may output signals to the display controller 345 that indicate which of the one or more sensors have sensor activity, a duration of the sensor activity, an applied pressure to the one or more sensor, etc. The display controller 345 may use the sensor outputs to determine a manner in which the user

has interacted with the display(s) 131. The display(s) 131 may be further associated with/include other devices, such as a camera, a microphone, and/or a speaker, that operate in connection with the display client 355.

[0050] Some processing techniques of the device 104 may be performed over three stages (e.g., stage 1: a rendering stage; stage 2: a composition stage; and stage 3: a display/transfer stage). However, other processing techniques may combine the composition stage and the display/transfer stage into a single stage, such that the processing technique may be executed based on two total stages (e.g., stage 1: the rendering stage; and stage 2: the composition/display/transfer stage). During the rendering stage, the GPU 310 may process a content buffer based on execution of an application that generates content on a pixel-by-pixel basis. During the composition and display stage(s), pixel elements may be assembled to form a frame that is transferred to a physical display panel/subsystem (e.g., the displays 131) that displays the frame.

[0051] Instructions executed by a CPU (e.g., software instructions) or a display processor may cause the CPU or the display processor to search for and/or generate a composition strategy for composing a frame based on a dynamic priority and runtime statistics associated with one or more composition strategy groups. A frame to be displayed by a physical display device, such as a display panel, may include a plurality of layers. Also, composition of the frame may be based on combining the plurality of layers into the frame (e.g., based on a frame buffer). After the plurality of layers are combined into the frame, the frame may be provided to the display panel for display thereon. The process of combining each of the plurality of layers into the frame may be referred to as composition, frame composition, a composition procedure, a composition process, or the like.

[0052] Certain types of displays, such as flexible displays, dual displays, triple displays, round displays, and other novel display panel identifier (ID) designs, are becoming increasingly popular. Also, in certain types of displays and devices, display border filling is widely used to match the mechanical/ID design. In some aspects of display processing, border filling for a frame (e.g., display shape border filling) may be performed in a hardware (HW) mixer (e.g., a DPU hardware mixer). This may conflict with display post-processing functionalities. For instance, before all frame processing starts, the border filling lines may already be added. This kind of border filling solution is utilized in some aspects of industry practice and implementation.

- [0053] FIG. 4 is a diagram 400 illustrating an example frame for display processing. As shown in FIG. 4, the frame in diagram 400 may include 20 lines and 12 columns of black pixel filling.
- [0054] FIG. 5 is a diagram 500 illustrating an example border filling process for display processing. As shown in FIG. 5, a number of lines (e.g., 12 lines) of black pixel filling may be added to a frame during a border filling process. For example, this process may be performed by a layer mixer or hardware mixer.
- [0055] In a border filling pipeline, all blocks and processing that are after the hardware mixer (i.e., frame data generation) may process additional border filling lines. This may cause the border filling lines to be erroneously processed. Additionally, other types of display processing blocks and functions may suffer based on this erroneous processing. Some types of displays, such as dual flexible display projects/devices, may benefit from a solution to the border filling function problem. This problem may also be applicable to flexible IDs and flexible display devices. Accordingly, it may be beneficial to utilize a border filling function without any errors. Further, it may be beneficial to utilize DPU and display processing features and functionalities that are related to the border filling function without any limitations.
- [0056] Aspects of the present disclosure may utilize a border filling function without any border filling errors. Aspects of the present disclosure may also utilize display processing features without any limitations. For instance, aspects presented herein may utilize DPU and display processing features and functionalities that are related to the border filling function without any limitations.
- [0057] In some aspects, during a panel initiation procedure, aspects presented herein may send first frame data with border filling color. For example, the first frame data may be black (e.g., pure black 0) or any appropriate filling color. The resolution may be a certain type of resolution (e.g., display panel native 1080 x 2400), where a number of lines are used for border filling (e.g., 90 widths and 300 lines are used for border filling). In some aspects, during run-time, aspects presented herein may keep all display composition/mixing/processing intact and configure display frame resolutions to valid pixel regions. As such, a DPU and whole display processing stack may not handle border filling lines. Aspects of the present disclosure may configure DPU/mixer/processing blocks resolutions to a certain resolution (e.g., 1010 x 2100), which may correspond to valid pixel regions. Also, aspects of the present disclosure

may configure all operating system (OS) and application resolutions for rendering and user interface (UI) design to a particular resolution (e.g., 1010 x 2100).

[0058] In some instances, during run-time, all frames that are transmitted may include a display serial interface (DSI) valid region partial updating (e.g., 1010 x 2100). This sequential partial update may be performed by sending the rectangle coordinates (e.g., 1010 x 2100) once to the panel, and then continuing a valid region refresh of a same resolution (e.g., 1010 x 2100). Alternatively, aspects presented herein may send the rectangle coordinates per-frame (e.g., 1010 x 2100). The display border filling shapes and/or valid display regions may be adjusted during run-time to match device adjustments for ID/scenarios/power/always-on display (AOD). Further, each time a display border filling shape and valid display region changes, one frame black pixel (e.g., panel native resolution) or other color filling pixels may be sent to the panel. Based on this, the DPU, the OS, and the whole device may be configured to the updated valid region resolution. Also, updated rectangle coordinates and updated valid region resolutions may be sent to the panel.

[0059] FIG. 6 is a flowchart 600 of an example method of display processing. As shown in FIG. 6, flowchart 600 includes a display panel flexible shape border filling flow. At a first step, DPUs herein may send, to a panel, a first frame (e.g., a frame with 1080 x 2400 resolution) with black filling pixels. At a second step, DPUs herein may send, to the panel, a sequential frame partial update (PU) (e.g., an update of 1010 x 2100 resolution). DPUs herein may also configure a host device display processing and rendering resolution to a certain resolution (e.g., 1010 x 2100 resolution). At a third step, DPUs herein may send, to the panel, an Nth frame (e.g., a frame with 1080 x 2400 resolution) with black filling pixels. At a fourth step, DPUs herein may send, to the panel, a sequential frame partial update (PU) (e.g., an update of 800 x 1400 resolution). DPUs herein may also configure a host device display processing and rendering resolution to a certain resolution (e.g., 800 x 1400 resolution).

[0060] FIG. 7A is a diagram 700 illustrating an example frame for display processing. As shown in FIG. 7A, diagram 700 includes a border fill with a flexible resolution and shape. FIG. 7B is a diagram 750 illustrating an example frame for display processing. As shown in FIG. 7B, diagram 750 depicts a first frame black pixel (e.g., with resolution 1080 x 2400) that is utilized for border filling a frame. For instance, the border filling may be 90 widths and 300 lines of black pixel filling that corresponds to a valid pixel region of a certain resolution (e.g., 1010 x 2100 resolution).

- [0061]** Aspects of the present disclosure may include a number of benefits or advantages. For instance, aspects of the present disclosure may provide a display border filling solution with full display processing features and functions concurrently running. Aspects presented herein may allow for a flexible display border fill and a flexible resolution with full display processing features and functions. Aspects presented herein may also be utilized for flexible extendable displays with flexible resolutions. Further, aspects presented herein may reduce the amount of DSI bandwidth and power utilized by avoiding redundant pixel transmissions. For example, aspects presented herein may allow valid pixels to be transmitted.
- [0062]** When utilizing aspects presented herein, DPUs may use border filling with a partial update and full frame color. Also, when utilizing aspects presented herein, DPUs may directly align the OS resolution with partial update regions. Further, aspects presented herein may allow for seamless resolution switching for flexible display and flexible ID. For instance, aspects presented herein may directly use a partial update to seamless update and change device OS resolutions and contents. Additionally, for a DSI link transmission, aspects of the present disclosure may transmit valid pixel values, which may reduce the amount of power and bandwidth utilized.
- [0063]** FIG. 8 is a communication flow diagram 800 of display processing in accordance with one or more techniques of this disclosure. As shown in FIG. 8, diagram 800 includes example communications between DPU 802 (or other display processor), application 804 (e.g., a game), and display 806 (e.g., a display panel), in accordance with one or more techniques of this disclosure.
- [0064]** At 810, DPU 802 may transmit, to a display panel (e.g., display 806), a first frame including a border filling region with a plurality of first pixels (e.g., frame 812), where each of the plurality of first pixels includes a border filling color. The border filling color may be at least one of black, gray, blue, or red.
- [0065]** At 820, DPU 802 may configure at least one second frame including a valid pixel region with a plurality of second pixels (e.g., frame 832), where each of the plurality of second pixels includes content data and a second pixel resolution. The at least one second frame may be configured at a display processing unit (DPU).
- [0066]** At 830, DPU 802 may transmit, to the display panel (e.g., display 806), the at least one second frame including the valid pixel region with the plurality of second pixels (e.g., frame 832).

- [0067] At 840, DPU 802 may receive, from at least one application or an operating system (e.g., application 804), an indication of a resolution update for the at least one second frame (e.g., indication 842). The second pixel resolution may be aligned with a pixel resolution of the at least one application or the operating system. The at least one application may be at least one user device or at least one operating application for the operating system.
- [0068] At 850, DPU 802 may adjust the valid pixel region of the at least one second frame based on the indication of the resolution update.
- [0069] At 860, DPU 802 may configure, upon adjusting the valid pixel region of the at least one second frame, an updated pixel resolution of the plurality of second pixels of the at least one second frame based on the indication of the resolution update. In some aspects, the updated pixel resolution of the plurality of second pixels may be aligned with an updated resolution of the at least one application.
- [0070] At 870, DPU 802 may retransmit, to the display panel (e.g., display 806), the first frame including the border filling region with the plurality of first pixels (e.g., frame 872).
- [0071] At 880, DPU 802 may transmit, to the display panel (e.g., display 806), the at least one second frame including the adjusted valid pixel region and the updated pixel resolution of the plurality of second pixels (e.g., frame 882).
- [0072] FIG. 9 is a flowchart 900 of an example method of display processing in accordance with one or more techniques of this disclosure. The method may be performed by a DPU, such as an apparatus for display processing, a display processor, a wireless communication device, and/or any apparatus that may perform display processing as used in connection with the examples of FIGs. 1-8.
- [0073] At 902, the DPU may transmit, to a display panel, a first frame including a border filling region with a plurality of first pixels, where each of the plurality of first pixels includes a border filling color, as described in connection with the examples in FIGs. 1-8. For example, as described in 810 of FIG. 8, DPU 802 may transmit, to a display panel, a first frame including a border filling region with a plurality of first pixels, where each of the plurality of first pixels includes a border filling color. Further, step 902 may be performed by display processor 127 in FIG. 1. The border filling color may be at least one of black, gray, blue, or red.
- [0074] At 904, the DPU may configure at least one second frame including a valid pixel region with a plurality of second pixels, where each of the plurality of second pixels

includes content data and a second pixel resolution, as described in connection with the examples in FIGs. 1-8. For example, as described in 820 of FIG. 8, DPU 802 may configure at least one second frame including a valid pixel region with a plurality of second pixels, where each of the plurality of second pixels includes content data and a second pixel resolution. Further, step 904 may be performed by display processor 127 in FIG. 1. The at least one second frame may be configured at a display processing unit (DPU).

[0075] At 906, the DPU may transmit, to the display panel, the at least one second frame including the valid pixel region with the plurality of second pixels, as described in connection with the examples in FIGs. 1-8. For example, as described in 830 of FIG. 8, DPU 802 may transmit, to the display panel, the at least one second frame including the valid pixel region with the plurality of second pixels. Further, step 906 may be performed by display processor 127 in FIG. 1.

[0076] At 908, the DPU may receive, from at least one application or an operating system, an indication of a resolution update for the at least one second frame, as described in connection with the examples in FIGs. 1-8. For example, as described in 840 of FIG. 8, DPU 802 may receive, from at least one application or an operating system, an indication of a resolution update for the at least one second frame. Further, step 908 may be performed by display processor 127 in FIG. 1. The second pixel resolution may be aligned with a pixel resolution of the at least one application or the operating system. The at least one application may be at least one user device or at least one operating application for the operating system.

[0077] At 910, the DPU may adjust the valid pixel region of the at least one second frame based on the indication of the resolution update, as described in connection with the examples in FIGs. 1-8. For example, as described in 850 of FIG. 8, DPU 802 may adjust the valid pixel region of the at least one second frame based on the indication of the resolution update. Further, step 910 may be performed by display processor 127 in FIG. 1.

[0078] At 912, the DPU may configure, upon adjusting the valid pixel region of the at least one second frame, an updated pixel resolution of the plurality of second pixels of the at least one second frame based on the indication of the resolution update, as described in connection with the examples in FIGs. 1-8. For example, as described in 860 of FIG. 8, DPU 802 may configure, upon adjusting the valid pixel region of the at least one second frame, an updated pixel resolution of the plurality of second pixels of the

at least one second frame based on the indication of the resolution update. Further, step 912 may be performed by display processor 127 in FIG. 1. In some aspects, the updated pixel resolution of the plurality of second pixels may be aligned with an updated resolution of the at least one application.

[0079] At 914, the DPU may retransmit, to the display panel, the first frame including the border filling region with the plurality of first pixels, as described in connection with the examples in FIGs. 1-8. For example, as described in 870 of FIG. 8, DPU 802 may retransmit, to the display panel, the first frame including the border filling region with the plurality of first pixels. Further, step 914 may be performed by display processor 127 in FIG. 1.

[0080] At 916, the DPU may transmit, to the display panel, the at least one second frame including the adjusted valid pixel region and the updated pixel resolution of the plurality of second pixels, as described in connection with the examples in FIGs. 1-8. For example, as described in 880 of FIG. 8, DPU 802 may transmit, to the display panel, the at least one second frame including the adjusted valid pixel region and the updated pixel resolution of the plurality of second pixels. Further, step 916 may be performed by display processor 127 in FIG. 1.

[0081] In configurations, a method or an apparatus for display processing is provided. The apparatus may be a DPU, a display processor, or some other processor that may perform display processing. In aspects, the apparatus may be the display processor 127 within the device 104, or may be some other hardware within the device 104 or another device. The apparatus, e.g., display processor 127, may include means for transmitting, to a display panel, a first frame including a border filling region with a plurality of first pixels, where each of the plurality of first pixels includes a border filling color; means for configuring at least one second frame including a valid pixel region with a plurality of second pixels, where each of the plurality of second pixels includes content data and a second pixel resolution; means for transmitting, to the display panel, the at least one second frame including the valid pixel region with the plurality of second pixels; means for receiving, from at least one application or an operating system, an indication of a resolution update for the at least one second frame; means for adjusting the valid pixel region of the at least one second frame based on the indication of the resolution update; means for configuring, upon adjusting the valid pixel region of the at least one second frame, an updated pixel resolution of the plurality of second pixels of the at least one second frame based on

the indication of the resolution update; means for retransmitting, to the display panel, the first frame including the border filling region with the plurality of first pixels; and means for transmitting, to the display panel, the at least one second frame including the adjusted valid pixel region and the updated pixel resolution of the plurality of second pixels.

[0082] The subject matter described herein may be implemented to realize one or more benefits or advantages. For instance, the described display processing techniques may be used by a DPU, a display processor, or some other processor that may perform display processing to implement the sequential flexible display resolution techniques described herein. This may also be accomplished at a low cost compared to other display processing techniques. Moreover, the display processing techniques herein may improve or speed up data processing or execution. Further, the display processing techniques herein may improve resource or data utilization and/or resource efficiency. Additionally, aspects of the present disclosure may utilize sequential flexible display resolution techniques in order to improve memory bandwidth efficiency and/or increase processing speed at a DPU.

[0083] It is understood that the specific order or hierarchy of blocks in the processes / flowcharts disclosed is an illustration of example approaches. Based upon design preferences, it is understood that the specific order or hierarchy of blocks in the processes / flowcharts may be rearranged. Further, some blocks may be combined or omitted. The accompanying method claims present elements of the various blocks in a sample order, and are not meant to be limited to the specific order or hierarchy presented.

[0084] The previous description is provided to enable any person skilled in the art to practice the various aspects described herein. Various modifications to these aspects will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other aspects. Thus, the claims are not intended to be limited to the aspects shown herein, but is to be accorded the full scope consistent with the language of the claims, wherein reference to an element in the singular is not intended to mean “one and only one” unless specifically so stated, but rather “one or more.” The word “exemplary” is used herein to mean “serving as an example, instance, or illustration.” Any aspect described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other aspects.

- [0085]** Unless specifically stated otherwise, the term “some” refers to one or more and the term “or” may be interpreted as “and/or” where context does not dictate otherwise. Combinations such as “at least one of A, B, or C,” “one or more of A, B, or C,” “at least one of A, B, and C,” “one or more of A, B, and C,” and “A, B, C, or any combination thereof” include any combination of A, B, and/or C, and may include multiples of A, multiples of B, or multiples of C. Specifically, combinations such as “at least one of A, B, or C,” “one or more of A, B, or C,” “at least one of A, B, and C,” “one or more of A, B, and C,” and “A, B, C, or any combination thereof” may be A only, B only, C only, A and B, A and C, B and C, or A and B and C, where any such combinations may contain one or more member or members of A, B, or C. All structural and functional equivalents to the elements of the various aspects described throughout this disclosure that are known or later come to be known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the claims. Moreover, nothing disclosed herein is intended to be dedicated to the public regardless of whether such disclosure is explicitly recited in the claims. The words “module,” “mechanism,” “element,” “device,” and the like may not be a substitute for the word “means.” As such, no claim element is to be construed as a means plus function unless the element is expressly recited using the phrase “means for.”
- [0086]** In one or more examples, the functions described herein may be implemented in hardware, software, firmware, or any combination thereof. For example, although the term “processing unit” has been used throughout this disclosure, such processing units may be implemented in hardware, software, firmware, or any combination thereof. If any function, processing unit, technique described herein, or other module is implemented in software, the function, processing unit, technique described herein, or other module may be stored on or transmitted over as one or more instructions or code on a computer-readable medium.
- [0087]** In accordance with this disclosure, the term “or” may be interpreted as “and/or” where context does not dictate otherwise. Additionally, while phrases such as “one or more” or “at least one” or the like may have been used for some features disclosed herein but not others, the features for which such language was not used may be interpreted to have such a meaning implied where context does not dictate otherwise.
- [0088]** In one or more examples, the functions described herein may be implemented in hardware, software, firmware, or any combination thereof. For example, although the

term “processing unit” has been used throughout this disclosure, such processing units may be implemented in hardware, software, firmware, or any combination thereof. If any function, processing unit, technique described herein, or other module is implemented in software, the function, processing unit, technique described herein, or other module may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. Computer-readable media may include computer data storage media or communication media including any medium that facilitates transfer of a computer program from one place to another. In this manner, computer-readable media generally may correspond to (1) tangible computer-readable storage media, which is non-transitory or (2) a communication medium such as a signal or carrier wave. Data storage media may be any available media that may be accessed by one or more computers or one or more processors to retrieve instructions, code and/or data structures for implementation of the techniques described in this disclosure. By way of example, and not limitation, such computer-readable media may comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media. A computer program product may include a computer-readable medium.

[0089] The code may be executed by one or more processors, such as one or more digital signal processors (DSPs), general purpose microprocessors, application specific integrated circuits (ASICs), arithmetic logic units (ALUs), field programmable logic arrays (FPGAs), or other equivalent integrated or discrete logic circuitry. Accordingly, the term “processor,” as used herein may refer to any of the foregoing structure or any other structure suitable for implementation of the techniques described herein. Also, the techniques could be fully implemented in one or more circuits or logic elements.

[0090] The techniques of this disclosure may be implemented in a wide variety of devices or apparatuses, including a wireless handset, an integrated circuit (IC) or a set of ICs, e.g., a chip set. Various components, modules or units are described in this disclosure to emphasize functional aspects of devices configured to perform the disclosed techniques, but do not necessarily need realization by different hardware units.

Rather, as described above, various units may be combined in any hardware unit or provided by a collection of inter-operative hardware units, including one or more processors as described above, in conjunction with suitable software and/or firmware. Accordingly, the term “processor,” as used herein may refer to any of the foregoing structure or any other structure suitable for implementation of the techniques described herein. Also, the techniques may be fully implemented in one or more circuits or logic elements.

- [0091]** The following aspects are illustrative only and may be combined with other aspects or teachings described herein, without limitation.
- [0092]** Aspect 1 is an apparatus for display processing including at least one processor coupled to a memory and configured to: transmit, to a display panel, a first frame including a border filling region with a plurality of first pixels, where each of the plurality of first pixels includes a border filling color; configure at least one second frame including a valid pixel region with a plurality of second pixels, where each of the plurality of second pixels includes content data and a second pixel resolution; transmit, to the display panel, the at least one second frame including the valid pixel region with the plurality of second pixels; receive, from at least one application or an operating system, an indication of a resolution update for the at least one second frame; and adjust the valid pixel region of the at least one second frame based on the indication of the resolution update.
- [0093]** Aspect 2 is the apparatus of aspect 1, where the at least one processor is further configured to: configure, upon adjusting the valid pixel region of the at least one second frame, an updated pixel resolution of the plurality of second pixels of the at least one second frame based on the indication of the resolution update.
- [0094]** Aspect 3 is the apparatus of any of aspects 1 and 2, where the at least one processor is further configured to: retransmit, to the display panel, the first frame including the border filling region with the plurality of first pixels.
- [0095]** Aspect 4 is the apparatus of any of aspects 1 to 3, where the at least one processor is further configured to: transmit, to the display panel, the at least one second frame including the adjusted valid pixel region and the updated pixel resolution of the plurality of second pixels.
- [0096]** Aspect 5 is the apparatus of any of aspects 1 to 4, where the updated pixel resolution of the plurality of second pixels is aligned with an updated resolution of the at least one application.

- [0097]** Aspect 6 is the apparatus of any of aspects 1 to 5, where the second pixel resolution is aligned with a pixel resolution of the at least one application or the operating system.
- [0098]** Aspect 7 is the apparatus of any of aspects 1 to 6, where the at least one application is at least one user device or at least one operating application for the operating system.
- [0099]** Aspect 8 is the apparatus of any of aspects 1 to 7, where the border filling color is at least one of black, gray, blue, or red.
- [0100]** Aspect 9 is the apparatus of any of aspects 1 to 8, where the at least one second frame is configured at a display processing unit (DPU).
- [0101]** Aspect 10 is the apparatus of any of aspects 1 to 9, further including at least one of an antenna or a transceiver coupled to the at least one processor.
- [0102]** Aspect 11 is a method of display processing for implementing any of aspects 1 to 10.
- [0103]** Aspect 12 is an apparatus for display processing including means for implementing any of aspects 1 to 10.
- [0104]** Aspect 13 is a non-transitory computer-readable medium storing computer executable code, the code when executed by at least one processor causes the at least one processor to implement any of aspects 1 to 10.

CLAIMS

WHAT IS CLAIMED IS:

1. An apparatus for display processing, comprising:
 - a memory; and
 - at least one processor coupled to the memory and configured to:
 - transmit, to a display panel, a first frame including a border filling region with a plurality of first pixels, wherein each of the plurality of first pixels includes a border filling color;
 - configure at least one second frame including a valid pixel region with a plurality of second pixels, wherein each of the plurality of second pixels includes content data and a second pixel resolution;
 - transmit, to the display panel, the at least one second frame including the valid pixel region with the plurality of second pixels;
 - receive, from at least one application or an operating system, an indication of a resolution update for the at least one second frame; and
 - adjust the valid pixel region of the at least one second frame based on the indication of the resolution update.
2. The apparatus of claim 1, wherein the at least one processor is further configured to:
 - configure, upon adjusting the valid pixel region of the at least one second frame, an updated pixel resolution of the plurality of second pixels of the at least one second frame based on the indication of the resolution update.
3. The apparatus of claim 2, wherein the at least one processor is further configured to:
 - retransmit, to the display panel, the first frame including the border filling region with the plurality of first pixels.
4. The apparatus of claim 2, wherein the at least one processor is further configured to:
 - transmit, to the display panel, the at least one second frame including the adjusted valid pixel region and the updated pixel resolution of the plurality of second pixels.

5. The apparatus of claim 2, wherein the updated pixel resolution of the plurality of second pixels is aligned with an updated resolution of the at least one application.
6. The apparatus of claim 1, wherein the second pixel resolution is aligned with a pixel resolution of the at least one application or the operating system.
7. The apparatus of claim 1, wherein the at least one application is at least one user device or at least one operating application for the operating system.
8. The apparatus of claim 1, wherein the border filling color is at least one of black, gray, blue, or red.
9. The apparatus of claim 1, wherein the at least one second frame is configured at a display processing unit (DPU).
10. The apparatus of claim 1, further comprising at least one of an antenna or a transceiver coupled to the at least one processor.
11. A method of display processing, comprising:
 - transmitting, to a display panel, a first frame including a border filling region with a plurality of first pixels, wherein each of the plurality of first pixels includes a border filling color;
 - configuring at least one second frame including a valid pixel region with a plurality of second pixels, wherein each of the plurality of second pixels includes content data and a second pixel resolution;
 - transmitting, to the display panel, the at least one second frame including the valid pixel region with the plurality of second pixels;
 - receiving, from at least one application or an operating system, an indication of a resolution update for the at least one second frame; and
 - adjusting the valid pixel region of the at least one second frame based on the indication of the resolution update.
12. The method of claim 11, further comprising:

configuring, upon adjusting the valid pixel region of the at least one second frame, an updated pixel resolution of the plurality of second pixels of the at least one second frame based on the indication of the resolution update.

13. The method of claim 12, further comprising:

retransmitting, to the display panel, the first frame including the border filling region with the plurality of first pixels.

14. The method of claim 12, further comprising:

transmitting, to the display panel, the at least one second frame including the adjusted valid pixel region and the updated pixel resolution of the plurality of second pixels.

15. The method of claim 12, wherein the updated pixel resolution of the plurality of second pixels is aligned with an updated resolution of the at least one application.

16. The method of claim 11, wherein the second pixel resolution is aligned with a pixel resolution of the at least one application or the operating system.

17. The method of claim 11, wherein the at least one application is at least one user device or at least one operating application for the operating system.

18. The method of claim 11, wherein the border filling color is at least one of black, gray, blue, or red.

19. The method of claim 11, wherein the at least one second frame is configured at a display processing unit (DPU).

20. An apparatus for display processing, comprising:

means for transmitting, to a display panel, a first frame including a border filling region with a plurality of first pixels, wherein each of the plurality of first pixels includes a border filling color;

means for configuring at least one second frame including a valid pixel region with a plurality of second pixels, wherein each of the plurality of second pixels includes content data and a second pixel resolution;

means for transmitting, to the display panel, the at least one second frame including the valid pixel region with the plurality of second pixels;

means for receiving, from at least one application or an operating system, an indication of a resolution update for the at least one second frame; and

means for adjusting the valid pixel region of the at least one second frame based on the indication of the resolution update.

21. The apparatus of claim 20, further comprising at least one of an antenna or a transceiver.

22. The apparatus of claim 20, further comprising means to perform the method of any of claims 11-19.

23. A non-transitory computer-readable medium storing computer executable code for display processing, the code when executed by a processor causes the processor to:

transmit, to a display panel, a first frame including a border filling region with a plurality of first pixels, wherein each of the plurality of first pixels includes a border filling color;

configure at least one second frame including a valid pixel region with a plurality of second pixels, wherein each of the plurality of second pixels includes content data and a second pixel resolution;

transmit, to the display panel, the at least one second frame including the valid pixel region with the plurality of second pixels;

receive, from at least one application or an operating system, an indication of a resolution update for the at least one second frame; and

adjust the valid pixel region of the at least one second frame based on the indication of the resolution update.

24. The computer-readable medium of claim 23, wherein the code when executed by the processor causes the processor to perform the method of any of claims 11-19.

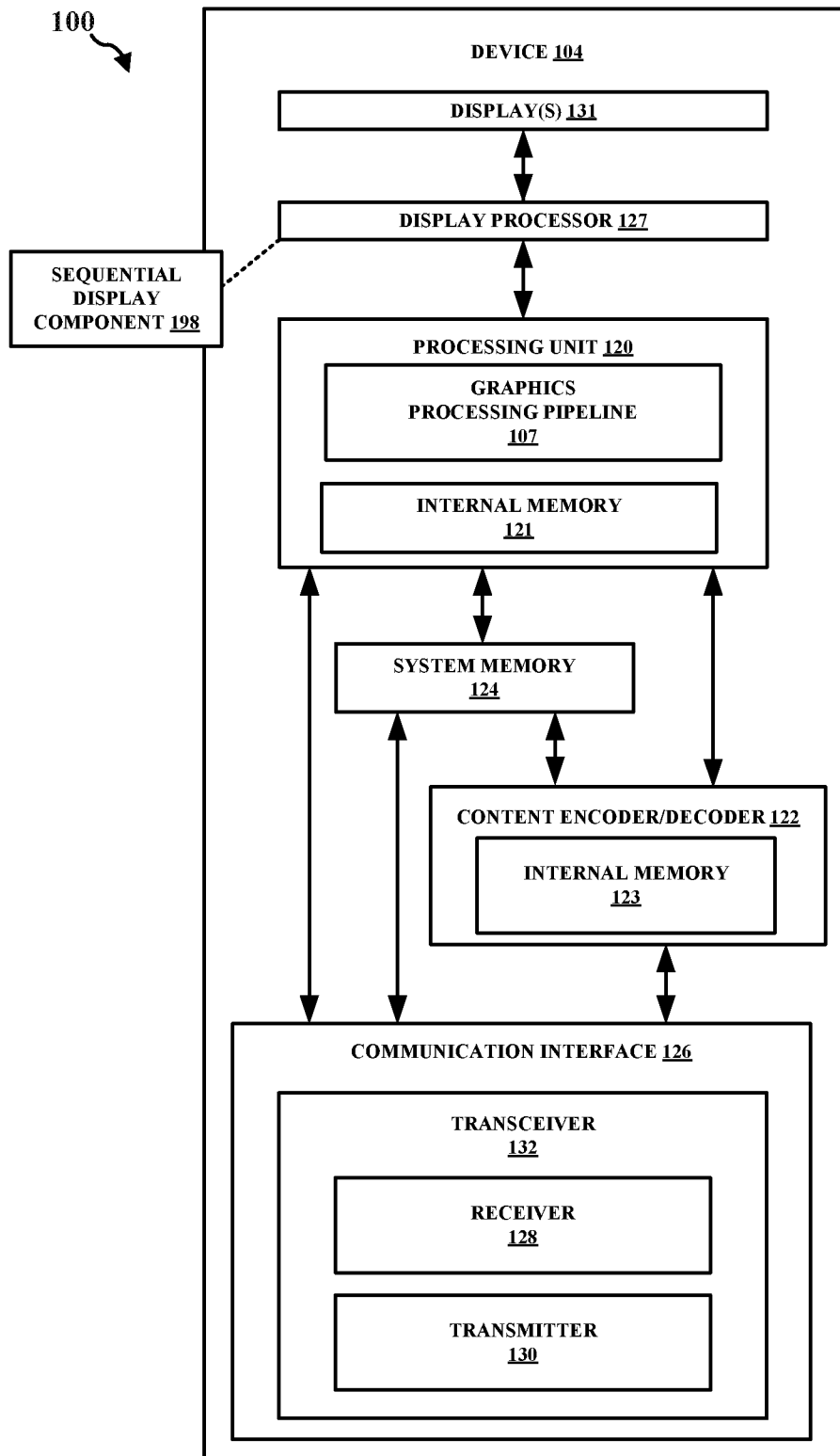
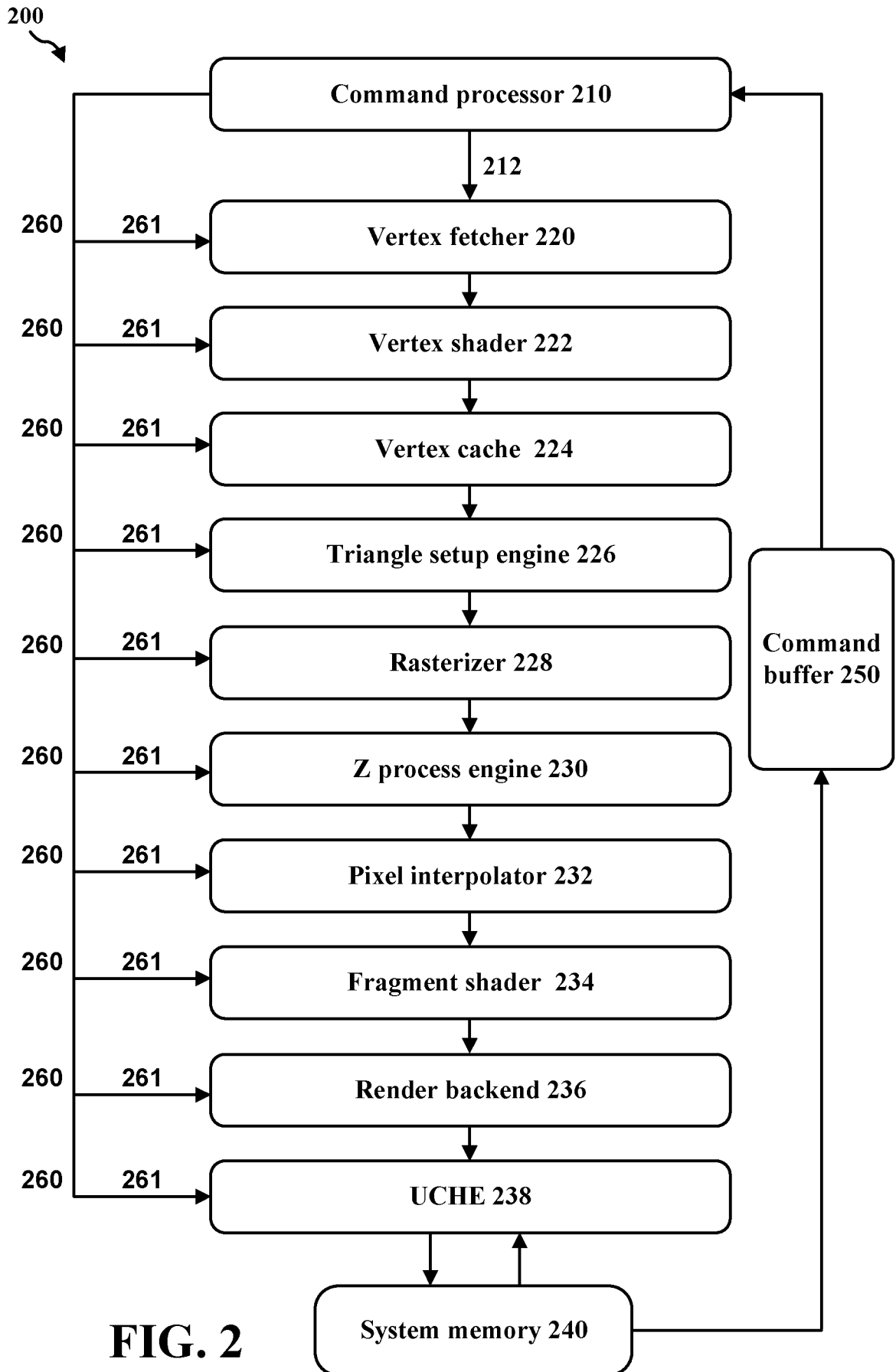


FIG. 1



300 ↗

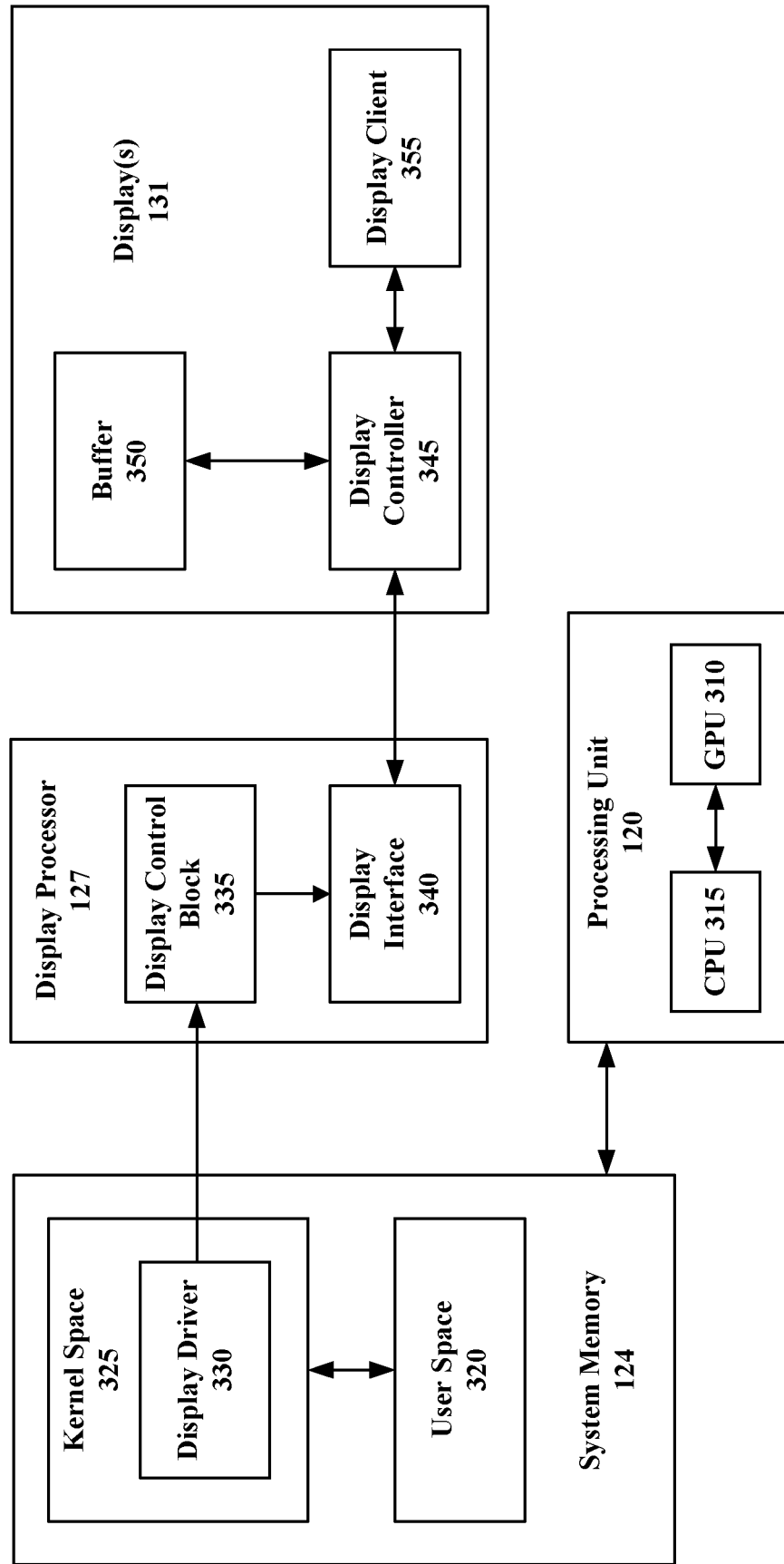


FIG. 3

400 ↗

20 Lines – 12 columns black pixel filling

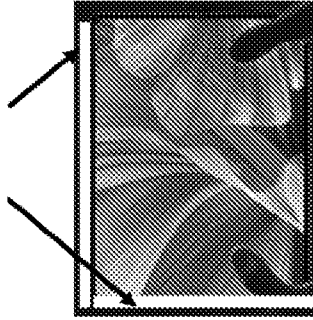


FIG. 4

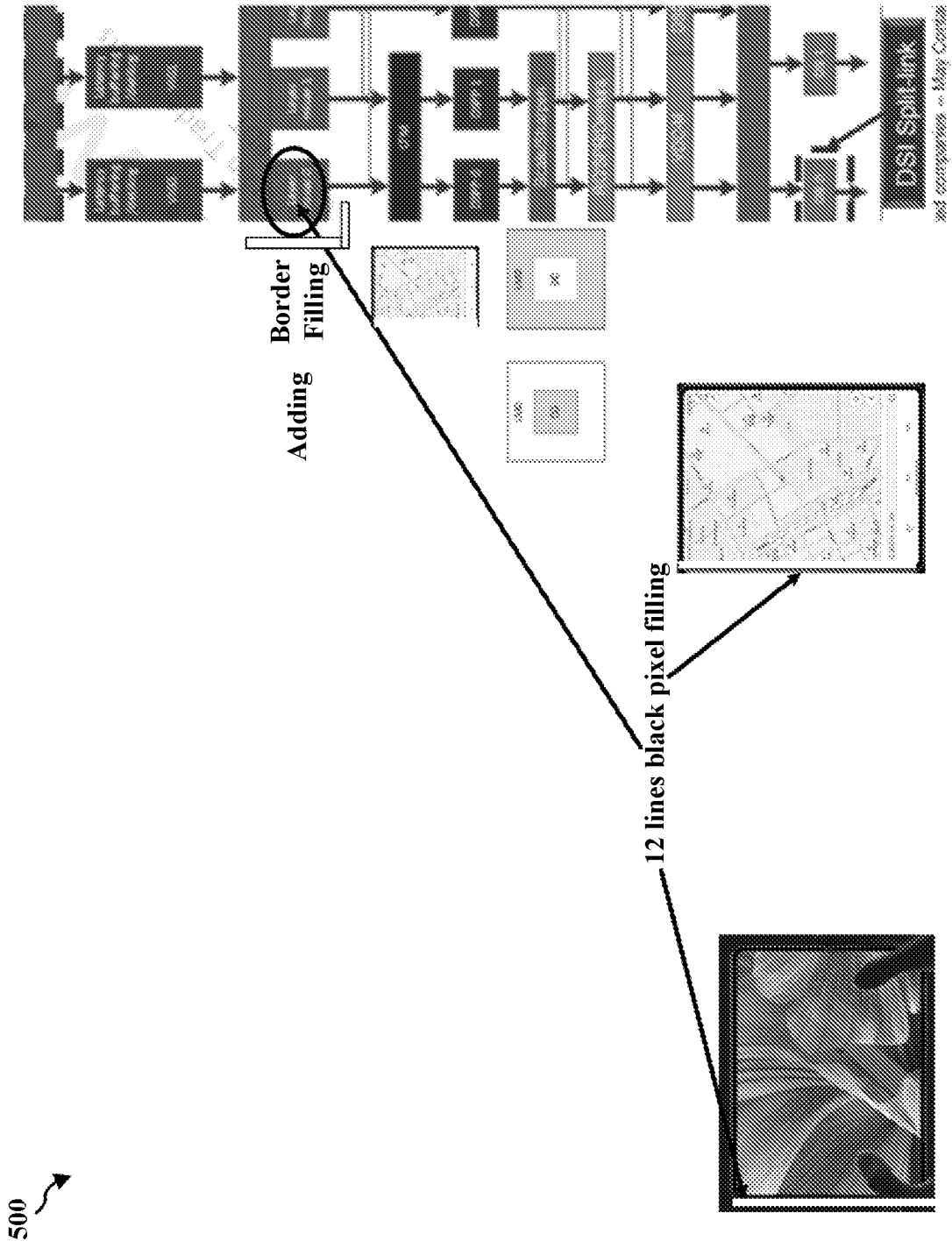


FIG. 5

600 ↗

Display Panel Flexible Shape Border Filling Flow

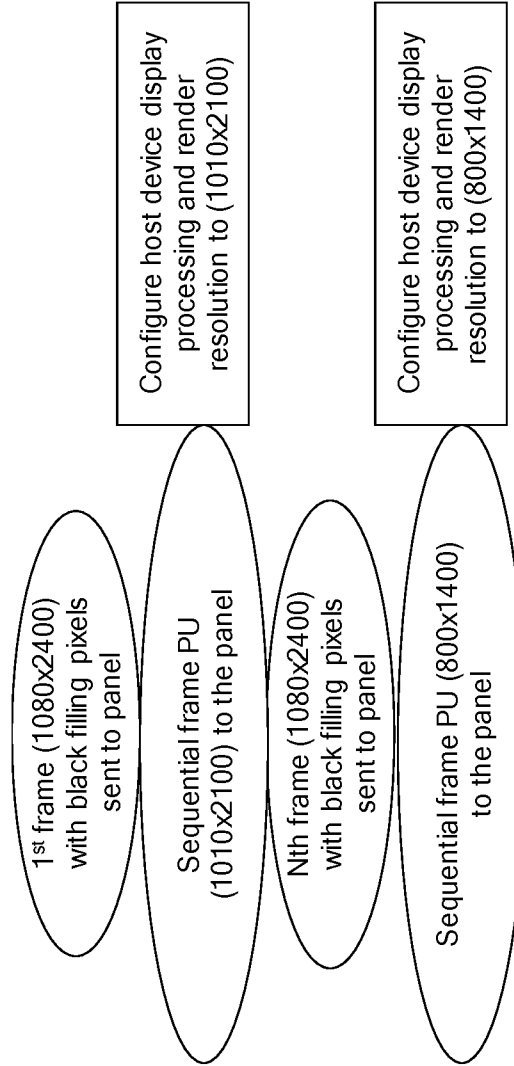
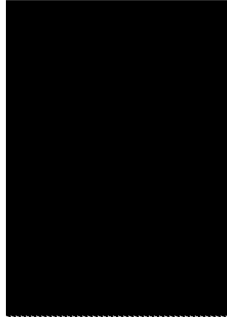


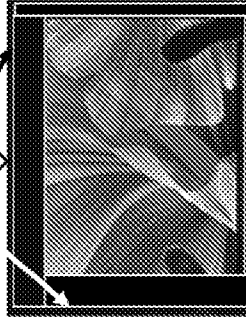
FIG. 6

750 ↗

1080x2400 1st frame black pixel



90 widths - 300 lines black pixel filling
1010x2100 valid region



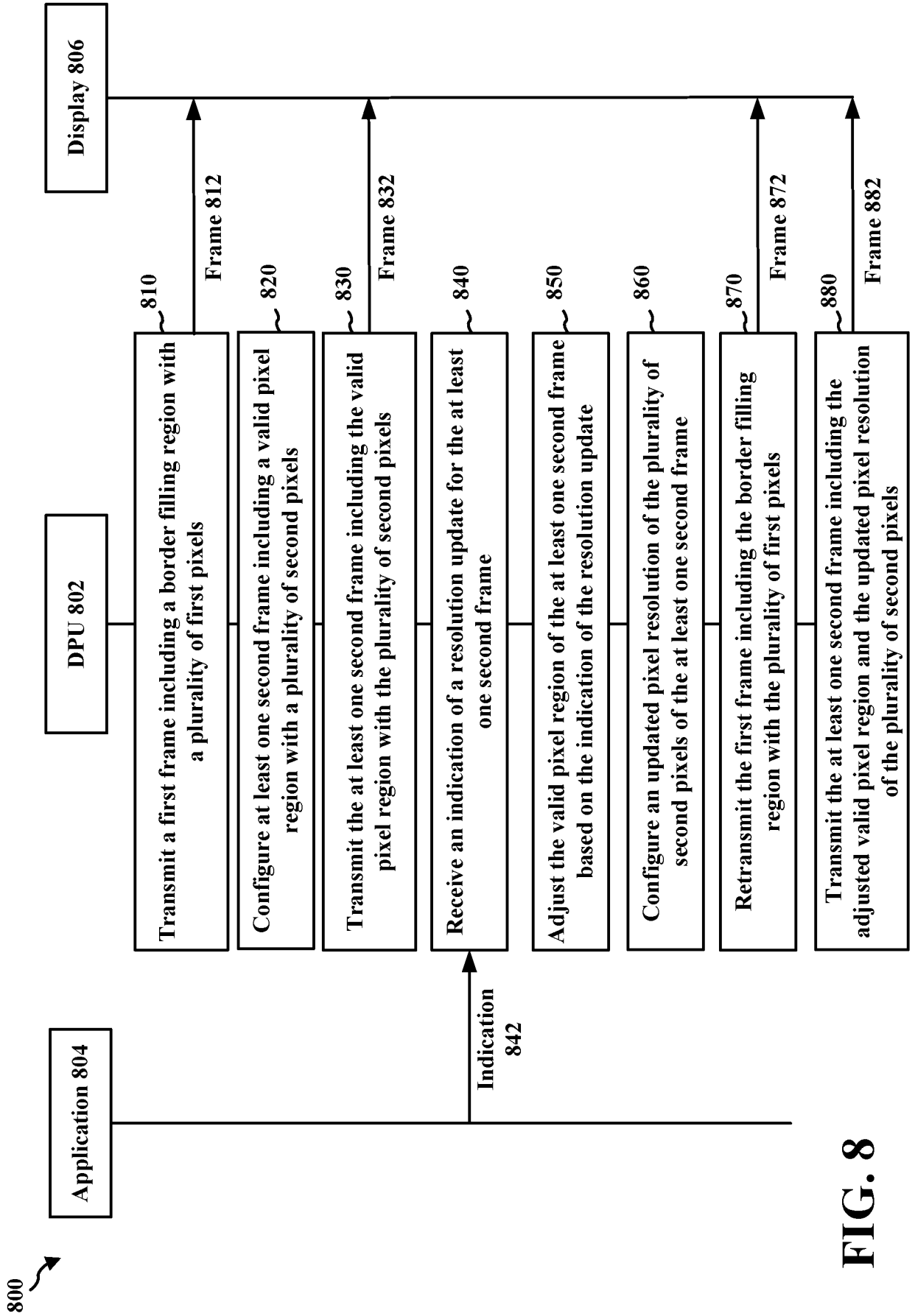
700 ↗

Flexible Resolution and
Shape, Border Fill



FIG. 7A

FIG. 7B



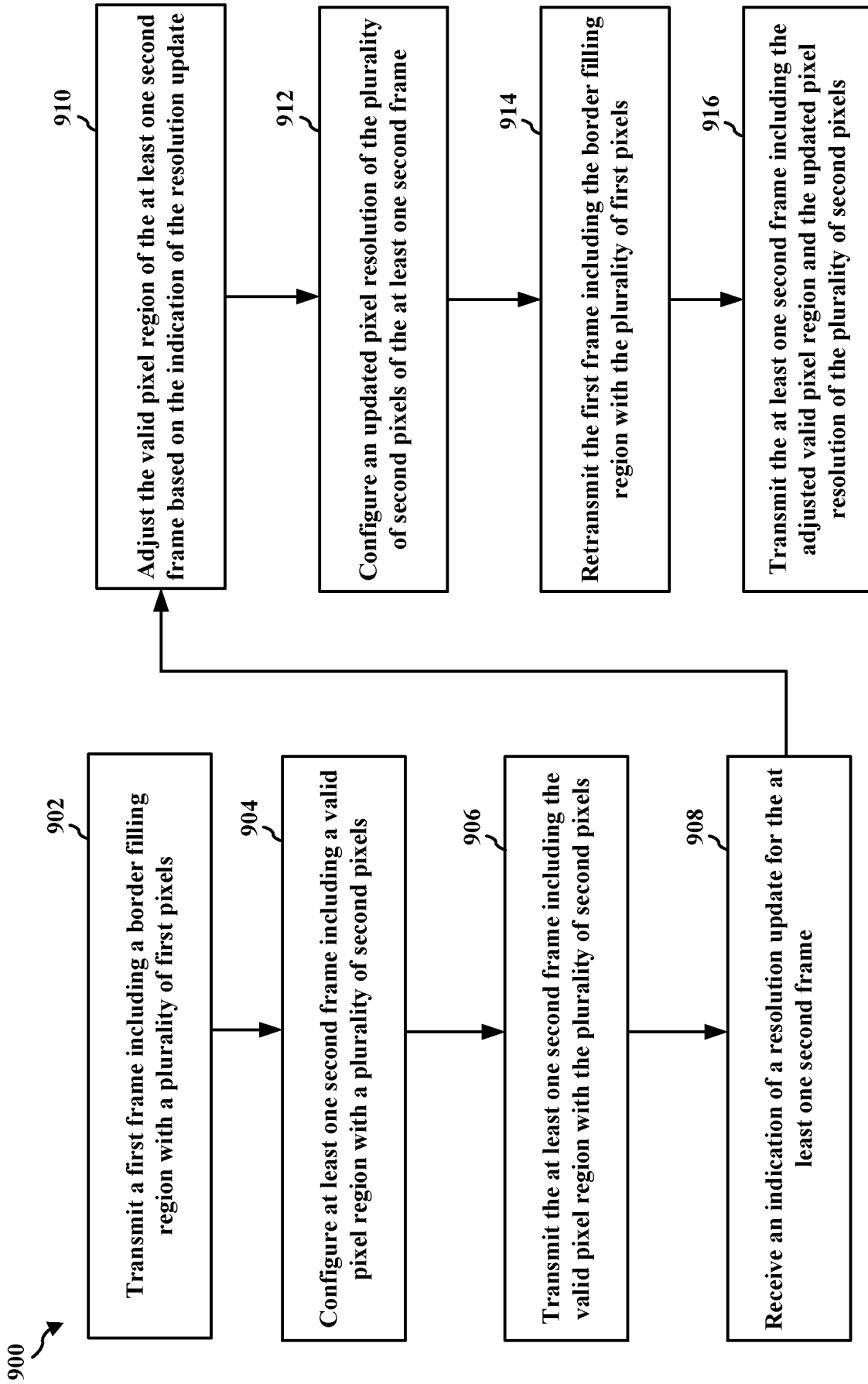


FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2022/074517

A. CLASSIFICATION OF SUBJECT MATTER		
G06F 3/147(2006.01)i; H04N 5/265(2006.01)i; G09G 5/391(2006.01)i		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) G06F; H04N; G09G		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) CNTXT, CJFD, ENTXTC, ENTXT: flexible, display+, panel, pixel?, transmit+, send+, sent, frame?, border?, region?, block?, black, resolution, DPU		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 109891381 A (GOOGLE INC.) 14 June 2019 (2019-06-14) the whole document	1-24
A	CN 111034193 A (QUALCOMM INC.) 17 April 2020 (2020-04-17) the whole document	1-24
A	CN 111915987 A (LG DISPLAY CO., LTD.) 10 November 2020 (2020-11-10) the whole document	1-24
A	CN 103379335 A (VIXS SYSTEMS INC.) 30 October 2013 (2013-10-30) the whole document	1-24
A	US 2016112638 A1 (MICROSOFT CORP.) 21 April 2016 (2016-04-21) the whole document	1-24
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 08 October 2022		Date of mailing of the international search report 14 October 2022
Name and mailing address of the ISA/CN National Intellectual Property Administration, PRC 6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China Facsimile No. (86-10)62019451		Authorized officer WANG, Yang Telephone No. 86-10-62089466

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2022/074517

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	109891381	A	14 June 2019	WO	2018089105	A1	17 May 2018
				DE	202017105882	U1	17 April 2018
				EP	3538986	A1	18 September 2019
				US	2018136720	A1	17 May 2018

CN	111034193	A	17 April 2020	US	2019068885	A1	28 February 2019
				WO	2019045876	A1	07 March 2019

CN	111915987	A	10 November 2020	KR	20200128925	A	17 November 2020
				US	2020357362	A1	12 November 2020

CN	103379335	A	30 October 2013	US	2013279563	A1	24 October 2013
				EP	2654298	A2	23 October 2013

US	2016112638	A1	21 April 2016	WO	2016061012	A1	21 April 2016
