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(54) Method of addressing a liquid crystal display

(57) A ferroelectric liquid crystal display comprises data electrodes connected to a data signal generator and strobe electrodes connected to a strobe signal generator. The strobe signal generator 6 supplies strobe signals Vs1 to Vs4 in sequence to the strobe electrodes and the data signal generator supplies data signals Vd1 to Vd4 simultaneously and in synchronism with the strobe signals so as to refresh sequentially the rows of pixels formed at the intersections of the data electrodes 1 and the strobe electrodes. Each data signal is selected from a plurality having the same polarity behaviour with respect to time, the same RMS voltage, and no net direct component.

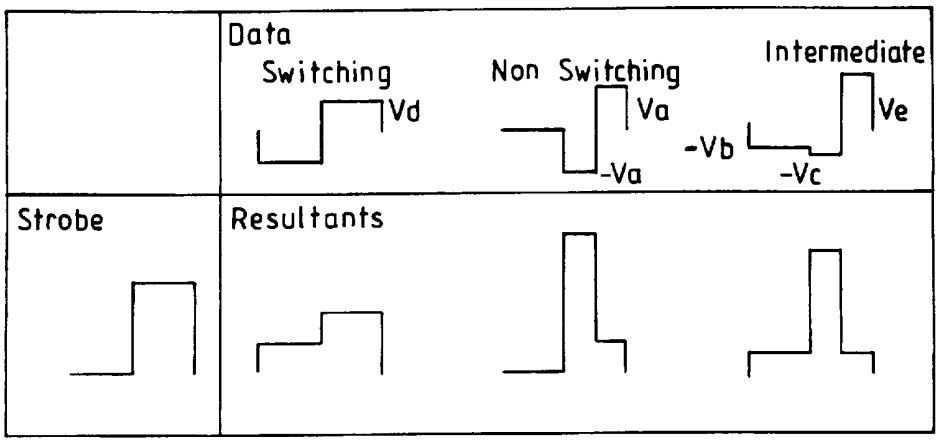

FIG.5.

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

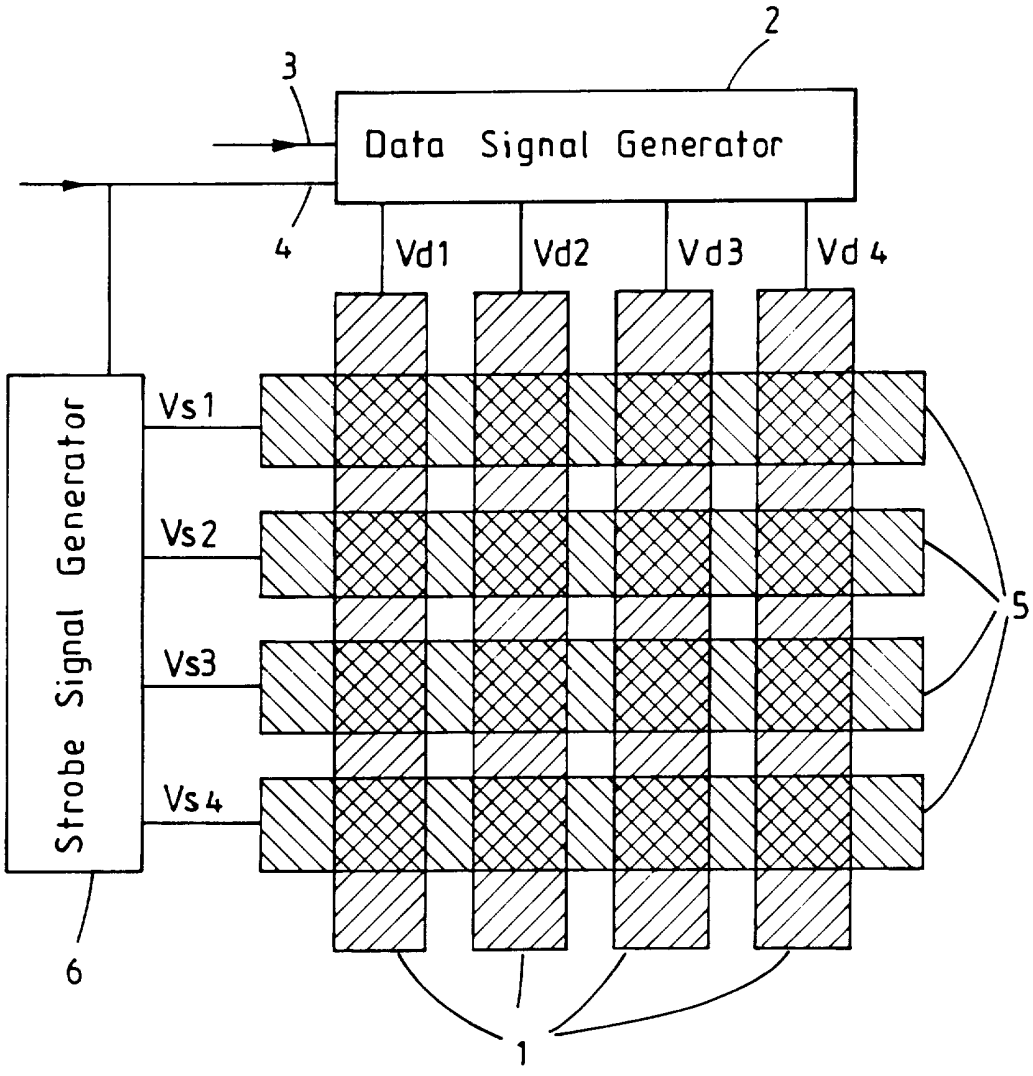
2
3
Data Signal Generator
4
Vd1
Vd2
Vd3
Vd4
Strobe Signal Generator
Vs1
Vs2
Vs3
Vs4
5
6
1

FIG.1.

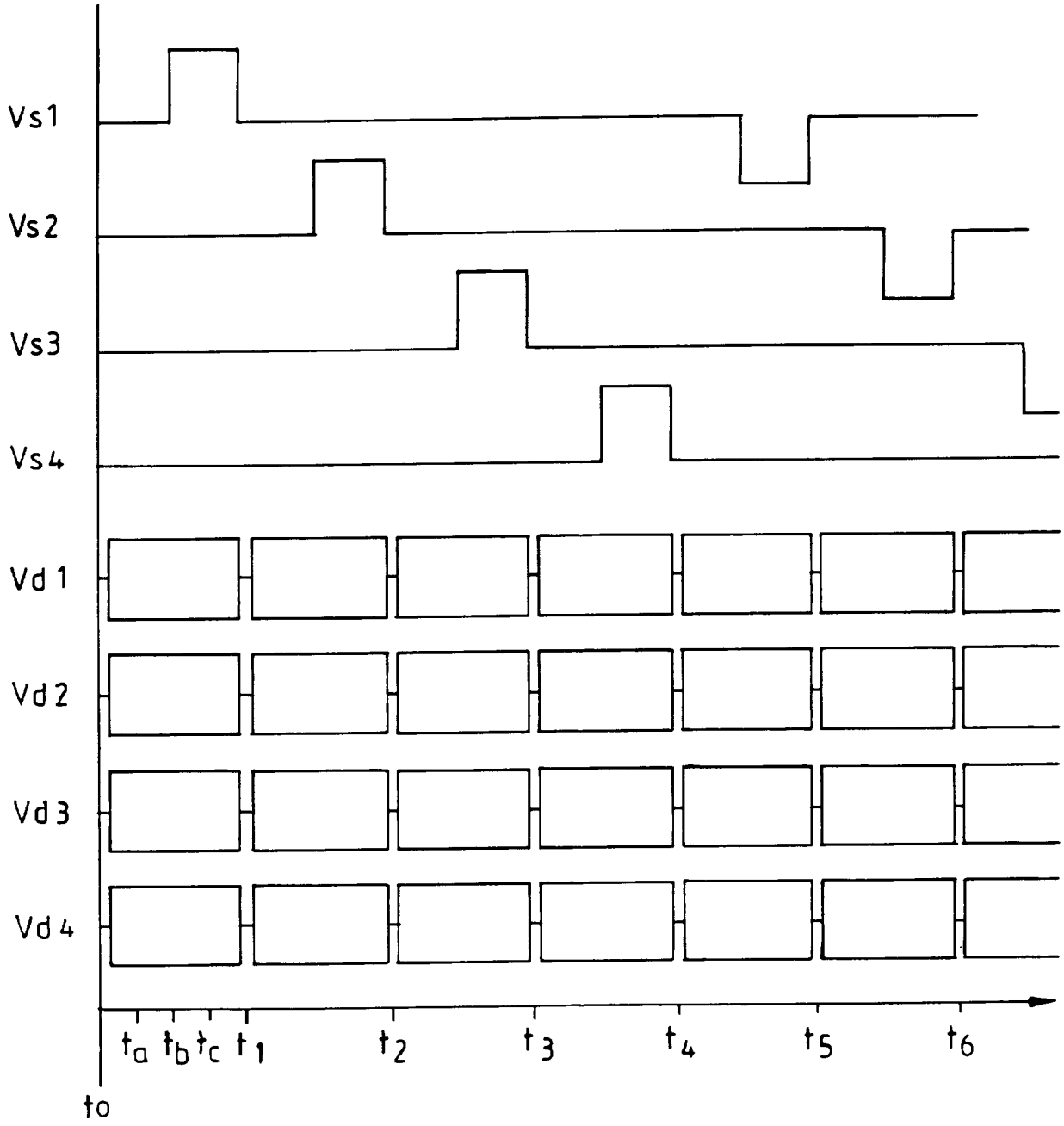

FIG.2.

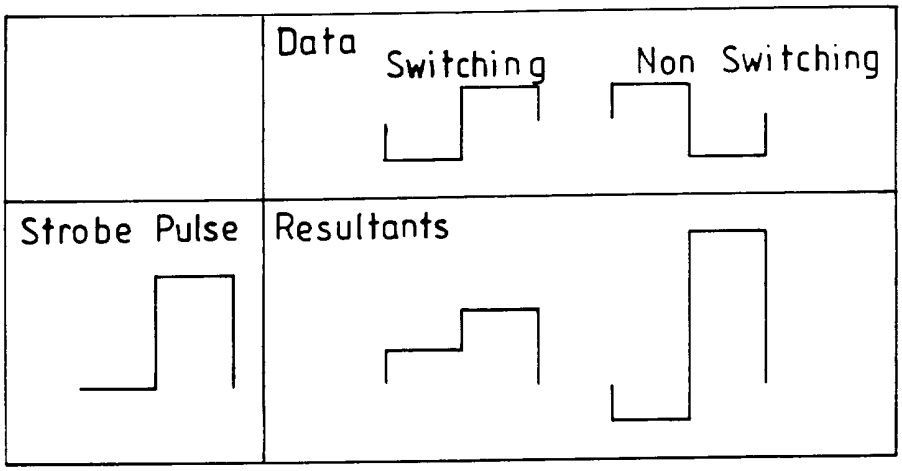
Data
Switching
Non Switching
Strobe Pulse
Resultants

FIG.3.

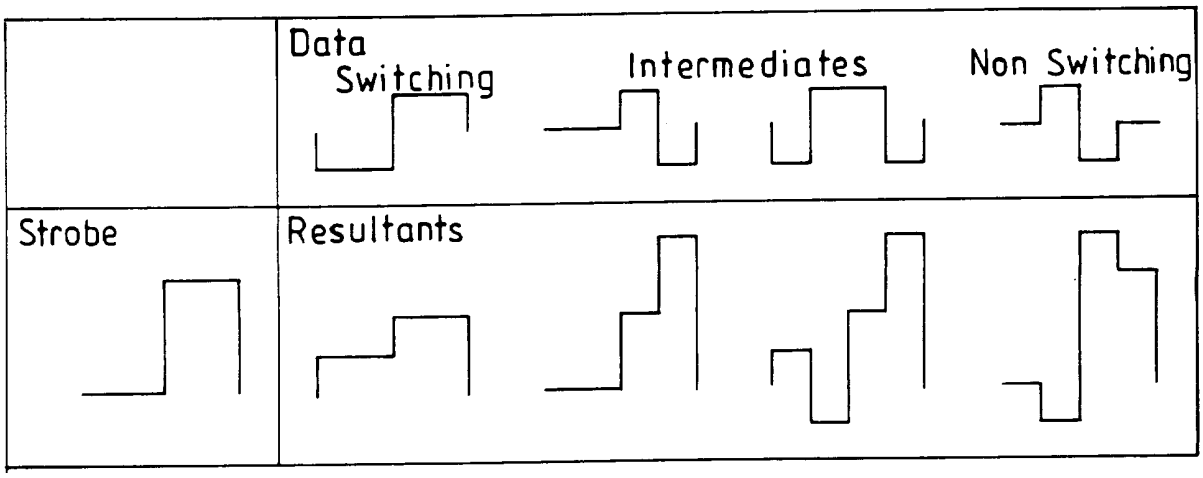
Data
Switching
Intermediates
Non Switching
Strobe
Resultants

FIG.4.

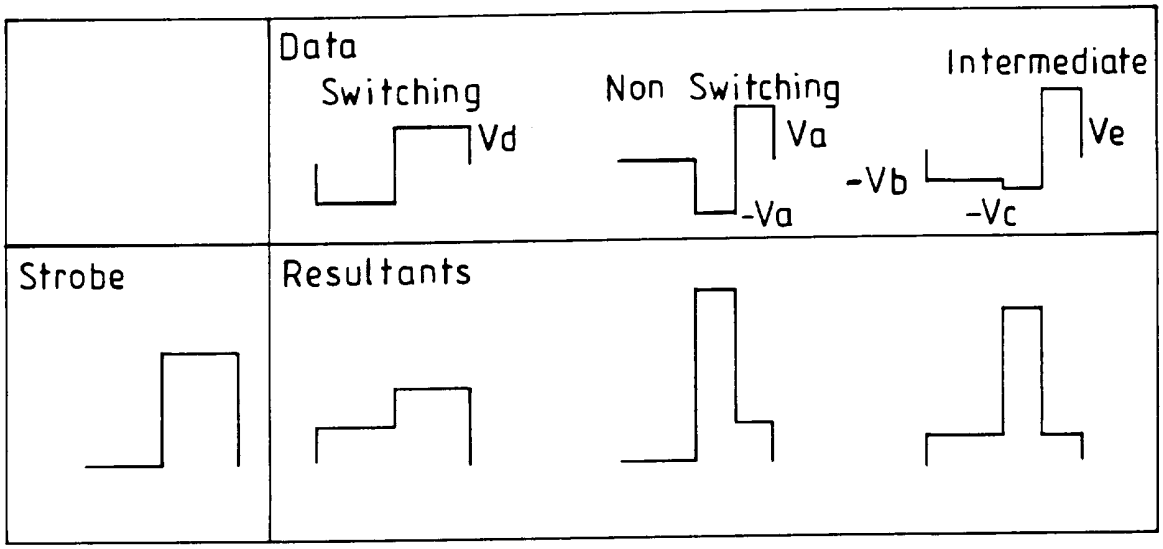
Data
Switching
Vd
Non Switching
Va
-Va
Intermediate
-Vb
Ve
-Vc
Strobe
Resultants

FIG.5.

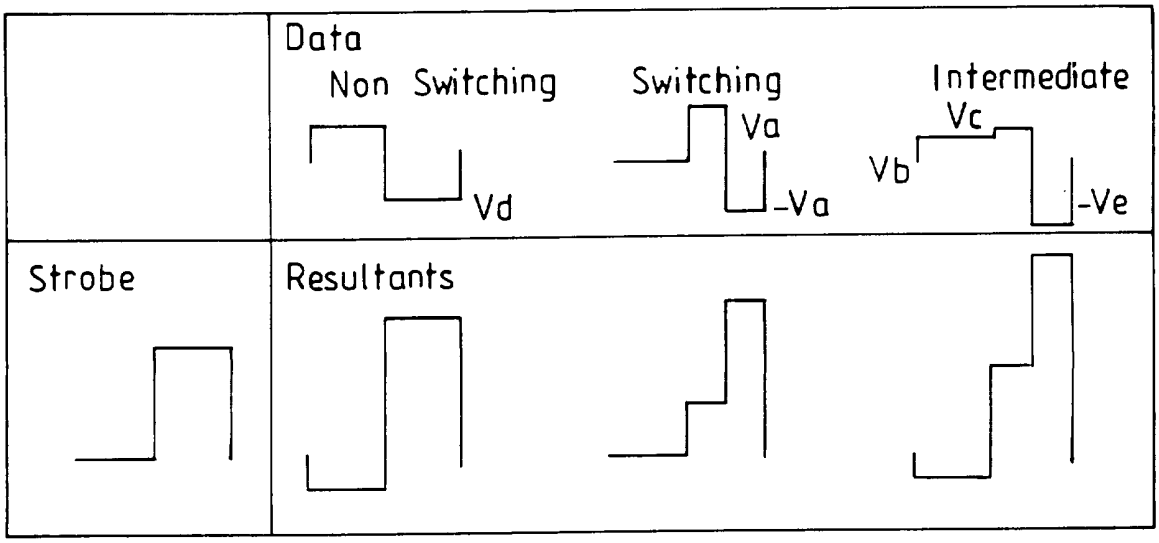
Data
Non Switching
Vd
Switching
Va
-Va
Intermediate
Vc
Vb
-Ve
Strobe
Resultants

FIG.6.

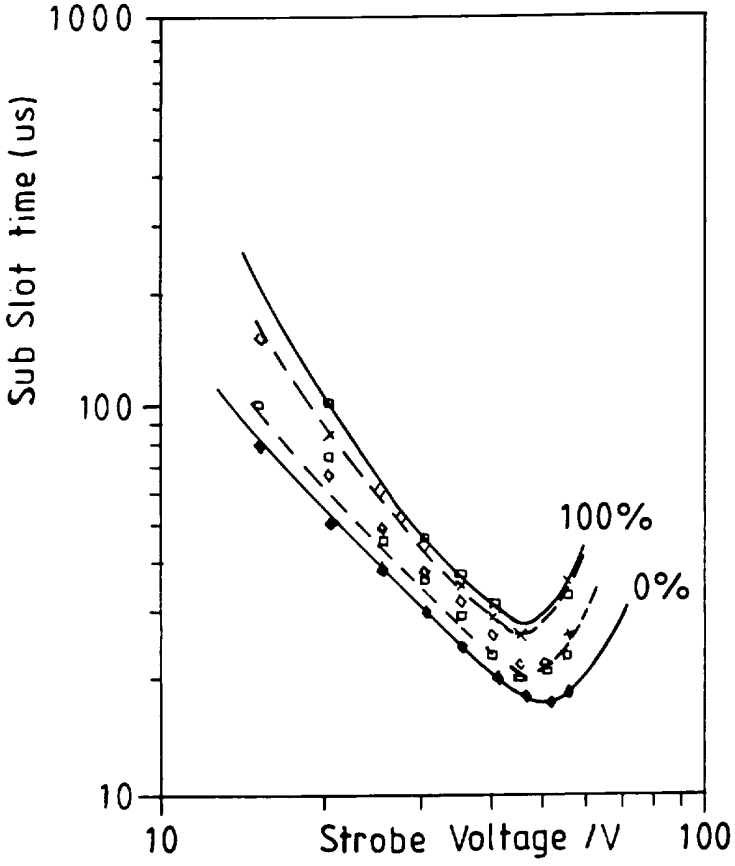
1000
100
10
Sub Slot time (us)
100%
0%
10
Strobe Voltage /V
100

FIG.7.

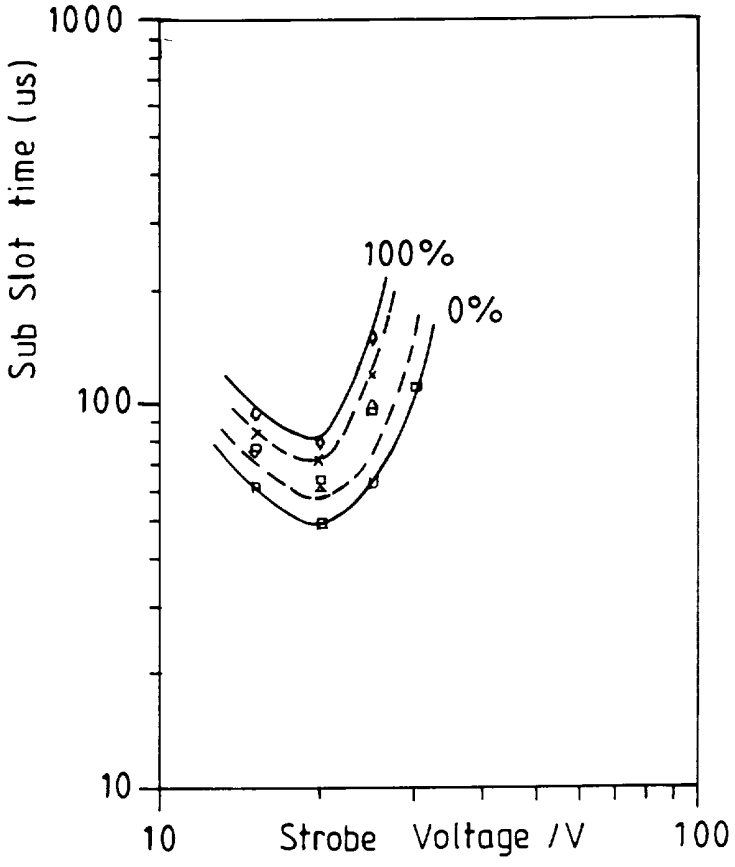
1000
100
10
Sub Slot time (us)
100%
0%
10
Strobe Voltage /V
100

FIG.8.

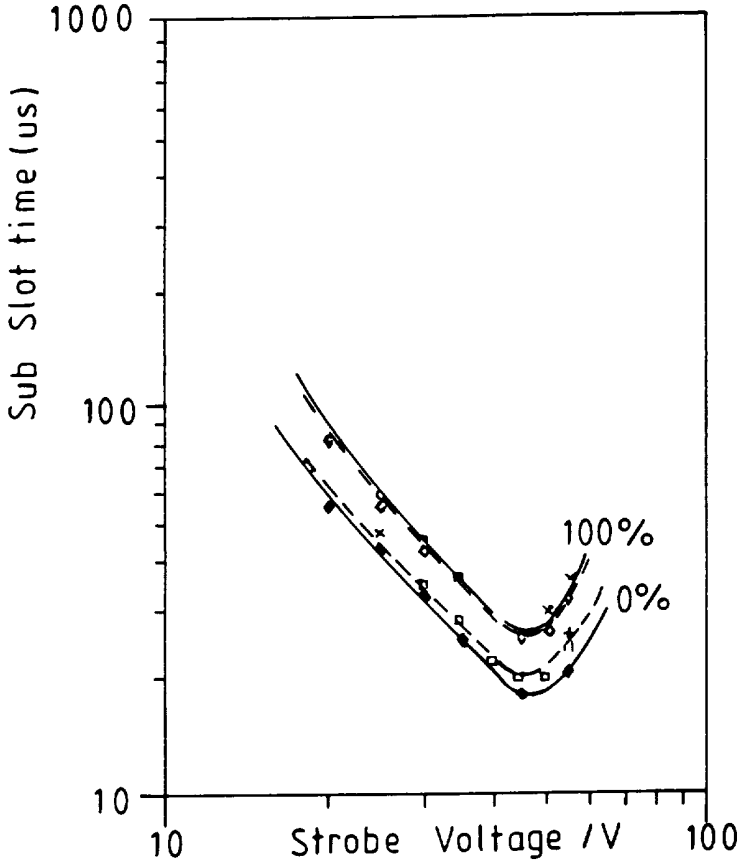
1000
100
10
Sub Slot time (us)
100%
0%
10
Strobe Voltage /V
100

FIG.9.

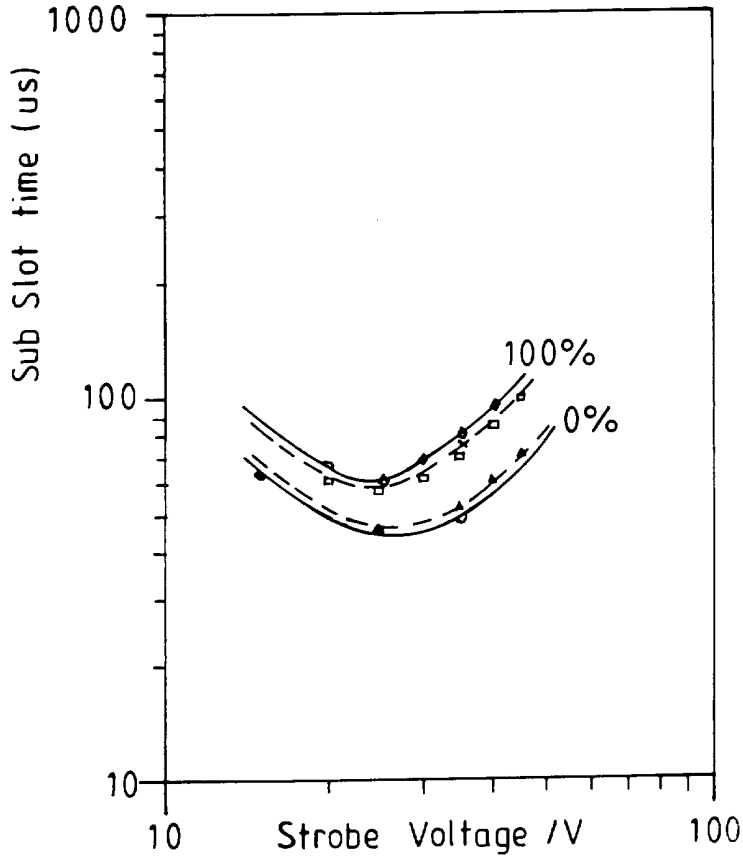
1000
100
10
Sub Slot time (us)
100%
0%
10
Strobe Voltage /V
100

FIG.10.

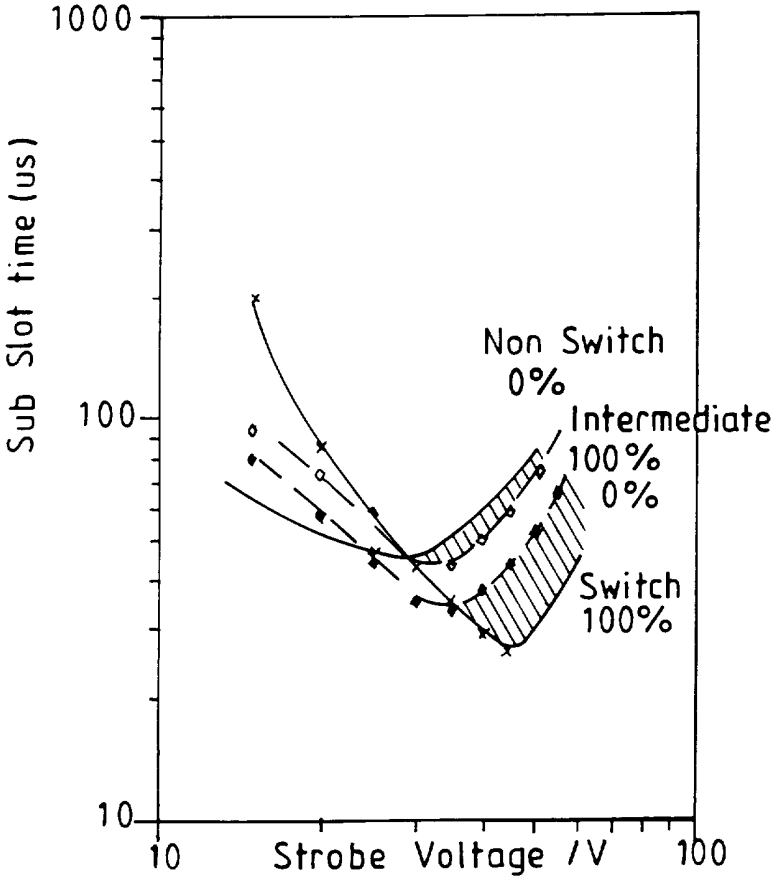
1000
100
10
Sub Slot time (us)
Non Switch
0%
Intermediate
100%
0%
Switch
100%
10
Strobe Voltage /V
100

FIG.11.

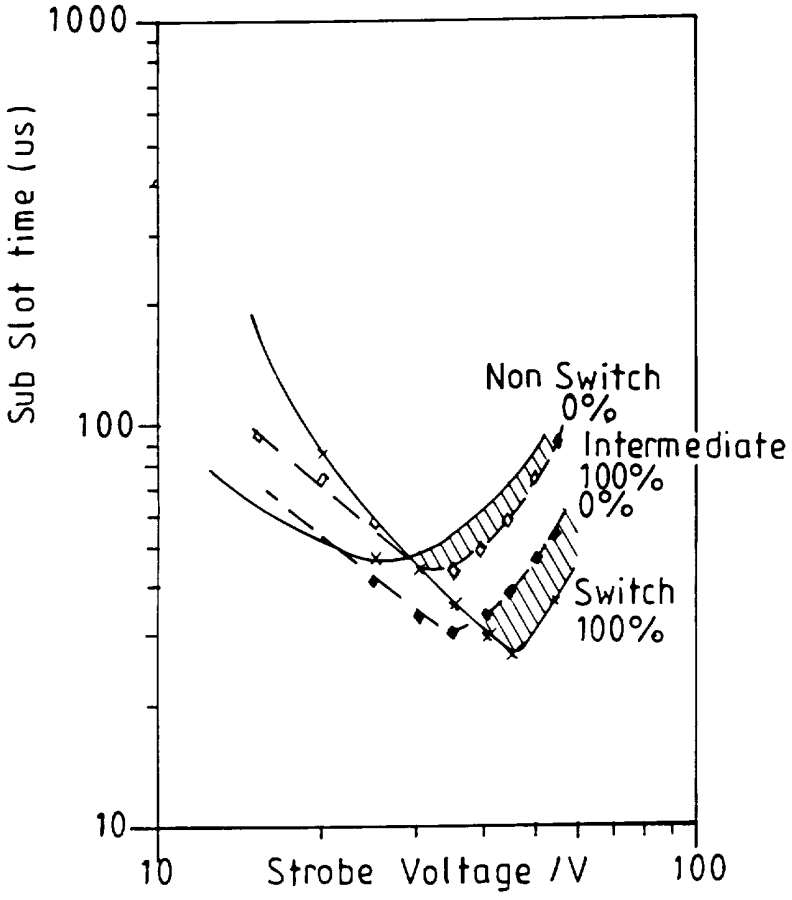
1000
100
10
Sub Slot time (us)
Non Switch
0%
Intermediate
100%
0%
Switch
100%
10
Strobe Voltage /V
100

FIG.12.

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LIQUID CRYSTAL DISPLAY, DATA SIGNAL GENERATOR, AND METHOD OF ADDRESSING A LIQUID CRYSTAL DISPLAY.

The present invention relates to a liquid crystal display, a data signal generator, and a method of addressing a liquid crystal display.

Ferro-electric liquid crystal displays (FLCDs) are prime contenders for use in high resolution display applications including high definition television (HDTV) panels. However, such applications require that the display be capable of producing a large number of grey levels, for instance 256 grey levels for HDTV. Although digital methods are known for producing grey levels in FLCDs, involving spatial and temporal multiplexing or "dither" techniques, it has not been possible to achieve more than 64 grey levels in practical panels.

It is possible to produce grey levels using analogue methods. For instance, by providing four grey levels by analogue methods in combination with two "bits" of spatial dither and two bits of temporal dither, 256 grey levels can be produced in practical FLCDs. However, in order to achieve four analogue grey levels, it is necessary to produce FLCDs having two or more different switching threshold levels within each pixel (picture element). The problem is then to "address" the different analogue grey levels.

Displays of this type comprise row and column electrodes extending on opposite sides of the liquid crystal. The intersections of these electrodes define liquid crystal pixels. Strobe signals are applied sequentially to, for instance, the row electrodes whereas data signals are applied simultaneously to the column electrodes and in synchronism with the

strobe signals. Thus, the data to be displayed are written into the display a row at a time.

During the period in which a given row is addressed, a finite strobe voltage is applied to that row and DC balanced data pulses are applied to the columns. In the simplest case, two data types are used which in combination with the strobe voltage yield either a switching or non-switching resultant. These data pulses are typically the negatives of each other. If multi-threshold grey levels are used within a pixel, then more than two data types exist.

Before and after the addressing period of each row, the pixels within it are subject to random data pulses and these act to modify the τ-V switching characteristics of those pixels. If the addressing scheme being used has a narrow operating window, then for some pixel patterns the discrimination between switching and non-switching pulses can be reduced or even lost.

The switching curve generally has a finite width which is made up of two components. The first is a basic switch width, dependent on material and device characteristics. The second component, which typically doubles the basic switch width, is caused by pixel pattern dependence. It is desirable to remove or at least reduce this component and reduce the switch width towards its basic width.

According to a first aspect of the invention, there is provided a liquid crystal display as defined in the appended Claim 1.

According to a second aspect of the invention, there is provided a data signal generator as defined in the appended Claim 12.

According to a third aspect of the invention there is provided a method as defined in the appended Claim 17.

Preferred embodiments of the invention are defined in the other appended claims.

It is thus possible to provide a technique which reduces or overcomes the problem of pixel pattern dependence within a liquid crystal display. This technique may be used with black and white displays where pixel patterning is a problem. The technique is particularly useful for displays having analogue grey level capability and reduces or overcomes the problem of pixel patterning. This represents a significant advance in the use of FLCDs for large direct view high resolution display applications, particularly where fast addressing of analogue grey levels is required.

The invention will be further described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a schematic diagram of a liquid crystal display to which the invention may be applied;

Figure 2 is a timing diagram illustrating strobe and data signals for a display of the type shown in Figure 1;

Figure 3 illustrates strobe and data signals of a known binary (black/white) addressing scheme;

Figure 4 illustrates strobe and data signals of a known grey level addressing scheme;

Figures 5 and 6 illustrate strobe and data signals of an addressing scheme constituting an embodiment of the invention; and

Figures 7 to 12 are graphs showing τ-V characteristics which may be obtained using the addressing schemes illustrated in Figures 3 to 6.

Figure 1 shows a liquid crystal display comprising a 4 x 4 array of pixels. In practice, a display would comprise many more pixels arranged as a square or rectangular matrix but a 4 x 4 array has been shown for the sake of simplicity of description.

The display comprises four column electrodes 1 connected to respective outputs of a data signal generator 2 so as to receive data signals Vd1 to Vd4. The generator 2 has a data input 3 for receiving data to be displayed, for instance one row at a time. The generator 2 has a synchronising input 4 for receiving timing signals so as to control the timing of the supply of the data signals Vd1 to Vd4 to the column or data electrodes 1.

The display further comprises four row electrodes 5 connected to respective outputs of a strobe signal generator 6 so as to receive respective strobe signals Vs1 to Vs4. The generator 6 has a synchronising input which is also connected to receive timing signals for

controlling the timing of supply of the strobe signals to the row or strobe electrodes 5.

The display further comprises a liquid crystal arranged as a layer between the data electrodes 1 and the strobe electrodes 5. The liquid crystal comprises a ferroelectric liquid crystal of smectic type which is essentially bistable. The liquid crystal may be of the type having a minimum in its τ-V characteristic. A suitable material comprises SCE8 available from Merck (U.K.) Ltd. The thickness of the liquid crystal layer is approximately 2 micrometers with parallel rubbed alignment layers providing approximately 5° of surface tilt. The intersections between the data and strobe electrodes define individual pixels which are addressable independently of each other.

Figure 2 is a diagram illustrating the timing and waveforms of the data and strobe signals in accordance with an existing technique of operating a display of the type shown in Figure 1. The strobe signals Vs1 to Vs4 are supplied in sequence to the row electrodes 5 with each strobe signal occupying a respective time slot. Thus, the strobe signal Vs1 is supplied during the time slot t_0 to t_1, the strobe Vs2 is supplied during the time slot t_1 to t_2, and so on with the sequence repeating for consecutive groups of four time slots. Further, each time slot is divided into four sub-slots, for instance as illustrated for the first slot with the sub-slots starting at t_0, t_a, t_b, and t_c. During its active time slot, for instance the first time slot for the strobe signal Vs1, the strobe signal has zero level for the first two sub-slots and a predetermined level Vs for the third and fourth time sub-slots. In order to prevent DC imbalance, the polarities of the strobe signals may be reversed after each complete frame refresh of the display.

The data signals Vd1 to Vd4 are supplied simultaneously with each other and in synchronism with the strobe signals, as shown in Figure 2. For the purpose of illustration, each data signal is illustrated by a rectangular box in Figure 2.

Figure 3 shows data and strobe waveforms of a known addressing scheme, together with the resultant waveforms appearing across the pixels. Each of the two data pulses is DC balanced i.e. has no net direct component. Further, the RMS voltages of the two data signals are the same. However, whereas the first data signal comprises a negative pulse followed by a positive pulse and forms a "switching" data signal, the second "non-switching" data signal comprises a positive pulse followed by a negative pulse. Such an addressing scheme is suitable for use with monochrome or black and white displays, although different analogue grey levels could be addressed by varying the amplitude of the data signals.

Figure 4 illustrates another known addressing scheme having four data signals so as to permit two intermediate grey levels to be addressed. The data signals have no net direct component but, in this case, have different RMS voltages. Further, the polarity behaviour with respect to time varies for the different data signals. Thus, the "switching" data signal comprises a negative pulse followed by a positive pulse whereas the non-switching data signal and one of the intermediate data signals comprises a shorter positive pulse followed by a shorter negative pulse. The other intermediate signal comprises a short negative pulse followed by a longer positive pulse followed by a short negative pulse.

/

Figure 5 illustrates the data signals of an addressing scheme constituting an embodiment of the invention. A switching data signal, a non-switching data signal, and one intermediate data signal are illustrated so as to permit one intermediate grey level to be addressed. Each of the data signals has no net direct component. The switching data signal comprises a negative pulse of amplitude Vd occupying two time sub-slots, followed by a positive pulse of amplitude Vd occupying two time sub-slots. The non-switching data signal is zero for two sub-slots, minus Va for one sub-slot, and +Va for the final sub-slot. The intermediate data signal is at -Vb for two sub-slots, -Vc for one sub-slot, and +Ve for one sub-slot. Thus, each of the data signals comprises a negative portion followed by a positive portion i.e. all of the data signals exhibit the same polarity behaviour with respect to time.

In order for the data signals to have the same RMS voltage, the various pulse amplitudes mentioned above fulfil the following conditions:

$$Va = (\sqrt{2})Vd$$
$$Vb = Vd/2$$
$$Vc = ((\sqrt{6})-1)Vd/2$$
$$Ve = ((\sqrt{6})+1)Vd/2$$

The switching data signal shown in Figure 5 corresponds to the switching data signal of the known JOERS/Alvey addressing scheme.

Figure 6 illustrates another addressing scheme constituting a preferred embodiment of the invention. In this scheme, the data signal waveforms are inverted with respect to those shown in Figure 5. Thus, the data signals exhibit the same polarity behaviour with respect to time but, in

this case, each data signal comprises a positive portion followed by a negative portion. the non-switching data signal corresponds to that of the known JOERS/Alvey addressing scheme.

Figures 7 and 8 show τ-V characteristics of a display of the type illustrated in Figure 1 for black and white operation using data signals of the known JOERS/Alvey type as illustrated in Figure 3. The broken lines show the τ-V characteristics without the effects of pixel patterning whereas the full lines show the effects of pixel patterning before and after a strobe signal. Figure 7 relates to switching data signals whereas Figure 8 relates to non-switching data signals. The τ-V characteristics are substantially effected by pixel patterning.

Figure 9 and 10 correspond to Figures 7 and 8 respectively, but using the addressing scheme illustrated in Figure 5. The effects of pixel patterning are greatly reduced by using data signals having the same polarity behaviour with respect to time.

Figures 11 and 12 illustrate the use of the data signals of Figure 5 in a display of the type shown in Figure 1 and providing an intermediate grey level. Figure 11 illustrates performance in the absence of pixel patterning whereas Figure 12 illustrates performance with pixel patterning. The shaded regions illustrate the "driving windows" for the display. As is apparent by comparing Figures 11 and 12, using the addressing scheme illustrated in Figure 5, the effects of pixel patterning do not compromise the addressing of the pixels. Only the switch width for the intermediate data signal is significantly effected by pixel patterning but a reasonable drive window remains so that the three grey levels of each pixel can be reliably addressed.

It is thus possible to reduce the pixel pattern dependence of drive schemes, both for black and white displays and for displays capable of intermediate grey levels. This represents a significant advance in the use of FLCDs for large direct view high resolution display application and such addressing schemes may be necessary for fast addressing of analogue intermediate grey levels.

CLAIMS

1. A liquid crystal display comprising: a plurality of data electrodes; a plurality of strobe electrodes; a plurality of liquid crystal pixels formed at intersections between the data electrodes and the strobe electrodes; a strobe signal generator arranged to supply strobe signals sequentially to the strobe electrodes, and a data signal generator arranged to supply any selected one of a plurality of different data signals to each of the data electrodes in synchronism with the strobe signals, the data signals having the same polarity behaviour with respect to time.

2. A display as claimed in Claim 1, in which each of the data signals comprises a first pulse of a first polarity followed by a second pulse of a second polarity opposite the first polarity.

3. A display as claimed in Claim 1 or 2, in which the data signals have the same RMS voltage.

4. A display as claimed in any one of the preceding claims, in which each of the different data signals has no net direct component.

5. A display as claimed in any one of the preceding claims, in which each pixel has X different switching thresholds, where X is an integer greater than or equal to two, and the plurality of different data signals comprises at least (X + 1) different data signals.

6. A display as claimed in any one of the preceding claims, in which the liquid crystal is a bistable liquid crystal.

7. A display as claimed in any one of the preceding claims, in which the liquid crystal is a smectic liquid crystal.

8. A display as claimed in any one of the preceding claims, in which the liquid crystal is a ferroelectric liquid crystal.

9. A display as claimed in any one of the preceding claims, in which the liquid crystal has a minimum in its τ-V characteristic.

10. A display as claimed in any one of the preceding claims, in which the peak amplitude of each of the different data signals is less than the peak amplitude of the strobe signals.

11. A display as claimed in any one of the preceding claims, in which each of the different data signals comprises a rectangular waveform.

12. A data signal generator for a liquid crystal display of the type comprising: a plurality of data electrodes; a plurality of strobe electrodes; and a plurality of liquid crystal pixels formed at intersections between the data electrodes and the strobe electrodes, the data signal generator being arranged to produce any selected one of a plurality of different data signals having the same polarity with respect to time.

13. A generator as claimed in Claim 12, in which each of the data signals comprises a first pulse of a first polarity followed by a second pulse of a second polarity opposite the first polarity.

14. A generator as claimed in Claim 12 or 13, in which the data signals have the same RMS voltage.

15. A generator as claimed in any one of Claims 12 to 14, in which each of the different data signals has no net direct compound.

16. A generator as claimed in any one of Claims 12 to 15, in which each of the different data signals comprises a rectangular waveform.

17. A method of addressing a liquid crystal display of the type comprising: a plurality of data electrodes; a plurality of strobe electrodes; and a plurality of liquid crystal pixels formed at intersections between the data electrodes and the strobe electrodes, the method comprising supplying strobe signals sequentially to the strobe electrodes and supplying any selected one of a plurality of different data signals to each of the data electrodes in synchronism with the strobe signals, the data signals having the same polarity behaviour with respect to time.

Patents Act 1977
Examiner's report to the Comptroller under Section 17
(The Search report)

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Relevant Technical Fields

(i) UK Cl (Ed.N) G5C (CHB)

(ii) Int Cl (Ed.6) G09G 3/36

Search Examiner
MR G M PITCHMAN

Date of completion of Search
9 FEBRUARY 1995

Databases (see below)
(i) UK Patent Office collections of GB, EP, WO and US patent specifications.

(ii) ONLINE DATABASES: EDOC, WPI, JAPIO

Documents considered relevant following a search in respect of Claims :-
1 to 17

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages		Relevant to claim(s)
A	GB 2225473 A	(STC) see Figure 2	1 to 17
A	WO 94/18665 A1	(SECRETARY OF STATE FOR DEFENCE) see Figures 7 to 20	1 to 17
A	WO 92/02925 A1	(SECRETARY OF STATE FOR DEFENCE) see Figures 4 to 12	1 to 17

Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).