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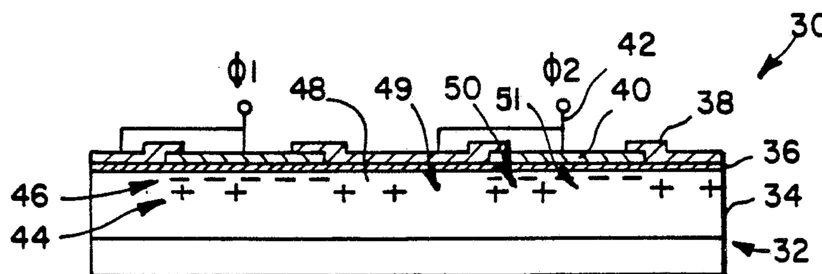

(57) Abstract

A charge-coupled device (CCD) (30) of the two-phase type is disclosed. The CCD (30) comprises two polysilicon levels which are electrically connected to form one clock phase. In order to provide a CCD of improved transfer efficiency, two implanted regions (48-51) of different dopant levels are provided under each polysilicon level. When the CCD is clocked, a four-tier potential profile is produced.

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CHARGE-COUPLED DEVICE

The present invention relates to a charge-coupled device (CCD), and more particularly, 5 to such a device which has improved transfer efficiency.

It is known in two-phase CCD devices to employ either a true two-phase structure with two distinct potential levels under a single gate 10 electrode or a pseudo two-phase structure in which there is a uniform, but distinct, potential level under each of two electrically-connected gate electrodes which form one clock phase. In applications involving long device cells and in 15 high-speed applications, the transfer efficiency of these conventional structures is not entirely satisfactory. Thus, ways have been sought to improve the transfer efficiency in CCD's while at the same time not unduly complicating the process of making 20 the device.

U.S. Patent No. 3,767,983, is directed to improving the transfer efficiency in a charge transfer device of the bucket brigade type. The device disclosed in this patent includes two 25 different threshold voltages in the transfer region between each pair of successive storage sites. There is a substantially abrupt transition between the two different threshold voltages in the transfer region. The abrupt transition is provided to improve the 30 transfer efficiency of the device by solving the problem of feedback voltage which occurs between the transferor zone (source) and the transferee zone (drain). Such a problem does not exist in CCD's, however, and thus, this patent does not provide a 35 solution to the problem of increasing the transfer efficiency in a CCD.

It is an object of the present invention to overcome the problems in the prior art discussed above and to provide an improved CCD.

In accordance with one aspect of the invention, there is provided a charge-coupled device for storage and transfer in a predetermined direction of varying amounts of mobile charge carriers, the device having a plurality of phases, the device comprising: a substrate of a first conductivity type; a layer of a second conductivity type on the substrate; an insulating layer on the layer of a second conductivity type; electrode means for each phase of said device, said electrode means including a pair of gate electrodes on said insulating layer, said pair of gate electrodes being electrically connected together, a plurality of the electrode means being disposed to form a path in the predetermined direction; and at least three implanted regions of different dopant levels under each of the electrode means.

In accordance with another aspect of the invention, there is provided a method of making a charge-coupled device, the method comprising the steps of: implanting a buried channel of a first conductivity type on a substrate of a second conductivity type; defining an area on the substrate by means of photoresist and polysilicon for the electrode means of one phase of the device; implanting the area with the first and second conductivity types to form at least three regions of different dopant levels under the area.

In one embodiment of the present invention, two polysilicon levels are used for each clock phase of a two-phase CCD. The polysilicon levels are electrically connected to form the gate electrodes of one phase of the device, and two dopant levels are

provided under each polysilicon level. When the CCD is clocked, a four-tier potential profile is produced beneath each phase.

The CCD of the present invention has a very high transfer efficiency, and thus, it is particularly suitable for use in high speed applications and in devices having relatively long cells. The high transfer efficiency results from the multiple potential levels and the resulting increased electric fields which are formed when the CCD is being clocked. A further advantage of the present invention is the method disclosed herein of making a CCD in which two levels of polysilicon are used in a manner to minimize the number of mask steps and provide self-aligned profiles. In the practice of this method, the effective number of potential steps per phase in a CCD can be doubled with only one additional implant.

Embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings in which:

Fig. 1 is a sectional view of a prior-art CCD of the pseudo two-phase type;

Fig. 2 is a potential profile of the CCD shown in Fig. 1;

Fig. 3 is a sectional view of the CCD of the present invention;

Fig. 4 is a potential profile of the CCD shown in Fig. 3;

Figs. 5-9 show the steps performed in making the CCD of the present invention;

Fig. 10 is a graph showing horizontal field versus cell length for a conventional two-phase CCD; and

Fig. 11 is a graph showing horizontal field versus cell length for the CCD of the present invention.

With reference to Fig. 1, there is shown a prior-art CCD which is designated 10. CCD 10 is of the pseudo two-phase type, and comprises a P-type substrate 12. A N-type buried channel 14 is formed in substrate 12, and an insulating layer 16 is formed over buried channel 14. P-type implants are made as shown at 18, and polysilicon gate electrodes 20 and 22 are formed on layer 16. Electrodes 20 and 22 are electrically connected by a conductor 24 to form either phase one ($\phi 1$) or phase two ($\phi 2$) of the device 10.

A potential diagram of prior-art device 10 is shown in Fig. 2 in which electrodes 20 and 22 are indicated schematically. As shown in Fig. 2, the resulting potential profile 26 of device 10 when it is being clocked is a two-tier profile in which, for example, tiers at 2V and 4V occur in a phase which is turned off and tiers at 6V and 8V occur when a phase is turned on. The two tiers for each phase are required for uni-directional charge transfer. A disadvantage of the device 10 is that the electric field across the cell, as illustrated by the diagram in Fig. 10, is less than adequate for charge transfer in long device cell applications and for high-speed applications.

A CCD 30 which is constructed in accordance with the present invention is shown in Fig. 3. CCD 30 is a two-phase device and comprises a P-type substrate 32 having a N-type buried channel 34 formed therein. A gate oxide 36 is formed over the buried channel 34, and polysilicon gate electrodes 38 and 40 are formed on oxide 36. Electrodes 38 and 40 are electrically connected by a conductor 42 to form either ϕ 1 or $\phi 2$ of device 30. As shown in Fig. 3, electrodes 38 and 40 have different levels of

polysilicon; electrode 40 is generally planar, and electrode 38 is formed with portions which overlap adjacent electrodes 40.

As noted above, two polysilicon levels are used for each phase in device 30. It is also a feature of the present invention to provide two implanted regions of different dopant levels under each electrode 38, 40, such that there are two potentials formed under each polysilicon level. Thus, as shown in Fig. 3, a P-type implant 44 is made under each of the electrodes 38, 40, and an N-type implant 46 is made under each of the electrodes 40. As a result of implants 44 and 46, there are formed under electrodes 38 and 40 a first region 48 having a P-type implant in the N-type buried channel 34, a second region 49 having no implant in the buried channel 34, a third region 50 having a P-type implant and an N-type implant in the buried channel 34, and a fourth region 51 having an N-type implant in the buried channel 34.

A potential diagram for device 30 is shown in Fig. 4, and as can be seen therein, a four-tier potential profile 50 is produced in device 30 when the device 30 is being clocked. As a result of increasing the number of tiers, or steps, under each electrode 38, 40, and thereby increasing the drift field across the cell, as shown in Fig. 11, the transfer efficiency of device 30 is substantially increased. Using two-dimensional electrostatics modeling, the electric field for the CCD structure, under typical operating conditions, can be calculated. The magnitude of this field is shown for a prior-art structure in Fig. 10 and for the structure of the present invention in Fig. 11. The peaks in Figs. 10 and 11 represent the change from one potential tier to the next; the valleys in these

figures show the drop in the field across a given tier. A higher field value speeds-up charge transport. It can be seen in Fig. 11 that there is a greater number of high field peaks and the field value across each tier remains at a higher level than in Figure 10. The net result is more field-aided transport of charge across the cell resulting in lower transfer times and improved charge transfer efficiency.

A manufacturing process for producing device 30 is shown in Figs. 5-9. As shown in Fig. 5, the process is carried out using a P-type substrate 32 having an N-type buried channel 34 implanted therein in a known manner. A gate oxide 36 is grown on the substrate 32 over buried channel 34, followed by the deposition of a layer 37 of polysilicon, a layer 39 of silicon nitride, and a layer 41 of silicon dioxide.

As shown in Fig. 5, a first gate electrode area 53 is defined by a photoresist 43, and the silicon nitride layer 39 and the silicon dioxide layer 41 are removed in the areas 53. A N-type material is implanted through the polysilicon 37 and gate oxide 36 in the areas 53. Photoresist 43 is then stripped off, and a photoresist 45 is applied to define the width of a stepped potential region with respect to the edge of a first gate electrode. A P-type implant is then made, as shown in Fig. 6, which provides for the decrease in the channel potential in the stepped potential region. Resist 45 is then stripped off, as well as the remaining deposited oxide, and the exposed polysilicon is locally oxidized by a conventional LOCOS (Local Oxidation of Silicon) process as shown in Fig. 7. The remaining silicon nitride layer 39 is then removed by etching, and the polysilicon layer 37 is removed in the areas not locally oxidized.

As shown in Fig. 8, a photoresist 47 is applied to define the width of a second stepped-potential region with respect to the edge of the first gate electrode. In a next step, a P-type material is implanted to provide for the necessary shift in channel potential in the second stepped-potential region. Resist 47 is then stripped, and a second polysilicon layer is deposited and patterned to form second gate electrodes 38. The two gate electrodes are tied together by conductor 42 so that the electrodes can be simultaneously clocked.

It will be apparent that modifications can be made in the process disclosed herein for making a CCD device without departing from the scope of the present invention. For example, the N-type offset implant (Fig. 5), which is made prior to the implant for the first stepped-potential region, can be replaced with an unmasked P-type implant; this results in a lower offset for the the first gate electrode channel potential and requires that the order of the gate electrodes within the phase be interchanged. Another alternative is to replace the N-type (or P-type) implant, which is made prior to the first stepped-potential implant, with an unmasked implant prior to the deposition of the second layer of polysilicon; this implant can be either N-type or P-type depending on the order of the gate electrodes. It is also possible to substitute either or both P-type stepped-potential implants with N-type implants, which are aligned to the trailing edge (right edge as shown in Figs. 5-9) of the gate electrode; this modification can be used with any of the above configurations depending on the order the gate electrodes or on implant preference. Further, the process disclosed herein can be extended to processes with more than two layers of polysilicon and/or more than two-phase CCD architectures.

Claims:

1. A charge-coupled device for storage and transfer in a predetermined direction of varying amounts of mobile charge carriers, said device having a plurality of phases, said device comprising:

a substrate (32) of a first conductivity type;

a layer (34) of a second conductivity type on said substrate (32);

an insulating layer (36) on said layer of a second conductivity type;

electrode means (38, 40)for each phase of said device, said electrode means including a pair of gate electrodes (38, 40) on said insulating layer (36), said pair of gate electrodes (38, 40) being electrically connected together, a plurality of said electrode means (38, 40) being disposed to form a path in said predetermined direction; and

at least three implanted regions (48-51) of different dopant levels under each of said electrode means (38, 40).

2. A charge-coupled device, as defined in claim 1, wherein the gate electrodes (38, 40) in each phase are formed from polysilicon, and the polysilicon level of one of the electrodes (38) in said pair of gate electrodes is different from the polysilicon level of the other electrode (40).

3. A charge-coupled device, as defined in claim 2, wherein there are at least two implanted regions (48-51) of different dopant levels under each of said electrodes (38, 40).

4. A charge-coupled device for storage and transfer in a predetermined direction of information represented by varying amounts of mobile charge carriers, said device comprising:

a substrate (32) of a first conductivity type;

a layer (34) of a second conductivity type on said substrate (32);

5 an insulating layer (36) disposed on said layer (34) of a second conductivity type;

a plurality of gate electrodes (38, 40) disposed over said insulating layer (36) so as to form a path in said predetermined direction,

10 successive pairs of said electrodes (38, 40) being electrically connected to form one phase of said device, one of the electrodes (38, 40) in each phase being formed of a first level of material and the other electrode being formed of

15 a second level of material; and

at least two implanted regions (48-51) of different dopant levels under each of said electrodes (38, 40).

5. A charge-coupled device, as defined in

20 claim 4, wherein the dopant level in each of the regions (48-51) under a pair of electrically-connected electrodes (38, 40) is different whereby a four-tier potential profile (50) is produced by a pair of electrodes (38, 40).

25 6. A charge-coupled device, as defined in claim 4, wherein said first conductivity type is a P-type.

7. A charge-coupled device, as defined in claim 4, wherein said second conductivity type is an

30 N-type.

8. A charge-coupled device, as defined in claim 4, wherein said gate electrodes (38, 40) are formed of polysilicon.

9. A charge coupled device, as defined in

35 claim 4, wherein the implanted regions (48-51) under

one of the electrodes in a phase are a first region (48) of N-type and P-type and a second region (49) of N-type.

10. A charge-coupled device, as defined in claim 9, wherein the implanted regions under the other electrodes are one region (50) of N-type and P-type and another region (51) of N-type.

11. A charge-coupled device of the two-phase type, said device comprising:

a semiconductor substrate (32);

two electrically-connected gate electrodes (38, 40) for each of said phases formed on said substrate (32), the electrodes(38, 40) in each phase being formed from polysilicon and the polysilicon level of one of the electrodes (38) being different from the level of the other electrode (40); and

said substrate (32) having two regions (48-51) of different dopant levels under each of said electrodes.

12. A method of making a charge-coupled device, said method comprising the steps of:

implanting a buried channel of a first conductivity type on a substrate of a second conductivity type;

defining an area on said substrate by means of photoresist and polysilicon for the electrode means of one phase of said device;

implanting said area with said first and second conductivity types to form at least three regions of different dopant levels under said area.

13. A method of making a charge-coupled device, as defined in claim 12, wherein polysilicon layers are deposited on said area to form two gate electrodes which are electrically connected.

14. A method of making a charge-coupled device, as defined in claim 13, wherein said area is implanted with said first and second semiconductor types to form two regions of different dopant levels
5 under each of said electrodes.

15. A method of making a charge-coupled device, as defined in claim 12, wherein a polysilicon layer is deposited on said area, and an edge of said polysilicon is used in the implanting of one of said
10 materials to define a boundary of one of said regions.

16. A method of making a charge-coupled device, said method comprising the steps of:

implanting a buried channel of a first conductivity type on a substrate of a second
15 conductivity type;

growing a gate oxide on the substrate over the buried channel;

depositing successive layers of polysilicon, silicon nitride, and silicon dioxide over said
20 gate oxide;

defining a first gate electrode area by means of photoresist and removing the nitride and oxide layers in these areas to expose the polysilicon layers;

25 implanting a material of said second conductivity type through the exposed polysilicon and through the gate oxide;

defining a stepped potential region under said first gate electrode area by means of
30 photoresist;

implanting a material of said second conductivity type in said stepped potential region;

locally oxidizing exposed polysilicon and
35 then etching to form a first gate electrode;

defining a second stepped potential region adjacent said first gate electrode by means of photoresist and said first gate electrode;

implanting a material of said second conductivity type in said second stepped potential region;

depositing a second polysilicon layer to form a second gate electrode; and

electrically connecting the first and second gate electrodes together.

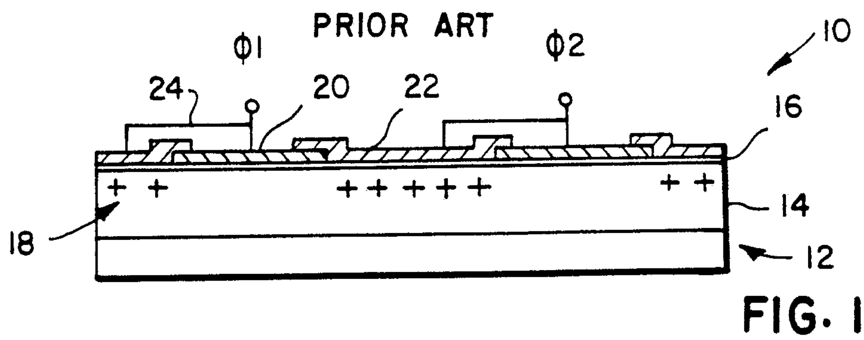

FIG. 1

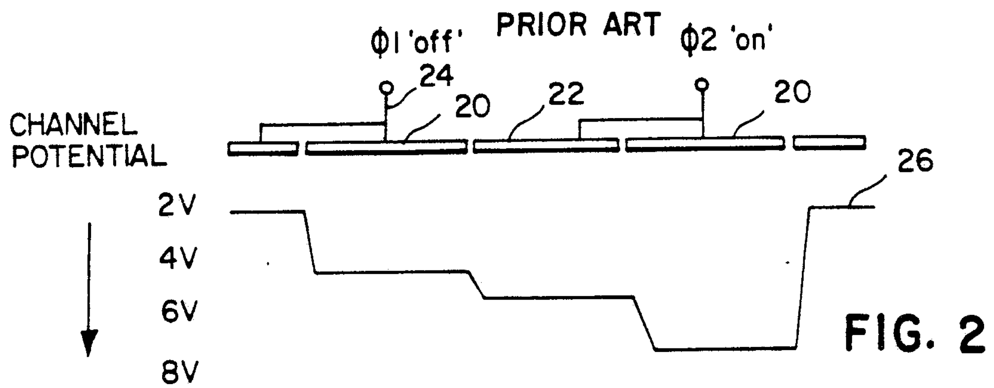

FIG. 2

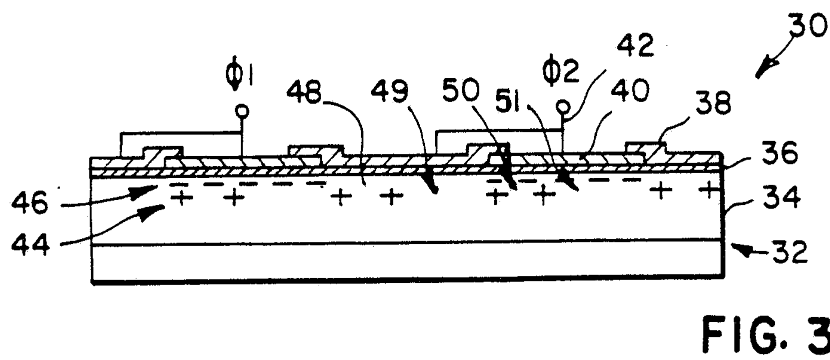

FIG. 3

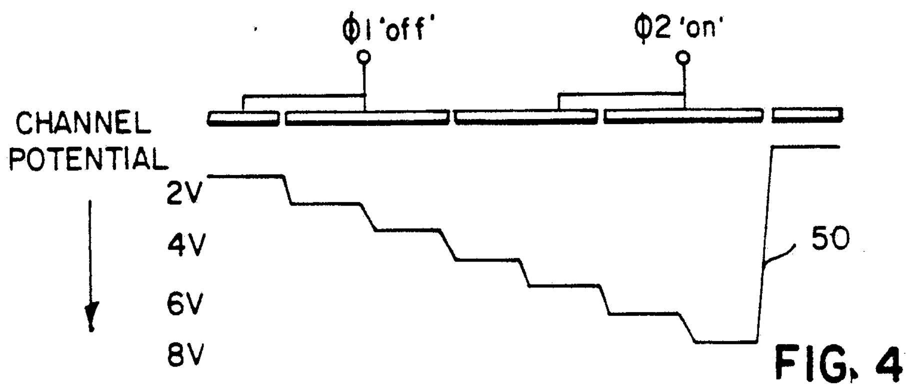

FIG. 4

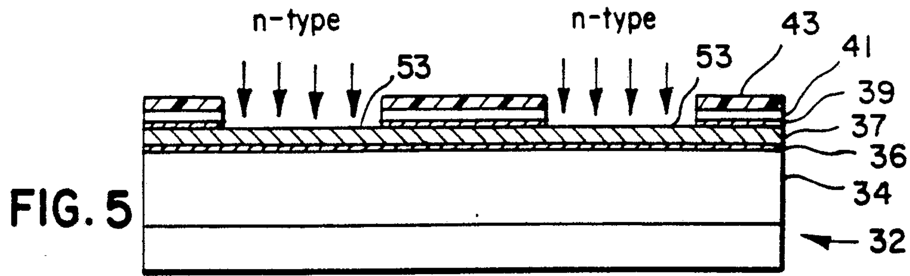

FIG. 5

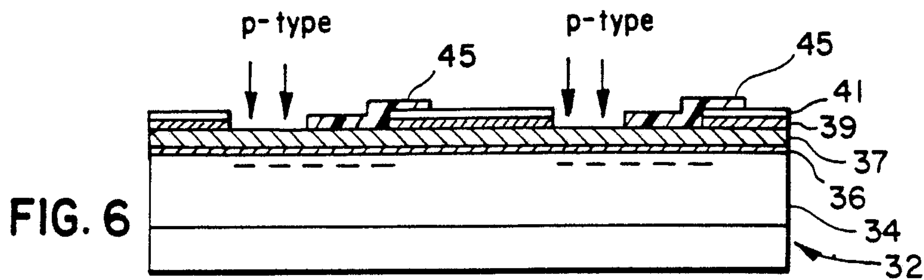

FIG. 6

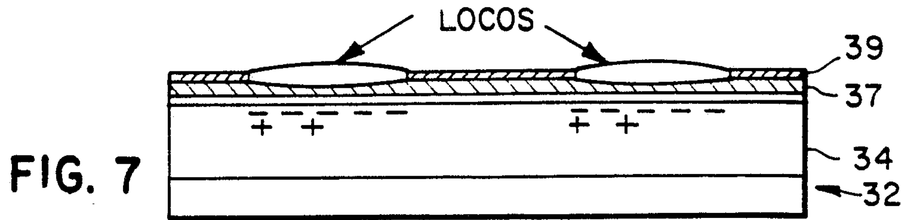

FIG. 7

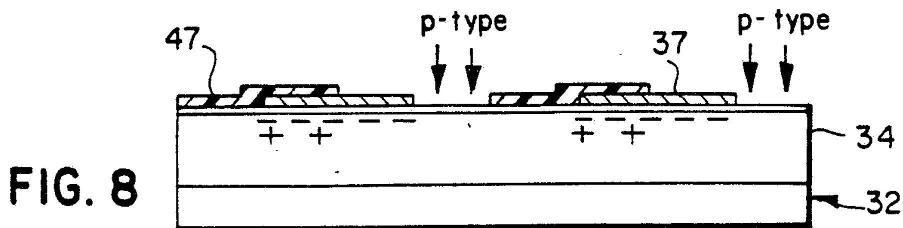

FIG. 8

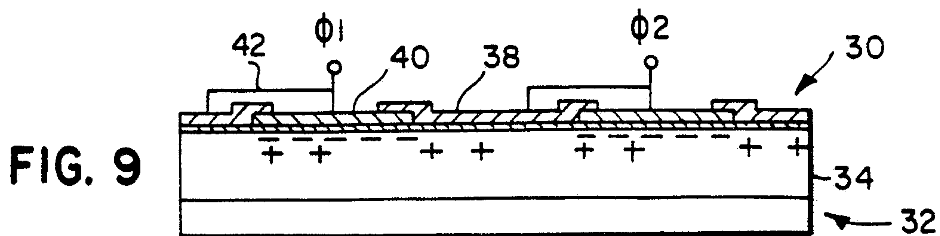

FIG. 9

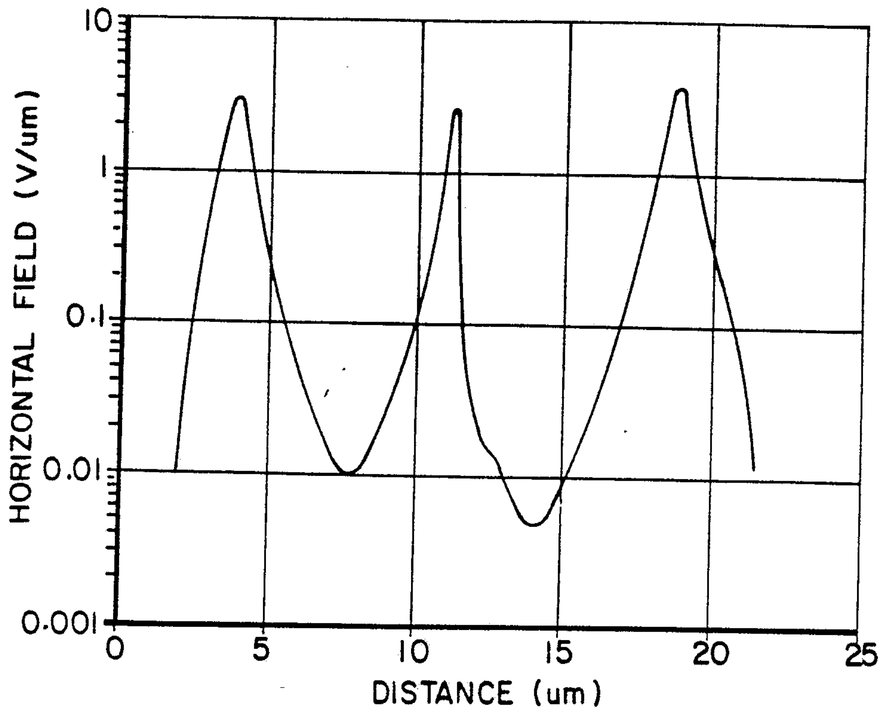

FIG. 10

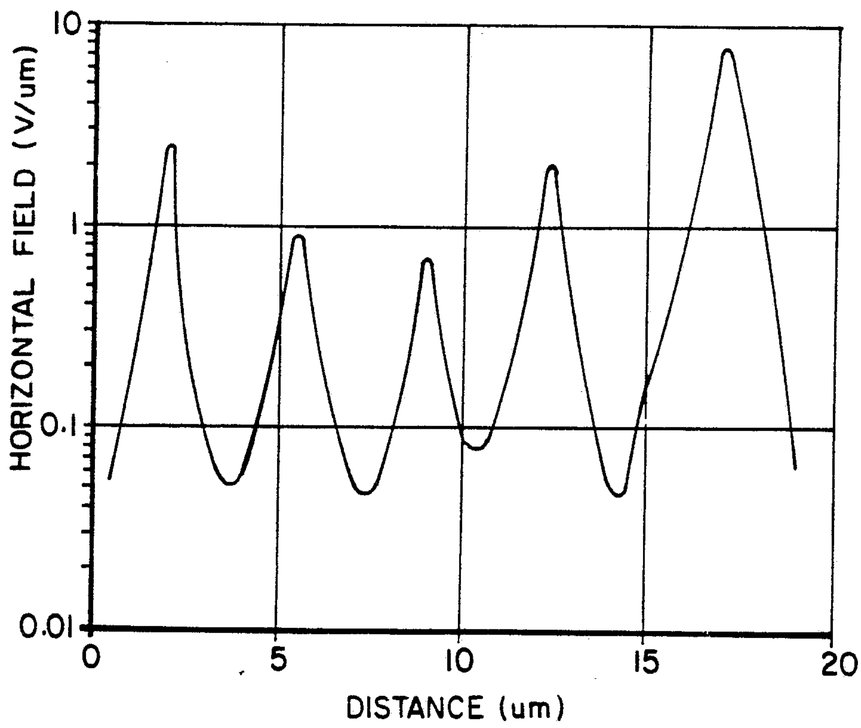

FIG. 11

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 89/03637

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC^5: H 01 L 29/796, H 01 L 21/339

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC^5	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	US, A, 3796932 (AMELIO et al.) 12 March 1974, see column 5, line 13 - column 6, line 12; column 12, line 45 - column 13, line 4; column 19, lines 30-53; figure 1	1,4,6,7
Y		2,3,8,11-14
	--	
Y	International Electron Devices Meeting, Technical Digest, 3-5 December 1979, Washington, D.C., IEEE (New York, US), C.L. Chen et al.: "The effect of interpoly structure variation on charge transfer efficiency of a buried channel CCD", pages 606-610, see page 608, figure 1	2,3,8,11
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Y	DE, A, 2916098 (HITACHI LTD) 31 October 1979, see page 11, line 3 - page 13, line 16; figures 6-11	12-14
A		16
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* Special categories of cited documents: [10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
6th December 1989	08 JAN. 1990
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	T.K. WILLIS

Form PCT/ISA/210 (second sheet) (January 1985)

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This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		CA-A- 1096041	17-02-81
		CA-A- 1003107	04-01-77
		CA-A- 1003108	04-01-77
		DE-A,B,C 2231616	11-01-73
		FR-A,B 2143837	09-02-73
		GB-A- 1376640	11-12-74
		NL-A- 7208841	02-01-73
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		SE-B- 409773	03-09-79
		SE-A- 7509111	14-08-75
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		JP-A- 54140485	31-10-79
		JP-A- 54140464	31-10-79
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		US-A- 4239559	16-12-80

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