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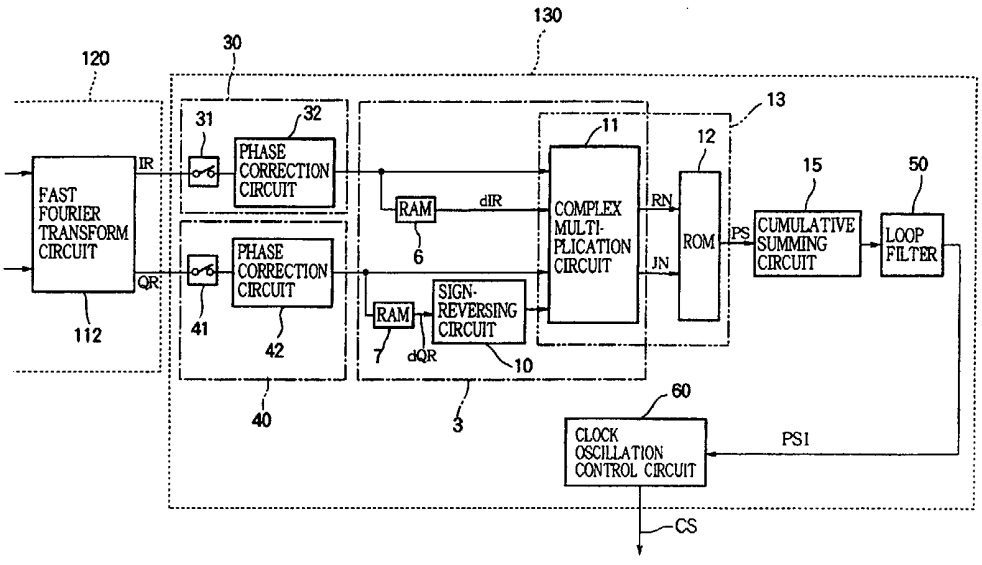
(54) Abstract Title
Clock recovery circuit and method for OFDM

(57) A clock recovery circuit controls a clock oscillator according to phase error detected from a demodulated signal (IR, QR). The demodulated signal, obtained from a signal transmitted by orthogonal frequency division multiplexing, is divided into consecutive symbols, each symbol having components corresponding to different sub-carrier frequencies. The clock recovery circuit selects (31, 41) predetermined components, such as pilot signal components, transmission and multiplexing configuration control signal components, or auxiliary channel signal components, and computes phase deviations between different pairs of the selected components within each symbol (7, 10, 11, 12). These phase deviations are summed (15) over each symbol to obtain the phase error (PSI), enabling large phase errors to be detected, and enabling phase error to be detected even in the absence of frequency error.

FIG.2



GB 2 364 221 A

FIG. 1

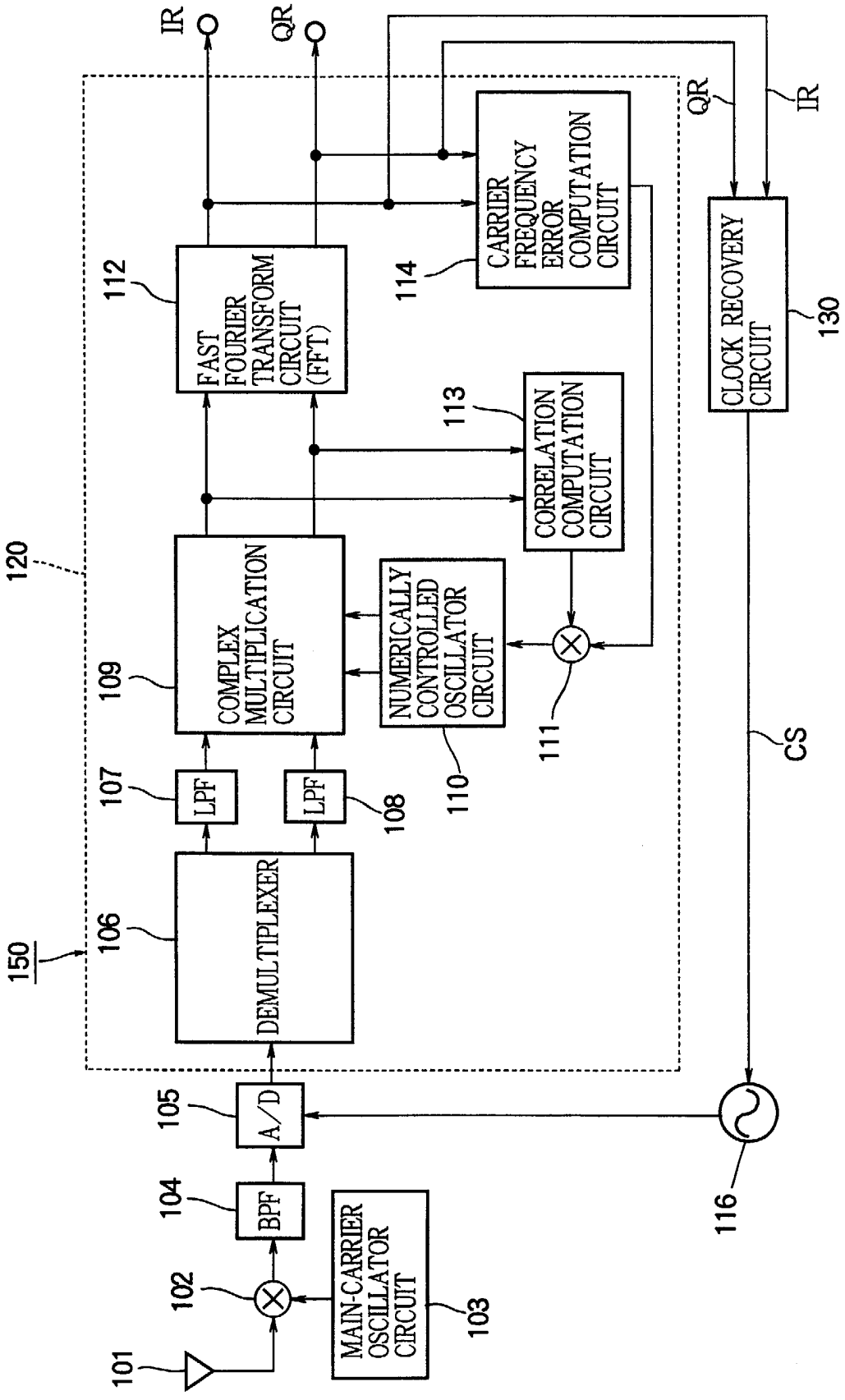

IR
QR
FAST FOURIER TRANSFORM CIRCUIT (FFT)
112
CARRIER FREQUENCY ERROR COMPUTATION CIRCUIT
114
CLOCK RECOVERY CIRCUIT
130
120
113
CORRELATION COMPUTATION CIRCUIT
COMPLEX MULTIPLICATION CIRCUIT
109
NUMERICALLY CONTROLLED OSCILLATOR CIRCUIT
110
111
LPF
107
LPF
108
150
106
DEMULTIPLEXER
105
A/D
104
BPF
102
MAIN-CARRIER OSCILLATOR CIRCUIT
103
101
116
CS

FIG.2

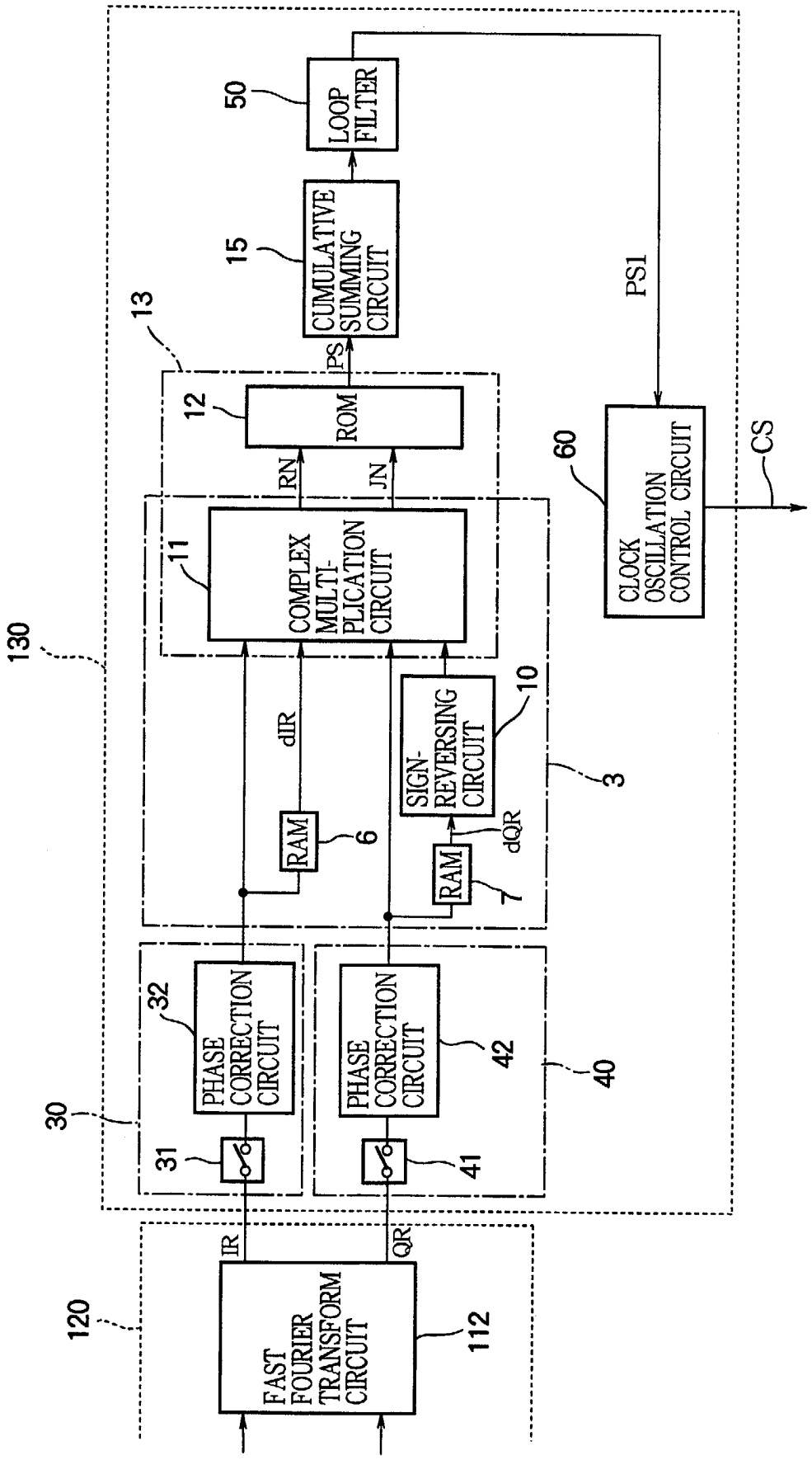

FAST FOURIER TRANSFORM CIRCUIT
112
120
IR
QR
PHASE CORRECTION CIRCUIT
32
31
PHASE CORRECTION CIRCUIT
42
41
30
40
RAM
6
RAM
7
dIR
dQR
SIGN-REVERSING CIRCUIT
10
3
130
COMPLEX MULTI-PLICATION CIRCUIT
11
RN
JN
ROM
12
13
IPS
CUMULATIVE SUMMING CIRCUIT
15
LOOP FILTER
50
PS1
CLOCK OSCILLATION CONTROL CIRCUIT
60
CS

FIG.3

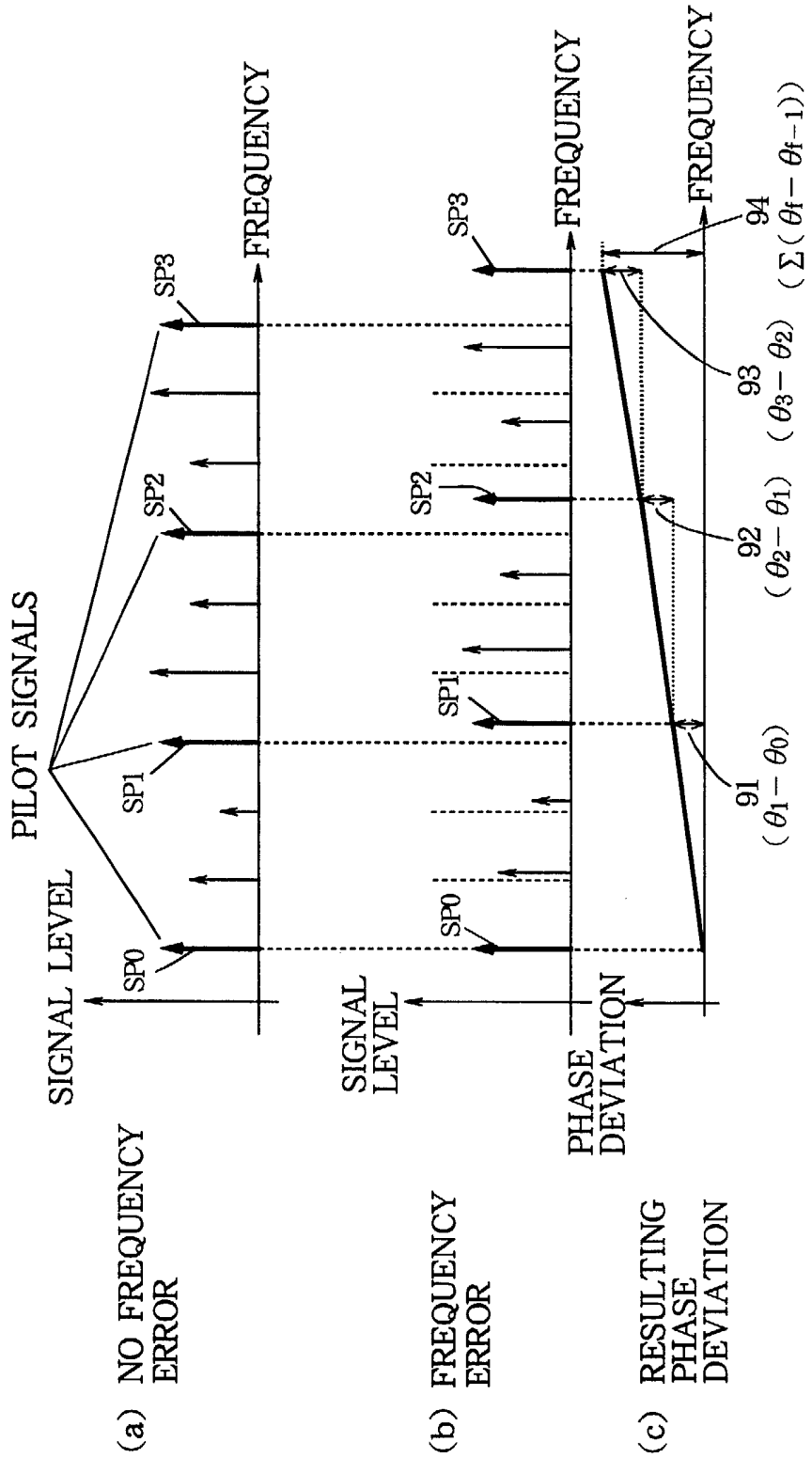

(a) NO FREQUENCY ERROR
SIGNAL LEVEL
PILOT SIGNALS
SP0
SP1
SP2
SP3
FREQUENCY
(b) FREQUENCY ERROR
SIGNAL LEVEL
SP0
SP1
SP2
SP3
FREQUENCY
PHASE DEVIATION
(c) RESULTING PHASE DEVIATION
FREQUENCY
91 (θ1 − θ0)
92 (θ2 − θ1)
93 (θ3 − θ2)
94 (Σ(θf − θf−1))

FIG.4

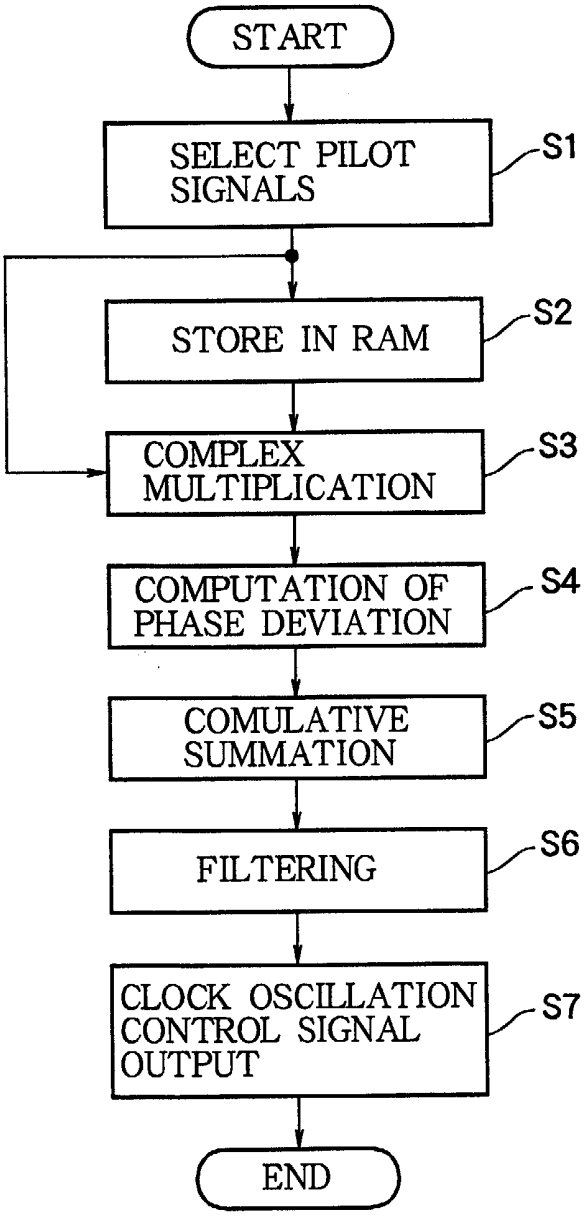

START
SELECT PILOT SIGNALS
S1
STORE IN RAM
S2
COMPLEX MULTIPLICATION
S3
COMPUTATION OF PHASE DEVIATION
S4
COMULATIVE SUMMATION
S5
FILTERING
S6
CLOCK OSCILLATION CONTROL SIGNAL OUTPUT
S7
END

FIG.5

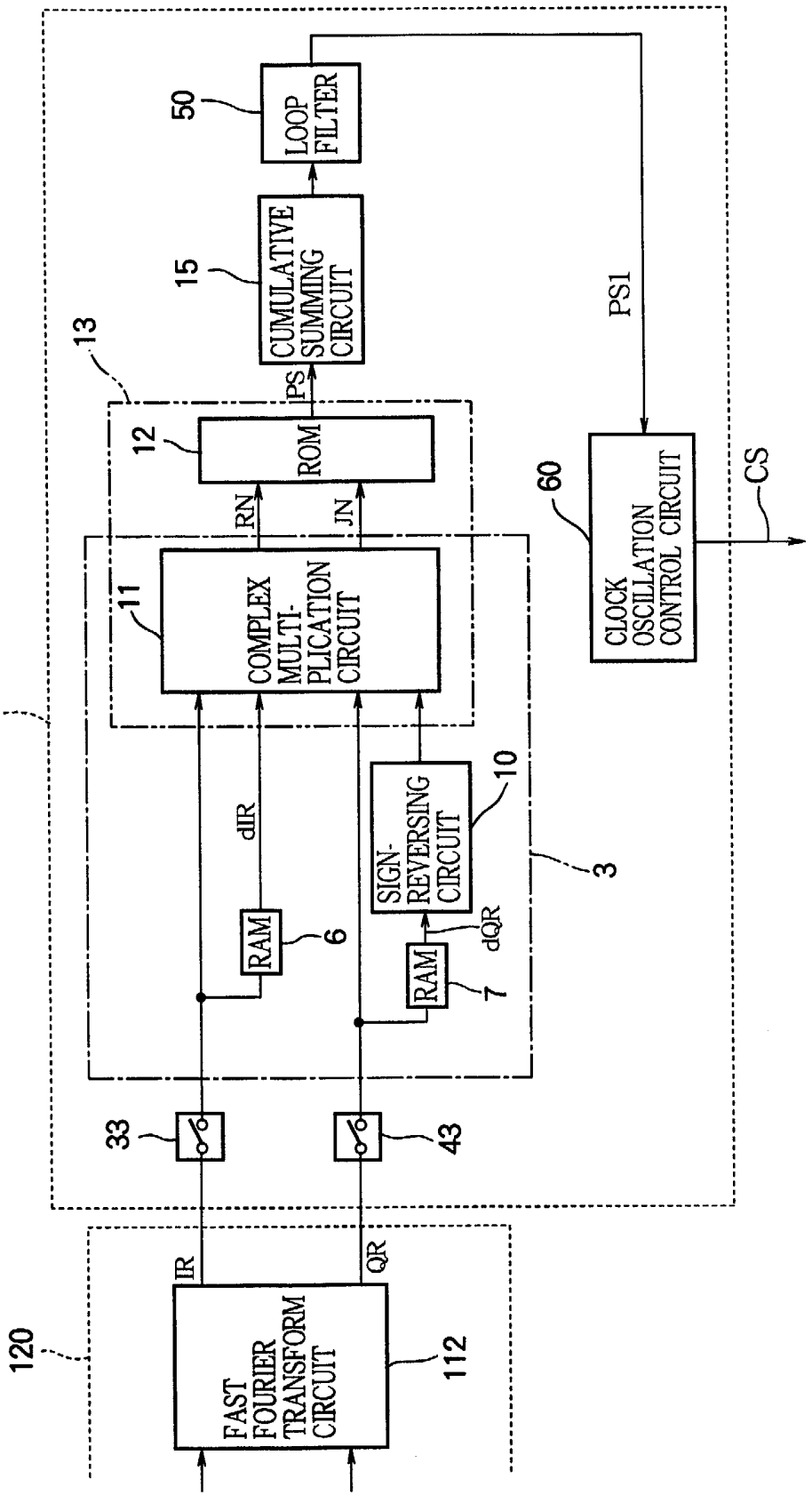

120
FAST FOURIER TRANSFORM CIRCUIT
112
IR
QR
131
33
43
3
dIR
dQR
RAM
6
RAM
7
SIGN-REVERSING CIRCUIT
10
11
COMPLEX MULTI-PLICATION CIRCUIT
RN
JN
12
ROM
13
PS
15
CUMULATIVE SUMMING CIRCUIT
50
LOOP FILTER
PS1
60
CLOCK OSCILLATION CONTROL CIRCUIT
CS

FIG.6

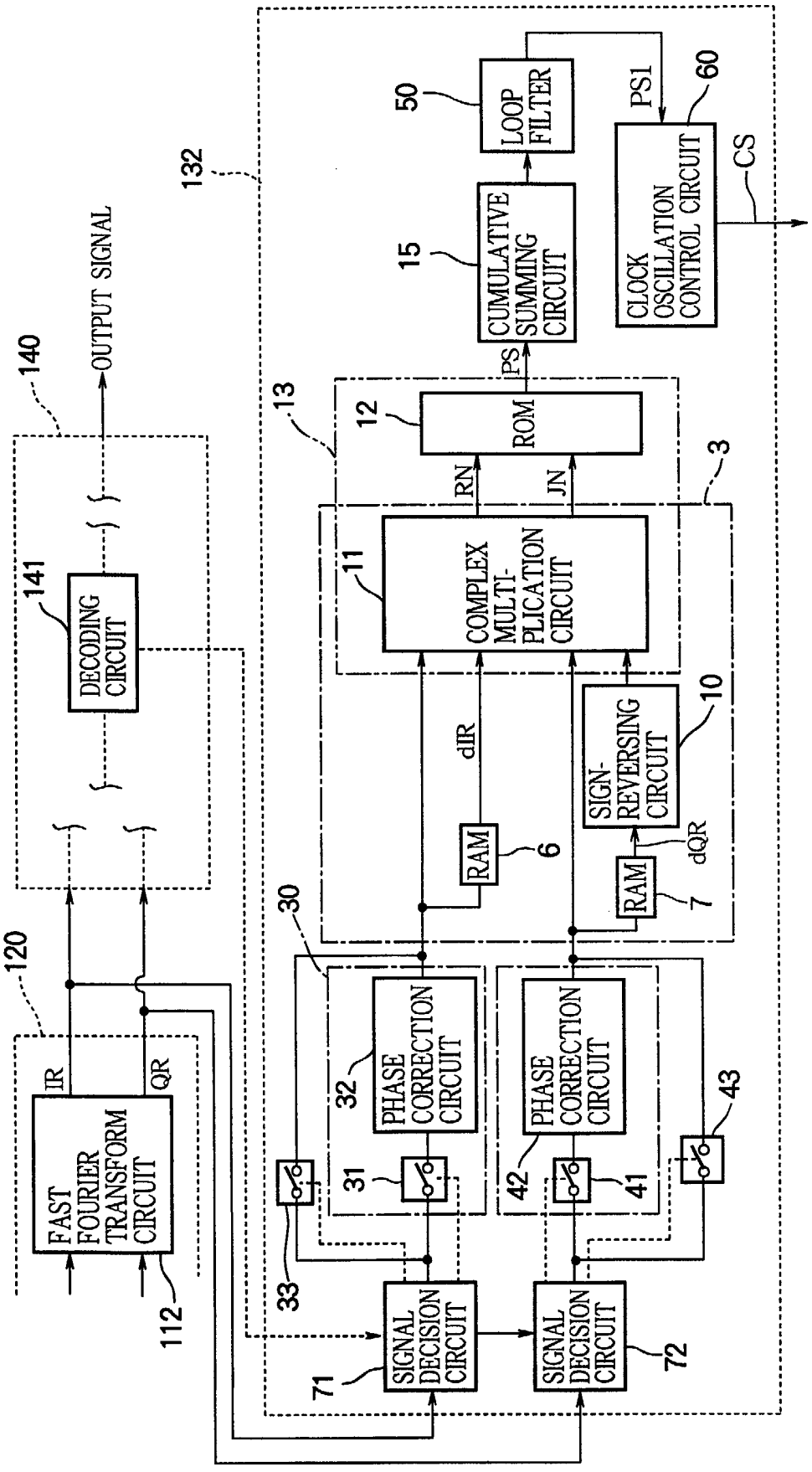

FAST FOURIER TRANSFORM CIRCUIT
IR
QR
112
120
DECODING CIRCUIT
141
140
OUTPUT SIGNAL
132
SIGNAL DECISION CIRCUIT
71
SIGNAL DECISION CIRCUIT
72
33
30
PHASE CORRECTION CIRCUIT
32
PHASE CORRECTION CIRCUIT
42
31
41
43
RAM
6
RAM
7
dIR
dQR
SIGN-REVERSING CIRCUIT
10
COMPLEX MULTI-PLICATION CIRCUIT
11
13
3
RN
JN
ROM
12
PS
CUMULATIVE SUMMING CIRCUIT
15
LOOP FILTER
50
PS1
CLOCK OSCILLATION CONTROL CIRCUIT
60
CS

FIG.7

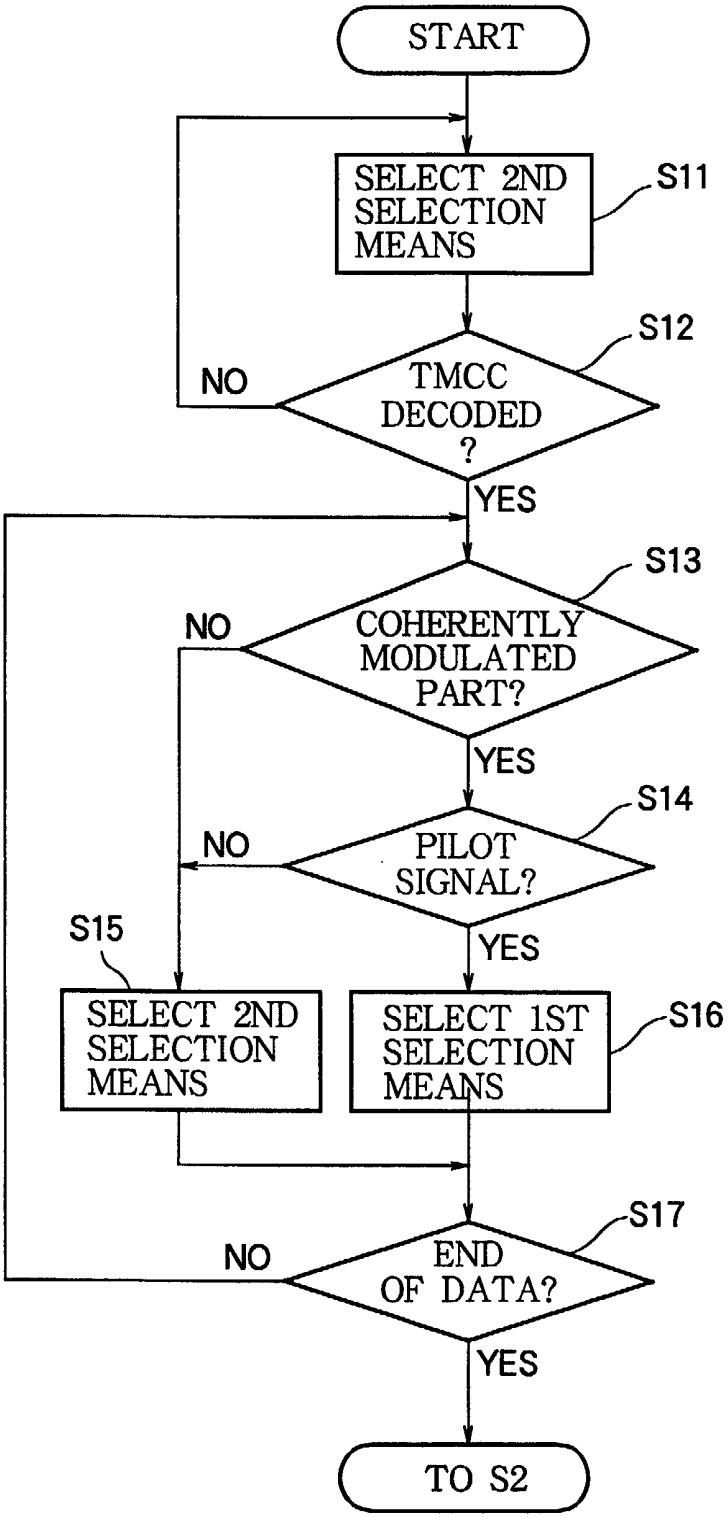

START
SELECT 2ND SELECTION MEANS
S11
S12
NO
TMCC DECODED ?
YES
S13
NO
COHERENTLY MODULATED PART?
YES
S14
NO
PILOT SIGNAL?
S15
YES
SELECT 2ND SELECTION MEANS
SELECT 1ST SELECTION MEANS
S16
S17
NO
END OF DATA?
YES
TO S2

FIG.8

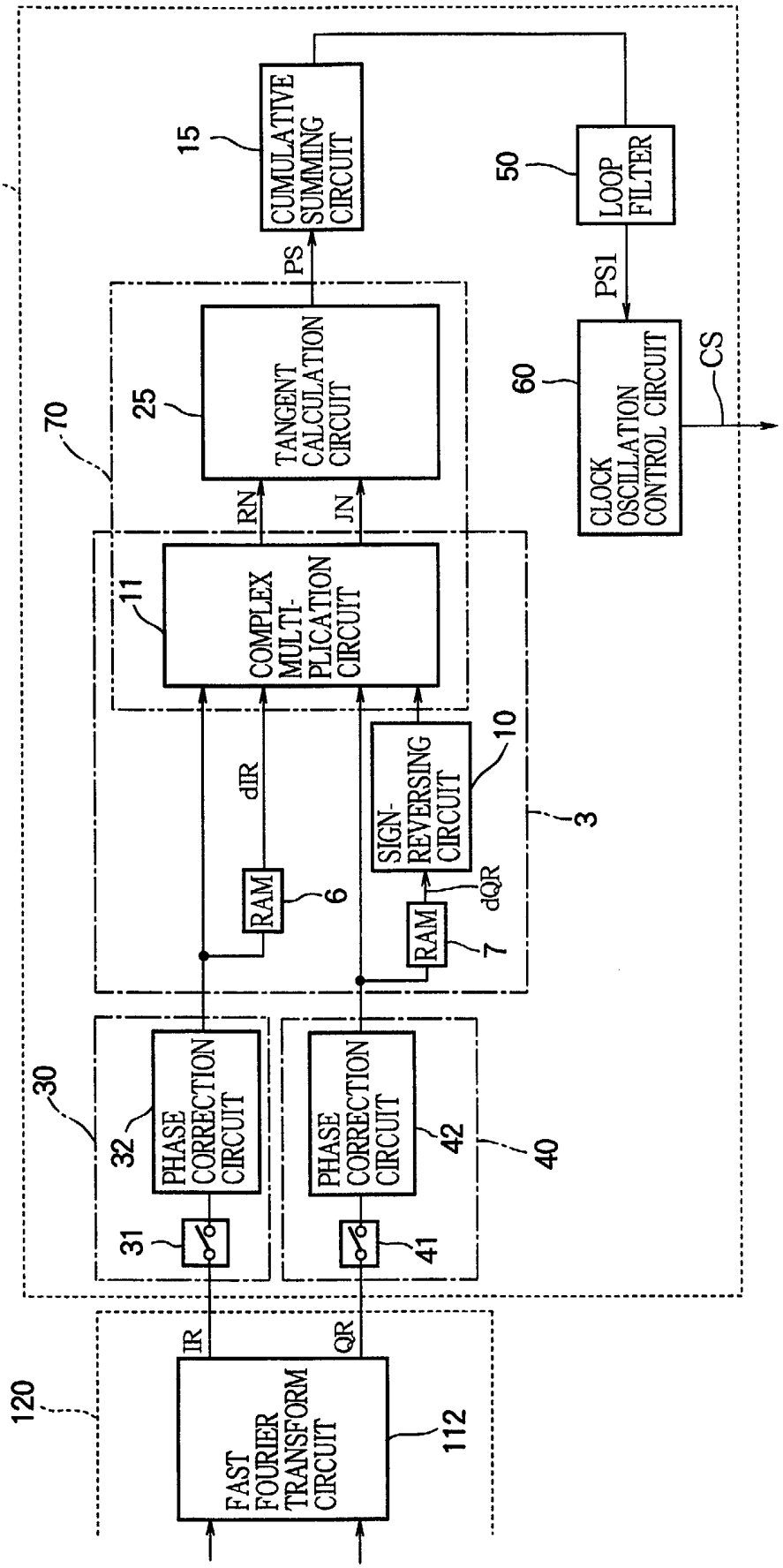

133
120
FAST FOURIER TRANSFORM CIRCUIT
112
IR
QR
30
PHASE CORRECTION CIRCUIT
32
31
40
PHASE CORRECTION CIRCUIT
42
41
3
RAM
6
dIR
RAM
7
dQR
SIGN-REVERSING CIRCUIT
10
70
COMPLEX MULTI-PLICATION CIRCUIT
11
RN
JN
TANGENT CALCULATION CIRCUIT
25
PS
CUMULATIVE SUMMING CIRCUIT
15
LOOP FILTER
50
PS1
CLOCK OSCILLATION CONTROL CIRCUIT
60
CS

FIG.9

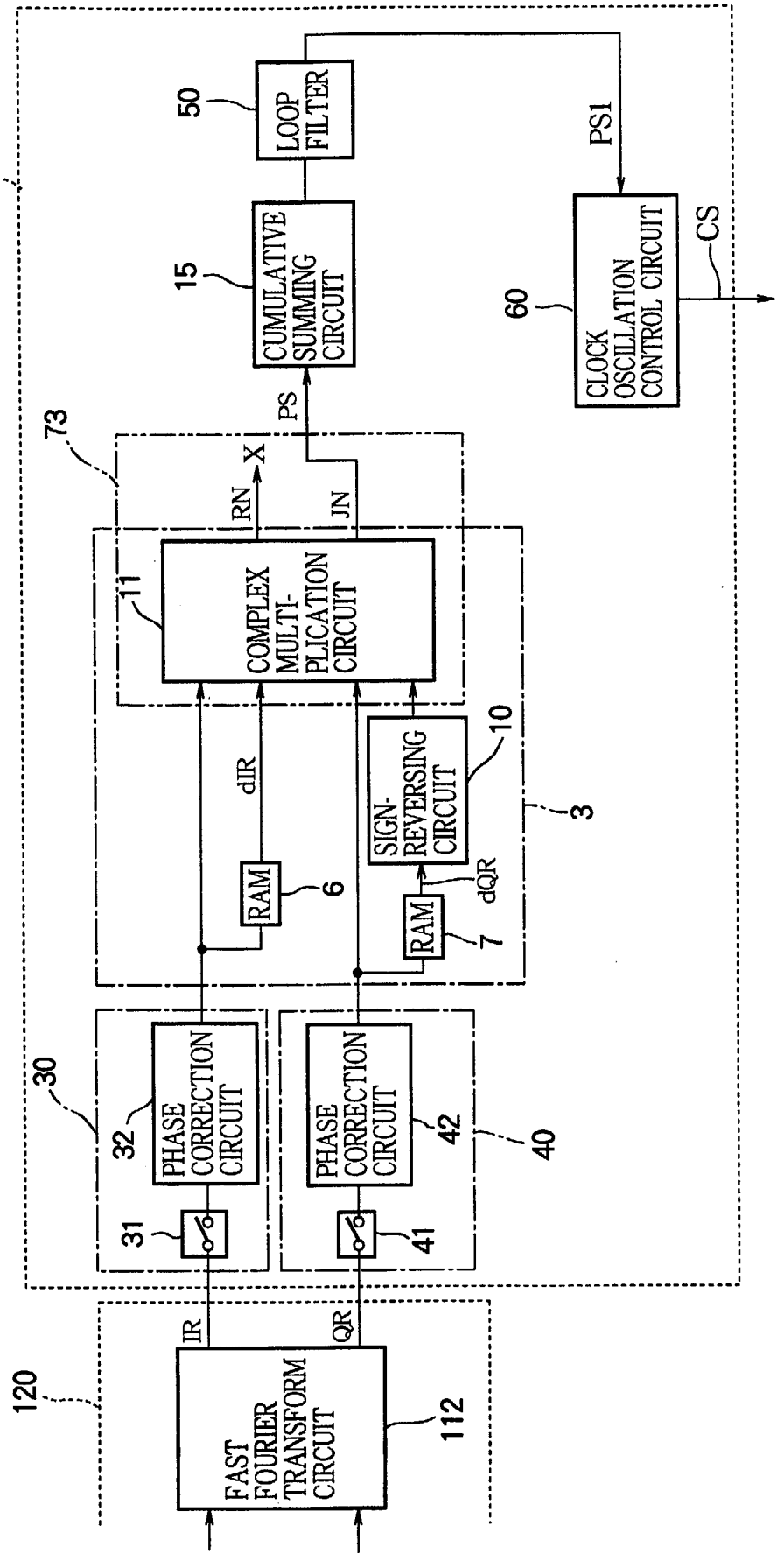

134
120
FAST FOURIER TRANSFORM CIRCUIT
112
IR
QR
30
PHASE CORRECTION CIRCUIT
32
31
40
PHASE CORRECTION CIRCUIT
42
41
3
RAM
6
dIR
RAM
7
dQR
SIGN-REVERSING CIRCUIT
10
73
COMPLEX MULTI-PLICATION CIRCUIT
11
RN
X
JN
PS
15
CUMULATIVE SUMMING CIRCUIT
50
LOOP FILTER
PS1
60
CLOCK OSCILLATION CONTROL CIRCUIT
CS

FIG. 10

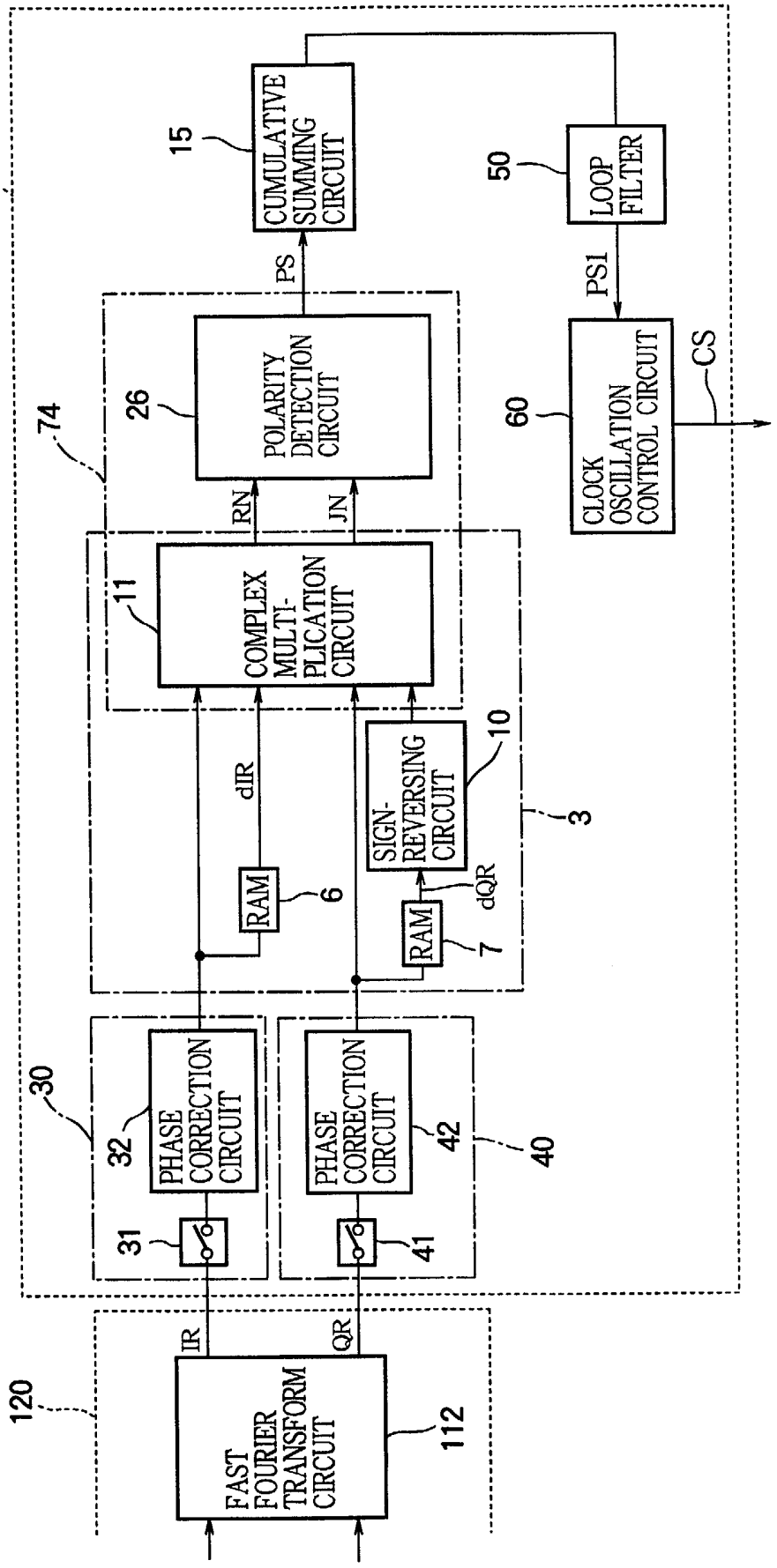

135
15
CUMULATIVE SUMMING CIRCUIT
50
LOOP FILTER
PS
PS1
74
26
POLARITY DETECTION CIRCUIT
60
CLOCK OSCILLATION CONTROL CIRCUIT
CS
RN
JN
11
COMPLEX MULTI-PLICATION CIRCUIT
dIR
10
SIGN-REVERSING CIRCUIT
3
RAM
6
dQR
RAM
7
30
32
PHASE CORRECTION CIRCUIT
PHASE CORRECTION CIRCUIT
42
40
31
41
IR
QR
120
FAST FOURIER TRANSFORM CIRCUIT
112

FIG.11

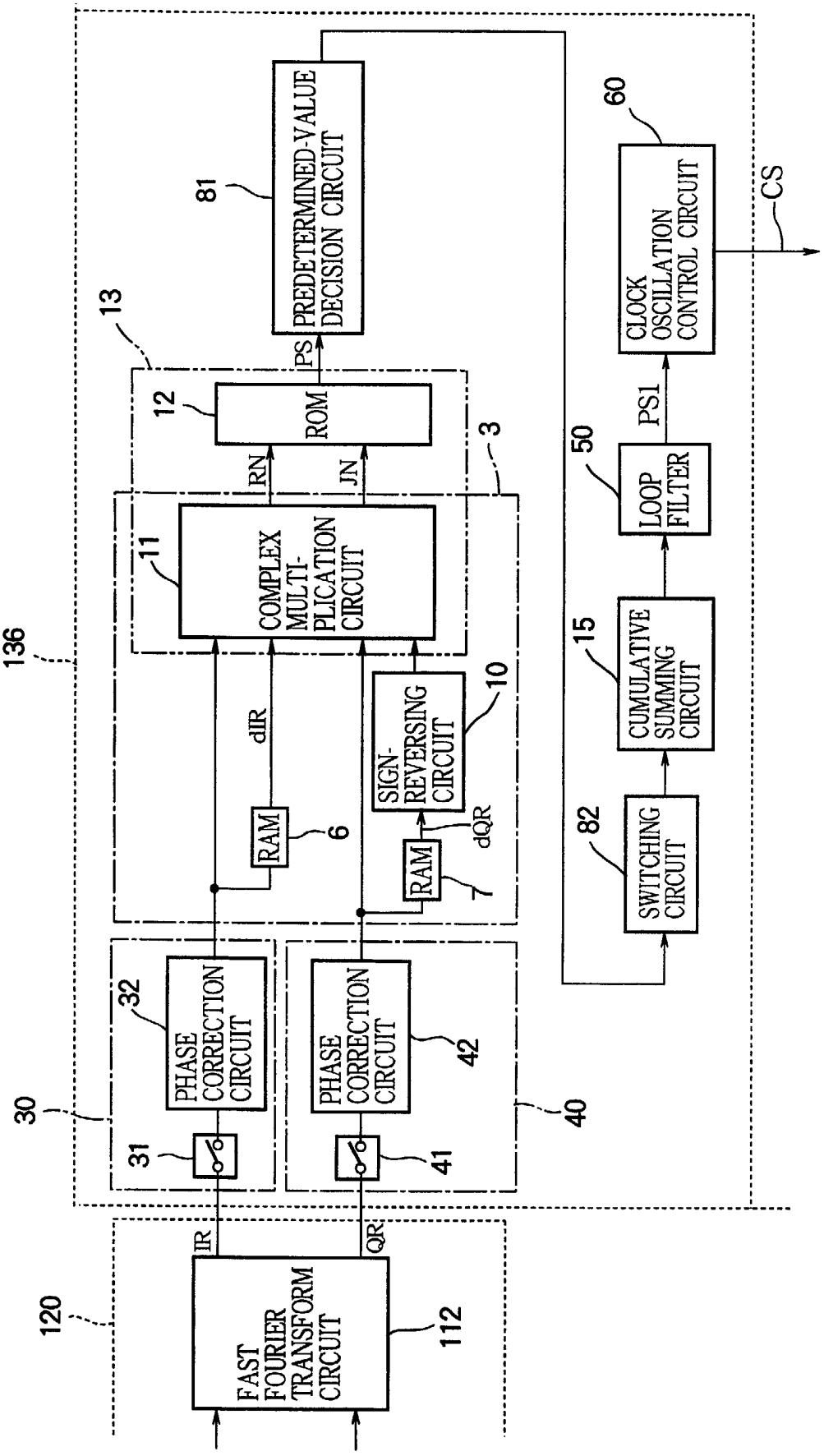

136
120
112
FAST FOURIER TRANSFORM CIRCUIT
IR
QR
30
40
31
41
32
42
PHASE CORRECTION CIRCUIT
PHASE CORRECTION CIRCUIT
RAM
6
RAM
7
dIR
dQR
SIGN-REVERSING CIRCUIT
10
11
COMPLEX MULTI-PLICATION CIRCUIT
3
12
ROM
RN
JN
13
81
PREDETERMINED-VALUE DECISION CIRCUIT
PS
82
SWITCHING CIRCUIT
15
CUMULATIVE SUMMING CIRCUIT
50
LOOP FILTER
PS1
60
CLOCK OSCILLATION CONTROL CIRCUIT
CS

FIG. 12

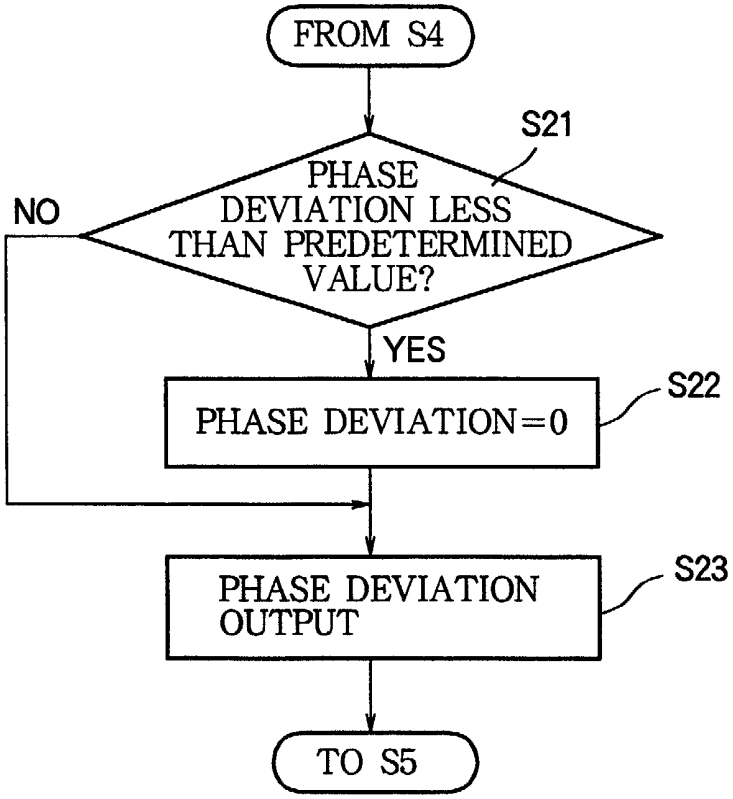
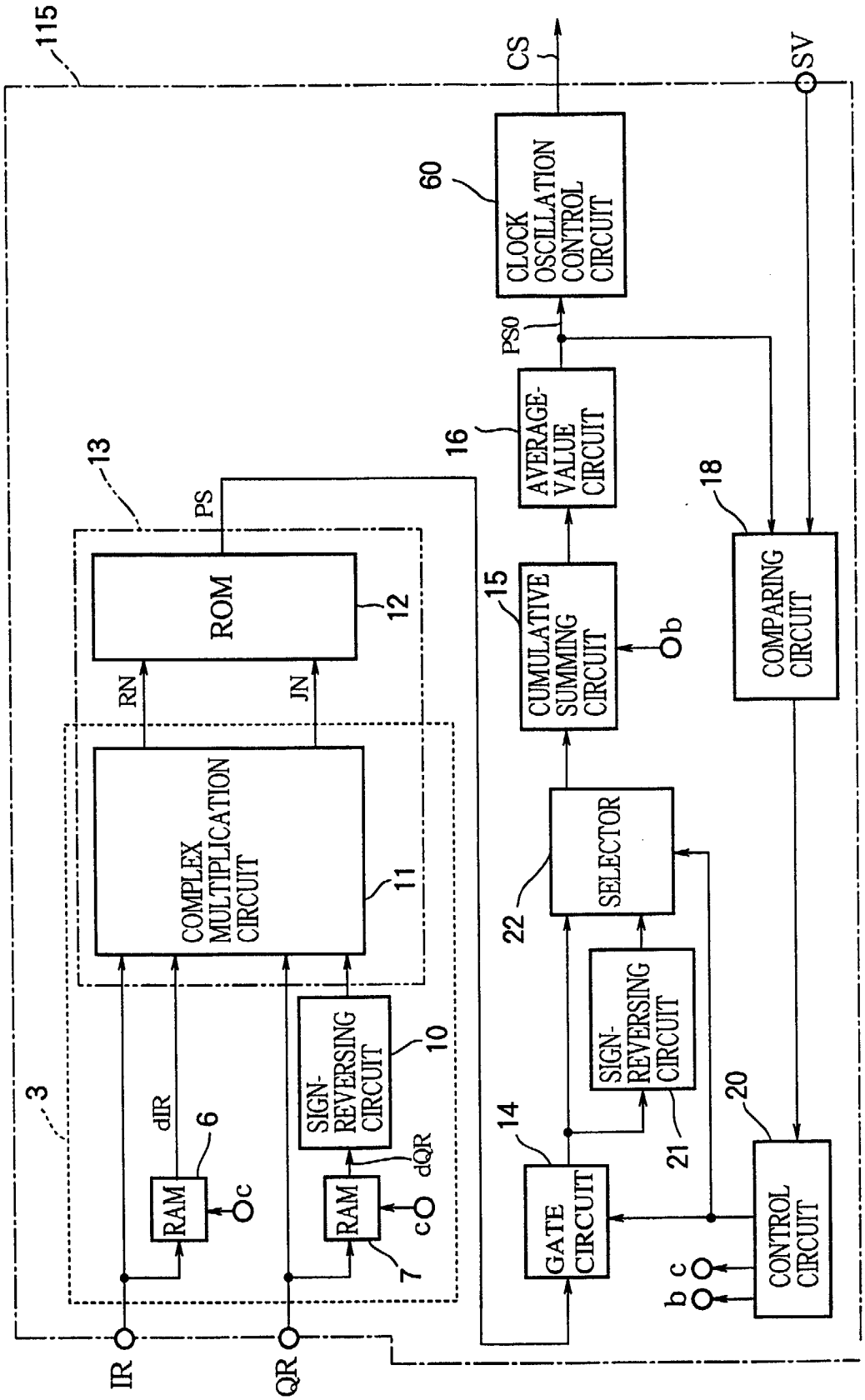

FROM S4
S21
PHASE DEVIATION LESS THAN PREDETERMINED VALUE?
NO
YES
PHASE DEVIATION=0
S22
PHASE DEVIATION OUTPUT
S23
TO S5

FIG.13


115
CS
SV
60
CLOCK OSCILLATION CONTROL CIRCUIT
PS0
16
AVERAGE-VALUE CIRCUIT
18
COMPARING CIRCUIT
13
PS
ROM
12
15
CUMULATIVE SUMMING CIRCUIT
b
RN
JN
COMPLEX MULTIPLICATION CIRCUIT
11
22
SELECTOR
3
dIR
6
RAM
c
SIGN-REVERSING CIRCUIT
10
SIGN-REVERSING CIRCUIT
dQR
RAM
c
7
14
GATE CIRCUIT
21
20
CONTROL CIRCUIT
b c
IR
QR

CLOCK RECOVERY CIRCUIT AND METHOD

BACKGROUND OF THE INVENTION

The present invention relates to a clock recovery apparatus and clock recovery method useful in an OFDM receiver that receives a modulated signal modulated on the basis of the OFDM system.

The modulation system referred to as OFDM (Orthogonal Frequency Division Multiplexing) has recently been proposed as a method of transmitting digital signals. OFDM is a system that provides numerous orthogonal sub-carriers in the transmission band, assigns data to the amplitude and phase of each sub-carrier, and performs digital modulation by using a technology such as PSK (Phase Shift Keying) or QAM (Quadrature Amplitude Modulation). Since this OFDM system divides the transmission band by means of the numerous sub-carriers and transmits the numerous sub-carriers in parallel, the transmission band allotted per sub-carrier is narrowed and the modulation speed per sub-carrier is slowed, but since the number of sub-carriers is large, the overall transmission speed does not differ from conventional modulation systems.

Since numerous sub-carriers are transmitted separately in parallel, the modulation rate in this OFDM system is also slowed because the amount of signal per symbol included in an arbitrary time unit is decreased, but OFDM has the advantage of being robust under interference from multipath interfering waves, because when multipath interfering waves are present in the channel, the relative amount of multipath interfering waves received during the time when the signal for one symbol is being received can be reduced.

Owing to the features described above, the OFDM system is advantageous for transmitting digital signals in terrestrial waves that are strongly affected by multipath

interference due to topography, buildings, and the like, and OFDM has been adopted in the Japanese terrestrial digital broadcasting system.

To demodulate an OFDM modulated signal correctly in a receiver of the OFDM type, however, it is necessary to obtain various types of synchronization in the demodulating circuits, and the clock signal on which all processing in the demodulation process is based must also be synchronized with the clock signal on the transmitting side.

A clock recovery method that has been proposed previously will be described here as a method for synchronizing the clock signal generated on the receiving side with the clock signal on the transmitting side.

FIG. 13 is a block diagram of a clock recovery circuit in an OFDM receiver shown in Japanese Unexamined Patent Publication No. 10-308715.

The clock recovery circuit 115 in the drawing comprises a differential demodulating circuit 3, a ROM (Read Only Memory) 12, a gate circuit 14, a cumulative summing circuit 15 (cumulative summing means), an average-value circuit 16, a comparing circuit 18, a control circuit 20, a sign-reversing circuit 21, a selector 22, and a clock oscillation control circuit 60 (control means); the differential demodulating circuit 3 further has RAMs (Random Access Memory) 6, 7 (memory means), a sign-reversing circuit 10, and a complex multiplication circuit 11.

An analog sub-carrier-frequency signal (IF signal) that has first been demodulated from a main-carrier-frequency signal is digitized by an analog/digital (A/D) conversion circuit in the OFDM receiver, and I-channel data IR (denoted IR below) and Q-channel data QR (denoted QR below), which are generated from the IF signal for each symbol in a sub-carrier-frequency signal (baseband signal) demodulating circuit, are input to the differential demodulating circuit

3, which calculates and outputs real-component data RN and imaginary-component data JN on the basis of the IR and QR. Incidentally, IR and QR are output from a fast Fourier transform (FFT) circuit that performs a discrete Fourier transform in the baseband signal demodulating circuit.

The RAMs 6, 7 in the differential demodulating circuit 3 store the input IR and QR a symbol at a time, responsive to a control signal c output from the control circuit 20, described later, and output the stored data (IR or QR) for each symbol delayed by one symbol period. The sign-reversing circuit 10 outputs the data output from RAM 7 after reversing the positive or negative sign thereof.

If the IR and QR delayed by RAM 6 and RAM 7 are denoted dIR and dQR, respectively, the complex multiplication circuit 11 carries out the complex calculation shown in equation (1) below on the non-delayed IR and QR, separates the calculated results into the real-component data RN and imaginary-component data JN, and outputs them. Incidentally, in the following description, j denotes an imaginary number.

$$(IR + jQR)(dIR - jdQR) \quad ...(1)$$

The ROM (Read Only Memory) 12 stores arctangent (inverse tangent function) data, and outputs phase deviation data PS corresponding to the input real-component data RN and imaginary-component data JN. The complex multiplication circuit 11 and ROM 12 described above also form a computation circuit 13.

From the phase deviation data PS output from the ROM 12, the gate circuit 14, obeying a control signal from the control circuit 20, selects just the components corresponding to pilot signals inserted on the transmitting side, and supplies them to the sign-reversing circuit 21 and selector 22. The sign-reversing circuit 21 reverses the sign

of the input phase deviation data PS (only the components corresponding to pilot signals), and supplies them to the selector 22.

The selector 22, which is controlled by a control signal from the control circuit 20, selects the phase deviation PS input directly from the gate circuit 14, corresponding to a pilot signal, when the phase deviation PS is for a positive frequency component, selects the phase deviation input from the sign-reversing circuit 21 when the phase deviation PS is for a negative frequency component, and supplies the selected quantity to the cumulative summing circuit 15.

The cumulative summing circuit 15 is initialized by a control signal b supplied from the control circuit 20 just before the phase deviations PS for each symbol are input; then it cumulatively sums the phase error PS corresponding to the pilot signals, and outputs it for each symbol.

The average-value circuit 16 averages the cumulatively summed phase errors, output from the cumulative summing circuit 15 for each symbol, over several symbols and generates output at each symbol, thereby outputting a phase error PS0 from which the Gaussian noise included in the phase error has been removed.

The comparing circuit 18 detects that the frequency of the clock signal output from the clock oscillator circuit used in the OFDM receiver has been locked in, which occurs when the symbol-to-symbol differences between the outputs of the average-value circuit 16 vanish because the differentially demodulated data are zero for each symbol, and notifies the control circuit 20. That is, the comparing circuit 18 compares a reference value SV, having a value equal to the output value of the average-value circuit 16 when the symbol-to-symbol differentially demodulated data are zero, and the phase error PS0, which is the current

output value of the average-value circuit 16, and outputs the result of the comparison to the control circuit 20 at each symbol.

The control circuit 20 receives the comparison results of the comparing circuit 18 at each symbol, controls the gate circuit 14 and selector 22 so that they adapt to the timing of the phase deviation PS of each pilot signal, and outputs control signal b to the cumulative summing circuit 15 and control signal c to RAM 6 and RAM 7, thereby controlling them so that the signals input and output from them are input and output for each symbol period.

The clock oscillation control circuit 60 outputs a control signal CS for controlling the oscillation frequency of a clock oscillator used in the OFDM receiver, not shown in the drawing, on the basis of the output data PS0 of the average-value circuit 16.

By using the clock recovery circuit described above, the OFDM receiver shown in Japanese Unexamined Patent Publication No. 10-308715 synchronizes the clock signal generated by the clock oscillator circuit in the OFDM receiver with the clock signal on the transmitting side.

When the sub-carrier signal of the OFDM receiver is demodulated, however, a discrete Fourier transform is performed in the fast Fourier transform circuit, converting the time-domain signal to a frequency-domain signal. The region defining the conversion range in the time domain during this conversion is referred to as a time window. If there is a frequency error or phase error in the clock signal, this time window will be displaced.

For example, when there is only phase error in the clock signal, with no frequency error, the time window is displaced by a fixed time for all symbols, imparting a fixed phase rotation to the frequency components of the sub-carriers of all symbols.

Conversely, when there is only frequency error in the clock signal a displacement that varies with each symbol arises in the time window, imparting a time-varying phase rotation to the frequency components of the sub-carriers.

Here, when the phase error is first detected for all of the sub-carrier signals of the current symbol from all of the sub-carrier signals one symbol before and all of the sub-carrier signals of the current symbol, then only the components corresponding to pilot signals are selected from the phase error and the clock signal is recovered on the basis of the selected components of the phase error, as in the OFDM receiver shown in the above-mentioned Japanese Unexamined Patent Publication No. 10-308715, phase error due to frequency error of the clock signal is included in the detected phase error, but phase error due to phase error of the clock signal is not included.

This is because, when there is frequency error in the clock signal, a time-varying phase rotation occurs in the sub-carriers, as noted above, so the phase of the sub-carrier varies between the pilot signals from symbol to symbol, but when there is only phase error in the clock signal, the phase of the sub-carrier signals does not vary from symbol to symbol, so it cannot be detected as a symbol-to-symbol phase deviation.

The result is that the clock recovery circuit described in the above-mentioned Patent Publication could not control phase error in the clock signal, and had the problem of being unable to improve the clock signal lock-in performance.

Furthermore, if the clock signal lock-in performance cannot be improved, frequency error will be left in the clock signal. When there is frequency error in the clock signal in an OFDM receiver, not only does the bit error rate characteristic worsen in the recovered signal, but there is also the problem of impairments due to inter-sub-carrier

interference, because orthogonality among the sub-carriers is lost.

The present invention addresses the above problems, with the object of providing a clock recovery circuit that can accurately generate a clock signal without frequency error and phase error, for use in an OFDM receiver.

SUMMARY OF THE INVENTION

The invented clock recovery circuit receives a demodulated signal, detects phase error from the demodulated signal, and controls a clock oscillator according to the phase error. The demodulated signal is obtained from a signal transmitted by orthogonal frequency division multiplexing, and is divided into consecutive symbols, each symbol having a plurality of components corresponding to different sub-carrier frequencies. The clock recovery circuit comprises selection means selecting predetermined components from among the components of each symbol of the demodulated signal, memory means storing the predetermined components selected by the selection means, computation means using the predetermined components stored in the memory means to compute phase deviations between different pairs of said predetermined components within each symbol, and cumulative summing means cumulatively summing said phase deviations over each symbol, thereby obtaining the phase error.

In one aspect of the invention, the predetermined components include pilot signal components.

In another aspect of the invention, the predetermined components include transmission and multiplexing configuration control signal components.

In another aspect of the invention, the predetermined components include auxiliary channel signal components.

In another aspect of the invention, the clock recovery

circuit also has signal decision means determining whether the components of each symbol were coherently modulated or differentially modulated, causing the selection means to select pilot signal components as the predetermined components from among the components that were coherently modulated, and causing the selection means to select transmission and multiplexing configuration control signal components and auxiliary channel signal components as said predetermined components from among the components that were differentially modulated.

In any of the above aspects of the invention, the computation means may use a tangent approximation to compute the phase deviations.

Alternatively, the computation means may use a sine approximation to compute the phase deviations.

Alternatively, the computation means may output polarity values as the phase deviations.

The clock recovery circuit may also have decision means comparing the phase deviations with a predetermined value, and changing those phase deviations less than the predetermined value to zero.

In the invented method of recovering a clock signal from a demodulated signal, phase error is detected from the demodulated signal, and a clock oscillator is controlled according to the phase error. The demodulated signal is obtained from a signal transmitted by orthogonal frequency division multiplexing, and is divided into consecutive symbols, each symbol having a plurality of components corresponding to different sub-carrier frequencies. The invented method comprises the steps of selecting predetermined components from among the components of each symbol of the demodulated signal, storing the predetermined components in a memory, using the predetermined components stored in the memory to compute phase deviations between

different pairs of said predetermined components within each symbol, and cumulatively summing said phase deviations over each symbol, thereby obtaining the phase error.

BRIEF DESCRIPTION OF THE DRAWINGS

In the attached drawings:

FIG. 1 is a block diagram showing an OFDM receiver in which a clock recovery circuit of Embodiment One of the present invention is employed;

FIG. 2 is a block diagram showing the clock recovery circuit of Embodiment One;

FIG. 3 is a diagram expressing the phase error that appears in the frequency component of the sub-carrier output from the fast Fourier transform circuit (transform means) in the clock recovery circuit of Embodiment One of the present invention when there is frequency error in the clock signal;

FIG. 4 is a flowchart showing the operation of Embodiment One;

FIG. 5 is a block diagram showing the clock recovery circuit of Embodiment Two of the present invention;

FIG. 6 is a block diagram showing the clock recovery circuit of Embodiment Three of the present invention;

FIG. 7 is a flowchart showing the operation of the selection means in Embodiment Three;

FIG. 8 is a block diagram showing the clock recovery circuit of Embodiment Four of the present invention;

FIG. 9 is a block diagram showing the clock recovery circuit of Embodiment Five of the present invention;

FIG. 10 is a block diagram showing the clock recovery circuit of Embodiment Six of the present invention;

FIG. 11 is a block diagram showing the clock recovery circuit of Embodiment Seven of the present invention;

FIG. 12 is a flowchart showing the operation of the decision means and switching means in the clock recovery

circuit of Embodiment Seven; and

FIG. 13 is a block diagram showing a conventional clock recovery circuit.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments illustrating the present invention will be described below.

Embodiment One

FIG. 1 is a block diagram showing the configuration of an OFDM receiver in which a clock recovery circuit of Embodiment One of the present invention is employed.

The OFDM receiver 150 shown in FIG. 1 comprises a receiving antenna 101, a multiplying circuit 102, a main-carrier oscillator circuit 103, a bandpass filter (BPF) 104, an analog/digital (A/D) conversion circuit 105, a sub-carrier-frequency signal demodulation circuit 120, a clock oscillator 116, and a clock recovery circuit 130. The sub-carrier-frequency signal demodulation circuit 120 further comprises a demultiplexer 106, low-pass filters (LPFs) 107 and 108, a complex multiplication circuit 109, a numerically controlled oscillator circuit 110, a summing circuit 111, a fast Fourier transform (FFT) circuit 112, a correlation computation circuit 113, and a carrier-frequency error computation circuit 114.

The receiving antenna 101 receives a wireless signal modulated by OFDM (an OFDM modulated signal). The multiplying circuit 102 multiplies the received wireless signal by a certain main-carrier-frequency signal output from the main-carrier oscillator circuit 103. The bandpass filter (BPF) 104 extracts an intermediate frequency (IF) signal from the output of the multiplying circuit 102, the intermediate frequency becoming the sub-carrier frequency band. The analog/digital (A/D) conversion circuit 105 converts the analog IF signal extracted by the BPF 104 to a

digital signal.

The demultiplexer 106 separately outputs I-channel IF data and Q-channel IF data from the digitized IF signal. Low-pass filter (LPF) 107 removes unwanted high-frequency components included in the I-channel IF data; LPF 108 removes unwanted high-frequency components included in the Q-channel IF data.

The complex multiplication circuit 109 multiplies the input I-channel IF data and Q-channel IF data by a sub-carrier-frequency signal supplied and controlled by the numerically controlled oscillator circuit 110, thereby generating the I-channel demodulated data and Q-channel demodulated data while removing frequency error. The fast Fourier transform (FFT) circuit 112 generates the I-channel demodulated data IR and the Q-channel demodulated data QR, on which a discrete Fourier transform has been performed, by analyzing the I-channel demodulated data and Q-channel demodulated data, which are time signals input from the complex multiplication circuit 109, into frequencies.

From the transferred guard period of the output signal of the complex multiplication circuit 109 used as is and the guard period of the signal delayed by the effective symbol period, the correlation computation circuit 113 calculates and outputs the correlation value of the two signals. From the output of the FFT circuit 112, the carrier-frequency error computation circuit 114 detects the offset of the output of each frequency, thereby detecting the frequency error of the demodulated data IR and QR, and outputs it to the summing circuit 111. The summing circuit 111 adds the correlation value output by the correlation computation circuit 113 and the frequency error output by the carrier-frequency error computation circuit 114, and supplies their sum to the numerically controlled oscillator circuit 110.

In the sub-carrier-frequency signal demodulation

circuit 120, the frequency error of the transformed data IR and QR output from the downstage FFT circuit 112 can be minimized because the FFT circuit 112 is made to start computing at the timing at which the correlation is maximized by the complex multiplication circuit 109, as described above.

From the demodulated data IR and QR, the clock recovery circuit 130 generates and outputs a control signal CS to control the oscillation frequency of the clock oscillator 116. The clock oscillator 116 generates the clock signal according to the control signal CS output from the clock recovery circuit 130, and supplies it to the A/D conversion circuit 105 and other circuits.

FIG. 2 is a block diagram showing the configuration of the clock recovery circuit of Embodiment One of the present invention.

In the clock recovery circuit 130 shown in FIG. 2, incidentally, parts with the same functions as in the conventional clock recovery circuit 115 shown in FIG. 13 have the same reference characters.

The points on which the clock recovery circuit 130 of FIG. 2 and the conventional clock recovery circuit 115 shown in FIG. 3 differ are that in the clock recovery circuit 130, selectors 30 and 40 are provided as first selection means selecting only the data corresponding to the pilot signals designated by the transmitting side from the demodulated data IR and QR, before the demodulated data IR and QR are input to the differential demodulating circuit 3, and the processing circuit from when the computation circuit 13 comprising the complex multiplication circuit 11 and ROM 12 outputs the phase deviation data PS until a signal is input to the clock oscillation control circuit 60 comprises the cumulative summing circuit 15 and a loop filter 50 (filter means).

Selector 30 includes a switch 31 that selects only the

data corresponding to the pilot signals from the demodulated data IR, and a phase correction circuit 32 that removes a phase value designated by the transmitting side from the data selected by switch 31. Similarly, selector 40 includes a switch 41 that selects only the data corresponding to the pilot signals from the demodulated data QR, and a phase correction circuit 42 that removes a phase value designated by the transmitting side from the data selected by switch 41.

The phases corresponding to the pilot signals designated by the transmitting side are, for example, phase values designated in the Japanese Digital Terrestrial Broadcasting Standards. In the Japanese Digital Terrestrial Broadcasting Standards, the amplitude and phase of the subcarriers corresponding to the pilot signals are predetermined by the transmitting side, and the predetermined values are also known to the receiving side. Specifically, if the transmitting side designates the phase of a pilot signal as zero or π, the receiving side is informed in advance that the phase of the carrier signal corresponding to the received pilot signal will be zero or π. If the known phase of the sub-carrier corresponding to this pilot signal is π, the phase correction circuits 32, 42 correct the phase of the pilot signal by subtracting π and output the corrected signal.

In the differential demodulating circuit 3 of the present embodiment, differential demodulation is performed only on the data corresponding to pilot signals. The demodulated data IR and QR output from the phase correction circuits 32 and 42 are stored in the RAMs 6 and 7, at which time only the data corresponding to pilot signals in the demodulated data IR and QR are stored, and delayed demodulated data dIR and dQR, which have been delayed by a time equivalent to one interval between the occurrence of pilot signals, are output. The sign-reversing circuit 10

outputs the delayed demodulated data output from RAM 7 after reversing the sign thereof, but here too, only the delayed demodulated data dQR corresponding to pilot signals are output.

The complex multiplication circuit 11 performs a complex computation on the non-delayed demodulated pilot-signal data IR and QR and the delayed demodulated pilot-signal data dIR and dQR delayed by the RAMs 6 and 7, and outputs the result, separating it into pilot-signal real-component data RN and pilot-signal imaginary-component data JN.

From its stored arctangent (inverse tangent function) data, the ROM 12 reads the data corresponding to the input pilot-signal real-component data RN and imaginary-component data JN, and outputs them as pilot-signal phase deviation data PS.

The cumulative summing circuit 15 cumulatively sums the pilot-signal phase deviation data PS output from the ROM 12 over one symbol period. The loop filter 50 removes noise components from the cumulatively summed data of the pilot-signal phase deviation data PS output from the cumulative summing circuit 15. From the output data (the cumulatively summed data of the pilot-signal phase deviation data PS) of the loop filter 50, the clock oscillation control circuit 60 outputs the control signal CS that controls the oscillation frequency of the clock oscillator 116.

FIG. 3 (a), (b), and (c) are diagrams for explaining the phase error that appears in the frequency components of the demodulated data IR and QR input to the clock recovery circuit 130 in FIG. 2 when there is frequency error in the clock signal generated by the clock oscillator 116 in FIG. 1. FIG. 3 (a) is a diagram showing the frequency components of the demodulated data IR and QR when there is no frequency error in the clock signal; FIG. 3 (b) is a diagram showing

the frequency components of the demodulated data IR and QR when there is frequency error in the clock signal; and FIG. 3 (c) is a drawing showing the phase error of the frequency components of the pilot signals in the demodulated data IR and QR when there is frequency error in the clock signal.

In FIG. 3 (a) and (b), SP0 is the lowest-frequency pilot signal in one symbol; SP1 and SP2 are higher-frequency pilot signals in the same symbol as pilot signal SP0; and SP3 is the highest-frequency pilot signal in the same symbol as pilot signal SP0.

In FIG. 3 (c), 91 is the phase deviation ($\theta_1 - \theta_0$) between the phase θ_0 of the lowest-frequency pilot signal SP0 and the phase θ_1 of pilot signal SP1; 92 is the phase deviation ($\theta_2 - \theta_1$) between the phase θ_1 of pilot signal SP1 and the phase θ_2 of pilot signal SP2; and 93 is the phase deviation ($\theta_3 - \theta_2$) between the phase θ_2 of pilot signal SP2 and the phase θ_3 of the highest-frequency pilot signal SP3. Furthermore, 94 is the cumulative sum of the phase deviations 91 to 93 of adjacent pilot signals in the same symbol, this being a phase deviation $\Sigma(\theta_f - \theta_{f-1})$.

The cumulatively summed phase deviation 94 matches the phase deviation from the lowest-frequency pilot signal SP0 to the highest-frequency pilot signal SP3 in the same symbol. That is, if the cumulative sum of the phase deviations of the frequency components of adjacent pilot signals in the same symbol is taken over one symbol period, it will be equal to the phase deviation from the lowest-frequency pilot signal to the highest-frequency pilot signal occurring in the same symbol.

Next, the operation of Embodiment One of the present invention, shown in FIG. 1 and FIG. 2, will be described.

FIG. 4 is a flowchart showing the operation of Embodiment One.

The data of the sub-carriers corresponding to the pilot

signals designated on the transmitting side are selected by selectors 30 and 40 from the demodulated data IR and QR output from the FFT circuit 112 in the sub-carrier-frequency signal demodulation circuit 120, and the selected data are output (step S1).

The demodulated pilot-signal data output from selectors 30 and 40 are supplied to RAMs 6 and 7. RAM 6 stores the demodulated pilot-signal data IR, and RAM 7 stores the demodulated pilot-signal data QR; the stored data are held until the demodulated data IR and QR corresponding to the next pilot signal are supplied. RAM 6 and RAM 7 thus output delayed demodulated data dIR and dQR in which the stored demodulated data have been delayed by a time equivalent to one interval between pilot signals (step S2).

The delayed demodulated data dQR output from RAM 7 are also output with plus/minus sign reversed by the sign-reversing circuit 10.

The demodulated data IR, the demodulated data QR, the delayed demodulated data dIR, and the sign-reversed delayed demodulated data dQR of the pilot signals are supplied to the complex multiplication circuit 11, and complex multiplication is carried out. The result of the computation in the complex multiplication circuit 11 is separated into real-component data RN and imaginary-component data JN and output from the complex multiplication circuit 11 (step S3).

Arctangent (inverse tangent function) data corresponding to the real-component data RN and imaginary-component data JN output from the complex multiplication circuit 11 are read out in the ROM 12, and the phase deviations PS between adjacent pilot signals are calculated and output, based on those values (step S4).

The cumulative summing circuit 15 adds up the phase deviation data PS between adjacent pilot signals output from the ROM 12 in the same symbol over one symbol period. When

the cumulative sum for a one-symbol portion has been completed, the cumulatively summed result is output, and the cumulative sum is initialized (step S5).

The cumulatively summed result output from the cumulative summing circuit 15 when the cumulative sum for a one-symbol portion has been completed is supplied to the loop filter 50. The cumulatively summed result is output as phase deviation data PS1 from which unwanted noise components have been removed by the loop filter 50 (step S6).

From the phase deviation data PS1, which is the cumulative sum of the pilot-signal phase deviations in the same symbol, detected as described above, the clock oscillation control circuit 60 detects frequency error and phase error of the clock signal present in the phase deviation data PS1, and outputs a control signal CS for controlling the oscillation frequency of the clock oscillator 116 (step S7).

The A/D conversion circuit 105, sub-carrier-frequency signal demodulation circuit 120, clock recovery circuit 130, and clock oscillator 116 shown in FIG. 1 thus form a phase-locked loop (PLL) that controls the frequency of the clock signal.

In the present embodiment, data having the phase deviation between adjacent pilot signals in the same symbol as a parameter are obtained by performing complex multiplication after selecting the pilot signals, as described above. That is, the phase deviation of the sub-carrier-frequency components corresponding to the pilot signals in the same symbol is calculated in the present embodiment, as shown in FIG. 3 (c). Even when the phase of the sub-carriers does not vary between symbols, the phase deviations due to frequency error and phase error in the clock signal can thus be detected, and the clock signal lock-in performance can be improved.

Calculating the phase deviation 94 in one operation, without performing cumulative addition as in the present embodiment, would also be conceivable. The largest phase deviation value that can be calculated at once by the computation circuit 13 is $+2\pi$, however, so if the phase deviation 94 from the lowest-frequency pilot signal SP0 to the highest-frequency pilot signal SP3 in the same symbol was $+3\pi$, for example, and if it were calculated in one operation, it could not be calculated correctly; a spurious phase deviation of $+\pi$ would be calculated.

The number of pilot signals in a symbol is generally large, so the phase deviations 91 to 93 between adjacent pilot signals will not be equal to or greater than $+2\pi$, but cases in which the phase deviation 94 in the same symbol is equal to or greater than $+2\pi$, e.g. to $+3\pi$, are conceivable.

In the configuration of the present embodiment, however, if the phase deviations 91 to 93 between adjacent pilot signals are all less than $+2\pi$, then even if the total phase deviation 94 from the lowest-frequency pilot signal SP0 to the highest-frequency pilot signal SP3 in the same symbol is $+2\pi$ or more, the phase deviation 94 in the same symbol can be calculated correctly, because the phase deviations 91 to 93 between adjacent pilot signals are summed over one symbol period, and the detection range of the phase deviation 94 from the lowest-frequency pilot signal SP0 to the highest-frequency pilot signal SP3 in the same symbol can be expanded to $+2\pi$ or more.

Since the number of pilot signals in a symbol is large, as mentioned above, the frequency of calculation of the phase deviation 94 can also be increased, by calculating the phase deviation at periods shorter than one symbol period, for example. In that case, the clock signal lock-in speed and performance can be improved, because the calculation accuracy of the phase deviation is improved.

If the clock signal lock-in performance is improved as described above, impairments due to inter-sub-carrier interference can be mitigated during demodulation, and the bit error rate characteristic of the recovered signal can be improved.

Embodiment Two

Whereas the above-described Embodiment One used phase information of the pilot signals, Embodiment Two uses phase information of TMCC signals or AC signals.

A TMCC signal is a signal used for multiplexing control (Transmission and Multiplexing Configuration Control); it carries the most basic information needed for demodulating the transmitted signal in the receiver, such as transmission parameters including, for example, the modulation system, the error correcting code system, and the like. An AC signal is a signal used for an auxiliary channel for carrying additional information such as second audio, text information, or the like.

In OFDM transmission according to the Japanese Terrestrial Digital Broadcasting Standards, differentially modulated parts for which modulation of the sub-carriers by DQPSK or the like is specified and coherently modulated parts for which modulation by QPSK, QAM or the like is specified are transmitted together. Pilot signals are included in the coherently modulated parts as signals for coherent demodulation, but pilot signals are not included in the differentially modulated parts. In the above-described Embodiment One, accordingly, phase deviation cannot be calculated while a differentially modulated part is being received. The present embodiment is therefore adapted to calculate the phase deviation from phase information of sub-carrier frequency components corresponding to TMCC signals and AC signals, instead of pilot signals, when a differentially modulated signal is received.

According to the above Japanese Terrestrial Digital Broadcasting Standards, the frequency components of the sub-carriers corresponding to the TMCC signals and AC signals in the same symbol are all transmitted with the same phase. Accordingly, the phase deviation in the same symbol can be easily calculated using the phase information of the TMCC signals and AC signals, just as with the pilot signals shown in the above-described Embodiment One.

FIG. 5 is a block diagram showing the configuration of the clock recovery circuit of Embodiment Two of the present invention.

In the clock recovery circuit 131 shown in FIG. 5, incidentally, parts with the same functions as in the conventional clock recovery circuit 115 shown in FIG. 13 and the clock recovery circuit 130 of Embodiment One shown in FIG. 2 have the same reference characters.

The configuration of the OFDM receiver in which the clock recovery circuit 131 of Embodiment Two of the present invention is used is moreover similar to the configuration of FIG. 1 used in Embodiment One.

The points on which the clock recovery circuit 131 of the present embodiment in FIG. 5 and the clock recovery circuit 130 of Embodiment One in FIG. 2 differ are that clock recovery circuit 130 had first selection means comprising selectors 30 and 40 that selected only data corresponding to the pilot signals designated on the transmitting side from the demodulated data IR and QR, while clock recovery circuit 131 has second selection means comprising selectors 33 and 34 that select only the data corresponding to the TMCC signals and AC signals designated by the transmitting side.

Selector 33 has a switch function that selects only the data corresponding to the TMCC signals and AC signals from the demodulated data IR. Similarly, selector 43 has a switch

function that selects only the data corresponding to the TMCC signals and AC signals from the demodulated data QR.

Furthermore, the phase correction circuits 32 and 42 that were necessary in Embodiment One are unnecessary, because the TMCC signals and AC signals are transmitted with the same phase in the same symbol. Structures other than the above are similar to Embodiment One.

Next, the operation of Embodiment Two of the present invention will be described.

In the operation of Embodiment Two, step S1 in the operation of Embodiment One, explained using FIG. 4, is not a process of selecting pilot signals, but is changed to a process of selecting TMCC signals and AC signals. The pilot signals used in the subsequent steps are therefore also changed to the TMCC signals and AC signals.

With the TMCC signals and AC signals, the phase deviations of the sub-carrier frequency components in the same symbol can also be calculated in the differentially modulated parts, which do not include pilot signals, as described above. It is also possible to increase the number of frequency components for detecting phase deviation by using both the TMCC signals and the AC signals, so the calculation accuracy of the phase deviation can be improved, because the frequency of calculation of the phase deviation can be increased, and the clock signal lock-in speed and performance can be improved.

Embodiment Three

Whereas the above-described Embodiment One used phase information of the pilot signals, and Embodiment Two used phase information of the TMCC signals and AC signals, Embodiment Three uses phase information of the pilot signals, TMCC signals, and AC signals, switching between them at each received modulated part.

As stated above, in OFDM transmission according to the

Japanese Terrestrial Digital Broadcasting Standards, differentially modulated parts for which modulation of the sub-carriers by DQPSK or the like is specified and coherently modulated parts for which modulation by QPSK, QAM or the like is specified are transmitted together, and pilot signals are included in the aforesaid coherently modulated parts as signals for coherent demodulation, but pilot signals are not included in the differentially modulated parts. The TMCC signals and AC signals are included in both the coherently modulated parts and the differentially modulated parts, but the arrangement of the transmitted frequencies when included in the coherently modulated parts and when included in the differentially modulated parts differs partly. Also, since the coherently modulated parts and the differentially modulated parts are output for transmission together, the transmitting side is adapted to transmit timing information about the switchover of the modulation parts by means of the TMCC signals. The receiving side detects the aforesaid modulation-part switchover timing information of the received modulated signal by analyzing (decoding) the TMCC signals, and carries out demodulation appropriate for each modulation part by using that timing information.

Accordingly, in the period from the time when the OFDM receiver starts receiving until it decodes the TMCC signals, it is unclear as to the timing of the switchover between the coherently modulated parts and the differentially modulated parts. Therefore, in the initial receiving state, the present embodiment calculates the phase deviation using only the phase information of the frequency components corresponding to the TMCC signals and AC signals transmitted with a common frequency arrangement in the differentially modulated parts and the coherently modulated parts, and in the state in which it has detected the timing information by

decoding the TMCC signals and the arrangement in the transmitted output of the differentially modulated parts and the coherently modulated parts has become clear, it calculates the phase deviation using the phase information of the pilot signals, TMCC signals, and AC signals with the frequency arrangement designated for each modulation part.

FIG. 6 is a block diagram showing the configuration of the clock recovery circuit of Embodiment Three of the present invention.

In the clock recovery circuit 132 shown in FIG. 6, incidentally, parts with the same functions as in the conventional clock recovery circuit 115 shown in FIG. 13, the clock recovery circuit 130 of Embodiment One shown in FIG. 2, and the clock recovery circuit 131 of Embodiment Two shown in FIG. 5 have the same reference characters.

The configuration of the OFDM receiver in which the clock recovery circuit 132 of Embodiment Three of the present invention is used is moreover similar to the configuration of FIG. 1 used in Embodiment One.

The points on which the clock recovery circuit 132 of the present embodiment in FIG. 6 differs from the clock recovery circuit 130 of Embodiment One in FIG. 2 or the clock recovery circuit 131 of Embodiment Two in FIG. 5 are that in the clock recovery circuit 130 or clock recovery circuit 131, the selection means comprised only the selectors 30 and 40 constituting the first selection means, or only the selectors 33 and 43 constituting the second selection means, but the clock recovery circuit 132 of the present embodiment has both selection means, the selectors 30 and 40 constituting the first selection means and the selectors 33 and 43 constituting the second selection means, and is provided with signal decision circuits 71 and 72 (signal decision means) that decide whether the demodulated data input to the clock recovery circuit 132 are in a

differentially modulated part or a coherently modulated part, in order to control the operation of the selection means.

Selector 30 and selector 33 are connected in parallel between the signal decision circuit 71 and the differential demodulating circuit 3. Similarly, selector 40 and selector 43 are connected in parallel between the signal decision circuit 72 and the differential demodulating circuit 3.

The demodulated data IR and timing information obtained as a result of the decoding of the TMCC signals by a decoding circuit 141, described below, are input to signal decision circuit 71. Signal decision circuit 71 also outputs the demodulated data IR and a control signal for controlling the selection operation of selector 30 and selector 33. Similarly, demodulated data QR and timing information obtained as a result of the decoding of the TMCC signals by the decoding circuit 141 are input to signal decision circuit 72. Signal decision circuit 72 also outputs the demodulated data QR and a control signal for controlling the selection operation of selector 40 and selector 43.

The decoding circuit 141 is a circuit in the output signal generating circuit 140, disposed downstage of the sub-carrier-frequency signal demodulation circuit 120, that decodes signals coded on the transmitting side. As described above, timing information about switchovers between coherently modulated parts and differentially modulated parts is included in the TMCC signals transmitted by the transmitting side in the present embodiment. The decoding circuit 141 can accordingly obtain timing information about switchovers between the coherently modulated parts and the differentially modulated parts by decoding the TMCC signals. The timing information thus obtained is sent to the signal decision circuits 71 and 72.

Next, the operation of Embodiment Three of the present invention, shown in FIG. 6, will be described.

In the operation of Embodiment Three, step S1 in the operation of Embodiment One, explained using FIG. 4, is not a process of selecting pilot signals, but is changed to a process of selecting between selectors 30 and 40, which constitute the first selection means, and selectors 33 and 43, which constitute the second selection means, by the signal decision circuits 71 and 72. By this process, and the particular functions of each selector, phase information of the pilot signals, TMCC signals, and AC signals is output correctly.

FIG. 7 is a flowchart showing the parts of the operation of Embodiment Three that differ from Embodiment One.

In the initial state, at the start of reception, when the TMCC signals have not yet been decoded, the signal decision circuits 71 and 72, using selectors 33 and 43, select and output data corresponding to the TMCC signals and AC signals transmitted with a common frequency arrangement in the differentially modulated parts and the coherently modulated parts among the demodulated data IR and QR output from the FFT circuit 112 in the sub-carrier-frequency signal demodulation circuit 120 (step S11).

The signal decision circuits 71 and 72 decide whether or not the decoding of the TMCC signals by the decoding circuit 141 has ended and timing information has been input (step S12), proceed to step S13 if timing information has been input (step 12: yes), and return to step S11 if timing information has not been input (step S12: no).

From the input timing information, the signal decision circuits 71 and 72 decide whether the demodulated data IR and QR are in a coherently modulated part or not (step S13), proceed to step S14 if they are in a coherently modulated part (step S13: yes), and proceed to step S15 if they are not in a coherently modulated part (step S13: no).

Selectors 30 and 40 decide whether the coherently modulated parts of the input demodulated data IR and QR are pilot signals or not (step S14), proceed to step S16 if they are pilot signals (step S14: yes), and proceed to step S15 if they are not pilot signals (step S14: no).

Selectors 33 and 34 output phase information of the TMCC signals and AC signals (step S15); selectors 30 and 40 output phase information of the pilot signals (step S16).

The signal decision circuits 71 and 72 decide whether the input demodulated data IR and QR have ended or not (step S17), proceed to step S2 in FIG. 4 if they have ended (step S17: yes), and return to step S13 if they have not ended (step S17: no).

By selecting and using the data of sub-carrier frequency components corresponding to the TMCC signals and AC signals transmitted with a common frequency arrangement in the differentially modulated parts and the coherently modulated parts just after reception begins, as described above, the present embodiment can perform lock-in of the clock signal regardless of whether in a differentially modulated part or a coherently modulated part.

It can also increase the number of sub-carrier frequency components for detecting the phase deviation, by selecting a selection means corresponding to pilot signals, or TMCC signals and AC signals, included in larger number in each modulated part, after the TMCC signals have been decoded and the frequency arrangement of each modulated part has been recognized.

Thus by using all of the pilot signals, TMCC signals, and AC signals, it can increase the number of frequency components for detecting phase deviation, improve the calculation accuracy of the phase deviation by increasing the calculation frequency of the phase deviation, and can improve the clock signal lock-in speed and performance.

Embodiment Four

In the above-described Embodiment One, when the phase deviation PS is calculated in the computation means 13, the data of the real component RN and imaginary component JN output from the complex multiplication circuit 11 are supplied to the ROM 12, and phase deviation data PS corresponding to the input real component RN and imaginary component JN data are output from the ROM 12, which stores arctangent (inverse tangent function) data. If the value of the phase calculated here using the arctangent (inverse tangent function) is sufficiently small in comparison with $\pm\pi/4$, for example, it can be approximated using the tangent function as will be described below. The present embodiment is adapted to use this tangent approximation capability to output a tangent approximation for the phase deviation data output from the computation means.

FIG. 8 is a block diagram showing the configuration of the clock recovery circuit of Embodiment Four of the present invention.

In the clock recovery circuit 133 shown in FIG. 8, incidentally, parts with the same functions as in the conventional clock recovery circuit 115 shown in FIG. 13 and the clock recovery circuit 130 of Embodiment One shown in FIG. 2 have the same reference characters.

The configuration of the OFDM receiver in which the clock recovery circuit 133 of Embodiment Four of the present invention is used is moreover similar to the configuration of FIG. 1 used in Embodiment One.

The point on which the clock recovery circuit 133 of the present embodiment in FIG. 5 and the clock recovery circuit 130 of Embodiment One in FIG. 2 differ is that in the clock recovery circuit 130, a ROM 12 was provided in the computation means 13, but in the clock recovery circuit 133 of the present embodiment, a tangent calculation circuit 25

is provided in the computation means 70.

The tangent calculation circuit 25 calculates the value of the tangent from the data of the real component RN and imaginary component JN output from the complex multiplication circuit 11.

The complex multiplication circuit 11 performs the calculation shown in equation (1), as shown in the description of the conventional clock recovery circuit 115. If the sub-carrier frequency component corresponding to the f-th pilot signal is written in complex notation as $A_f e\uparrow(j\theta_f)$, for example, where A indicates the amplitude and θ indicates the phase of the sub-carrier frequency component, then equation (1) can be written as in the next equation (2).

$$(A_f e\uparrow(j\theta_f))(A_{f-1} e\uparrow(-j\theta_{f-1}))$$
$$= A_{f-1}A_f \cos(\theta_f - \theta_{f-1}) + jA_{f-1}A_f \sin(\theta_f - \theta_{f-1})$$
$$= Re + Im \quad \ldots(2)$$

The tangent $\tan(\theta_f - \theta_{f-1})$ can be calculated from the real part Re and imaginary part Im of the above equation (2). When $\theta_f - \theta_{f-1}$ is sufficiently small in comparison to $\pm\pi/4$, as is normally the case, the phase deviation $\theta_f - \theta_{f-1}$ can be approximated by this tangent calculation.

$$Im/Re = \tan(\theta_f - \theta_{f-1}) \approx \theta_f - \theta_{f-1} \quad \ldots(3)$$

Next, the operation of Embodiment Four of the present invention, shown in FIG. 8, will be described.

In the operation of Embodiment Four, the processing of step S4 in the operation of Embodiment One, explained using FIG. 4, is not a process of calculating arctangent phase deviation data PS corresponding to the input data, carried out by the ROM 12 shown in Embodiment One, but is changed to a process of calculating tangent phase deviation data PS

from the input data, carried out by the tangent calculation circuit 25. The other operations of the present Embodiment Four are similar to the operations of Embodiment One.

Specifically, in clock recovery circuit 130, the output of the complex multiplication circuit 11 was input to the ROM 12, and the phase deviation data PS were output from the ROM 12, but in the clock recovery circuit 133 of the present embodiment, the output of the complex multiplication circuit 11 in the computation means 70 is input to the tangent calculation circuit 25, and the phase deviation data PS are output from the tangent calculation circuit 25.

By employment of the phase deviation data PS approximated using the tangent as described above, the phase deviation PS can be calculated easily, just by calculating the value of the tangent, without using a ROM 12 as in Embodiment One.

Embodiment Five

By taking advantage of the fact that when the value of the phase deviation PS is sufficiently small, the value of a phase calculated using the arctangent can be approximated with the tangent function, the above-described Embodiment Four was adapted not to use a ROM 12, but Embodiment Five is adapted to calculate the phase deviation PS by approximating the value of the phase calculated using the arctangent with the sine function.

FIG. 9 is a block diagram showing the configuration of the clock recovery circuit of Embodiment Five of the present invention.

In the clock recovery circuit 134 shown in FIG. 9, incidentally, parts with the same functions as in the conventional clock recovery circuit 115 shown in FIG. 13 and the clock recovery circuit 130 of Embodiment One shown in FIG. 2 have the same reference characters.

The configuration of the OFDM receiver in which the

clock recovery circuit 134 of Embodiment Five of the present invention is used is moreover similar to the configuration of FIG. 1 used in Embodiment One.

The point on which the clock recovery circuit 134 of the present embodiment in FIG. 9 and the clock recovery circuit 130 of Embodiment One in FIG. 2 differ is that in the clock recovery circuit 130, a ROM 12 was provided in the computation means 13, but in the clock recovery circuit 134 of the present embodiment, nothing but the complex multiplication circuit 11 is provided in the computation means 73.

The present embodiment uses the fact that when the value of $\theta_f - \theta_{f-1}$ is sufficiently small in relation to $\pm\pi/4$, the imaginary part Im in equation (2) shown in the description of the above Embodiment Four can be approximated with the equation (4) shown below.

$$A_{f-1}A_f\sin(\theta_f - \theta_{f-1}) \approx A_{f-1}A_f(\theta_f - \theta_{f-1}) \qquad \ldots(4)$$

If the value of $A_{f-1}A_f$ calculated by the complex multiplication circuit 11 varies only slightly, so that the result of cumulative addition of the value of equation (4) over one symbol in the cumulative summing circuit 15 can be regarded as, for example, the phase deviation in one symbol multiplied by a fixed value, then the value of equation (4) expresses the phase deviation, and a value corresponding to the phase error and frequency error of the clock signal can be detected. That is, the phase deviation PS can be approximated by the imaginary part of equation (2).

Next, the operation of Embodiment Five of the present invention, shown in FIG. 9, will be described.

In the operation of the present Embodiment Five, the processing of step S4 in the operation of Embodiment One, explained using FIG. 4, is not a process of calculating

arctangent phase deviation data PS corresponding to the input data, carried out by the ROM 12 shown in Embodiment One, but is changed to a process of using the imaginary-component data JN output from the complex multiplication circuit 11 as the phase deviation data PS. The real-component data RN output from the complex multiplication circuit 11 are not used. The other operations of the present Embodiment Five are similar to the operations of Embodiment One.

Specifically, in clock recovery circuit 130, the output of the complex multiplication circuit 11 was input to the ROM 12, and the phase deviation data PS were output from the ROM 12, but in the clock recovery circuit 134 of the present embodiment, the imaginary-component data JN from the complex multiplication circuit 11 in the computation means 73 are output, unchanged, as the phase deviation data PS.

By employment of phase deviation data PS thus calculated approximately with the sine function, the imaginary-component data in the multiplication result of the complex multiplication circuit 11 can be used without change as the phase deviation PS, and even in comparison with the approximation by the tangent function shown in Embodiment Four, the phase deviation can be obtained more easily, by omitting the process of dividing the imaginary part Im by the real part Re.

Embodiment Six

Whereas the above-described Embodiment Five was adapted to calculate the phase deviation PS in the computation means 73 by approximating it with a sine function, the present Embodiment Six is adapted to output only the polarity of the value approximated with the sine function from the computation means 74 as the phase deviation PS.

FIG. 10 is a block diagram showing the configuration of the clock recovery circuit of Embodiment Six of the present

invention.

In the clock recovery circuit 135 shown in FIG. 10, incidentally, parts with the same functions as in the conventional clock recovery circuit 115 shown in FIG. 13 and the clock recovery circuit 130 of Embodiment One shown in FIG. 2 have the same reference characters.

The configuration of the OFDM receiver in which the clock recovery circuit 135 of Embodiment Six of the present invention is used is moreover similar to the configuration of FIG. 1 used in Embodiment One.

The point on which the clock recovery circuit 135 of the present embodiment in FIG. 10 and the clock recovery circuit 130 of Embodiment One in FIG. 2 differ is that in the clock recovery circuit 130, a ROM 12 was provided in the computation means 13, but in the clock recovery circuit 135 of the present embodiment, a polarity detection circuit 26 is provided in the computation means 74.

In equation (4) in the above-described Embodiment Five, a case was shown in which the variation of $A_{f-1}A_f$, which is the result of multiplication of the amplitude values of the frequency components, calculated and output from the complex multiplication circuit 11, was negligibly small in comparison with the phase deviation PS. If the variation of $A_{f-1}A_f$ in equation (4) is not negligible in comparison with the phase deviation PS, however, then the approximation error can be kept small by treating the polarity of the imaginary part of equation (2), for example, as the phase deviation PS. A polarity detection circuit 26 that detects the polarity of the imaginary part of equation (2) from the output of the complex multiplication circuit 11 is therefore provided in the computation means 74 in the present embodiment. When the polarity of the imaginary part of equation (2) is positive, +1 is output by the polarity detection circuit 26 as the phase deviation PS, and when the

polarity is negative, -1 is output as the phase deviation PS.

Next, the operation of Embodiment Six of the present invention, shown in FIG. 10, will be described.

In the operation of the present Embodiment Six, the processing of step S4 in the operation of Embodiment One, explained using FIG. 4, is not a process of calculating arctangent phase deviation data PS corresponding to the data input from the ROM 12 shown in Embodiment One, but is changed to a process of detecting a polarity from the imaginary-component data JN output from the complex multiplication circuit 11. The real-component data RN output from the complex multiplication circuit 11 are not used. The other operations of the present Embodiment Six are similar to the operations of Embodiment One.

Specifically, in clock recovery circuit 130, the output of the complex multiplication circuit 11 was input to the ROM 12, and the phase deviation data PS were output from the ROM 12, but in the clock recovery circuit 135 of the present embodiment, the imaginary-component data output JN from the complex multiplication circuit 11 in the computation means 74 are input to the polarity detection circuit 26, and the phase deviation data PS are output from the polarity detection circuit 26.

Output of the polarity of a sine approximation to the phase deviation PS enables the polarity of the imaginary-component data in the output of the complex multiplication circuit 11 to be used, unchanged, as the phase deviation PS, and even in comparison with tangent approximation shown in Embodiment Four, the phase deviation can be obtained more easily, by omitting the process of dividing the imaginary part Im by the real part Re. Also, in comparison with the sine approximation shown in Embodiment Five, when the value of $A_{f-1}A_f$, which is the result of multiplication of the amplitude values of the frequency components as noted above,

varies greatly each time it is calculated and the variation cannot be ignored, there is the advantage that the calculation accuracy of the phase deviation can be improved.

Embodiment Seven

Whether or not the phase deviation PS of the sub-carrier-frequency components corresponding to the pilot signals, TMCC signals, and AC signals selected by the selection means in Embodiments One, Two, and Three described above falls short of a predetermined value is determined, and it if is determined that the phase deviation PS falls short of the predetermined value, control of the frequency of the clock signal on the basis of the phase deviation PS computed by the computation means 13 is disabled.

FIG. 11 is a block diagram showing the configuration of the clock recovery circuit of Embodiment Seven of the present invention.

In the clock recovery circuit 136 shown in FIG. 11, incidentally, parts with the same functions as in the conventional clock recovery circuit 115 shown in FIG. 13 and the clock recovery circuit 130 of Embodiment One shown in FIG. 2 have the same reference characters.

The configuration of the OFDM receiver in which the clock recovery circuit 136 of Embodiment Seven of the present invention is used is moreover similar to the configuration of FIG. 1 used in Embodiment One.

Incidentally, the present embodiment is applicable to all of the embodiments described above, but in the following description, it will be applied to Embodiment One.

The point on which the clock recovery circuit 136 of the present embodiment in FIG. 10 and the clock recovery circuit 130 of Embodiment One in FIG. 2 differ is that in the clock recovery circuit 130, the computation means 13 and the cumulative summing circuit 15 were directly interconnected, but in the clock recovery circuit 136 of the

present embodiment, a predetermined-value decision circuit 81 (decision means) and a switching circuit 82 (switching means) are provided between the computation means 13 and the cumulative summing circuit 15.

The predetermined-value decision circuit 81 is a circuit that decides whether or not the phase deviation PS output from the ROM 12 falls short of a predetermined value designated by the user. The switching circuit 82 is a circuit that does not output the value of the phase deviation PS to the downstage cumulative summing circuit 15 when the predetermined-value decision circuit 81 decides that the phase deviation PS falls short of the predetermined value, but outputs '0' instead.

The predetermined value designated by the user in the present embodiment is, for example, a value due to Gaussian noise generated from the computation means 13 even when demodulated data IR and QR are not actually being input to the clock recovery circuit 136, or a value to which the value of the computation error generated in the computation means 13 is added.

Next, the operation of Embodiment Seven of the present invention, shown in FIG. 11, will be described.

In the operation of Embodiment Seven, an additional process is inserted between the process of computing the phase deviation (step S4) and the cumulative summing process (step S5) in the operation of Embodiment One, explained using FIG. 4. The other operations of the present Embodiment Seven are similar to the operations of Embodiment One.

Specifically, in clock recovery circuit 130, the phase deviation PS computed by the computation means 13 was input directly to the cumulative summing circuit 15, but in the clock recovery circuit 136 of the present embodiment, the phase deviation PS output from the computation means 13 is input to the predetermined-value decision circuit 81, then

passes through the switching circuit 82 and is input to the cumulative summing circuit 15.

FIG. 12 is a flowchart showing the operation of the part inserted in the present Embodiment Seven between step S4 and step S5 in the operation of Embodiment One.

The predetermined-value decision circuit 81 decides whether or not the phase deviation PS output from the computation means 13 falls short of the predetermined value designated by the user (step S21), proceeds to step S22 if it falls short of the predetermined value (step S21: yes), and proceeds to step S23 if it does not fall short of the predetermined value (step S21: no).

If the phase deviation PS falls short of the predetermined value designated by the user, the switching circuit 82 does not output the phase deviation PS to the downstage cumulative summing circuit 15, but outputs phase deviation = 0 (step S22).

If the phase deviation PS does not fall short of the predetermined value designated by the user, the switching circuit 82 outputs the phase deviation PS to the downstage cumulative summing circuit 15, (step S23).

By setting the phase deviation to zero when the phase deviation PS output from the computation means 13 falls short of the predetermined value, as described above, the accumulation of Gaussian noise and computational errors as phase deviation PS in the cumulative summing circuit 15 can be eliminated, so unwanted noise components and the like can be removed from the phase deviation PS and the calculation accuracy of the phase deviation can be improved, whereby the clock signal lock-in speed and performance can be improved.

The present invention, being configured as described above, has such effects as those below.

The invented clock recovery circuit and method calculate the phase error of a symbol as a cumulative sum of

the phase deviations between predetermined components in the symbol, so

phase error due to either frequency error or phase error in the clock signal can be detected, improving the clock signal lock-in performance. The improved lock-in performance reduces inter-sub-carrier interference, and can improve the bit error rate characteristic of the recovered signal. Also, although the maximum value of the phase deviation between adjacent pilot signals that can be calculated at once is $+2\pi$, cumulative summation of these phase deviations within the same symbol can extend the phase error detection range to more than $+2\pi$.

In one aspect of the invention, the predetermined components include pilot signal components, so

the in-symbol phase deviation can be calculated with high accuracy, because there are many pilot signals per symbol, and the clock signal lock-in speed and performance can be improved.

In another aspect of the invention, the predetermined components include transmission and multiplexing configuration control (TMCC) signal components or auxiliary channel (AC) signal components, or both, so

the in-symbol phase deviation can be calculated with high accuracy, because there are also many TMCC and AC signal components per symbol, and the clock signal lock-in speed and performance can be improved.

In another aspect of the invention, the predetermined components include pilot signal components selected from among coherently modulated components, and TMCC and AC signal components selected from among differentially modulated components, so

the clock signal can be locked in by the use of either differentially modulated or coherently modulated parts of the received signal. Also, after the frequency arrangement

of each modulated part has been recognized, clock signal lock-in speed and performance can be improved by extracting either pilot signal components, or TMCC and AC signal components, whichever are more numerous. The improved lock-in speed leads to improvements in the bit error rate characteristic of the recovered signal quickly after reception begins.

In other aspects of the invention, the phase deviations are calculated by use of a tangent approximation, a sine approximation, or polarity values, so

the phase deviations can be calculated without use of a read-only memory (ROM) storing arctangent data.

In another aspect of the invention, phase deviations smaller than a predetermined value are set to zero, so

Gaussian noise and noise due to computation error can be removed from the phase error signal, improving the clock signal lock-in speed and performance.

CLAIMS:

1. A clock recovery circuit receiving a demodulated signal, detecting phase error from the demodulated signal, and controlling a clock oscillator according to said phase error, the demodulated signal having been obtained from a signal transmitted by orthogonal frequency division multiplexing, the demodulated signal being divided into consecutive symbols, each symbol having a plurality of components corresponding to different sub-carrier frequencies, comprising:

selection means selecting predetermined components from among the components of each said symbol of said demodulated signal;

memory means storing the predetermined components selected by said selection means;

computation means using the predetermined components stored in said memory means to compute phase deviations between different pairs of said predetermined components within each said symbol; and

cumulative summing means cumulatively summing said phase deviations over each said symbol, thereby obtaining said phase error.

2. The clock recovery circuit of claim 1, wherein said predetermined components include pilot signal components.

3. The clock recovery circuit of claim 1, wherein said predetermined components include transmission and multiplexing configuration control signal components.

4. The clock recovery circuit of claim 1, wherein said predetermined components include auxiliary channel signal components.

5. The clock recovery circuit of claim 1, further comprising signal decision means determining whether the components of each said symbol were coherently modulated or differentially modulated, causing said selection means to select pilot signal components as said predetermined components from among the components that were coherently modulated, and causing said selection means to select transmission and multiplexing configuration control signal components and auxiliary channel signal components as said predetermined components from among the components that were differentially modulated.

6. The clock recovery circuit of any one of claims 1 to 5, wherein said computation means uses a tangent approximation to compute said phase deviations.

7. The clock recovery circuit of any one of claims 1 to 5, wherein said computation means uses a sine approximation to compute said phase deviations.

8. The clock recovery circuit of any one of claims 1 to 5, wherein said computation means outputs polarity values as said phase deviations.

9. The clock recovery circuit of any one of claims 1 to 5, further comprising decision means comparing said phase deviations with a predetermined value, and changing those phase deviations less than said predetermined value to zero.

10. A method of recovering a clock signal from a demodulated signal by detecting phase error from the demodulated signal and controlling a clock oscillator according to said phase error, the demodulated signal having

been obtained from a signal transmitted by orthogonal frequency division multiplexing, the demodulated signal being divided into consecutive symbols, each symbol having a plurality of components corresponding to different sub-carrier frequencies, comprising the steps of:

selecting predetermined components from among the components of each said symbol of said demodulated signal;

storing said predetermined components in a memory;

using the predetermined components stored in said memory to compute phase deviations between different pairs of said predetermined components within each said symbol; and

cumulatively summing said phase deviations over each said symbol, thereby obtaining said phase error.

11. A circuit substantially as hereinbefore described as an embodiment and as shown in the respective accompanying drawings.

12. A receiver comprising a circuit as claimed in any preceding claim.

13. A method of recovering a clock signal substantially as hereinbefore described in an embodiment with reference to the respective accompanying drawings.

INVESTOR IN PEOPLE

Application No: GB 0100500.8 **Examiner:** Owen Wheeler
Claims searched: 1-13 **Date of search:** 18 October 2001

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.S): H4P (PAFX, PAL, PDRX, PJ)

Int Cl (Ed.7): H04L

Other: Online: EPODOC, JAPIO, WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	GB 2278257 A	[BBC]	
A	EP 0961448 A2	[MATSUSHITA] See figures 6 and 8.	
A,&	EP 0930751 A1	[VICTOR] See paragraphs 64-82, claim 1 and figures 5 and 6.	
A	WO 96/19056 A1	[HD DIVINE]	
A	JP 10 308715 A	[SONY]	
A,&	JP 10 135924 A	[VICTOR] Equivalent to EP 0930751.	

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