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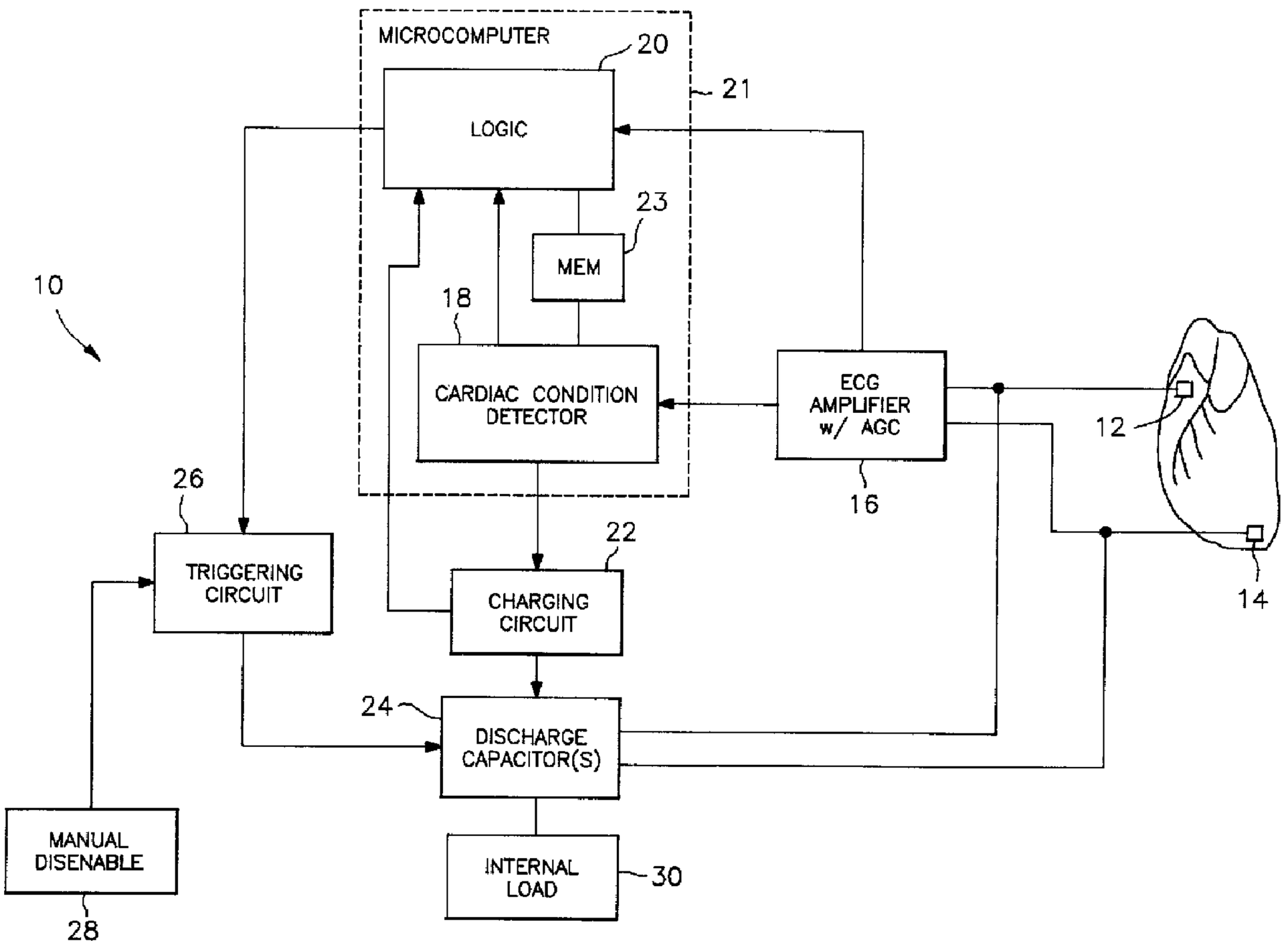
(54) Titre : SYSTEME DE DEFIBRILLATION ET DE CARDIOVERSION AVEC PERIODE D'INACTIVITE
(54) Title: NON-COMMITTED DEFIBRILLATION/CARDIOVERSION SYSTEM



(57) Abrégé/Abstract:
An automatic implantable defibrillator/cardioverter having a non-committed defibrillation/cardioversion algorithm. The defibrillator/cardioverter includes an ECG amplifier with automatic gain control (AGC) which detects the electrical activity of the

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(13) C

(57) Abrégé(suite)/Abstract(continued):
heart for analysis by a cardiac condition detector. Logic is provided which receives input from the ECG amplifier and the cardiac condition detector for analyzing the heart activity. The non-committed defibrillation algorithm sensing begins upon the determination of an arrhythmia. The capacitor is charged while the heart activity is simultaneously monitored. After the capacitor is charged, a check is made on the duration of the last detected R-R interval while so charging the capacitor, and a comparison is made between this R-R interval and a preset value. If the last R-R interval is greater than the preset value, a non-committing period is entered which lasts approximately 2 seconds. The purpose of the non-committing period is to allow detection to monitor the arrhythmia further before making the decision to discharge the capacitor or dump the charge internally. If any R-R interval detected during this interval is less than PCLL, this indicates that the arrhythmia has not reverted and the capacitor charge is delivered to the patients, synchronously with the second R-wave of the fast R-R interval. If no rapid interval is detected during this time, a post intervention (PI) monitoring routine is entered at the end of the non-committing period to further monitor cardiac activity and shock if necessary.

ABSTRACT OF THE DISCLOSURE

An automatic implantable defibrillator/cardioverter having a non-committed defibrillation/cardioversion algorithm. The defibrillator/cardioverter includes an ECG amplifier with automatic gain control (AGC) which detects the electrical activity of the heart for analysis by a cardiac condition detector. Logic is provided which receives input from the ECG amplifier and the cardiac condition detector for analyzing the heart activity. The non-committed defibrillation algorithm sensing begins upon the determination of an arrhythmia. The capacitor is charged while the heart activity is simultaneously monitored. After the capacitor is charged, a check is made on the duration of the last detected R-R interval while so charging the capacitor, and a comparison is made between this R-R interval and a preset value. If the last R-R interval is greater than the preset value, a non-committing period is entered which lasts approximately 2 seconds. The purpose of the non-committing period is to allow detection to monitor the arrhythmia further before making the decision to discharge the capacitor or dump the charge internally. If any R-R interval detected during this interval is less than PCLL, this indicates that the arrhythmia has not reverted and the capacitor charge is delivered to the patients, synchronously with the second R-wave of the fast R-R interval. If no rapid interval is detected during this time, a post intervention (PI) monitoring routine is entered at the end of the non-committing period to further monitor cardiac activity and shock if necessary.

NON-COMMITTED DEFIBRILLATION/CARDIOVERSION SYSTEM

Background of the Invention

The present invention relates to an implantable automatic defibrillator and more particularly to a feature in an implantable automatic defibrillator for diverting the charge on a defibrillator capacitor to an internal load.

In implantable cardiac treatment devices, such as an implantable defibrillator, a cardiac arrhythmia is detected based on sensed electrical and other activity of the heart. In defibrillation, the determination of a tachycardia, or fast beating heart, is indicative of impending ventricular fibrillation. Upon the determination of such an arrhythmia, a defibrillation capacitor is charged to a selected level for ultimately discharging and delivering an electrical shock to the heart.

Oftentimes, the arrhythmia of the heart is temporary and does not further develop into fibrillation, but reverts to normal sinus rhythm. This can occur while the defibrillation capacitor is charging or shortly after the capacitor has been charged. If the capacitor is discharged to a heart in normal sinus rhythm, the result could be detrimental, and at the worst put the heart into an arrhythmia. In addition, a high energy defibrillation shock normally causes some trauma to the patient; thus an unnecessary shock is to be avoided.

To avoid delivering an unnecessary defibrillation shock, it would be advantageous to delay the discharge of the defibrillation capacitor after it has been fully charged to allow

further monitoring if there is an indication that the arrhythmia has reverted to normal sinus rhythm during the charging process.

Some defibrillation devices incorporate delays for manually disenabling the capacitor discharge. See for example U.S. Patents to Bradley et al. (4,576,170) and Heilman et al. (4,210,149). These devices have built-in delays to allow the wearer to disenable the implantable device to prevent the delivery of a shock after the patient is audibly warned of an impending shock. The purpose of these devices is to allow the patient to override the implantable device in the event that a false detection occurs.

These devices fail in that a truly accurate examination of the heart activity is not made when disenabling the device. Therefore, it is possible to ignore a malignant heart condition.

Summary of the Invention

It is a primary object of an aspect of the present invention to provide a non-committed defibrillation/cardioversion system and algorithm in an implantable defibrillator whereby the heart activity is monitored during and after the charging of a defibrillation capacitor to further evaluate the heart condition before discharging the defibrillation capacitor.

According to one aspect of the present invention there is provided a system for defibrillating/cardioverting the heart comprising:

means for sensing the electrical activity of the heart including the interval between successive R-waves of the ECG;

means for detecting an arrhythmia of the heart;

means for storing the interval between successive R-waves;

defibrillation capacitor means;

means for charging said defibrillation capacitor means to a predetermined voltage level upon detecting an arrhythmia of the heart using said means for detecting;

means for triggering the discharge of said defibrillation capacitor means; and

logic means including means for providing a first delay of a first predetermined period of time subsequent to said capacitor being charged to said predetermined level means for providing a second delay of a second predetermined period of time subsequent to said first delay, means for comparing the stored interval between successive R-waves detected during charging of the defibrillation capacitor means with a preset value during said first delay; means for entering said second delay of said second predetermined period of time if said stored interval between successive R-waves is greater than said preset value, and means for discharging said defibrillation capacitor to the heart if any interval between successive R-waves is less than said preset value during said second delay.

Preferably, the logic means further comprises means for determining a variable time interval between the last R-wave detected while charging the defibrillation capacitor means and the end of the first delay of the first predetermined period of time if the stored interval of successive R-waves is not greater than the preset value during the first delay. The logic means compares the variable time interval with a preset time interval to enter the second delay if the variable time interval exceeds the preset time interval.

It is also preferred that the system further comprises an internal load and wherein the logic means further comprises means for determining if a detected arrhythmia has reverted if no R-R interval detected during the second delay is less than the preset value or after discharge of the defibrillation capacitor means if an R-R interval is less than the preset value. The logic means

operates the means for triggering to divert the predetermined voltage level of the defibrillation capacitor to the internal load if the arrhythmia has reverted. The logic means further provides a synchronization time window of a third predetermined period of time if a detected arrhythmia has not reverted. The means for sensing detects an R-wave during the third predetermined period of time and the logic means operates the means for triggering to effect discharge of the defibrillation capacitor at the occurrence of a detected R-wave during the synchronization time window or effecting discharge of the defibrillation capacitor at the end of the synchronization time window if no R-wave is detected during the third predetermined period of time.

In a preferred embodiment, the logic means further comprises means for triggering the means for charging to charge the defibrillation capacitor means to an appropriate voltage level if a detected arrhythmia has not reverted after the second delay and charge on the defibrillation capacitor means has leaked to below the predetermined voltage window.

Preferably, the system further comprises memory means for programming the logic means wherein the first predetermined period of time is 200 milliseconds and the second predetermined period of time is 2 seconds.

The abort algorithm of the present invention can be used in cardioverting a high rate tachycardia (often known as a malignant tachyarrhythmia) with a relatively low energy and synchronized shock, as well as ventricular fibrillation with a relatively high energy synchronous or asynchronous shock.

The above and other objects and advantages of the present invention will become more apparent when reference is made to the following description taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

Figure 1 is a schematic block diagram illustrating the various components of the non-committed defibrillation system of the present invention.

Figures 2 and 3 are flow charts illustrating the procedural steps for implementing the abort algorithm of the present invention.

Figure 4 is an illustration of the particular time intervals of the abort algorithm related to the charging and discharging of a defibrillation capacitor.

Detailed Description of the Drawings

Referring first to Figure 1, the various components of the present invention will be described. The non-committed defibrillation system, generally showed at 10, includes sensing/discharging electrodes 12 and 14 mounted on or about the heart which are connected to ECG sense amplifier 16. The ECG amplifier 16 may contain one or more sense channels, but also includes automatic gain control (AGC).

The ECG amplifier 16 is connected to a cardiac condition detector 18 and to logic 20 for analyzing the heart activity detected by the ECG amplifier 16. Logic 20 can be embodied as software, firmware, or in the form of conventional logic gates and circuits. A detailed description of a flow diagram of logic 20 is set forth hereinafter. The cardiac condition detector 18 includes the ability to measure time intervals between successive R-waves as well as other functions well known in the art for diagnosing the function of the heart.

The logic 20 and cardiac condition detector 18 may be incorporated as one unit, such as for example, in a microcomputer

21 as shown, but regardless, include means for performing rate detection such as determining the R-R interval, probability density function (PDF) detection, and other arrhythmia monitoring schemes which are known in the art, and which are not part of the essence of the present invention. In addition, a memory 23 is also provided in the microcomputer 21, as is well known in the art, for storing cardiac condition information such as R-R wave intervals and programmable data.

A charging circuit 22 is provided for charging the discharge capacitor 24. The charging circuit is connected to logic 20 for communicating therewith. Also connected to logic 20 is a triggering circuit 26 for controlling the discharge of the capacitor 24. In addition, a manual disenable 28 is provided for causing the triggering circuit 26 to prevent the capacitor 24 from discharging to the electrodes 12 and 14. The triggering circuit 26 triggers the capacitor 24 to discharge through the electrodes 12 and 14 or through an internal load 30.

Referring now to Figures 2 - 4, together with Figure 1, the abort algorithm will now be described. Figures 2 and 3 illustrate the logic flow pattern embodied by logic 20 of the system illustrated in Figure 1. The ECG sense amplifier 16 senses the electrical activity of the heart via electrodes 12 and 14. This information is analyzed by the cardiac condition detector 18. The abort algorithm is entered once an initial determination is made that the heart is in an arrhythmia. If it is determined that a tachycardia or other arrhythmia is present at step 32 by some

other means or mechanism not considered part of the present invention, the capacitor 24 is charged to a selected level at step 34 to ultimately defibrillate the heart. Also, while the capacitor 24 is being charged in step 34, the electrical activity f the heart is continuously sensed by the ECG amplifier 16 to monitor the R-waves. Once the capacitor 24 is fully charged, a first delay of 200 msec is initiated at step 36.

The first delay is programmable but preferably lasts approximately 200 msec. During this time, the ECG sense amplifier 16 is allowed to settle to facilitate discharge of the capacitor to be synchronized with a R-wave if necessary. Also, this time window permits block out any effect that the charging circuit 22 may have on the automatic gain control circuitry in the ECG sense amplifier 16. In addition, a manual dump at step 38 can be accomplished by the manual disenable 28 during this time window should it be determined by a physician, for example, that it is not desirable to deliver the shock. If this latter step is chosen, the dump is made at step 40 to the internal load 30.

Otherwise, the preliminary steps 41A-41C are entered. Step 41A illustrates the selective nature of the abort algorithm. The physician/technician can program the device to employ or not to employ the abort algorithm. When not activated, only committed shocks would be delivered. In step 41B, it is determined whether a maximum number of aborts has already been effected during the current state of operation of the algorithm. In addition, as shown in step 41C, there is preferably a maximum number of times that the algorithm can enter the non-committing period (referred to hereinafter). While

this parameter can be reset by a physician/technician, it is normally fixed for the period of time between physician check-ups. In effect, the algorithm will permit only so many delays (and capacitor diversions) before going fully committed. Therefore, patients with spaced short-run ventricular tachyarrhythmias will not cause the device to waste battery charge due to repeated charge and subsequent internal discharge of the capacitor. As indicated in Figure 2, once this maximum value is met, the device will deliver committed shocks. The microcomputer 21 keeps track of the various parameters specified in steps 41A-41C.

If the abort algorithm is turned on and none of the maximums specified in steps 41B and 41C are met, the decision step 42 is entered for making a comparison of the most recent R-R interval, detected while charging the capacitors in step 34 (stored in memory 23), with a tachycardia primary rate cycle length limit (PCLL). One of two branches is taken depending on the result at step 42.

If this R-R interval is greater than PCLL, a second delay is initiated at step 44. This second delay is programmable and can last up to, but no more than 2 seconds. The purpose of this delay is to allow further monitoring of the heart activity before a decision to discharge or dump the capacitor 24 is made. This delay period is termed a non-committing period during which discharge of the capacitor 24 is not triggered unless a certain cardiac condition is detected. At this point, the indication after the first delay is that the arrhythmia might revert spontaneously. R-wave activity is constantly monitored by the cardiac condition detector 18 during the non-committing period.

During the non-committing period, if any R-R interval detected is less than PCLL, at step 46, discharge of the defibrillation capacitor 24 is immediately effected in step 48 on the second R-wave of the first fast interval detected. If, on the other hand, the result in step 46 is negative, the post intervention (PI) routine 50 shown in Figure 3 is entered at the end of the non-committing period via a first track indicated in step 49A. The charge on the capacitor 24 is allowed to remain at this time. Also, after the shock delivered in step 48, the PI routine is entered via a second track indicated in step 49B.

Referring now to Figure 3, in the PI routine, the electrical activity of the heart is continuously monitored at step 52 for a certain present period of time or certain present number of cardiac cycles. After the time-out or count-out in step 52, based on the continuously monitored cardiac activity, a determination is made at step 53 to determine if the arrhythmia has reverted. The details of steps 52 and 53 may involve many types of cardiac analysis not considered a part of the present invention. If the arrhythmia has reverted, it is determined in step 54A whether the PI routine was entered via track 1 (step 49A) or track 2 (step 49B). If the answer to the inquiry in step 54A is

affirmative, then the triggering circuit 26 triggers the discharge of capacitor 24 through the internal load 30 at step 54B.

If it is detected in step 53 that the arrhythmia has not reverted, then it is determined in step 55A whether the PI routine was entered via track 1 (step 49A) or track 2 (step 49B). An affirmative response in step 55A will cause the algorithm to continue from step 56. A negative response in step 55A will follow to step 55B in which it is determined if a programmable maximum number of shocks has been exceeded for a single arrhythmia episode. If this maximum is met, the algorithm enters a "wait" state as shown at step 55C during which time the algorithm can be reset by a physician/technician or by spontaneous reversion to normal heart rhythm. During the "wait" state, if the heart rate remains below the value of PCLL, the algorithm is reset. Thereafter, any new arrhythmia is considered a new arrhythmic episode whereas if the current arrhythmic state does not revert, the "wait state is continued but the heart rate is monitored and if the rate decreases to below PCLL, the algorithm resets. Otherwise, the capacitor is again charged in step 34.

Should it be found in step 55A that the PI routine was entered via track 1, the charging circuit 22 is activated to ensure that the capacitor 24 is fully charged to the selected or appropriate level by effectively "topping off" the charge on the capacitor 24 at step 56. This step is sometimes necessary if the capacitor charge has leaked subsequent its initial charging or a higher energy shock is necessary if the arrhythmia has accelerated

as determined in step 52. Thereafter, an optional 200 msec delay is entered at step 58 to allow for internal manual dump much like that shown at steps 38 and 40 in Figure 2. If no internal dump is made, a synchronization window is entered at steps 60, 62 and 64. In the synchronization window, a shock is delivered synchronized to an R-wave if one is detected. The term synchronized is intended to mean simultaneous with an R-wave or a programmed period of time after an R-wave.

If after the first delay in step 42, it is determined that the most recent R-R interval detected while charging the capacitor 24 in step 34 is less than or equal to PCLL, the branch on the left side of Figure 2 is taken to step 43. In step 43, a check is made on the time interval from the most recent R-wave (PTOC) detected while charging the capacitor 24 in step 34 to the end of the 200 msec first delay interval. The purpose of this comparison is that any occurrence of an R-wave during the first delay, whether or not detected, is considered to be fast provided the interval is less than PCLL even if it occurs at the end of the first delay. Consequently, if this interval is less than or equal to the PCLL, there is no indication that the heart rhythm is still not abnormally fast, and the algorithm goes to step 60 in Figure 3, and shocks the heart synchronously if possible and otherwise asynchronously. Otherwise, the non-committing period at step 44 is entered and the steps there are executed as previously described.

The abort algorithm of the present invention allows a precise determination of whether a detected arrhythmia has subsequently reverted before delivering a discharge to the patient. Therefore, unnecessary electrical shocks are avoided, preventing trauma. Several modifications of the algorithm as described above can be made. First, parameters such as PCLL, the first delay, the duration of the non-committing period and the duration of the synchronization window may be programmable or may vary dynamically with changes in cardiac activity. In this regard, the terms preset or predetermined are meant to include variable such as dynamically changing. Furthermore, conditions such as the comparison in step 46, may be modified so as to require several (a predetermined or variable number) of fast R-R intervals. Accordingly, other tests or analysis of the cardiac activity can be made during the non-committing period to trigger or inhibit discharge of the defibrillation capacitors to the heart. In this regard, physiological indicators of cardiac arrhythmias such as, blood pressure or oxygenation, can be employed in the algorithm in addition to or in substitution for heart rate. It is also possible to operate the algorithm without the first delay period of step 36. In this case, the algorithm would be implemented without step 43 so that a positive response in step 43 would follow directly to step 60.

The above description is intended by way of example only and is not intended to limit the present invention in any way except as set forth in the following claims.

What is claimed is:

1. A system for defibrillating/cardioverting the heart comprising:

means for sensing the electrical activity of the heart including the interval between successive R-waves of the ECG;

means for detecting an arrhythmia of the heart;

means for storing the interval between successive R-waves;

defibrillation capacitor means;

means for charging said defibrillation capacitor means to a predetermined voltage level upon detecting an arrhythmia of the heart using said means for detecting;

means for triggering the discharge of said defibrillation capacitor means; and

logic means including means for providing a first delay of a first predetermined period of time subsequent to said capacitor being charged to said predetermined level means for providing a second delay of a second predetermined period of time subsequent to said first delay, means for comparing the stored interval between successive R-waves detected during charging of the defibrillation capacitor means with a preset value during said first delay; means for entering said second delay of said second predetermined period of time if said stored interval between successive R-waves is greater than said preset value, and means for discharging said defibrillation capacitor to the heart if any interval between successive R-waves is less than said preset value during said second delay.

2. The system of claim 1, wherein said logic means further comprises means for determining a variable time interval between the last R-wave detected while charging the defibrillation capacitor means and the end of said first delay of said first predetermined period of time if said stored interval of successive R-waves is not greater than said preset value during said first delay, and compares said variable time interval with a preset time interval to enter said second delay if said variable time interval exceeds said preset time interval.

3. The system of claim 2, and further comprising an internal load, and wherein said logic means further comprises means for determining if a detected arrhythmia has reverted if no R-R interval detected during the second delay is less than said preset value or after discharge of the defibrillation capacitor means if an R-R interval is less than said preset value, and operates the means for triggering to divert said predetermined voltage level of said defibrillation capacitor to said internal load if the arrhythmia has reverted, the logic means further providing a synchronization time window of a third predetermined period of time if a detected arrhythmia has not reverted, said means for sensing detecting an R-wave during said third predetermined period of time and said logic means operating the means for triggering to effect discharge of said defibrillation capacitor at the occurrence of a detected R-wave during said synchronization time window or effecting discharge of said defibrillation capacitor at the end of said synchronization time window if no R-wave is detected during said third predetermined period of time.

4. The system of claim 3, wherein said logic means further comprises means for triggering said means for charging to charge said defibrillation capacitor means to an appropriate voltage level if a detected arrhythmia has not reverted after said second delay and charge on the defibrillation capacitor means has leaked to below the predetermined voltage level.

5. The system of claim 3 and further comprising memory means for programming said logic means wherein said first predetermined period of time is 200 milliseconds and said second predetermined period of time is 2 seconds.

6. The system of claim 3, wherein said third predetermined period of time is 2 seconds.

FIG. 1

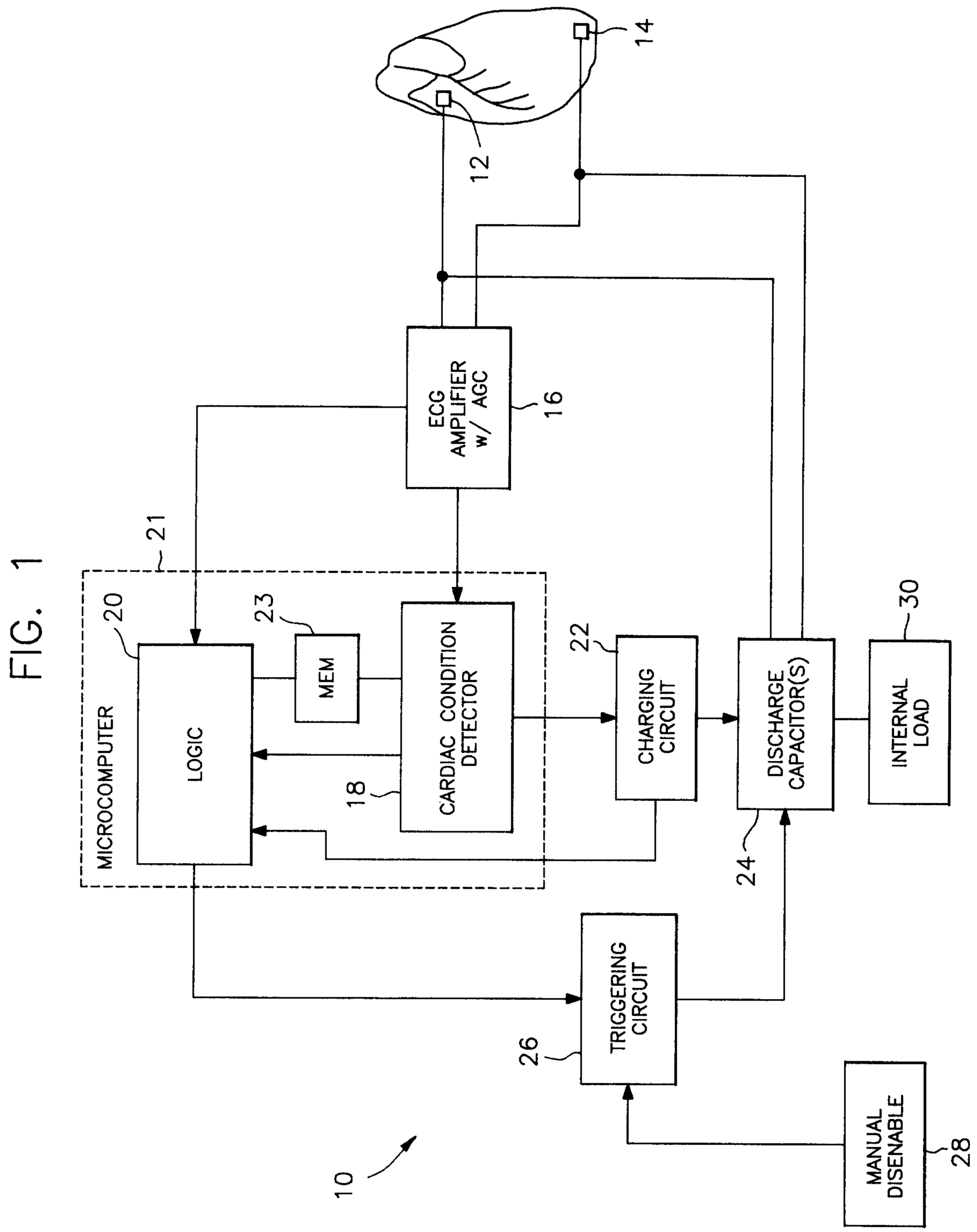

14
12
ECG AMPLIFIER w/ AGC
16
21
MICROCOMPUTER
20
LOGIC
23
MEM
CARDIAC CONDITION DETECTOR
18
22
CHARGING CIRCUIT
DISCHARGE CAPACITOR(S)
24
INTERNAL LOAD
30
TRIGGERING CIRCUIT
26
MANUAL DISENABLE
28
10

FIG. 2

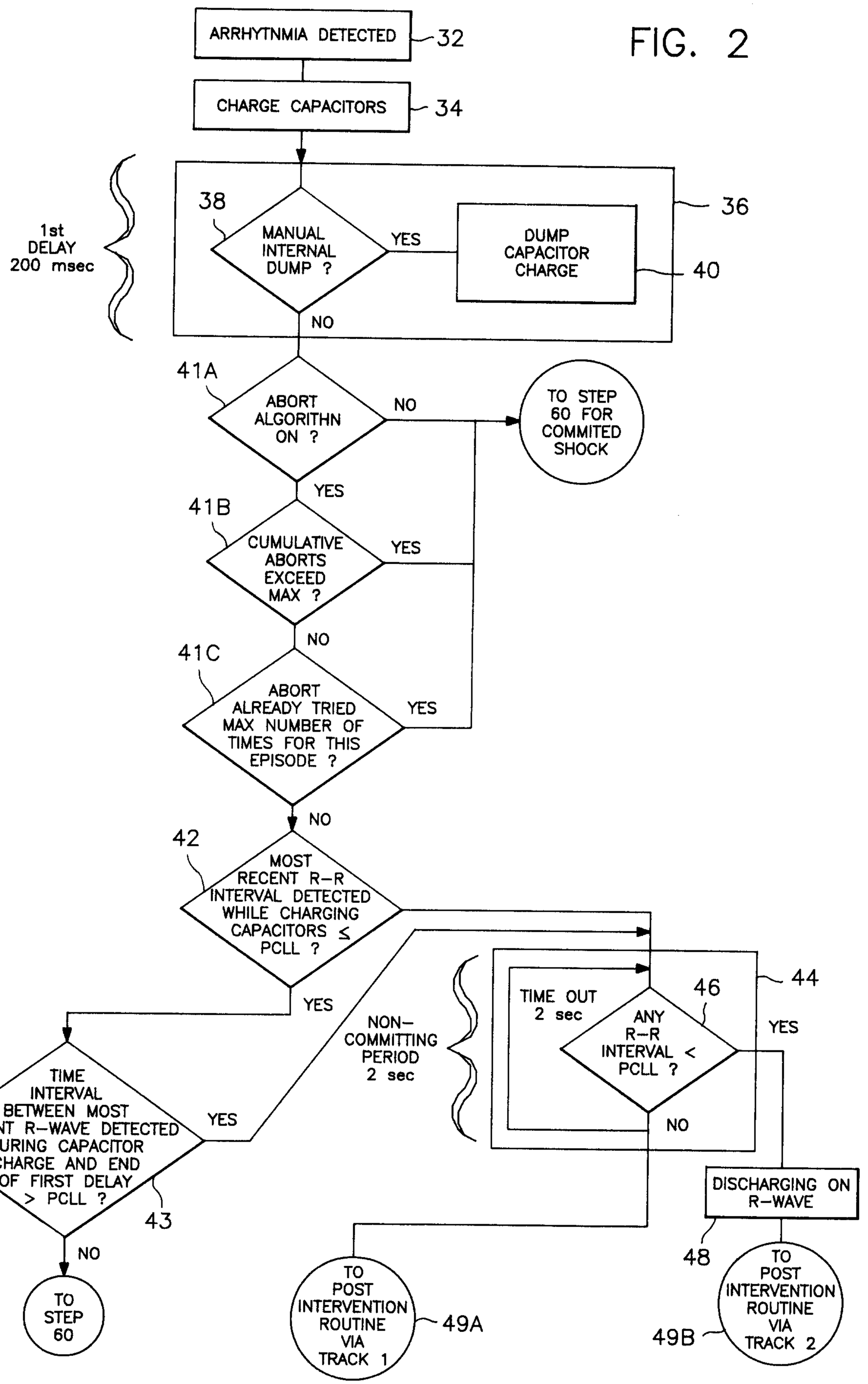

ARRHYTNMIA DETECTED
32
CHARGE CAPACITORS
34
1st DELAY 200 msec
38
MANUAL INTERNAL DUMP ?
YES
DUMP CAPACITOR CHARGE
40
36
NO
41A
ABORT ALGORITHN ON ?
NO
TO STEP 60 FOR COMMITED SHOCK
YES
41B
CUMULATIVE ABORTS EXCEED MAX ?
YES
NO
41C
ABORT ALREADY TRIED MAX NUMBER OF TIMES FOR THIS EPISODE ?
YES
NO
42
MOST RECENT R-R INTERVAL DETECTED WHILE CHARGING CAPACITORS ≤ PCLL ?
YES
NO
TIME INTERVAL BETWEEN MOST RECENT R-WAVE DETECTED DURING CAPACITOR CHARGE AND END OF FIRST DELAY > PCLL ?
YES
NO
43
TO STEP 60
NON-COMMITTING PERIOD 2 sec
TIME OUT 2 sec
46
ANY R-R INTERVAL < PCLL ?
YES
NO
44
DISCHARGING ON R-WAVE
48
TO POST INTERVENTION ROUTINE VIA TRACK 2
49B
TO POST INTERVENTION ROUTINE VIA TRACK 1
49A

FIG. 3

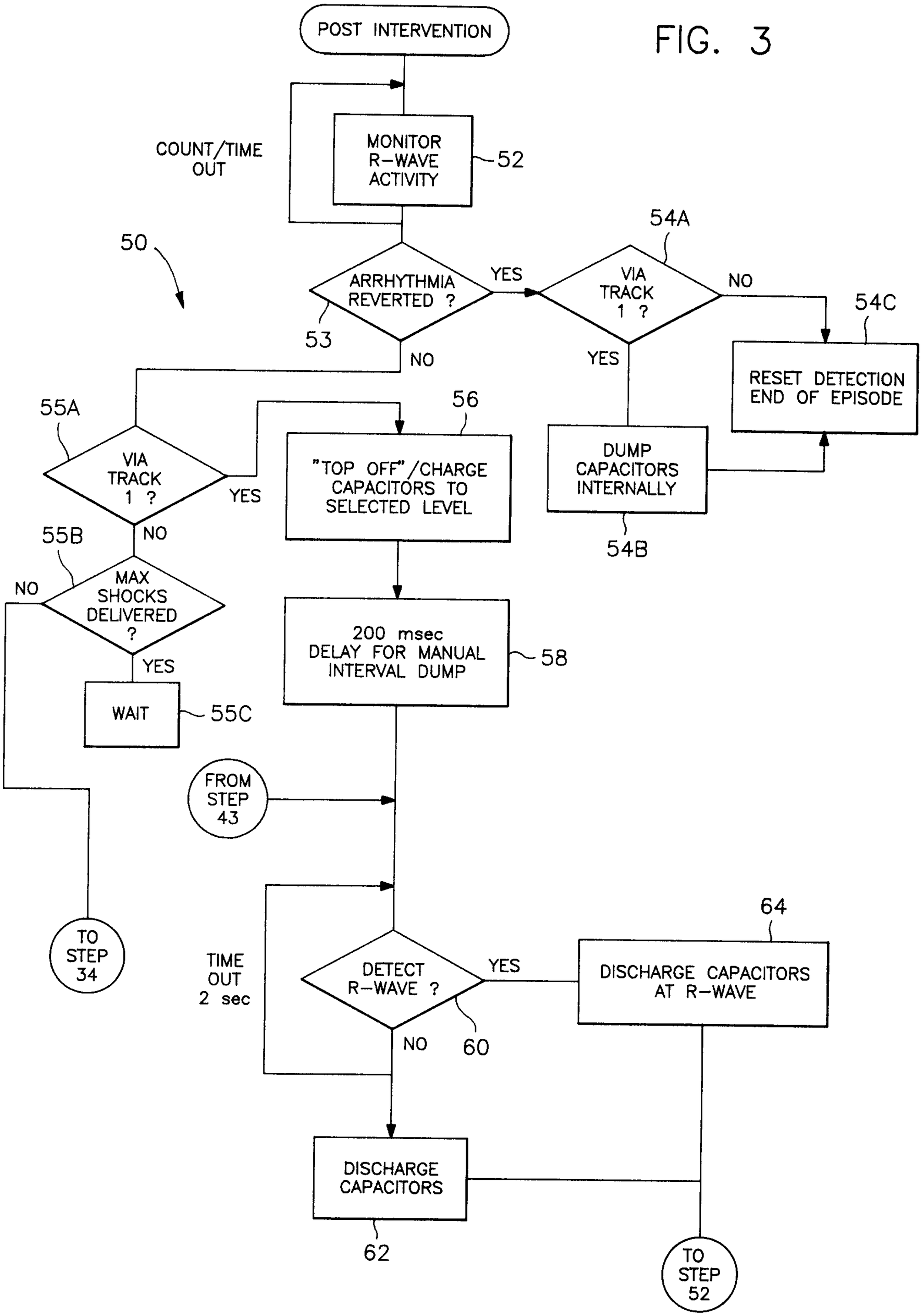
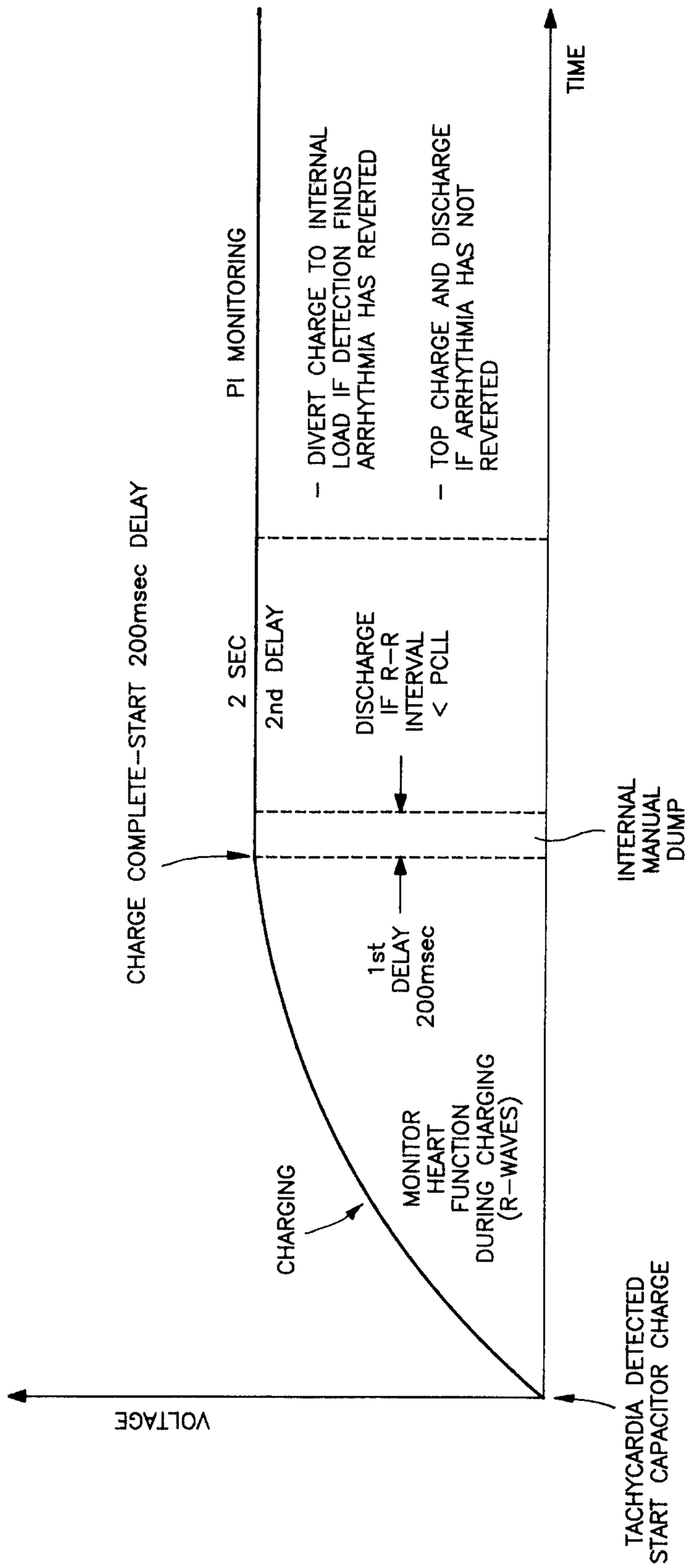
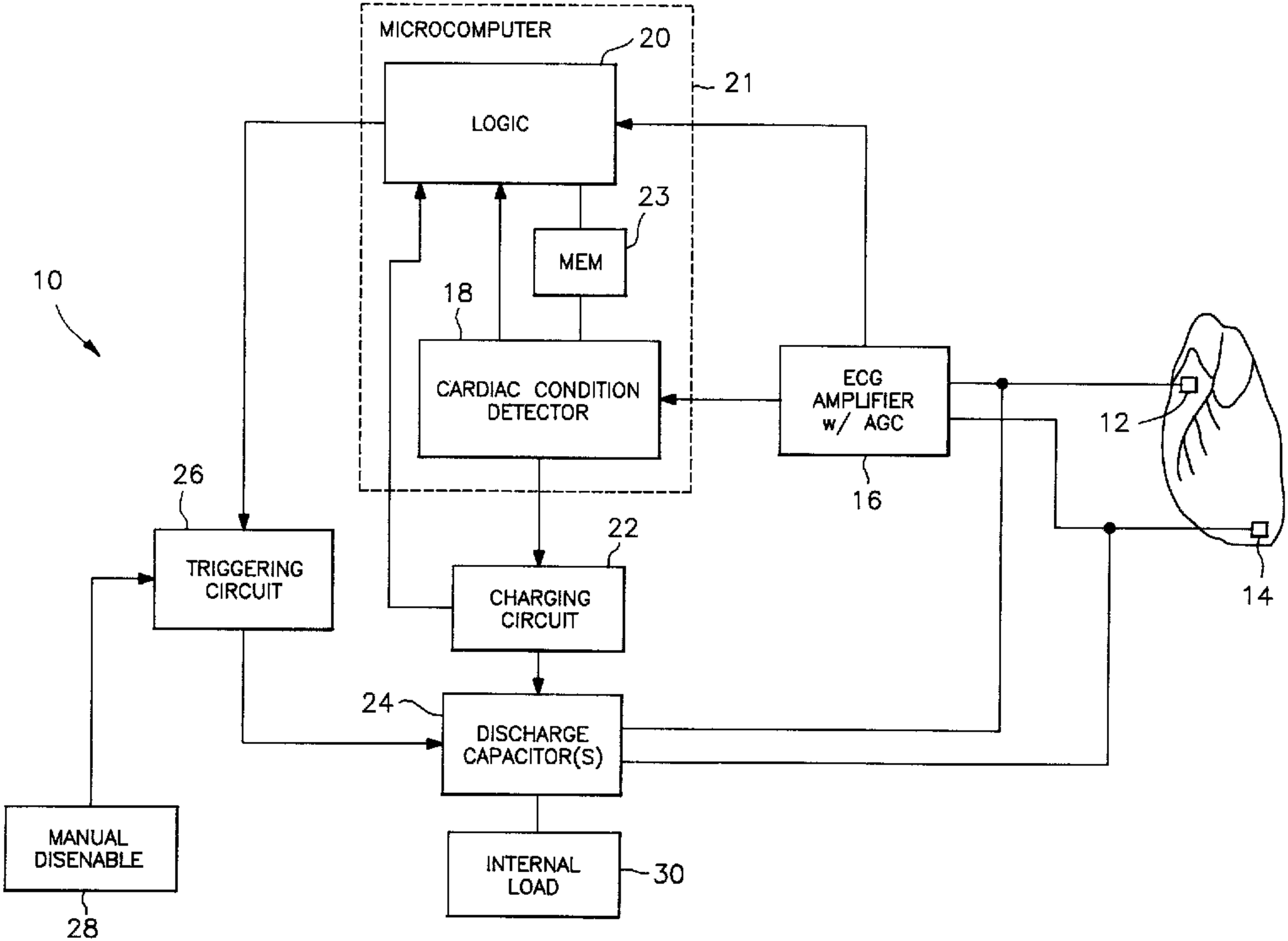

POST INTERVENTION
MONITOR R-WAVE ACTIVITY
52
COUNT/TIME OUT
50
ARRHYTHMIA REVERTED ?
53
YES
VIA TRACK 1 ?
54A
NO
RESET DETECTION END OF EPISODE
54C
NO
YES
DUMP CAPACITORS INTERNALLY
54B
55A
VIA TRACK 1 ?
YES
56
"TOP OFF"/CHARGE CAPACITORS TO SELECTED LEVEL
NO
55B
MAX SHOCKS DELIVERED ?
NO
YES
WAIT
55C
200 msec DELAY FOR MANUAL INTERVAL DUMP
58
FROM STEP 43
TO STEP 34
TIME OUT 2 sec
DETECT R-WAVE ?
YES
64
DISCHARGE CAPACITORS AT R-WAVE
NO
60
DISCHARGE CAPACITORS
62
TO STEP 52

FIG. 4


TIME
VOLTAGE
TACHYCARDIA DETECTED
START CAPACITOR CHARGE
CHARGING
CHARGE COMPLETE–START 200msec DELAY
MONITOR HEART FUNCTION DURING CHARGING (R–WAVES)
1st DELAY 200msec
INTERNAL MANUAL DUMP
2 SEC
2nd DELAY
DISCHARGE IF R–R INTERVAL < PCLL
PI MONITORING
– DIVERT CHARGE TO INTERNAL LOAD IF DETECTION FINDS ARRHYTHMIA HAS REVERTED
– TOP CHARGE AND DISCHARGE IF ARRHYTHMIA HAS NOT REVERTED


MICROCOMPUTER
20
21
LOGIC
23
MEM
18
CARDIAC CONDITION DETECTOR
ECG AMPLIFIER w/ AGC
16
12
14
10
26
TRIGGERING CIRCUIT
22
CHARGING CIRCUIT
24
DISCHARGE CAPACITOR(S)
MANUAL DISENABLE
28
INTERNAL LOAD
30