



(43) International Publication Date
18 September 2014 (18.09.2014)

- (51) International Patent Classification:
H01L 21/306 (2006.01)
- (21) International Application Number:
PCT/US2013/031441
- (22) International Filing Date:
14 March 2013 (14.03.2013)
- (25) Filing Language: English
- (26) Publication Language: English
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- (81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— with international search report (Art. 21(3))

(54) Title: DEFECT FREE SINGLE CRYSTAL THIN LAYER

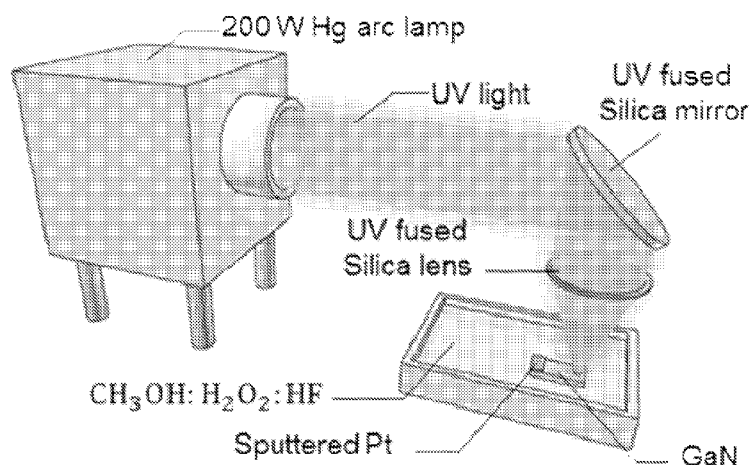


FIG. 2

(57) Abstract: A gallium nitride film can be a dislocation free single crystal, which can be prepared by irradiating a surface of a substrate and contacting the surface with an etching solution that can selectively etch at dislocations.



DEFECT FREE SINGLE CRYSTAL THIN LAYER

TECHNICAL FIELD

The invention features a single crystal thin layer and methods of making.

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BACKGROUND

Gallium nitride is a compound having a Wurtzite crystal structure and wide band gap of 3.4 eV. It has important applications in many fields, such as optoelectronics, high-power and high-frequency electronic devices, solid state devices, ultra high efficiency photovoltaic devices, and so on. The absence of free-standing seeding/substrate gallium nitride layer represents a significant challenge in the gallium nitride technology.

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SUMMARY

In general, a III-V semiconductor film, such as a gallium nitride film, can be dislocation free single crystalline. The III-V semiconductor film, such as a gallium nitride film, can have a thickness of between 10 nanometers to 1 micron, for example, between 10 nanometers and 200 nanometers or between 20 and 50 nanometers, and can be prepared by a combination of surface irradiation and chemical etching.

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In one aspect, a method for preparing III-V semiconductor film can include irradiating a surface of a substrate including the III-V semiconductor, and contacting the surface of the substrate while irradiating with a solution containing an etching solution to form the film on the substrate.

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In some embodiments, the III-V semiconductor can be selected from indium arsenide, indium phosphide, gallium arsenide, gallium phosphide, gallium antimonide, aluminum nitride, indium antimonide, aluminum arsenide, aluminum phosphide, aluminum antimonide, indium gallium arsenide, gallium arsenide phosphide, indium arsenide phosphide, indium gallium arsenide phosphide, indium aluminum gallium arsenide, indium gallium nitride, and aluminum gallium nitride. In some embodiments, the III-V semiconductor can be gallium nitride.

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In some embodiments, the substrate can include a silicon doped, n-doped, undoped (or un-intentionally doped), or p-doped gallium nitride on sapphire. In some embodiments, the substrate can include bulk gallium nitride. In some embodiments, the substrate can include gallium nitride on silicon carbide. In some embodiments, the

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substrate can include gallium nitride on silicon. Other kinds of substrate containing gallium nitride can also be used.

In some embodiments, the etching solution can include hydrogen fluoride and hydrogen peroxide. In some embodiments, the etching solution can include potassium
5 hydroxide. In some embodiments, the surface of the substrate can include a plurality of dislocations. In some embodiments, the etching solution can etch selectively at the dislocations.

In some embodiments, the surface of the substrate can be irradiated by an irradiation source, wherein the irradiation source can have an energy greater than the
10 bandgap of the III-V semiconductor or a wavelength below the bandgap of the semiconductor materials.

In some embodiments, the surface of the substrate can be irradiated by an ultraviolet light source, wherein the energy of the ultraviolet light source is greater than the bandgap of the III-V semiconductor. In some embodiments, the surface of the
15 substrate can be irradiated by an X-ray. In some embodiments, the surface of the substrate can be irradiated by a gamma ray.

Both the length of the irradiation and the density of the irradiation source on the surface of the substrate affect the etching process. In some embodiments, the method can include controlling the intensity of the irradiation source. In some embodiments, a
20 portion of the surface of the substrate can be coated with an electrode. In some embodiments, the material of the electrode can be selected from titanium, platinum, silver, and gold. In some embodiments, the method can include applying an electric field at the surface of the substrate. In some embodiments, the method can include drying the substrate.

25 In some embodiments, the thickness of the III-V semiconductor film can be between 10 nanometers to 1 micron, for example, between 10 nanometers and 200 nanometers or between 20 and 50 nanometers.

In some embodiments, the method can include transferring the III-V semiconductor film to a second substrate.

30 In another aspect, a film can include dislocation free single crystalline III-V semiconductor, wherein the dislocation free single crystalline III-V semiconductor can have a thickness of between 10 nanometers and 1 micron nanometers, for example, between 10 nanometers and 200 nanometers or between 20 and 50 nanometers.

In some embodiments, the film can include a plurality of pores. In some embodiments, the III-V semiconductor can be gallium nitride. In some embodiments, a plurality of gallium nitride wires can protrude through the dislocation free single crystalline gallium nitride. In some embodiments, the film can include a porous gallium nitride layer underneath the dislocation free single crystalline gallium nitride.

In another aspect, a structure can include dislocation free single crystalline III-V semiconductor on a substrate, wherein the substrate can be a polymer substrate, copper substrate, silicon substrate, glass substrate, silicon carbide substrate, sapphire substrate, quartz substrate, porcelain substrate, indium phosphide substrate, gallium nitride substrate, gallium arsenide substrate, beryllium oxide substrate, aluminum nitride substrate, alumina substrate, plastic substrate, or ceramic substrate.

In another aspect, a device for growing III-V semiconductor can include a film, wherein the film includes dislocation free single crystalline III-V semiconductor, and wherein the film can have a thickness of 10 nanometers to 1 micron, for example, between 10 nanometers and 200 nanometers or between 20 and 50 nanometers. After transferring the film, gallium nitride, indium gallium nitride, aluminum nitride, zinc oxide, Indium tin oxide or other materials can be overgrown on the film through which transistors, modulators, light-emitting diodes, laser diodes can be made.

In some embodiments, the III-V semiconductor is gallium nitride.

Other aspects, embodiments, and features will be apparent from the following description, the drawings, and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic drawing showing the formation of dislocation free gallium nitride layer on a bulk gallium nitride substrate.

FIG. 2 shows an exemplary UV-assisted electroless etching setup for the fabrication of the Gallium nitride film.

FIG. 3a is a top view scanning electron microscope (SEM) micrograph showing the hexagonal etch pits forming on the surface; FIG. 3b is a cross sectional SEM micrograph of a nascent pore domain, a nanowire is observed in the middle of the pore domain, and the boundary of the domain is marked in black; FIG. 3c is an image showing a relatively older pore domain encompassing porous gallium nitride formed of a primary and secondary pores, the vertical and horizontal arrows represent the fast anisotropic and

the slow isotropic etch processes, respectively; FIG. 3d is an image showing that a nano-layer is supported by few columns after the domains have coalesced; FIG. 3e is an image showing a nano-layer lying on a porous gallium nitride layer on top of the bulk gallium nitride; and FIG. 3f is an image showing that the pore domains are exposed after the
5 mechanical removal of the gallium nitride nano-layer where the centers of the domains are marked by black spots and the boundary of one domain is marked by a curve.

FIG. 4 is a series of cross sectional images of gallium nitride nano-layer lying on porous gallium nitride.

FIG. 5 shows top view of the nano-layer (top left) onto a porous gallium nitride
10 (bottom right).

FIG. 6a is an SEM image showing the tips of the NWs below the surface etch pits; FIG. 6b is a schematic drawing showing the gallium nitride nano-layer on top of porous gallium nitride with a nanowire (NW) formed from a TD lying exactly below the hexagonal etch pit; FIG. 6c is a cross sectional image; and FIG. 6d is a top view SEM
15 image of nanowires protruding through the etch pits in the gallium nitride layer.

FIG. 7a is a cross sectional SEM image of a bombarded sample with Ar⁺ ions after t min of UV assisted electroless etching, where the dashed lines present the etching fronts which propagate vertical at first then radial; and FIG. 7b is an SEM image showing the NWs embedded in the porous etch domain.

FIG. 8a is a transmission electron microscopy (TEM) image of a gallium nitride layer after transfer onto a carbon coated copper transmission electron microscopy (TEM) grid; FIG. 8b is a High-resolution transmission electron microscopy (HRTEM) of the gallium nitride layer pictured along the $[0001]$ zone axis, which shows a perfect hexagonal crystalline structure of the nano-layer, and the inset of FIG. 9b is the electron diffraction
25 (ED) pattern recorded along the $[0001]$ zone axis with the marked $(10\bar{1}0)$, $(01\bar{1}0)$ and (1100) diffraction spots; and FIG. 8c is the measured EDS spectrum from the gallium nitride nano-layer.

FIG. 9a is an SEM image of the surface etch pit in direct contact with the nanowire tip; FIG. 9b is a TEM image of the surface etch pit present in the nano-layer;
30 and FIG. 9c is a HRTEM image of the center of the pit showing a perfect single crystalline structure.

FIG. 10 is a measured micro-photoluminescence (μ PL) emission signal from the gallium nitride nano-layer showing a strong peak at 3.4 eV; inset (a) shows the

transferred gallium nitride layer onto a sapphire substrate as observed through an optical microscope; and inset (b) shows a schematic of the gallium nitride nano-layer onto sapphire while being probed by a UV laser focused by an objective lens.

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DETAILED DESCRIPTION

A dislocation free single crystalline III-V semiconductor, such as gallium nitride, layer (or nano-layer, or film, or nano-membrane) with a thickness of 10 nanometers to 1 micron, for example, between 10 nanometers and 200 nanometers or between 20 and 50 nanometers can be produced by irradiation, such as ultraviolet (UV), assisted electroless chemical etching, a cost effective and energy efficient technique. The dislocation free single crystalline III-V semiconductor, such as gallium nitride, layer can be formed, for example, by exfoliating from an original crystal having a 10^8cm^{-2} (threading dislocation density) TDD after all the threading dislocations (TDs) are selectively etched away. The III-V semiconductor, such as gallium nitride, thin layer can subsequently be transferred to a foreign substrate for subsequent epitaxial growth of high quality gallium nitride and its related materials. FIG. 1 is a schematic drawing showing the formation of dislocation free gallium nitride layer on a bulk gallium nitride substrate; the layer can be supported by a plurality of gallium nitride nanowires with some protruding through the surface.

Scanning and transmission electron microscopy (SEM and TEM) observations can help explain the physical processes behind the formation of the gallium nitride nano-layer. Further, electron microscopy and optical spectroscopy techniques reveal the single crystalline nature of the gallium nitride nano-layer. The dislocation free gallium nitride nano-layer can be transferred to a variety of hard or flexible substrates and function as a seed layer for subsequent epitaxial over-growth of dislocation free, high quality gallium nitride. The substrate can be polymer substrate, copper substrate, silicon substrate, glass substrate, silicon carbide substrate, sapphire substrate, quartz substrate, porcelain substrate, indium phosphide substrate, gallium nitride substrate, gallium arsenide substrate, beryllium oxide substrate, aluminum nitride substrate, alumina substrate, plastic substrate, or ceramic substrate.

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The membrane can be transferred using already developed printing/stamping transfer techniques. Yuan, H. C., et al. *Appl. Phys. Lett.* **2009**, 94, 013102; Sun, L., et al. *Small* **2010**, 6, 2553-2557, each of which is incorporated by reference in its entirety. The

membrane can be easily transferred to Silicon electronics and thus enabling the fast integration between Silicon and high quality gallium nitride (or similar materials).

This technology can pave the way for high efficiency low cost optoelectronic and high power electronic device applications, and facilitate the fast integration between high quality gallium nitride and other material systems such as silicon or plastics.

A dislocation free single crystalline III-V semiconductor layer (or nano-layer, or film) can have a thickness of 10 nanometers to 1 micron, for example, between 10 nanometers and 200 nanometers or between 20 and 50 nanometers. The layer can be produced by irradiation assisted electroless chemical etching. The III-V semiconductor can include indium arsenide, indium phosphide, gallium arsenide, gallium phosphide, gallium antimonide, indium antimonide, aluminum arsenide, aluminum phosphide, aluminum antimonide, indium gallium arsenide, gallium arsenide phosphide, indium arsenide phosphide, indium gallium nitride, aluminum gallium nitride, or gallium nitride.

Gallium nitride is an example of III-V semiconductor. The compound has a Wurtzite crystal structure and wide band gap of 3.4 eV. It has important applications in many fields, such as optoelectronic, high-power and high-frequency electronic devices, solid state devices, ultra high efficiency photovoltaic devices, and so on.

Gallium nitride based light emitting diodes (LEDs) and laser diodes (LDs) have ushered the way for several staggering technologies including solid-state lighting, high-density optical data storage, high power electronics and laser based projectors and TVs. See, for example, Ponce, F., et al., *Nature* **1997**, 386, 351-359, which is incorporated by reference in its entirety. Further scientific advancements and technological breakthroughs are however hindered by the reliance on the existing relatively low cost heterogeneous substrates. Having large thermal and lattice mismatches, the resulting hetero-epitaxy in commercial gallium nitride template substrates (gallium nitride -on-sapphire or gallium nitride -on-SiC) has high TDD (see, Lester et al. *Applied Physics Letters* **1995**, 66, 1249) of $10^7 - 10^{10} \text{ cm}^{-2}$ causing a decrease in the quantum efficiency and a reduction in the device lifetime. See, for example, Kim, H.-M., et al., *Nano letters* **2004**, 4, 1059-1062; Schubert, M. F., et al., *Applied Physics Letters* **2007**, 91, 231114; Lester, S. D., et al., *Applied Physics Letters* **1995**, 66, 1249, each of which is incorporated by reference in its entirety.

Researchers have been relentlessly working on epitaxial transfer and/or thick layer (30 – 300 μm) regrowth using metal-organic chemical vapor deposition (MOCVD), or

hydride vapor phase epitaxy (HVPE), essentially to achieve $\sim 10^6 \text{ cm}^{-2}$ pseudo-gallium nitride single crystal substrate. See, for example, Paskova, T., et al., *Selected Topics in Quantum Electronics, IEEE Journal of* **2009**, 15, 1041-1052; Paskova, T., et al., *Proceedings of the IEEE* **2010**, 98, 1324-1338, each of which is incorporated by reference
5 in its entirety. Several techniques are implemented to decrease TDD within the material including, epitaxial lateral overgrowth (ELOG), dislocation filtering, the growth of Aluminum nitride (AlN) or gallium nitride low temperature buffer layers, or overgrowth on porous or gallium nitride nanocolumns. See, for example, Nam, O. H., et al., *Applied physics letters* **1997**, 71, 2638-2640; Colby, R., et al., *Nano letters* **2010**, 10, 1568-1573;
10 Yoshida, S., et al., *Applied Physics Letters* **1983**, 42, 427-429; Bai, J., et al., *Journal of Applied Physics* **2006**, 99, 023513; Kang, J. H., et al., *Journal of Crystal Growth* **2012**;
Tang, T. Y., et al., *Journal of Applied Physics* **2009**, 105, 023501-023501-8, each of which is incorporated by reference in its entirety. Though the TDD is reduced to 10^5 cm^{-2} for the ELOG, the absence of free-standing seeding/substrate layer represents the most
15 significant challenge in the gallium nitride photonics technology. See, for example, Marchand, H., et al., *Applied Physics Letters* **1998**, 73, 747-749, which is incorporated by reference in its entirety. While ammonothermal growth can grow gallium nitride with TDD as low as 10^4 cm^{-2} , the process is relatively costly, energy hungry and suffers from very slow growth rate which makes its commercialization challenging. See, for example,
20 Hashimoto, T., et al., *Japanese Journal of Applied Physics* **2005**, 44, L797-L799; Dwiliński, R., et al., *Journal of Crystal Growth* **2008**, 310, 3911-3916, each of which is incorporated by reference in its entirety.

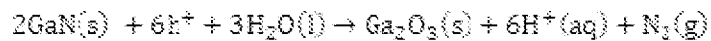
Other methods included growing gallium nitride nanowires or nano-pyramids onto different substrates since these nanostructures are characterized by a lower threading
25 dislocations (TDs). See, for example, Schuster, F., et al., *Nano Letters* **2012**, 12, 2199-2204; Guo, W., et al., *Nano letters* **2010**, 10, 3355-3359; Choi, J. H., et al., *Nature Photonics* **2011**, 5, 763-769, each of which is incorporated by reference in its entirety. There exists, however, a technology gap in which epitaxial films of gallium nitride with low TDD can be grown on different substrates of different lattice constants and thermal
30 coefficients in a high throughput, cost effective and energy efficient manner.

In addition, for a gallium nitride seed layer to be effective for subsequent epitaxial overgrowth, the seed layer is preferably to have a single crystalline structure. Otherwise,

structural dislocation will nucleate around crystal imperfections causing the overgrown of defective gallium nitride.

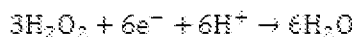
Etching of gallium nitride

5 Chemical etching of n- gallium nitride can depend on the presence of a surface charge region (SCR) at the gallium nitride /electrolyte interface which arises due to gallium nitride surface Fermi-level equilibration with the electrochemical potential of the electrolyte. See, for example, Rajeshwar, K., *Encyclopedia of Electrochemistry* **2007**, which is incorporated by reference in its entirety. This SCR is characterized by the
10 presence of surface electrical fields (\mathbb{E} -fields) which causes an upward bending in the conduction and valence bands. Photo-assisted chemical etching of n- gallium nitride occurs when incident photons, with energy more than the gallium nitride bandgap, excite electron-hole (e^- , h^+) pairs. If the pairs are excited away from the SCR they will simply recombine rendering them useless for surface reactions. However, if they are generated at
15 most at a distance equal to the hole diffusion length away from the SCR, holes may diffuse to the SCR where they will drift towards the interface under the effect of the \mathbb{E} -fields. Since holes are simply broken bonds, once the photo-generated holes reach the gallium nitride /electrolyte interface, they increase surface atoms energy causing the oxidation of the gallium nitride surface to gallium oxide (Ga_2O_3) according to the
20 following oxidation reaction.



See, for example, Minsky, M., et al., *Applied Physics Letters* **1996**, 68, 1531-1533; Youtsey, C., et al., *Journal of Electronic Materials* **1998**, 27, 282-287; Vajpeyi, A., et al., *Physica E: Low-Dimensional Systems and Nanostructures* **2005**, 28, 141-149, each of
25 which is incorporated by reference in its entirety.

After oxidation, Ga_2O_3 can be etched away by HF. Methanol can be added to reduce the solution surface tension allowing the produced N_2 gas not stick to the gallium nitride surface which would have prevented further etching from proceeding. As for the photo-generated electrons, they can be collected by an electrode (for example, a platinum
30 electrode) where they contribute in the reduction of hydrogen peroxide present at the platinum/electrolyte interface. See, for example, Vajpeyi, A., et al., *Physica E: Low-Dimensional Systems and Nanostructures* **2005**, 28, 141-149, which is incorporated by reference in its entirety.



Selective etching at the dislocations of a gallium nitride substrate

When the surface of a gallium nitride substrate includes a plurality of dislocations,
5 the etching solution can etch selectively at the dislocations. The intensity of the surface
internal \mathbb{E} -fields for curved semiconductor/electrolyte interfaces can be calculated. See,
for example, Zhang, X., *Journal of the Electrochemical Society* **1991**, 138, 3750-3756,
which is incorporated by reference in its entirety. In the presence of surface pits, with a
semi-spherical tip, the surface \mathbb{E} -fields are highly enhanced at the tip and thus, once
10 photo-generated holes reach the depletion region, they drift faster towards the tip of the
pit causing a faster etching at the tip. Previously published researches demonstrate,
through atomic force microscopy (AFM) and TEM measurements, that TDs terminating
at the gallium nitride surface cause the formation of surface depressions. See, for
example, Youtsey, C., et al., *Applied Physics Letters* **1999**, 74, 3537-3539; Visconti, P., et
15 al., *Applied Physics Letters* **2000**, 77, 3532-3534; Sasaki, H., et al., *Japanese Journal of
Applied Physics* **2006**, 45, 2531, each of which is incorporated by reference in its entirety.
These surface depressions, with enhanced local \mathbb{E} -fields, should have a higher density of
photo-generated holes and thus, the hexagonal surface pits are expected to initiate at these
depressions. This suggests that the TDs, although originally present in the bulk, can be
20 etched away in the surface layer due to the induced surface depressions.

In order to shed light on the processes responsible for the gallium nitride nano-
layer formation, the reasons behind the nucleation of the surface hexagonal etch pits can
be analyzed. Surface etching through pit formation indicates a non-uniform dissolution
rate among the microscopic sites on the gallium nitride surface available for etching. Such
25 a non-uniformity arises from one of the several possible limiting factors including: holes
photo-generation, holes transport to the interface and reactants and products respective
inward and outward fluxes to the interface. In some embodiments, using a magnetic
stirrer to enhance the chemical fluxes does not change the observation, crossing out the
possibility that the non-uniformity arises from unequal surface concentrations of the
30 reactants or products. It can be assumed that, on the microscopic scale, the UV intensity
across the gallium nitride surface is uniform, leading to an even holes generation rate on
the microscopic scale.

This leaves the holes transport to the interface as the most legitimate rate-limiting factor. Furthermore, gallium nitride is characterized by a low hole mobility and thus, and it can be assumed that the drift of photo-generated holes to the interface, under the effect of the surface \mathbb{E} -fields in the depletion region, is the decisive factor for etching. See, for example, Mnatsakanov, T. T., et al., *Solid-State Electronics* **2003**, 47, 111-115, which is incorporated by reference in its entirety.

Formation of gallium nitride film with low irradiation intensity

While n-type gallium nitride UV-assisted etching in $\text{CH}_3\text{OH}:\text{H}_2\text{O}_2:\text{HF}$ has been reported, no prior published work reports on the formation of a thin single crystalline gallium nitride layer. See, for example, Williamson, T. L., et al., *Journal of Applied Physics* **2003**, 94, 7526-7534; Li, X., et al., *Applied Physics Letters* **2002**, 80, 980-982; Chuah, L., et al., *Materials Science-Poland* **2008**, 26, (3), each of which is incorporated by reference in its entirety.

To form a single crystalline gallium nitride layer, a focusing lens can be used to create an optical power density and hence, a charge carrier concentration gradient across the sample surface. The sample surface can be in contact with an etching solution.

A dislocation free single crystalline gallium nitride film can be prepared using UV-assisted etching. A method for preparing gallium nitride film can include irradiating a surface of a gallium nitride substrate, and contacting the surface of the gallium nitride substrate while irradiating with a solution containing an etching solution to form the film on the substrate. Irradiation can come from various sources, such as UV light. The gallium nitride substrate can be a gallium nitride wafer. The etching solution can include hydrofluoric acid, hydrogen peroxide, potassium hydroxide, or methanol, or a combination thereof

A gallium nitride film can be formed through a combination of a vertical etching and a lateral etching below the surface of a gallium nitride substrate. In some embodiments, an HF based etching solution can first attack the cleaned surface of a gallium nitride substrate causing hexagonal etch pits to form. Etching can then proceed rapidly along the $[000\bar{1}]$ crystallographic direction causing the surface pores to get deeper. However, at a certain depth from the surface, along with the rapid vertical crystallographic etching mechanism, a second slower anisotropic lateral etching mechanism can appear. The depth from the surface can be from 10 nanometers to 1

micron, for example, between 10 nanometers and 200 nanometers or between 20 and 50 nanometers. This second etching mechanism can cause the pores to widen, however at a much slower rate than their vertical propagation. The presence of these two etching mechanisms can cause the formation of undersurface cavity like structures. As

5 undersurface gallium nitride gets etched away, a floating thin layer can be formed on top of a porous gallium nitride layer. The thin layer can have a thickness of 10 nanometers to 1 micron, for example, between 10 nanometers and 200 nanometers or between 20 and 50 nanometers.

It is preferred that the irradiation intensity on the surface of the substrate is low.

10 A high irradiation intensity can etch away the dislocation free single crystalline gallium nitride film. Both the length of the irradiation and the density of the irradiation source on the surface of the substrate affect the etching process. The irradiation source can be any source having a higher energy than the bandgap of the semiconductor film to be prepared, or any source having wavelengths below the bandgap of the semiconductor materials.

15 Examples of the irradiation source include UV light, x-ray, and gamma rays. If a certain energy density causes the formation of the membrane without applying a bias, a higher intensity can still be used if a bias is applied. So the maximum intensity can be a function of the applied bias. And the energy density (or energy intensity) of the irradiation source at the surface of the substrate can be adjusted or controlled to optimize the etching result.

20 In some embodiments, the light can focus on a portion of the surface of the gallium nitride substrate. While the portion of the surface under irradiation may be etched away, the portion of the gallium nitride substrate not under direct irradiation can produce dislocation free single crystalline gallium nitride layer. The irradiation intensity on the surface of the gallium nitride substrate can be changed or controlled by using
25 optics, such as filters, optical attenuator, optical diffuser, beam expander, or polarizer, a combination thereof.

A threading dislocation free single crystalline gallium nitride nano-layer can be prepared using a simple, inexpensive and energy efficient UV-assisted electroless etching technique. Scanning electron microscopy can be used to study the detailed formation
30 process of the gallium nitride nano-layer. TEM, EDS and μ PL measurements can confirm the single crystalline nature of the gallium nitride nano-layer. Through this method, a dislocation free single crystalline gallium nitride nano-layer can be exfoliated from an original crystal having high TDD, such as 10^8 cm^{-2} TDD, after all the TDs are

selectively etched away. This layer can be transferred to other hard or flexible substrates and serves as a seed layer for subsequent epitaxial growth of dislocation free, high quality gallium nitride. See, for example, Rogers, J., et al., *Nature* **2011**, 477, 45-53, which is incorporated by reference in its entirety. This technology will facilitate the fast integration
5 between high quality gallium nitride and other material systems such as silicon or plastics enabling the production of cost efficient, high quality optoelectronic and electronic devices.

Gallium nitride thin film can be prepared from a substrate containing a silicon doped c-plane oriented gallium nitride on sapphire, n-doped, un-doped or p-doped
10 gallium nitride can also be used; gallium nitride thin film can be prepared from a substrate containing bulk gallium nitride; gallium nitride thin film can be prepared from a silicon carbide substrate containing gallium nitride; gallium nitride can be prepared from a silicon substrate containing gallium nitride; and gallium nitride can be prepared from other substrates containing gallium nitride.

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EXAMPLES

Formation and characterization of a gallium nitride film

The gallium nitride wafers used in this study consist of 30 μm of silicon doped ($\sim 10^{18} \text{ cm}^{-3}$) c-plane oriented gallium nitride grown using metal-organic chemical vapor
20 deposition (MOCVD) technique on a sapphire substrate. The wafer has an initial TDD of 10^8 cm^{-2} . The gallium nitride wafer was cleaved into $7 \times 7 \text{ mm}^2$ pieces which are later degreased in acetone and isopropanol alcohol (IPA), respectively for 5 mins and finally cleaned in hot HNO_3 (65°C) for 15 mins for surface oxide removal. Some other samples are further cleaned into HCL for 10 mins or in HF for 2 hours to be certain of a complete
25 surface oxide removal. See, for example, Ohira, S., et al., *Physica Status Solidi (c)* **2008**, 5, 3116-3118, which is incorporated by reference in its entirety. The effect of the different cleaning procedures on the final results was not observed. A thin layer of platinum metal (150 nm) is sputtered on the side of each of the samples which are later immersed in an electrolyte composed of 1:2:2 $\text{CH}_3\text{OH}:\text{H}_2\text{O}_2:\text{HF}$ with the c-plane in contact with the
30 solution. In addition to platinum, titanium, gold or silver can also be used as electrode. In some embodiments, an electric field can be applied at the surface of the substrate during etching. The electrodes can have different configurations, such as standard electrode configuration. A fused silica lens is used to focus ultraviolet (UV) light emanating from a

200 W mercury (Hg) arc lamp onto the sample (FIG. 2). Once the desired etching period is reached, the sample is cleaned by dipping and rinsing in IPA and then dried using a critical point dryer (CPD).

FIG. 3 is a series of scanning electron microscope SEM micrographs showing
5 different stages along the layer formation. The HF based electrolyte solution first attacks the cleaned surface of the gallium nitride causing hexagonal etch pits to form (FIG. 3a). These surface pores nucleate at terminations of TDs. Once pores nucleate at the surface, etching proceeds rapidly along the $[000\bar{1}]$ crystallographic direction causing the surface pores to get deeper (represented by the arrow pointing down in FIG. 3b). However, at
10 certain depth from the surface, along with the rapid vertical crystallographic etching mechanism, appears a second slower anisotropic lateral etching mechanism. The depth from the surface can be from 10 nanometers to 1 micron, for example, between 10 nanometers and 200 nanometers or between 20 and 50 nanometers. This second etching mechanism causes the pores to widen, however at a much slower rate than their vertical
15 propagation. See, for example, Feenstra, R. M., et al., *Porous Silicon Carbide and Gallium Nitride: Epitaxy, Catalysis, and Biotechnology Applications*. Wiley: **2008**, which is incorporated by reference in its entirety. As the anisotropic etching proceeds laterally (represented by arrows pointing left and right in FIG. 3c), secondary vertical pores nucleate and propagate crystallographically along the $[000\bar{1}]$ direction (FIG. 3c). The
20 presence of these two etching mechanisms causes the formation of undersurface cavity like structures, or pore domains, which encompass a group of spatially confined vertical pores with a tiny opening at the top (FIG. 3c). See, for example, Erne, B., et al., *Journal of the Electrochemical Society* **1996**, 143, 305-314; O'Dwyer, C., et al., *Journal of The Electrochemical Society* **2007**, 154, H78-H85, which is incorporated by reference in its
25 entirety. At this stage, reactants and products need to diffuse in and out, respectively, from the tiny surface opening for etching to proceed. Since the pore domains are only embedded 10 nanometers to 1 micron deep from the surface, for example, between 10 nanometers and 200 nanometers or between 20 and 50 nanometers, a considerable amount of UV photons can still reach them generating e-h pairs on the domain walls
30 causing the UV assisted etching of gallium nitride to proceed.

As undersurface gallium nitride gets etched away, the pore domains become wider till they coalesce forming larger ones. Later, the surface layer is only supported by few columns which eventually get etched away forming a floating 10 nanometers to 1 micron

thin layer, for example, between 10 nanometers and 200 nanometers or between 20 and 50 nanometers, on top of a porous gallium nitride layer (FIG. 3d and FIG. 3e). The pore domains are imaged in FIG. 3f after the mechanical removal of the thin surface layer where the centers of the pore domains are marked by black spots and the boundary of one pore domain is marked by the red curve. As the sample dries, due to the water surface tension, the thin layer collapses downward and sticks to the porous gallium nitride. In order to overcome this sticking, which makes it nearly impossible for a subsequent mechanical exfoliation, the gallium nitride samples can be dried using CPD in liquid carbon dioxide. Some samples, after they are cleaned, are dipped in HF (50%) for 2 hours without the presence of UV or H₂O₂, which should be enough to dissolve any remaining formed oxides. See, for example, Ohira, S., et al., *Physica Status Solidi (c)* **2008**, 5, 3116-3118, which is incorporated by reference in its entirety. FIG. 4 shows cross-sectional images of the gallium nitride nanolayer lying on porous gallium nitride. FIG. 5 shows top view of the nano-layer (top left) onto the porous gallium nitride (bottom right).

According to the previous oxidation reaction, six holes are required to oxidize two Ga atoms and thus, at any surface where the hole concentration is less than the threshold ($n_{\text{h}}^{\text{c}} = 3 \text{ h}^{\text{+}} / \text{Ga atom}$) etching will not proceed. See, for example, Weyher, J., et al., *The European Physical Journal Applied Physics* **2004**, 27, 37-41, which is incorporated by reference in its entirety. During the UV-assisted electroless etching of gallium nitride, the formation of nanowires, or whiskers, is attributed to the presence of TDs which offer fast recombination channels for the e-h pairs and thus decrease the surrounding hole concentration below n_{h}^{c} preventing etching of the surrounding volume. See, for example, Youtsey, C., et al., *Applied Physics Letters* **1998**, 73, 797-799; Weyher, J., et al., *Journal of Applied Physics* **2001**, 90, 6105-6109, each of which is incorporated by reference in its entirety. The SEM images show the tips of the NWs directly below the surface etch pits (FIG. 6a) and thus in the middle of each of the undersurface cavities lies one gallium nitride NW (see FIG. 3b). This implies that the surface etch pits nucleate at the surface terminations of the TDs causing the formation of a TD free gallium nitride nano-layer. When the layer collapses downward under the effect of the water surface tension, the NWs can protrude through the holes which are present just on top of them (FIG. 6c and FIG. 6d).

To further prove the concept, that the exfoliated nano-layer is TD free, surface defects were created through Argon ion ($\text{Ar}^{\text{+}}$) bombardment using inductive coupled

plasma and then later etched the sample in the HF solution under UV illumination. FIG. 7a presents SEM image of a surface defect after 1 min of etching. It can be seen that etching initiates at the defect site and later propagates downward. Once the etching front reaches the bulk gallium nitride, it becomes radial causing the formation of the gallium nitride nano-layer. However, as observed in FIG. 7b, the domains are not formed around NWs, formed from TDs, but rather around the surface induced defects. This indicates that in that layer, all the TDs still exist which will act as dislocation nucleation sites if used for regrowth. However, the domains form around the NWs indicating that the TDs within the surface nano-layer got etched away during the exfoliation process.

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Demonstration of defect free single crystal gallium nitride film

Since any remaining crystal dislocations act as dislocation nucleation sites during overgrowth, the dislocated crystal can be completely etched away during exfoliation.

In order to get TEM micrographs of the nano-layer, a piece of the thin film is transferred to a carbon coated copper grid (FIG. 8a). The high resolution TEM (HRTEM) of the layer aligned to the c-plane is presented in FIG. 8b, with the inset showing the associated electron diffraction (ED) pattern. A high degree of crystallinity of the hexagonal lattice is observed. Measuring the interplanar distances from the $(10\bar{1}0)$, $(0\bar{1}10)$ and $(\bar{1}100)$ diffraction spots yields a value of 2.738 \AA which is equal to the tabulated data for the unstrained gallium nitride. These results indicate that the exfoliated layer is a single crystal gallium nitride thin nano-layer. The exfoliation of a dislocation free single crystalline gallium nitride thin film using a non-intrusive method has not been reported. Such a nano-layer, where TDs are etched away, does not contain any dislocation nucleation sites if used for subsequent growth. The collected energy dispersive X-ray spectroscopy (EDS) spectrum from the gallium nitride layer in FIG. 8c shows no peaks other than that associated with N, fluorine (F) and Ga. The F peak is believed to originate from residual F halogens that tie up with the Ga dangling bonds at the surface which is usually the case after nitrides exposure to HF. See, for example, King, S., et al., *Journal of Applied Physics* **1998**, 84, 5248-5260, which is incorporated by reference in its entirety.

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The SEM image in FIG. 9a shows that the tip of the gallium nitride NW is in direct contact with the etch pit present in the nano-layer. Since NWs are formed from etch resistant TDs, it is important that after exfoliation, there are no remnants of TDs in the

nano-layer. FIG. 9b shows a TEM image of the etch pit present on the nano-layer which is highlighted with a dashed square in FIG. 9a. While the top of a typical etch pit is hexagonal (FIG. 3a), the bottom looks more like a heart shape where the supposedly formed hexagon pit (dashed lines in FIG. 9b) got distorted by the fact that the TD did not allow any etching of its surrounding. A HRTEM image of the center of the hexagon (solid circle in FIG. 9b), where the NW tip was in direct contact with the nano-layer's crystal is shown in FIG. 9c. It is single crystalline indicating that the entire dislocated crystal is completely etched away.

TEM measurements show that the exfoliated nano-layer is single-crystalline, with no TDs observed in all specimens under study. The optical properties of the nano-layer were further characterized using micro-photoluminescence (μ PL). In order to remove any interference from the much stronger μ PL signal of the underlying porous and bulk gallium nitride, the nano-layer can be transferred onto a sapphire substrate ($E_g = 9.9$ eV) as shown in inset a of FIG. 10. A 325 nm laser ($E_{exc} = 3.8$ eV) is focused to a spot size of $28 \mu\text{m}^2$ (see inset b of FIG. 10) and the recorded μ PL data is shown in FIG. 10. The gallium nitride nano-layer exhibits a μ PL at 3.4 eV which is the characteristic band to band transition in the gallium nitride. The emission intensity at 2.15 eV (yellow luminescence) and at 2.43 eV (Green luminescence), which are attributed to different types of structural defects in the gallium nitride are incomparable with the 3.4 eV emission indicating that the layer's defects density is relatively low. See, for example, Reshchikov, M., et al., *Applied Physics Letters* **2001**, 78, 3041-3043, which is incorporated by reference in its entirety. This is in agreement with the observation based on SEM and TEM measurements. There were previous successful efforts of forming a gallium nitride ultra-thin membrane using bombardment with Argon ions followed by etching in potassium hydroxide (KOH). See, for example, Tiginyanu, I., et al., *Materials Letters* **2011**, 65, 360-362; Tiginyanu, I., et al., *Physica Status Solidi (RRL)-Rapid Research Letters* **2012**, each of which is incorporated by reference in its entirety. However, the formed membranes reported previously exhibit a peak cathodoluminescence emission at 2.2 eV indicating that they are mainly formed from defective gallium nitride generated by Argon ions bombardment. Etching gallium nitride after ion bombardment produces defective layers. However, the etching that initiates at the intrinsic crystal threading dislocations can generate dislocation free gallium nitride film or layer.

Other embodiments are within the scope of the following claims.

WHAT IS CLAIMED IS:

1. A method for preparing III-V semiconductor film comprising:
irradiating a surface of a substrate including the III-V semiconductor; and
5 contacting the surface of the substrate while irradiating with a solution
containing an etching solution to form the film on the substrate.
2. The method of claim 1, wherein the III-V semiconductor is selected from the
group consisting of indium arsenide, indium phosphide, gallium arsenide, gallium
10 phosphide, aluminum nitride, gallium antimonide, indium antimonide, aluminum
arsenide, aluminum phosphide, aluminum antimonide, indium gallium arsenide,
gallium arsenide phosphide, indium gallium arsenide phosphide, indium
aluminum gallium arsenide, indium arsenide phosphide, indium gallium nitride,
and aluminum gallium nitride.
- 15 3. The method of claim 1, wherein the III-V semiconductor is gallium nitride.
4. The method of claim 3, wherein the substrate includes a silicon doped, n-doped,
un-doped, or p-doped gallium nitride on sapphire.
- 20 5. The method of claim 3, wherein the substrate includes bulk gallium nitride.
6. The method of claim 3, wherein the substrate includes gallium nitride on silicon
carbide.
- 25 7. The method of claim 3, wherein the substrate includes gallium nitride on silicon.
8. The method of claim 1, wherein the etching solution includes hydrogen fluoride
and hydrogen peroxide.
- 30 9. The method of claim 1, wherein the etching solution includes potassium
hydroxide.

10. The method of claim 1, wherein the surface of the substrate includes a plurality of dislocations.
- 5 11. The method of claim 1, wherein the etching solution etches selectively at the dislocations.
12. The method of claim 1, wherein the surface of the substrate is irradiated by an irradiation source, wherein the irradiation source has an energy greater than the bandgap of the III-V semiconductor.
- 10 13. The method of claim 1, wherein the surface of the substrate is irradiated by an ultraviolet light source, wherein the energy of the ultraviolet light source is greater than the bandgap of the III-V semiconductor.
- 15 14. The method of claim 1, wherein the surface of the substrate is irradiated by an X-ray.
15. The method of claim 1, wherein the surface of the substrate is irradiated by a gamma ray.
- 20 16. The method of claim 12, wherein the method further comprising controlling the intensity of the irradiation source.
17. The method of claim 1, wherein a portion of the surface of the substrate is coated with an electrode.
- 25 18. The method of claim 17, wherein the material of the electrode is selected from titanium, platinum, silver, and gold.
- 30 19. The method of claim 1, wherein the method further comprising applying an electric field at the surface of the substrate.
20. The method of claim 1, wherein the method further comprises drying the substrate.

21. The method of claim 1, wherein the thickness of the III-V semiconductor film is between 10 nanometers and 1 micron.
- 5 22. The method of claim 1, wherein the method further comprises transferring the III-V semiconductor film to a second substrate.
23. A film comprising dislocation free single crystalline III-V semiconductor, wherein the dislocation free single crystalline III-V semiconductor has a thickness of
10 between 10 nanometers and 1 micron nanometers.
24. The film of claim 23, wherein the film includes a plurality of pores.
25. The film of claim 23, wherein the III-V semiconductor is gallium nitride.
15
26. The film of claim 25, wherein a plurality of gallium nitride wires protrude through the dislocation free single crystalline gallium nitride.
27. The film of claim 25, wherein the film further comprises a porous gallium nitride
20 layer underneath the dislocation free single crystalline gallium nitride.
28. A structure comprising dislocation free single crystalline III-V semiconductor on a substrate, wherein the substrate is a polymer substrate, copper substrate, silicon substrate, glass substrate, silicon carbide substrate, sapphire substrate, quartz
25 substrate, porcelain substrate, indium phosphide substrate, gallium nitride substrate, gallium arsenide substrate, beryllium oxide substrate, aluminum nitride substrate, alumina substrate, plastic substrate, or ceramic substrate.
29. A device for growing III-V semiconductor comprising a film, wherein the film
30 includes dislocation free single crystalline III-V semiconductor, and wherein the film has a thickness of 10 nanometers to 1 micron.
30. The device of claim 29, wherein the III-V semiconductor is gallium nitride.

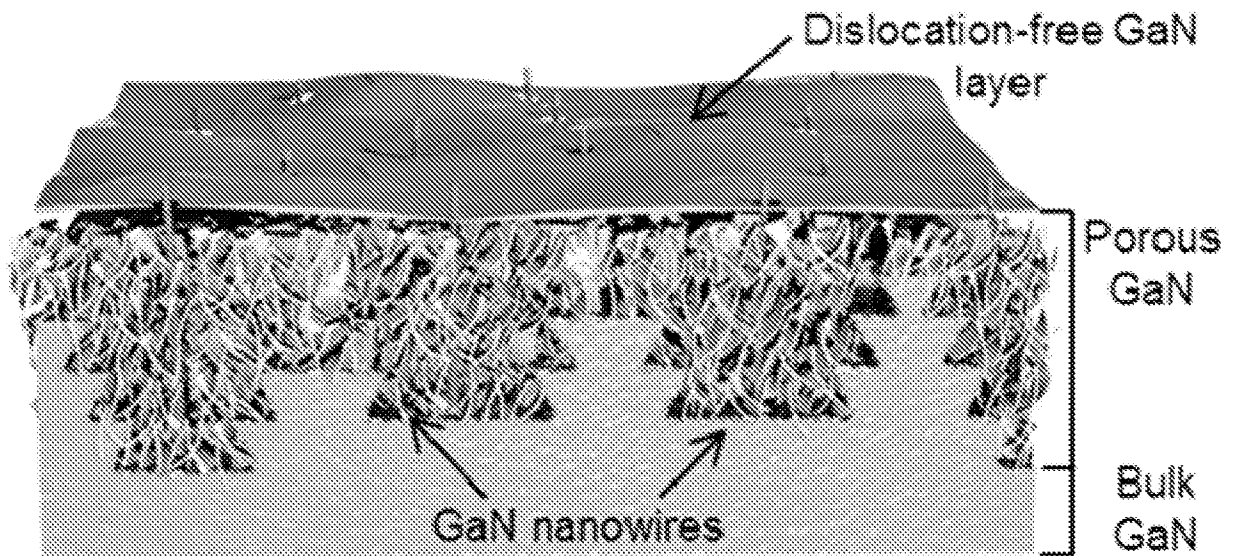


FIG. 1

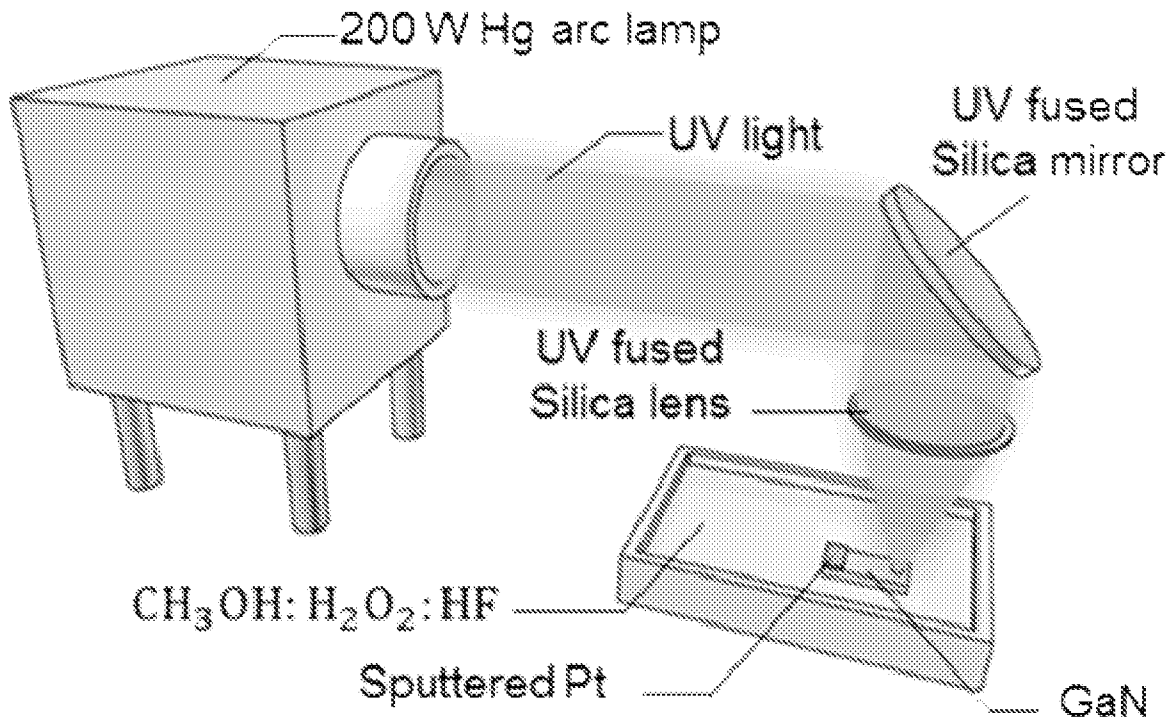


FIG. 2

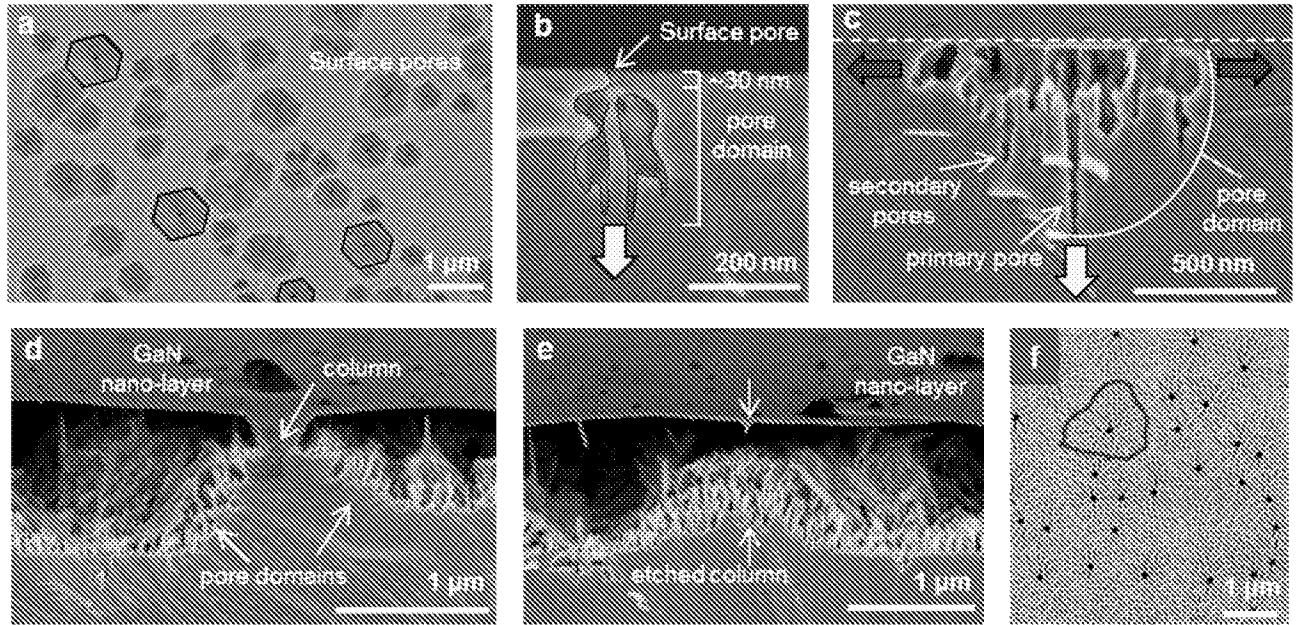


FIG. 3

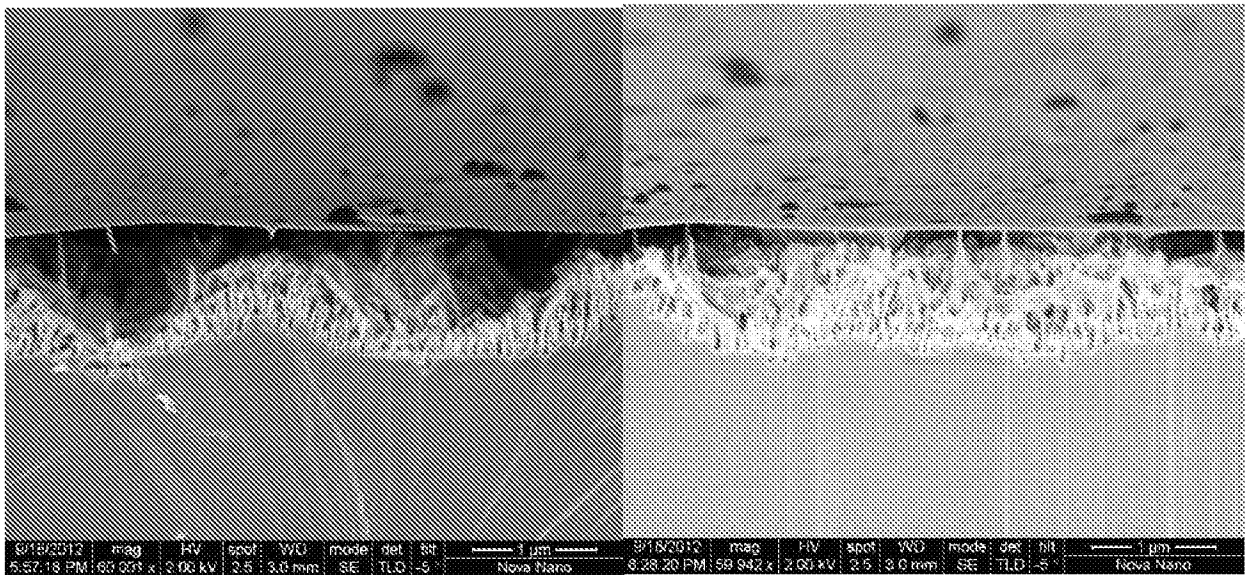


FIG. 4

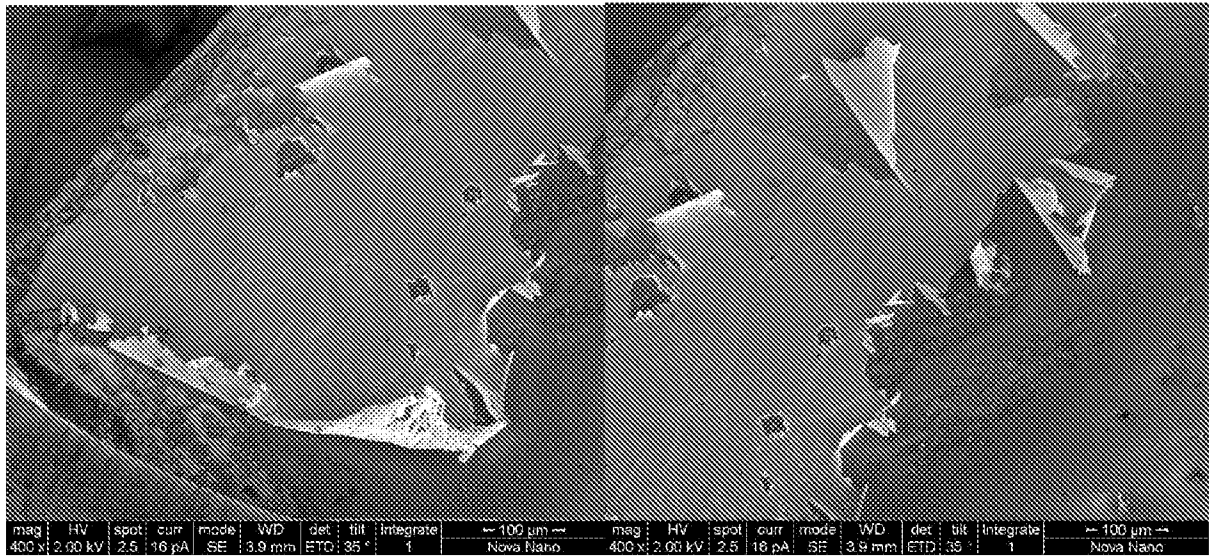


FIG. 5

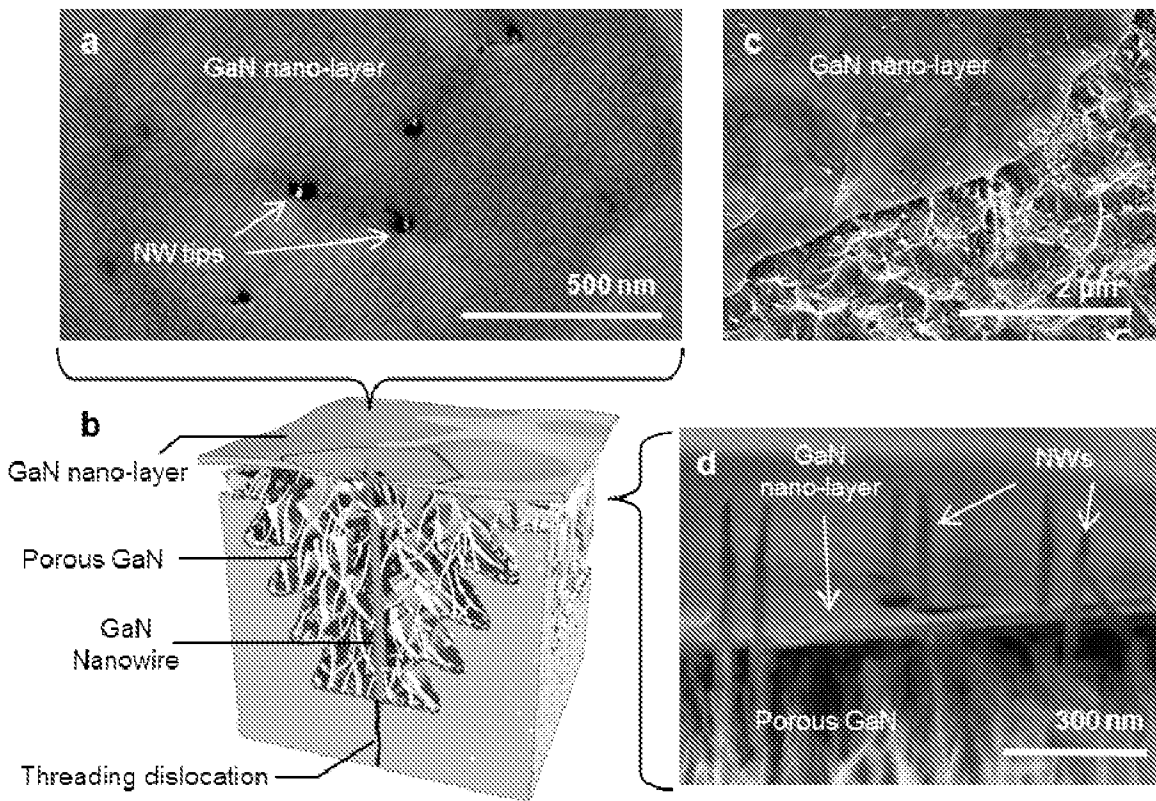


FIG. 6

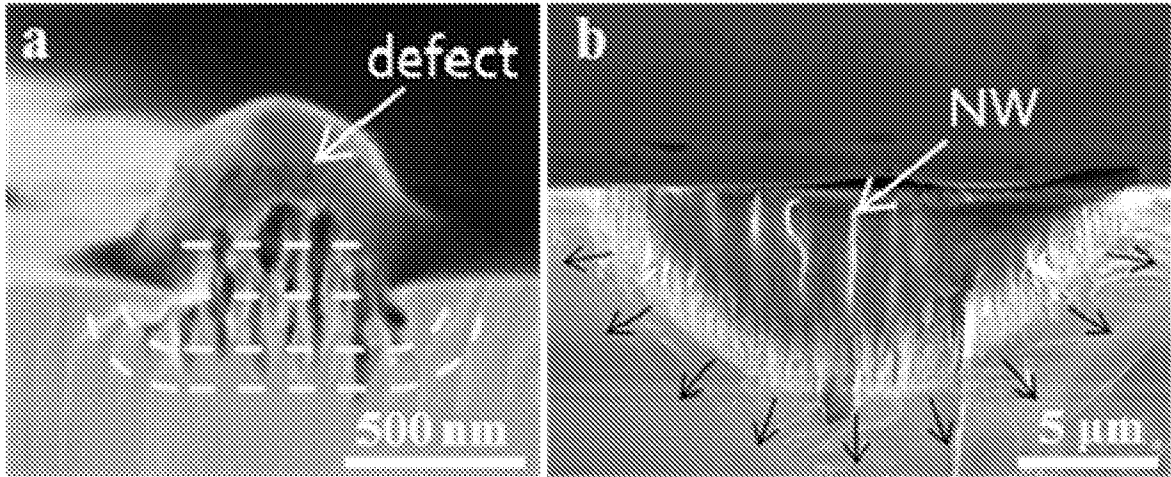


FIG. 7

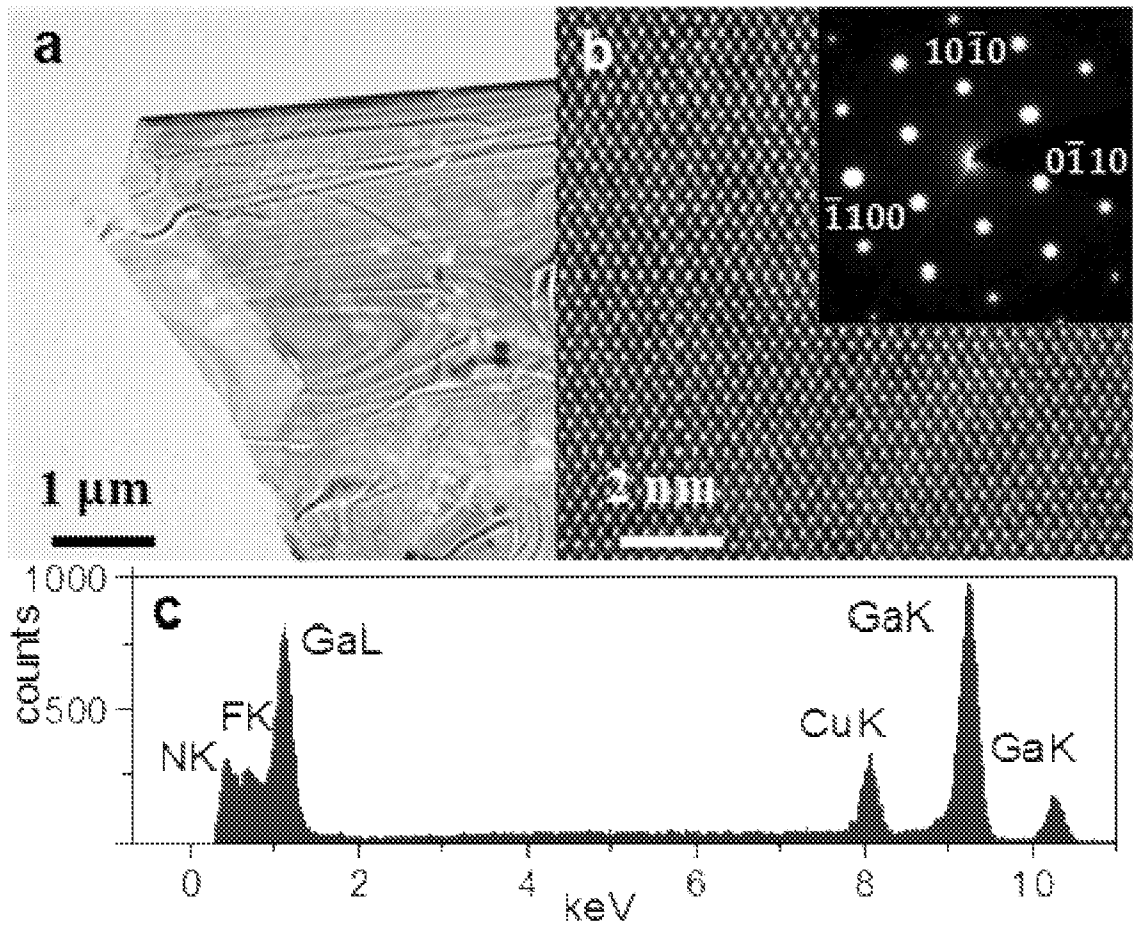


FIG. 8

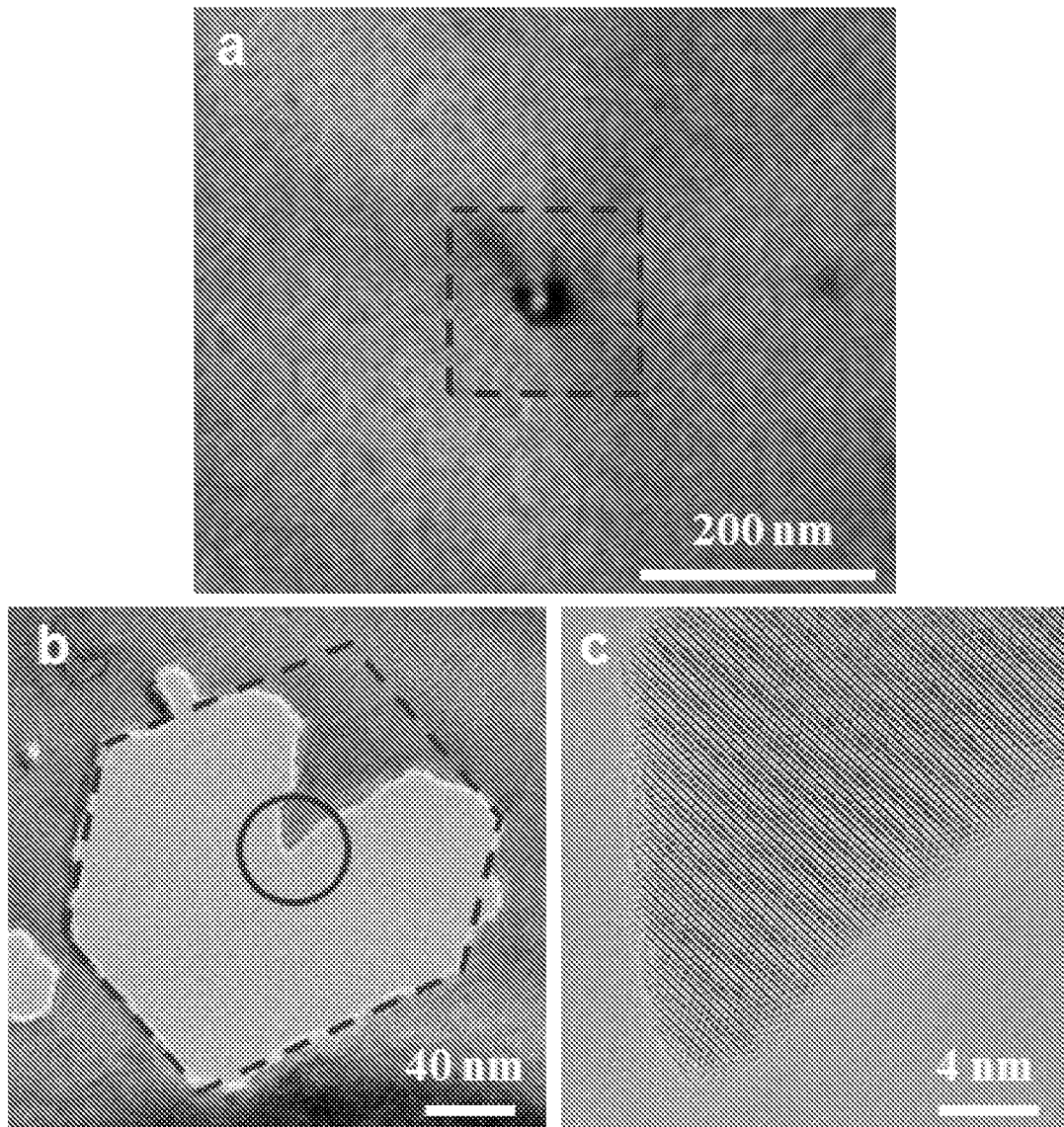


FIG. 9

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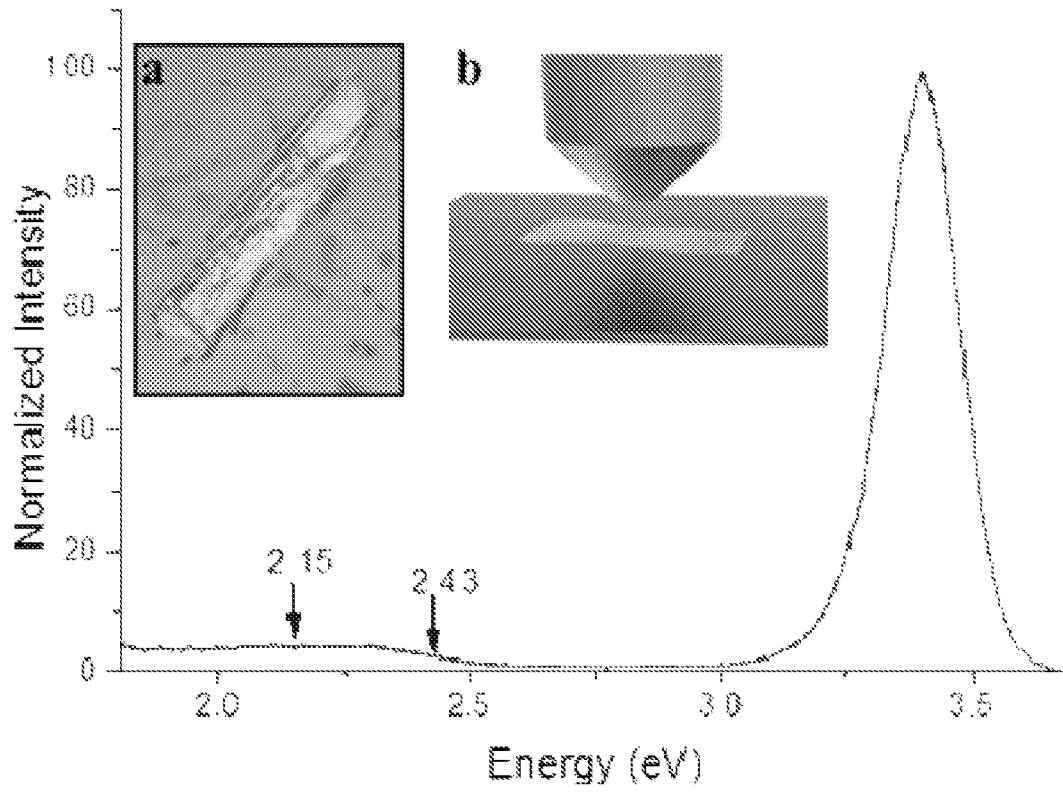


FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US13/31441

A. CLASSIFICATION OF SUBJECT MATTER IPC(8) - H01L 21/306 (2013.01) USPC - 438/718, 746; 257/E21.22 According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) IPC(8) - H01L 21/306 (2013.01) USPC - 438/708, 718, 745, 746; 252/79.3; 257/E21.22 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) MicroPatent (US Granted, US Applications, EP-A, EP-B, WO, JP, DE-G, DE-A, DE-T, DE-U, GB-A, FR-A); Google Patents; Google Scholar; IP.COM, IEEE Xplore; Search Terms Used: GaN, Gallium nitride, Indium gallium nitride, aluminum gallium nitride, AlGaN, InGaN, III-V semiconductors; photochemical etching, photoelectrochemical etching, light assisted etching, HF, hydrofluoric acid, hydrogen peroxide, metal, electrode*, platinum, gold, titanium, nanopores, nanowires, dislocation, fault, etch pits, thread*, membrane, single crystal.		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ----- Y X ----- Y Y Y Y	US 6,605,548 B1 (BARDWELL J) August 12, 2003, Figure 2, column 3, lines 38 – 58, column 5, lines 11 – 15. US 2013/0011656 A1 (ZHANG Y et al.) January 10, 2013, Abstract, Figure 21, paragraphs [0074] – [0076]. US 4,100,014 A (KUHN-KUHNENFELD et al.) July 11, 1978, Abstract, column 1, lines 30 – 35, column 1, lines 63 – 67. US 5,591,564 A (ROSTOKER M et al.) January 07, 1997, column 4, lines 31 -32, column 23, lines 22 – 44. OOI, B; NAJAR, A; SLIMANE, A; ELAFANDY, R; GASIM, A; LI, Q; and NG, T, "GaN-based Nano-pores and Nano-wires Fabricated Using Electroless Chemical Etching Process", Abstract #822, 221st ECS Meeting, 2012, The Electrochemical Society, Downloaded from the Internet on 06 May 2013: < http://ma.ecsdl.org/content/MA2012-01/18/822.abstract?cited-by=yes&legid=ecsmtgabs;MA2012-01/18/822#cited-by >, Figure 3(a), paragraph 4.	1-3, 5, 9, 10, 12, 13, 16-18 ----- 4, 6-8, 11, 14, 15, 19-22 23-25, 27-30 ----- 4, 6, 7, 19-22, 26 8, 11 14, 15 26
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/>		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 08 May 2013 (08.05.2013)	Date of mailing of the international search report <div style="text-align: center; font-size: 1.5em; font-weight: bold;">11 JUN 2013</div>	
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: <div style="text-align: right;">Shane Thomas</div> PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774	